EVIL Datasheet

Block diagram

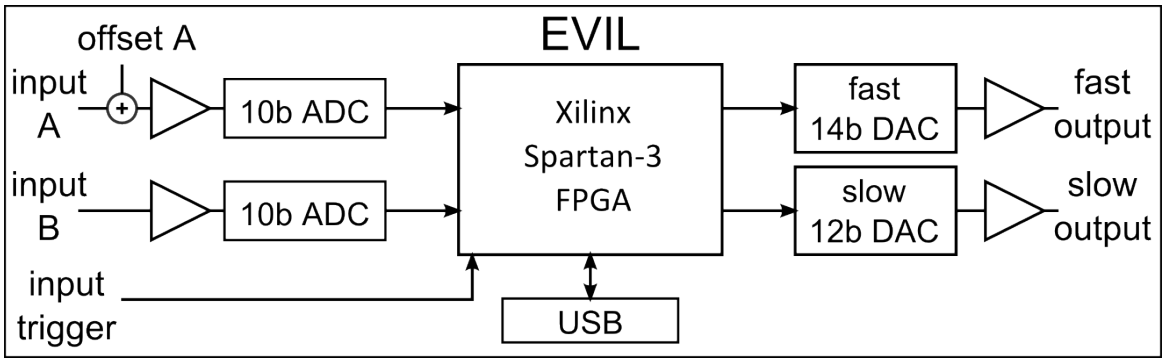

Figure 1 – Block diagram for the EVIL

Summary

The EVIL (Electronically Variable Interactive Lockbox) is made up of two 10-bit 96 MHz ADCs (Analog-to-Digital Converters), a Xilinx Spartan-3 FPGA, a 14-bit 96 MHz parallel DAC (Digital-to-Analog Converter), and a 12-bit 5 MHz serial DAC.

Currently we have implemented a dual-channel independent PI controller, suitable for many stabilization tasks around the lab. The system is also capable of streaming the ADC inputs, the internal ramp generator, or other system signals to the PC.

The EVIL can also be used as a development platform for the advanced user. By varying the FPGA (Field Programmable Gate Array) firmware, any type of linear or nonlinear function of the inputs can be implemented at the outputs. User-created firmware can be loaded into the FLASH for power-on availability.

Software/firmware features

- Dual PI controller and streaming of all control signals to PC
- Automatic relocking with sensitivity and dead time adjustment
- Saving/loading of locking parameters
- Real-time streaming and conversion of control signals
- Multiple EVILs can be controlled from the same software
- Interactive streaming view: can view different channels and perform real-time signal processing such as FFT

Specifications

System

- System latency (input to output, fast path): 250 ns
- PI control bandwidth: ∼500 kHz (higher possible with addition of D stage)

Digital

- ADCs: 10-bit parallel, 96 Msps (megasamples per second)
- Fast DAC: 14-bit parallel, 96 Msps
- Slow DAC: 12-bit serial, 5 Msps

Analog

- Input signal levels: ±10V (full-scale range of ADCs adjustable down to ±100mV)
- Analog input offset: ±10V adjustable on Channel A
- Output signal levels: ±10V (full-scale range of DACs adjustable down to ±1V)
- Input bandwidth: greater than 3 MHz (input gain-dependent)
- Output bandwidth: greater than 3 MHz (output gain-dependent)

WARNING: Damage may occur if the input analog gains are set too high for the input signal level. Use caution when installing on a new setup.

Power

- +15V: 750 mA
- -15V: 200 mA

CAUTION: System involves digital switching circuitry. Isolate power supply from sensitive analog devices.

GUI screenshots

The EVIL GUI supports loading and saving configurations, streaming from the EVIL at 250 ksps (one channel at a time), a live FFT, and real-time adjustment of all internal parameters. The GUI is written in Python and PyQT for easy scripting.

Once the system has been characterized, a separate monitoring oscilloscope is not needed for relocking. A screenshot of the EVIL software during operation is shown in Fig. 2.

EVIL casing

The EVIL board fits inside a standard 19” rack. The front panel is displayed in Fig. 3 and the EVIL within the casing is displayed in Fig. 4.

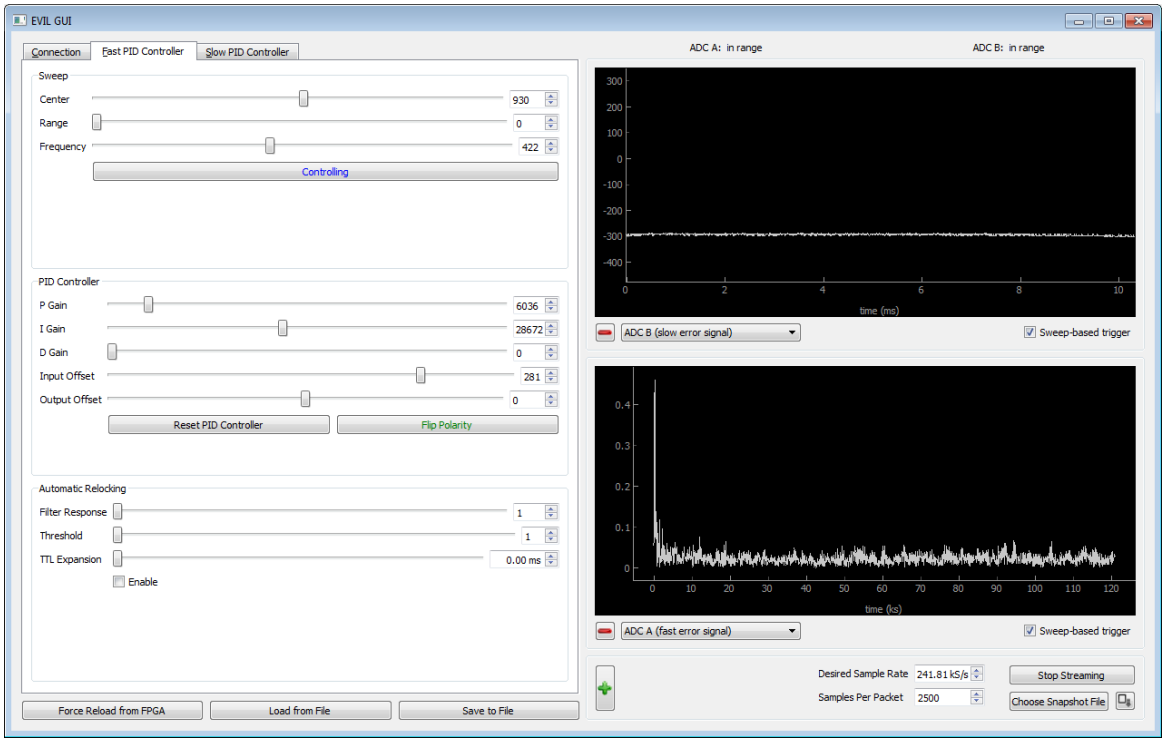

Figure 2 – Screenshot of the EVIL software running in the lab, showing the control environment on the left. Two control signals are shown on the right: the top right is the error signal of the locked system. The bottom right is a real-time FFT of the locked error signal.

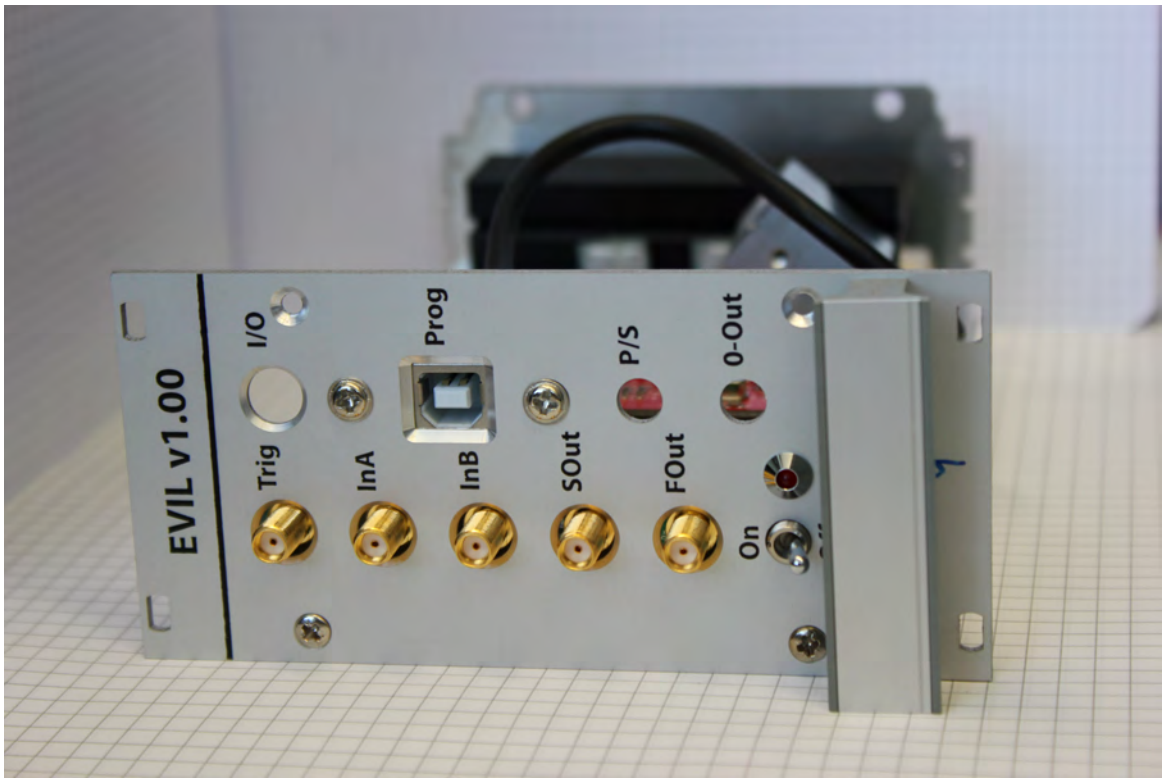

Figure 3 – Front panel of the EVIL.

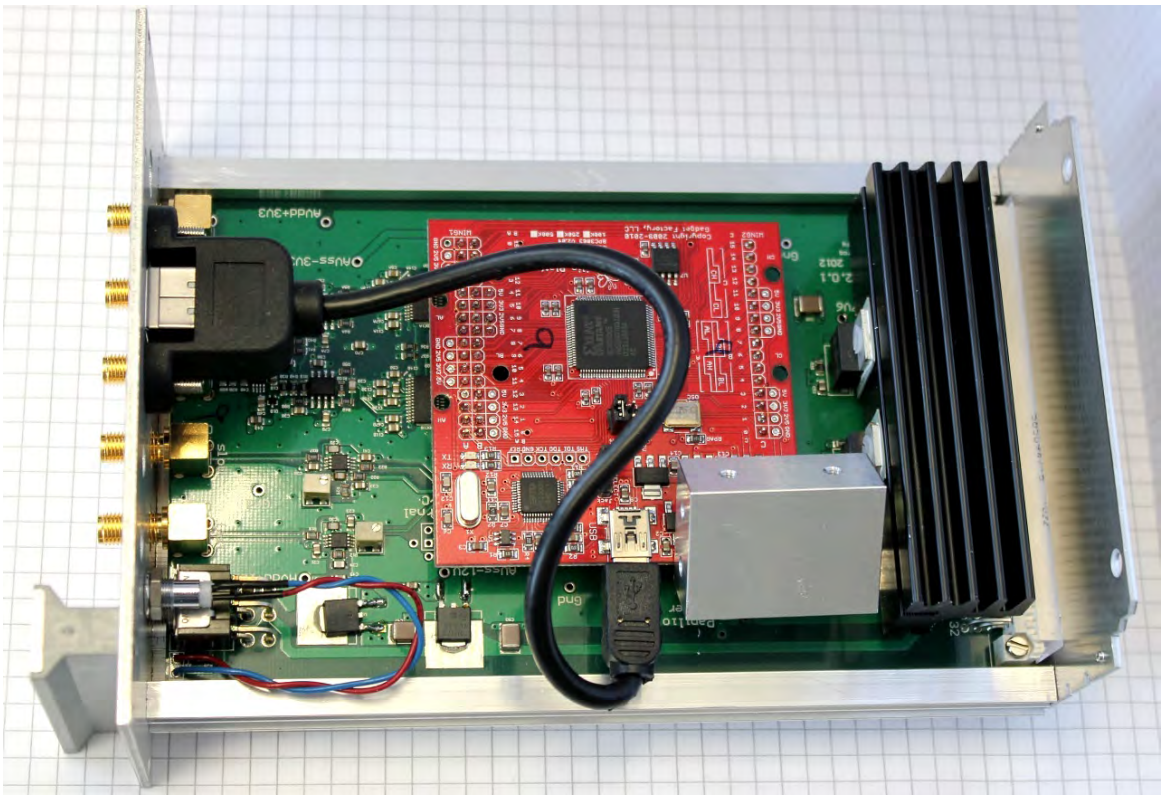

Figure 4 – EVIL side view (open). The FPGA is contained on the red daughterboard (Papilio 500K) and carries out the digital signal processing. The green carrier board holds the data converters, analog front-ends and power supplies.