ETH zürich

Vertiefungsrichtungen am D-ITET

Einführung vom 1. Juni 2021

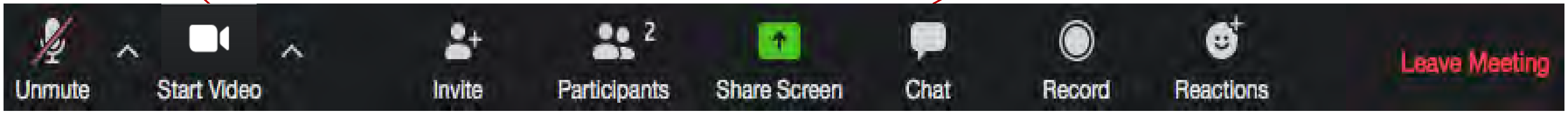
D ITET

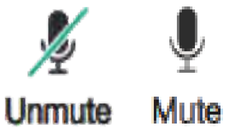
Zoom-Etiquette

Sie können die Kamera gerne einschalten.

Stop/Start Video

Verwenden Sie für Ihre Fragen auch den Chat.
Chat-Fragen werden gesammelt und am Ende der Veranstaltung beantwortet.





Bitte schalten Sie Ihr Mikrofon auf "stumm" und ändern Sie dies erst am Ende der Veranstaltung, wenn Sie Fragen stellen können.

Programm

Präsentation Vertiefungsrichtungen (Zoom-Meeting vom 1. Juni 2021)	
1. Vertiefungsrichtungen am D-ITET (Reto Kreuzer)	**15:15 - 15:25**
2. Communications (Prof. Hans-Andrea Loeliger)	**15:25 - 15:40**
3. Computers and Networks (Prof. Kaveh Razavi)	**15:40 - 15:55**
4. Electronics and Photonics: Electronic and Photonic Materials and Devices (Prof. Jürg Leuthold)	**15:55 - 16:10**
5. Energy and Power Electronics (Prof. Ulrike Grossner)	**16:10 - 16:25**
6. Electronics and Photonics: Integrated Circuits and Systems (Prof. Taekwang Jang)	**16:25 - 16:40**
7. Biomedical Engineering (Prof. Janos Vörös)	**16:40 - 16:55**

- Am Ende des Events können zu den Vertiefungsrichtungen Fragen gestellt werden (Q&A).

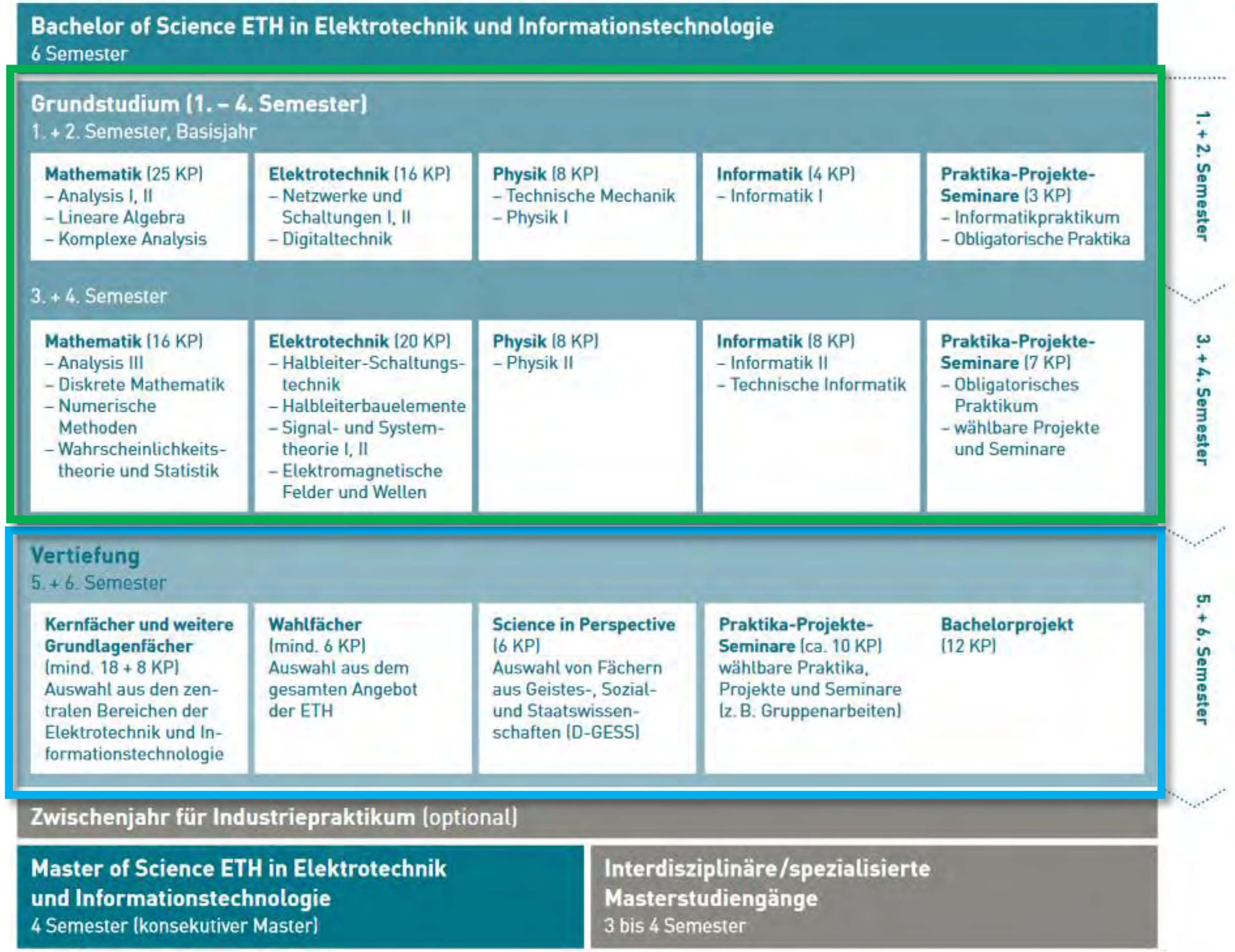
ETH zürich

Der Aufbau des Studiums am D-ITET

Reto Kreuzer, Studienkoordinator

D ITET

Zur Erinnerung: Der Aufbau des Bachelorstudiums



Bestandteile der Vertiefung im 3. Studienjahr

Kategorie	Was?	KP
Weitere Grundlagenfächer	Min. 2 aus einer Auswahl von 3 Fächern sind zu bestehen	min. 8
Praktika, Projekte, Seminare	im 2. und 3. Studienjahr zu erwerben, Liste von Angeboten in VVZ und auf Webseite des D-ITET, auch Fokus-Projekt	min. 15
Kernfächer	Mindestens 3 aus einer Liste von ca. 20 Fächern (siehe VVZ)	min. 18
Wahlfächer	Vorschläge sind im VVZ aufgeführt, aber Wahlfächer dürfen aus dem ganzen Angebot der ETH stammen, auch GESS-Fächer (Ausnahme: keine Praktika)	min. 6
Bachelorarbeit	Grosse Abschlussarbeit (kursbegleitend im 6. Semester)	12
Wissenschaft im Kontext (GESS)	Aus dem Angebot des D-GESS, können während des ganzen Studiums belegt werden	min. 6
frei zuteilbare Kreditpunkte (a.k.a. "ghost credits")	Diese Kreditpunkte können frei **jeder der oben aufgeführten Kategorien zugeteilt** werden	6

Weitere Grundlagenfächer

- Die **weiteren Grundlagenfächer** sind Teil des Grundstudiums (1. bis 4. Semester)
- Sie finden **ausschliesslich im Herbstsemester** statt
- Es müssen **2 aus 3** angebotenen Fächern bestanden und **8 KP** erworben werden
  - 227-0014-20 Computational Thinking, Prof. R. Wattenhofer
  - 227-0053-00 High-Frequency Design Techniques, Prof. C. Bolognesi
  - 227-0122-00 Introduction to Electric Power Transmission, Prof. Ch. Franck / Prof. G. Hug
- Weitere Informationen zu den finden Sie im Vorlesungsverzeichnis für das HS 2021

Siehe: https://ee.ethz.ch/de/studium/bachelorstudiengang/drittes-studienjahr/weitere-grundlagenfaecher.html

Praktika, Projekte und Seminare

In den Praktika, Projekten und Seminaren im zweiten und vor allem dem dritten Studienjahr sollen Studierende **praktische Kenntnisse und Fertigkeiten erwerben** aber auch das selbständiges Experimentieren und die Methodik von Projektarbeiten erlernen.

Das Angebot von "Praktika, Projekte, Seminare" umfasst folgende Angebote, aus denen mindesten **15 KP** erworben werden müssen:

- **P&S:** Praktika & Seminare
- Allgemeine **Fachpraktika** (max. 6 KP)
- **Gruppenarbeiten** (je 6 KP)
- Studierende des D-ITET könne auch an **Fokus-Projekten** (D-MAVT) teilnehmen (14 KP)

Siehe https://ee.ethz.ch/de/studium/bachelorstudiengang/drittes-studienjahr/praktika-projekte-seminare.html

Kernfächer und Vertiefungen

- Kernfächer dienen der **technischen Spezialisierung** in den verschiedenen Fachrichtungen der Elektrotechnik (**Vertiefungen**). Es müssen **18 KP** aus dieser Kategorie erworben werden.
- Auf der Website des D-ITET sind für folgende Vertiefungen im 3. Jahr **sinnvolle Fächerkombinationen für jede Vertiefung** publiziert:
  - Communications
  - Computers and Networks
  - Electronics and Photonics: *Integrated Circuits and Systems*
  - Electronics and Photonics: *Electronic and Photonic Materials and Devices*
  - Energy and Power Electronics
  - Biomedical Engineering
- Mehr dazu in den Präsentationen der einzelnen Vertiefungen im Anschluss

Siehe https://www.ee.ethz.ch/de/studium/bachelorstudiengang/drittes-studienjahr/kernfaecher.html

Wahlfächer

Weitere Fächer der **Vertiefung** (Kernfächer) **oder** ein **Blick über den Tellerrand**, z.B. in andere Ingenieurwissenschaften oder den Naturwissenschaften oder auch weitere GESS-Fächer.

Empfehlungen zur Wahl dieser Fächer sind im Vorlesungsverzeichnis publiziert, grundsätzlich steht aber das **ganze Kursangebot der ETH** zur Verfügung. Des Weiteren gilt:

- **Praktika** können **nicht** als Wahlfach **angerechnet** werden;
- Wahlfächer sollen dem **Niveau des dritten Studienjahres** des BSc EEIT entsprechen und sollen insbesondere nicht aus dem Basisjahr anderer Bachelorstudiengänge stammen, oder einen gleichem Inhalt wie bereits absolvierte Fächer haben;
- bei **Sprachfächern** gilt die **Weisung** zur Wissenschaft im Kontext (**GESS**) bezüglich der anrechenbaren Niveaus.

Siehe https://ee.ethz.ch/de/studium/bachelorstudiengang/drittes-studienjahr/wahlfaecher.html

Bachelor-Arbeit

- Das **Bachelorstudium wird mit einer Bachelor-Arbeit (12 KP) abgeschlossen**, sie steht unter der Leitung eines oder einer Professor*in;

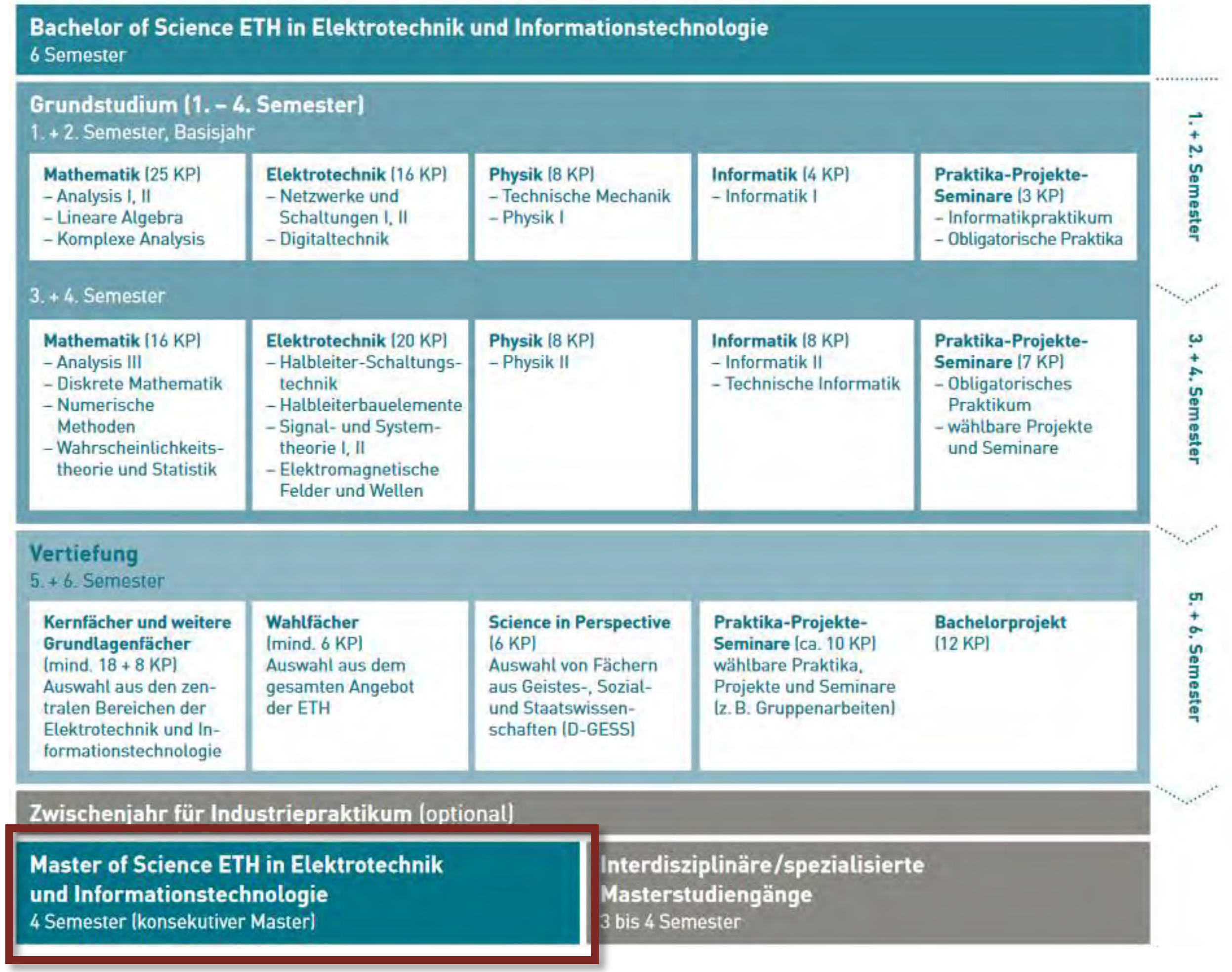
- die Arbeit entspricht einem Umfang ca. 360 Stunden und kann in Teil- oder Vollzeit durchgeführt werden. Sie wird in der Regel **kursbegleitend im 6. Semester** durchgeführt;

- die Bachelor-Arbeit soll die Studierenden erstmals in die **selbständige, strukturierte, methodische und wissenschaftliche** Tätigkeit einführen;

- die Themen und **Bedingungen** für Bachelor-Projekte werden **von den Betreuer*innen festgelegt** – das Thema kann dabei auch in Absprache mit den Studierenden festgelegt werden.

Siehe https://ee.ethz.ch/de/studium/bachelorstudiengang/drittes-studienjahr/bachelor-projekt.html

Der konsekutiver Masterstudiengang am D-ITET



Das Master-Studium (Studienreglement 2018)

Das Masterstudium ist wie folgt gegliedert:

– Kernfächer	24 KP
– Vertiefungsfächer	40 KP
– Semester-Projekt	12 KP
– Zur Wahl (Absprache Tutor*in)	12 KP
• Wahlfächer	
• Zweites Semester-Projekt	
• Industriepraktikum	
– Wissenschaft im Kontext (GESS)	2 KP
– Master-Arbeit	30 KP

Das Masterstudienreglement 2018 mit 120 KP gilt für Neueintritte (ohne ETH-Bachelor), Wiedereintritte (nach einer Exmatrikulation) und für Übertritte aus dem Bachelorstudiengang Elektrotechnik und Informationstechnologie nach Reglement 2018.

Kern- und Vertiefungsfächer

Auf Masterstufe ist eine weitere **Vertiefung des gewählten Fachbereichs** oder eine zusätzliche Vertiefung in einem neuen Fachbereich (siehe Website) möglich.

- ca. 4 Kern- und 7 Vertiefungsfächer (24+40 KP), in der Regel über **drei Semester** verteilt, Kursangebot im Vorlesungsverzeichnis unter *Master-Studium (Studienreglement 2018)*;
- **Kernfächer müssen zwingend aus der Liste im VVZ stammen** – bei Wahlfächern sind, in Absprache mit dem/der Tutor*in (D-ITET-Professor*in), auch Fächer ausserhalb möglich;
- Studierende **finden selbstständig** und spätestens bis Ende der vierten Semesterwoche **einen oder eine Tutor*in**, eine Liste findet sich auf der Website des D-ITET;
- Das Gespräch mit dem oder der Tutor*in zur Fächerwahl im Masterstudium wird mit dem **Learning-Agreement** abgeschlossen, einer verbindlichen Liste von zu absolvierenden Fächer (siehe *myStudies*, erst nach Einschreibung ins Masterstudium sichtbar).

Siehe https://ee.ethz.ch/de/studium/haupt-masterstudiengang/spezialisierungsrichtungen.html

Semester- und Masterarbeiten

Semester-Projekt/e (12 KP)

- Vertiefung der Einführung in das wissenschaftliche Arbeiten, betreut von einem oder einer Professor*in des D-ITET (oder assoziiert);
- Semester-Projekte dauern **14 Wochen** mit gleichzeitiger Fächerbelegung (Teilzeit) oder 7 Wochen bei Vollzeit-Bearbeitung;
- Einschreibung über *myStudies;*
- Projektangebote sind auf den Webseiten der Institute/Professuren publiziert;
- eine zweites Projekt ist möglich/anrechenbar.

Master-Arbeit (30 KP)

- Die Masterarbeit bildet den **Abschluss und Höhepunkt** des Studiums der Elektrotechnik und Informationstechnologie, sie dauert ein volles Semester (**6 Monate Vollzeit**) und wird unter der Leitung eines Professors/einer Professorin durchgeführt.

Siehe https://ee.ethz.ch/de/studium/haupt-masterstudiengang/projekte-und-masterarbeit.html

Exkurs zum Master-Studiengang nach Reglement 2008

Das Masterstudium nach Studienreglement 2008 umfasst 90 KP – weil aber alle Semester-Projekte seit HS 2018 i.S. der Gleichbehandlung mit 12 KP bewertet werden (früher 8 KP), müssen insgesamt 98 KP wie folgt erworben werden:

– Vertiefungsfächer	42 KP
– Zwei Semester-Projekte	je 12 KP
– Wissenschaft im Kontext (GESS)	2 KP
– Master-Arbeit	30 KP

Das Masterstudienreglement 2008 gilt **ausschliesslich** für Übertritte (keine Wiedereintritte!) aus dem Bachelorstudiengang Elektrotechnik und Informationstechnologie nach Studienreglement 2012 oder 2016 (Eintritte vor HS 2018, ohne Reglementswechsel).

Wer im HS 2021 lieber ins Master-Studium nach **Studienreglement 2018 übertreten** möchte, meldet sich bis 31. August 2021 beim Studiensekretariat (**info@ee.ethz.ch**).

Weiterhin viel Freude und Erfolg im Studium!

ETH zürich

Vertiefungsrichtung "Kommunikation"

Hans-Andrea Loeliger

Institut für Signal- und Informationsverarbeitung

Juni 2021

Was ist da drin?

Was ist da drin?

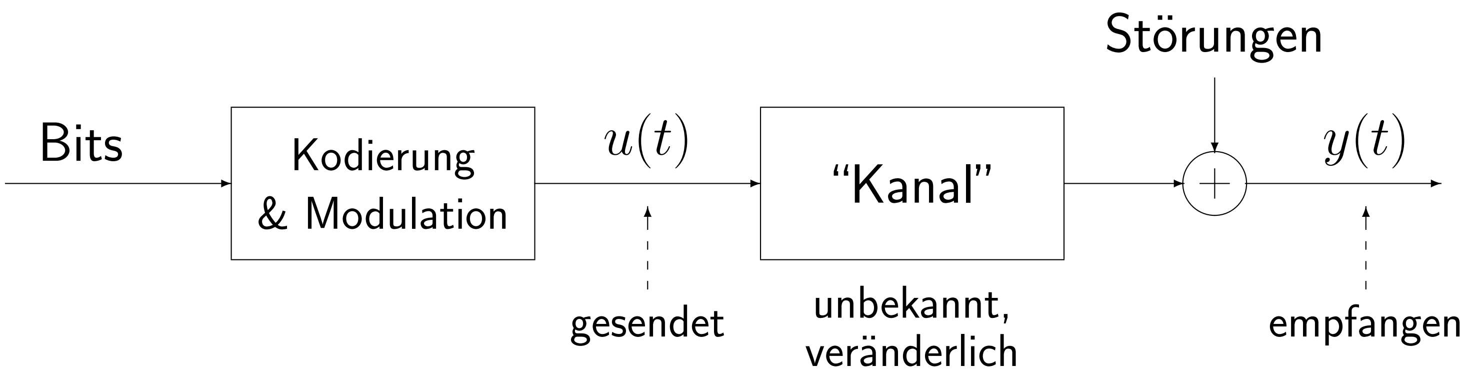
- Physik & Elektronik
- Digitaltechnik, Computertechnik, Software
- Signal- und Systemtheorie, Informations- und Kommunikations-theorie, Signalverarbeitung, ...

Gehört alles zusammen! Personifiziert durch

Claude Shannon (1916–2001)

- Entwurf digitaler Schaltungen mittels boolescher Algebra (Master-Arbeit, 1937)
- Abtasttheorem (1949)
- Begründer der Informationstheorie: Quantifizierung von "Information" und deren robuste (fehlertolerante) Kodierung (1948)
- Grundlegende Beiträge zur Kryptographie
- Computerschach (1950)
- Lebenslanger Bastler (mechanisch & elektrisch)

Themen der Nachrichtentechnik



- zeitdiskret $\leftrightarrow$ zeitkontinuierlich: Modulation & Demodulation
- "Inversion" des "Kanals" ($\approx$ Egalisation)
- Kanalschätzung
- robuste ($\approx$ fehlerkorrigierende) Kodierung und Dekodierung
- multi-input, multi-output (MIMO) Übertragung
- ...
- Realisierung in VLSI, digital und analog

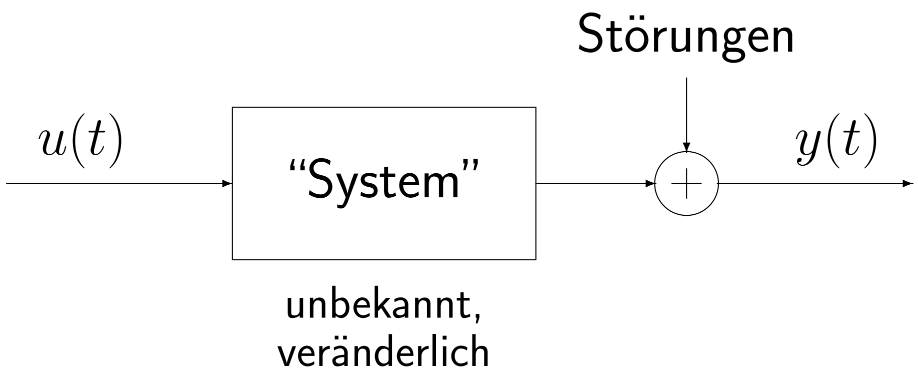
Information & Kommunikation

Die Fachgebiete

- Nachrichtentechnik
- Signalverarbeitung
- Maschinelles Lernen

haben keine klaren Grenzen und gehen ineinander über.

Beispielhafte Problemstellung:



Gegeben: $y(t)$; gesucht: $u(t)$

Signalverarbeitung, Beispiel 1:

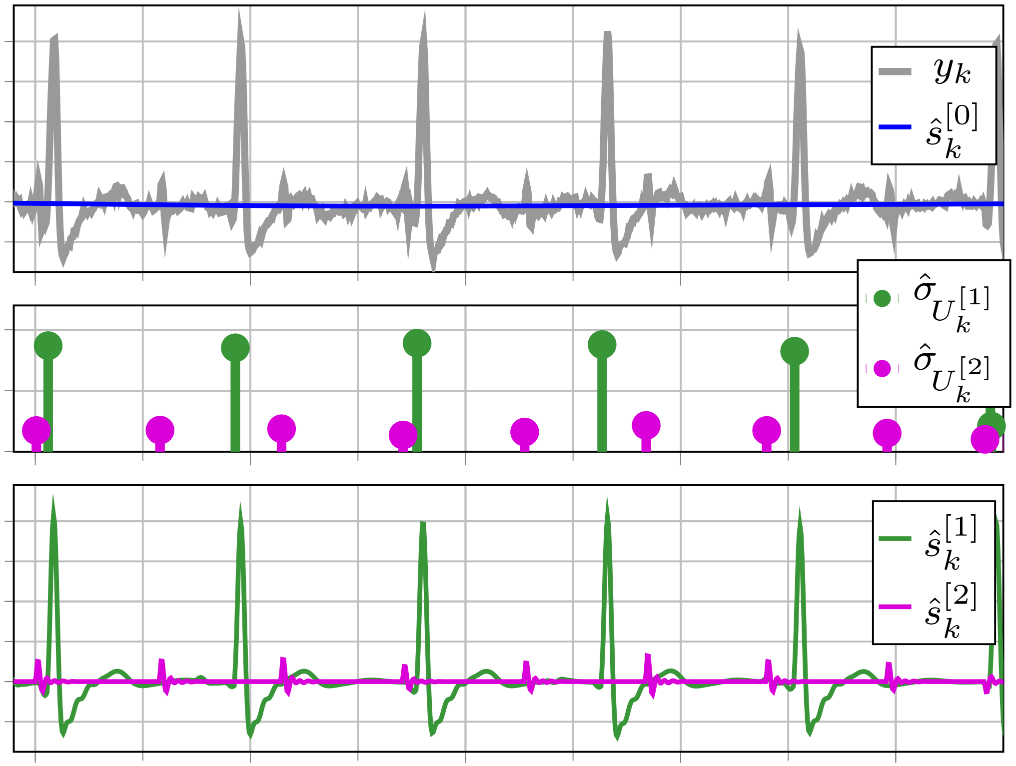
Computertomographie (CT)

Objekt,
wird zwischen Aufnahmen gedreht

Beispiel: Fast perfekte Rekonstruktion eines Objekts mit 256×256 $(= 65'536)$ Pixeln aus nur 12 Projektionen mit je 450 Sensorpixeln (d.h. aus total 5400 Sensorpixelwerten).

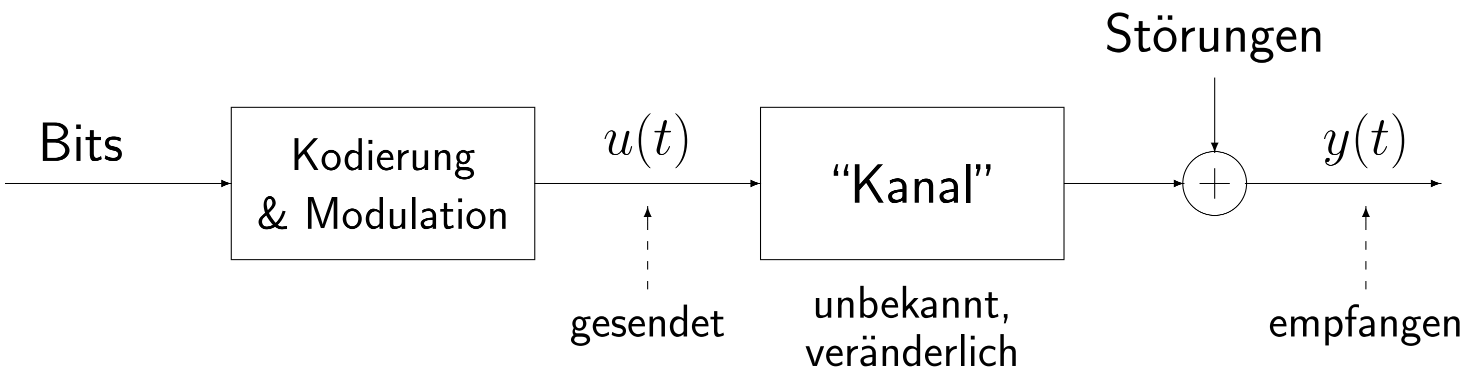
Signalverarbeitung, Beispiel 2:

“Blinde” Signaltrennung/Zerlegung



Beispiel: Automatische Trennung von EKG (Herzschlag) von schwangerer Frau und Kind. Die hier verwendete Methode ist nicht speziell auf EKG zugeschnitten und braucht keine Trainingsdaten *(unsupervised learning)*.

Themen der Nachrichtentechnik



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- ...
- Realisierung in VLSI, digital und analog

Vertiefung “Kommunikation”:

Empfohlene Fächer im Bachelorstudium

- Discrete-time & Statistical Signal Processing *(Loeliger)*
- Kommunikationssysteme *(Wittneben)*
- Communication & Detection Theory *(Lapidoth)*
- Communication Networks *(Vanbever)*

Ebenfalls passend:

- Introduction to Estimation and Machine Learning *(Loeliger)*
- Analog Integrated Circuits *(Huang)*
- Communication Electronics *(Huang)*
- VLSI I *(Gürkaynak, Benini)*
- High-Speed Signal Propagation *(Bolognesi)*
- Optics and Photonics *(Leuthold)*
- Elektromagnetische Wellen für Fortgeschrittene *(Leuchtmann)*
- Solid State Electronics and Optics *(Wood)*
- Biomedical Imaging *(Kozerke, Prüssmann)*
- ...

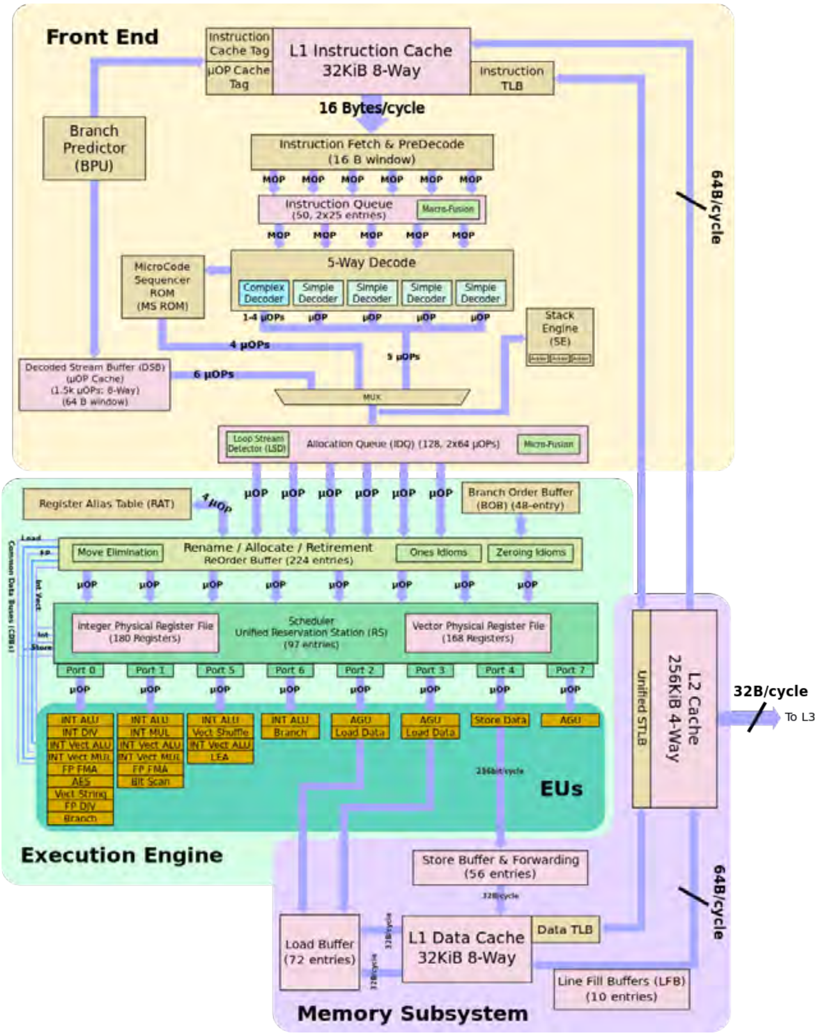
Computers and Networks
(and their security)

Prof. Kaveh Razavi
TIK, D-ITET

Computers and Networks

billions of transistors

billions of cycles per second



the complexity..

The New York Times

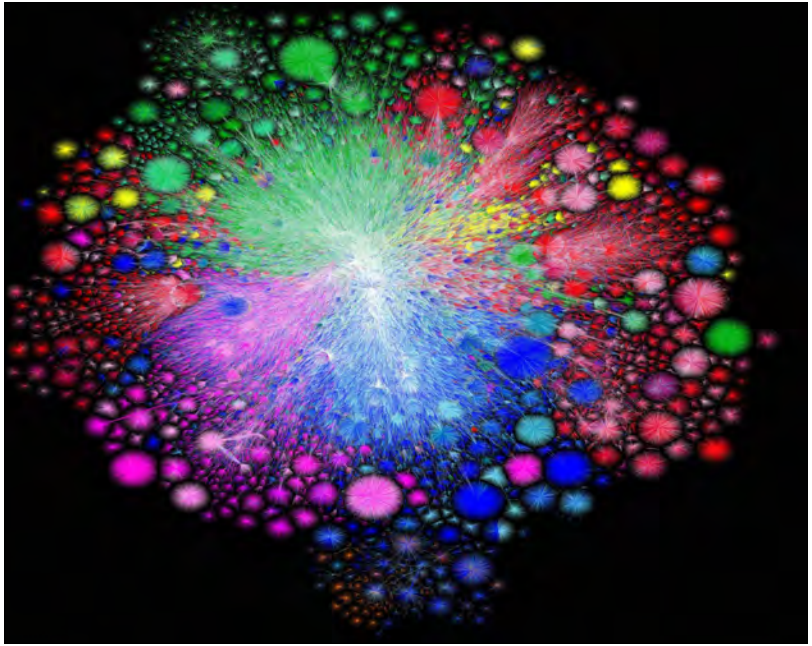
Intel Fixes a Security Flaw It Said Was Repaired 6 Months Ago

The chip maker patched several problems in May. Now it is issuing another fix, and researchers say the company hasn't been straight about its issues.

courtesy of Finn de Ridder (PhD candidate at TIK)

Computers and Networks

10s of billions of devices



Internet map (opte.org)

complexity everywhere!

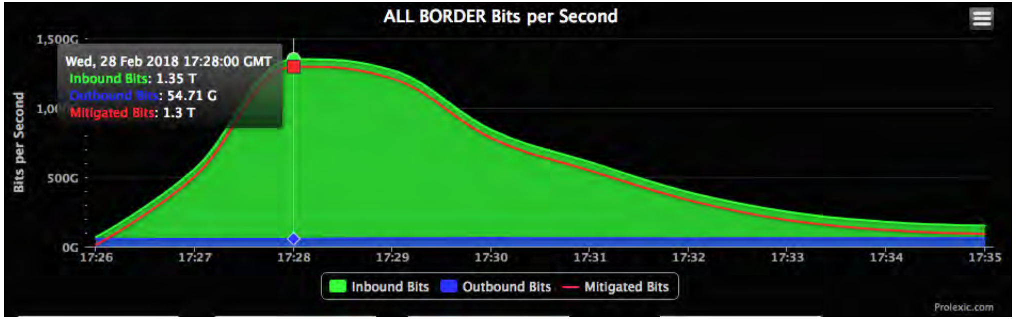
DDoS attack that disrupted internet was largest of its kind in history, experts say

Dyn, the victim of last week's denial of service attack, said it was orchestrated using a weapon called the Mirai botnet as the 'primary source of malicious attack'

- Major cyber attack disrupts internet service across Europe and US

Dyn estimated that the attack had involved '100,000 malicious endpoints', and the company said there had been reports of an extraordinary attack strength of 1.2 terabits (1,200 gigabytes) per second. Photograph: Alamy

Github was the target of the largest DDoS attack to date



The Guardian, Oct 2016

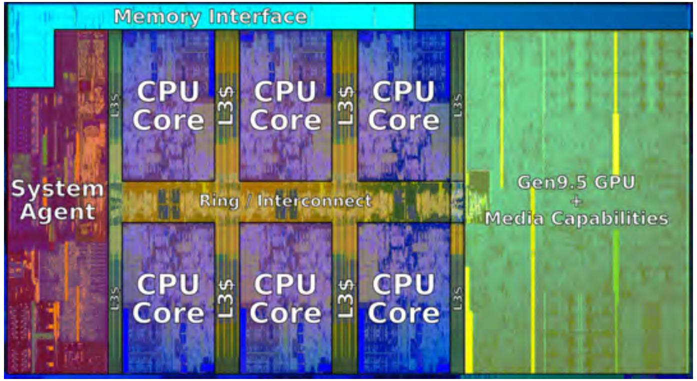
Akamai, Feb 2018

“Computers and Networks” as your specialization

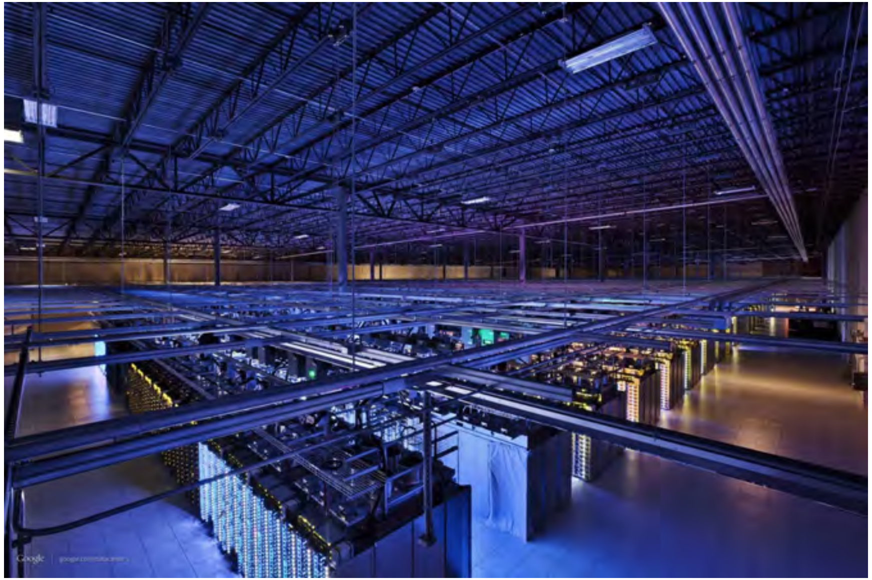
learn about and tackle this complexity in Computers and Networks by

- **analyzing** them
- **designing**, **building** and **operating** them
- **breaking** them apart and **securing** them.

At hardware-level



At systems-level



At algorithmic-level

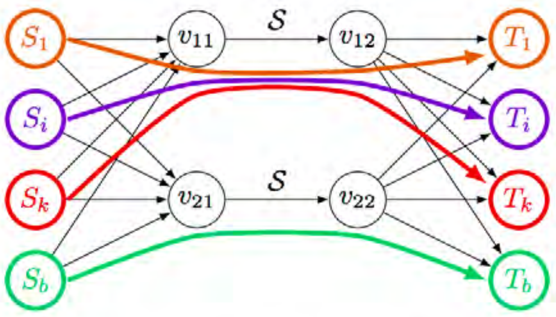


Fig. 9. In this network, there are k flows from $S_1, \ldots, S_k$ to $T_1, \ldots, T_k$ via the upper path v_{11}, v_{12} of combined size $\mathcal{S}$, and one flow from S_b to T_b via v_{21}, v_{22} of size $\mathcal{S}/2$. All edges have a capacity of $\mathcal{S}$. The task is to swap the assignments, i.e., move the k flows to the lower path, and the one bottom flow to the top path. Observe that the only consistent way to do so is to move flows of combined size $\mathcal{S}/2$ to the bottom path, then the bottom flow up, then the remaining flows down. As the k unsplittable flows correspond to a Partition instance, it is NP-hard to decide if this is possible.

Proposition 2. *The ECC value of a data word with a single bit asserted on a specific position is equal to the syndrome obtained when that specific bit is faulted.*

In the presence of an error $e = (e_1, e_2, \cdots, e_{k+r})$ with $e \neq 0_{1,k+r}$, $v' = v + e$, and because $S(v) = 0$, we can rewrite the syndrome as:

$$\begin{aligned} S(v+e) &= (v+e) \cdot H^T \\ &= v \cdot H^T + e \cdot H^T \\ &= S(v) + e \cdot H^T \\ &= e \cdot H^T \\ &= e \cdot ([-P^T | I_r]^T) \\ &= e \cdot ([-P^T | 0_{r,r}]^T + [0^T_{k,r} | I_r]^T) \end{aligned} \qquad (3)$$

Computer Engineering and Networks Laboratory (TIK)

Lothar Thiele

Computer Engineering

Roger Wattenhofer

Distributed Computing

Laurent Vanbever

Internet Systems

Kaveh Razavi

Computer Security

Computer Engineering and Networks Laboratory (TIK)

Lothar Thiele

Computer Engineering

Roger Wattenhofer

Distributed Computing

Laurent Vanbever

Internet Systems

Kaveh Razavi

Computer Security

Build efficient and useful distributed sensor networks

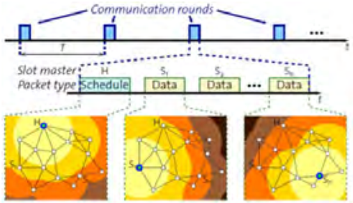
energy

when and for what should we use energy?

data

how do we calibrate unreliable sensors?

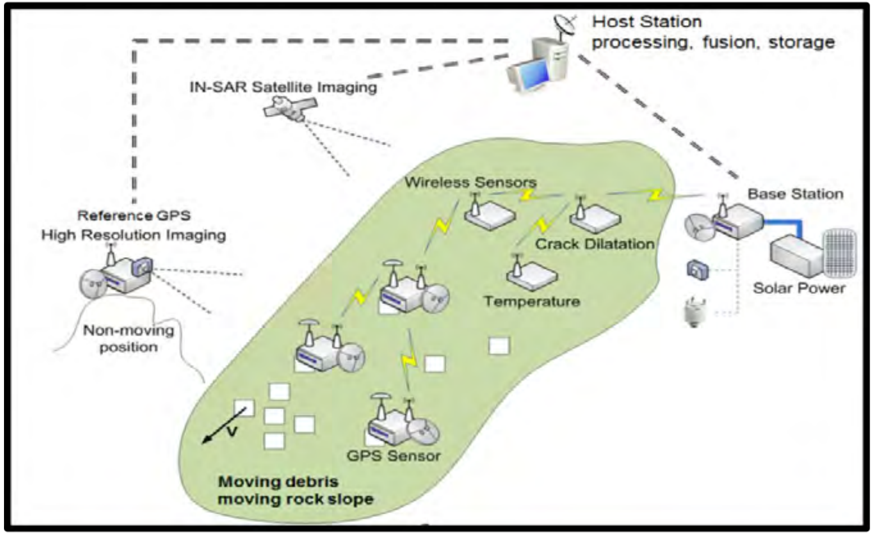
communication



how can we make communications
efficient, reliable, adaptive & precise?

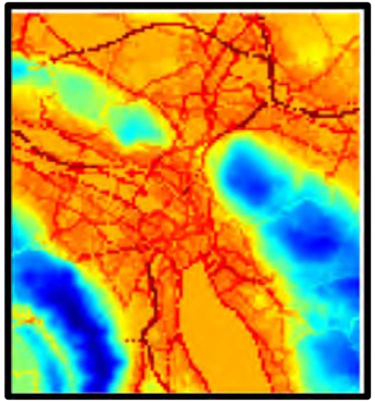
PermaSense

Monitoring Alpine regions at multiple scales



OpenSense

Environmental sensing in cities



Computer Engineering and Networks Laboratory (TIK)

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Distributed Computing

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Internet Systems

Kaveh Razavi

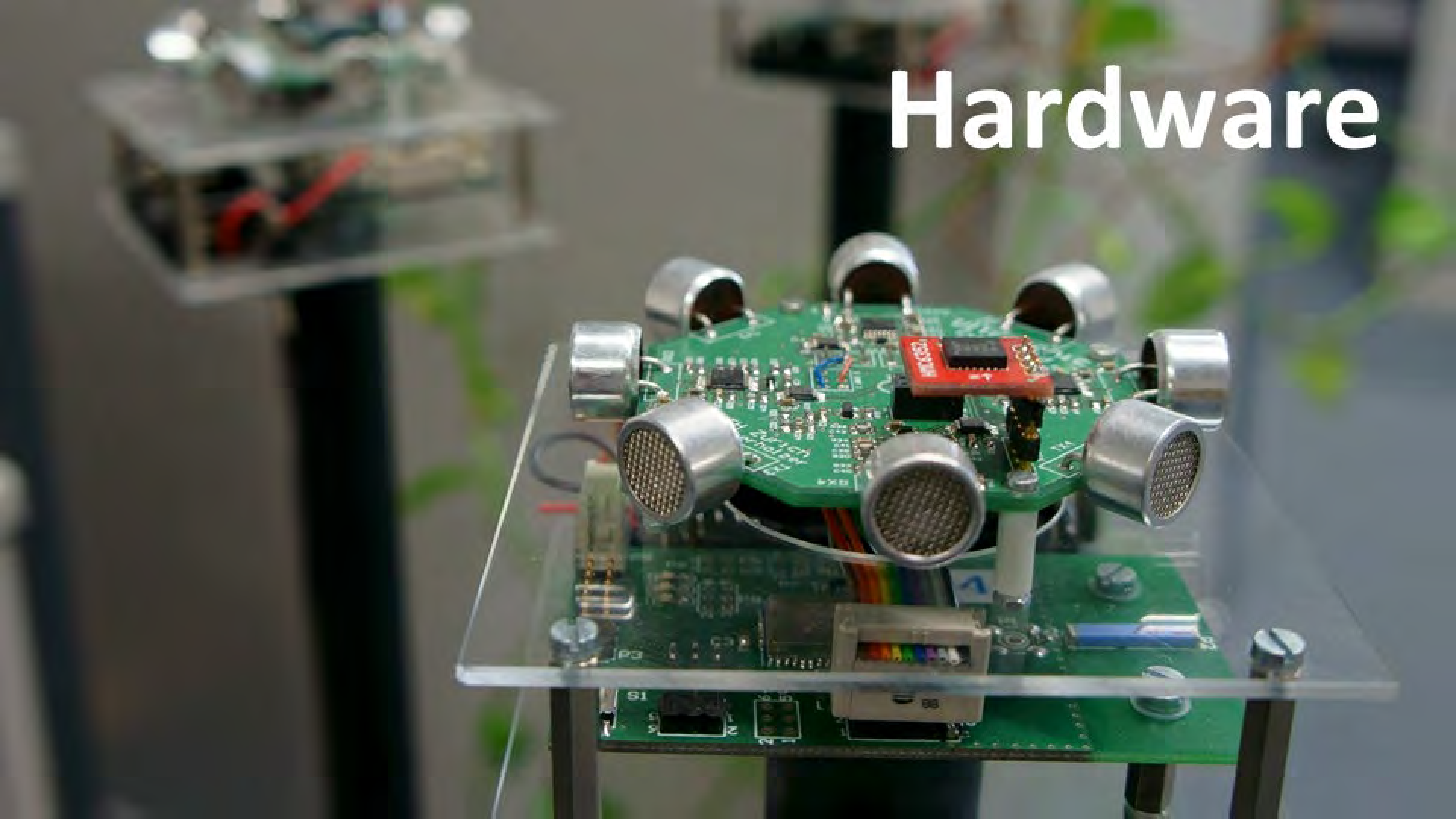
Computer Security

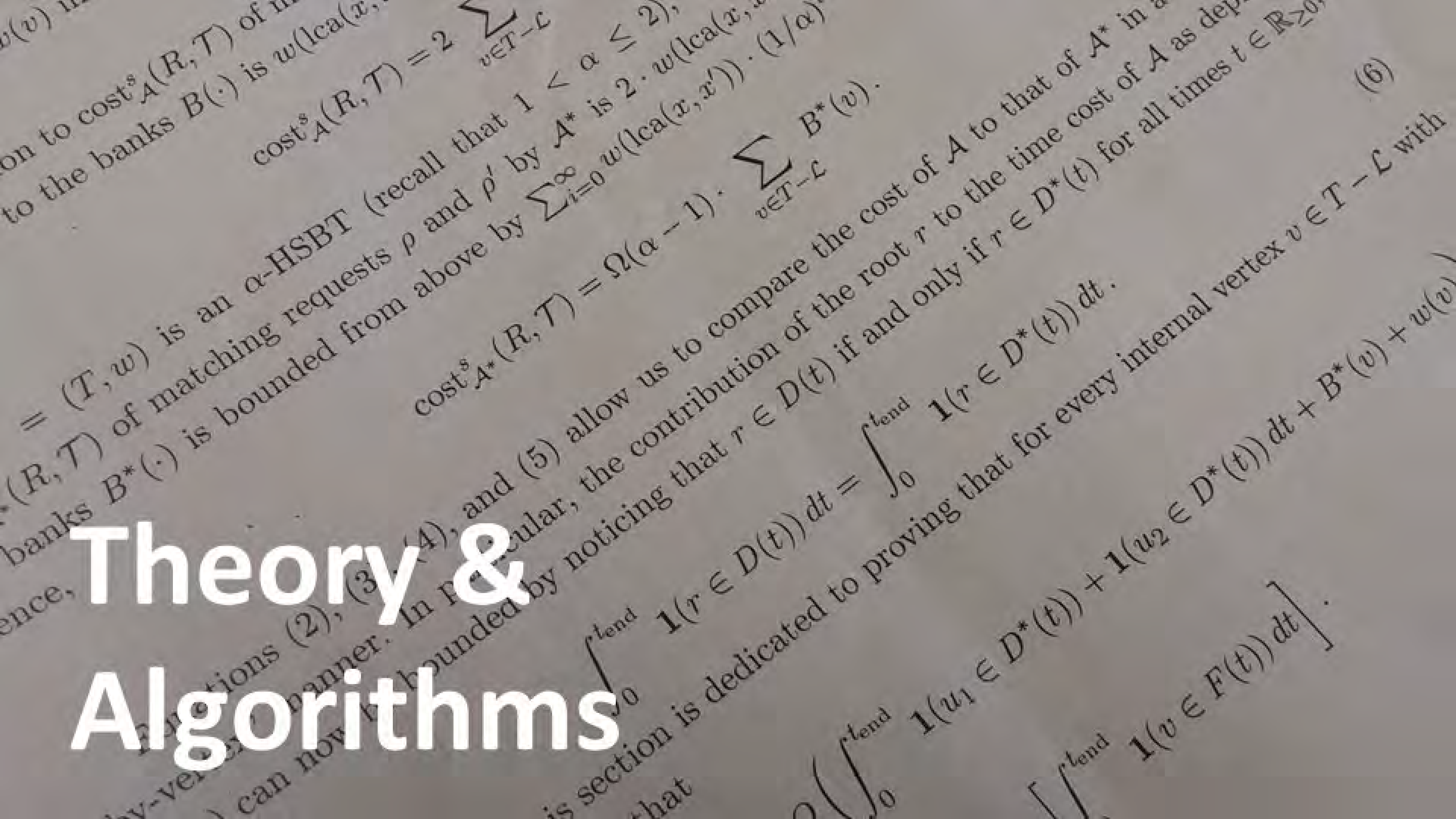
Networks
Social Networks
Neural Networks
Mobile Networks
Wireless Networks
Financial Networks
Economic Networks
Biological Networks
Computer Networks

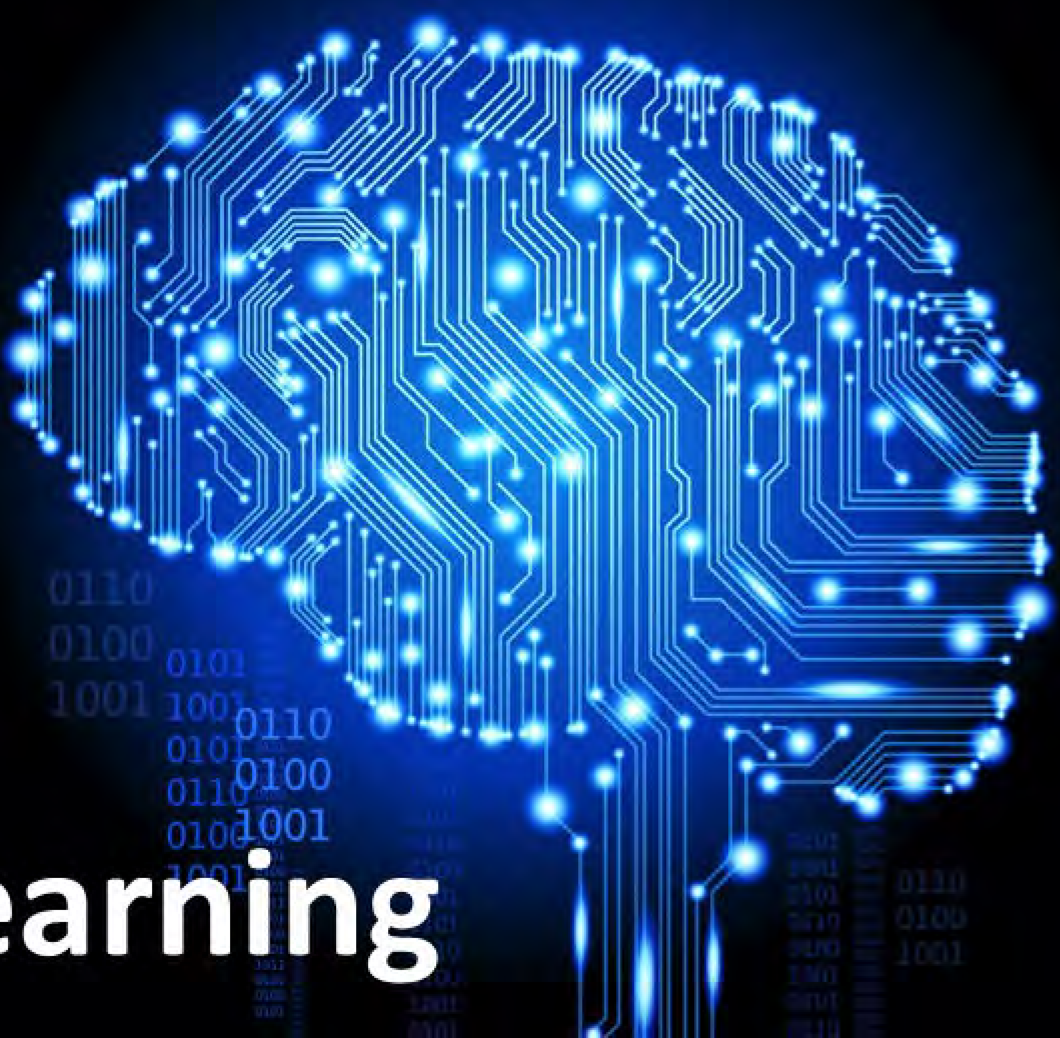
Data & Analysis

Software


Echofon
Facebook
iTunes
CameraBag
TED
Camera
Byline
Contacts
Bebot
Photos
App Store
NetNewsWire
Showtimes
Hipstamatic
Clock
Calendar
Tweetie
Settings
YouTube


Hardware


Theory &
Algorithms



Machine Learning

Computer Engineering and Networks Laboratory (TIK)

Lothar Thiele

Computer Engineering

Roger Wattenhofer

Distributed Computing

Laurent Vanbever

Internet Systems

Kaveh Razavi

Computer Security

Solving recurring problems in the Internet

considering a wide variety of dimensions

Manageability and reliability

Scalability

Security

Solving recurring problems in the Internet

considering a wide variety of dimensions

Manageability and reliability

poorly designed interfaces
low level of automation

Scalability

Security

Traders work on the floor of the New York Stock Exchange (NYSE) in July 2015. (Photo by Spencer Platt/Getty Images)

DOWNTIME

UPDATED: "Configuration Issue" Halts Trading on NYSE

The article has been updated with the time trading resumed.

A second update identified the cause of the outage as a "configuration issue."

A third update added information about a software update that created the configuration issue.

Operators of the **New York Stock Exchange** have identified the culprit in the trading venue's 3.5-hour outage Wednesday, blaming the incident on a "configuration issue."

"The New York Stock Exchange and NYSE MKT experienced a technical issue and, consistent with our regulatory obligations, the decision was made to suspend trading as we worked to identify the cause and resolve it," a NYSE spokesperson said in an emailed statement. "The root cause was determined to be a configuration issue."

The company issued an update Thursday, saying the configuration issue happened during the roll-out of a software update to comply with new time-stamp requirements for exchanges.

After it suspended all trading, NYSE, owned by **Intercontinental Exchange** (ICE), said the outage was not caused by a cyber attack.

The company did not provide much detail about the cause of the outage, but posted updates on Twitter and on its own website while the outage lasted, saying it was "doing our outmost to produce a swift resolution and will be providing further updates as soon as we can."

Forbes / Personal Finance

11,261 views

United Airlines Blames Router for Grounded Flights

Alexandra Talty,

FOLLOW ON FORBES (110)

FULL BIO

After a computer problem caused nearly two hours of grounded flights for United Airlines this morning and ongoing delays throughout the day, the airline announced the culprit: a faulty router.

Spokeswoman Jennifer Dohm said that the router problem caused "degraded network connectivity," which affected various applications.

A computer glitch in the airline's reservations system caused the Federal Aviation Administration to impose a groundstop at 8:26 a.m. E.T. Planes that were in the air continued to operate, but all planes on the ground were held. There were reports of agents writing tickets by hand. The ground stop was lifted around 9:47 a.m. ET.

Thousands of passengers were stranded after a computer glitch – apparently, cause by a router issue – grounded United Airlines flights worldwide. Photo by Justin Sullivan/Getty Images.

James Record, a professor of aviation at Dowling College told CNN Money that these kinds of problems occur at least several times a year and that, "This incident reflects the fact that much of the airline industry's computer and technology programs are old and have been cobbled together."

The New York Stock Exchange was also down today due to a computer glitch, which caused trading on the NYSE to halt for nearly two hours. The Wall Street Journal's homepage was also down as well. Department of Homeland Security Secretary Jeh Johnson said there was no indication that these incidents were related.

This was the latest in a string of computer issues for United since the company switched to the computer system used by merger partner Continental Airlines in 2012. A similar computer glitch occurred on June 2.

Solving recurring problems in the Internet

considering a wide variety of dimensions

Manageability and reliability

Scalability

too much redundant state, about too many things

Security

Scalable routing systems maintain:

- detailed information about nearby destination
- coarse-grained information about far-away destination

the Internet maintains
detailed information about every destination

Sign Post Forest, Watson Lake, Yukon

RISK ASSESSMENT / SECURITY & HACKTIVISM

Internet routers hitting 512K limit, some become unreliable

Table limit in some routers causes minor Internet outages; more to come.

by **Robert Lemos** - Aug 13, 2014 9:03pm CEST

Share Tweet 124

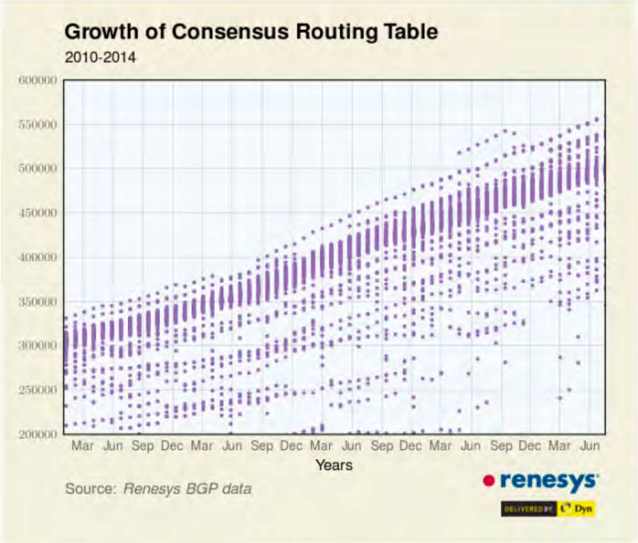


Chart courtesy of Renesys, a subsidiary of Dyn

From performance issues at hosting provider Liquid Web to outages at eBay and LastPass, large networks and websites suffered a series of disruptions and outages on Tuesday. Some Internet engineers are blaming the disruptions on a novel technical issue that impacts older Internet routers.

At the heart of the issue, the growth of routable networks on the Internet overwhelmed the amount of memory set aside in infrastructure hardware, typically routers and switches, that determines the appropriate way to route data through the Internet. For the first time, the lists of routable networks—also called border gateway protocol (BGP) tables—surpassed a significant power of two (two to the 19th power or 512K). Many older routers limit their use of a specialized, and expensive, type of memory known as ternary content-addressable memory (TCAM) to 512K by default.

Have fun solving these problems with state-of-the-art networking hardware: Reprogrammable switches with 12.8 Tbps of capacity

Computer Engineering and Networks Laboratory (TIK)

Lothar Thiele

Computer Engineering

Roger Wattenhofer

Distributed Computing

Laurent Vanbever

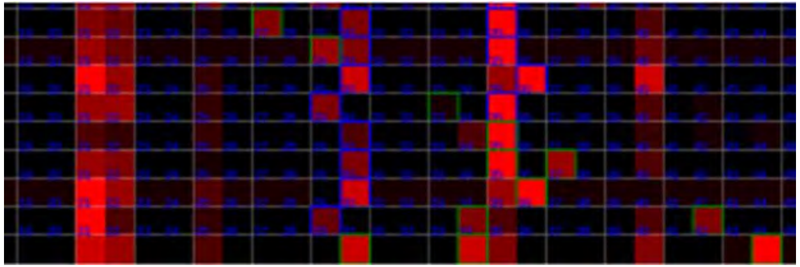
Internet Systems

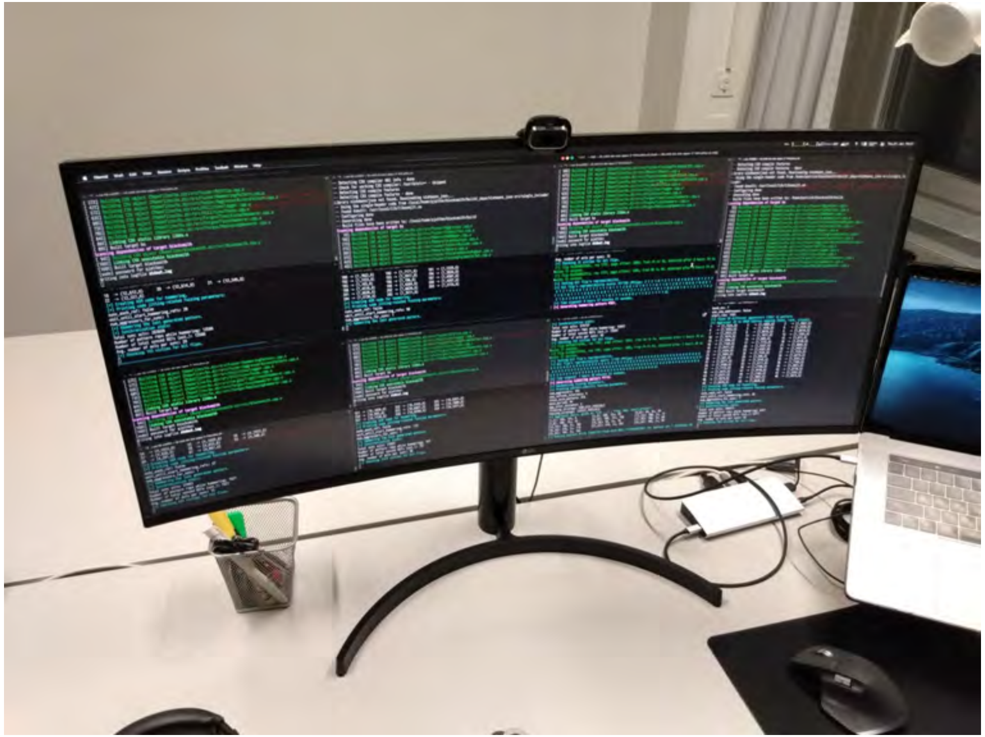
Kaveh Razavi

Computer Security

Goal: construction of reliable and secure systems

considering all layers of the computing stack





Requirement 2. *The overestimation error of a given entry should be limited to a known value.*

From Axiom 1, $1-\delta$ is the probability of having a maximum error of $\varepsilon \times M$. We now refer to a more recent extension of count-min [19], which generalizes the probability, decoupling it from e. The estimation and its probability are:

$$\hat{a}_i \leq a_i + w \times M(t) \tag{4}$$

$$P_r \geq 1 - \left(\frac{1}{w \times k}\right)^t \tag{5}$$

(a) A custom shunt probe.

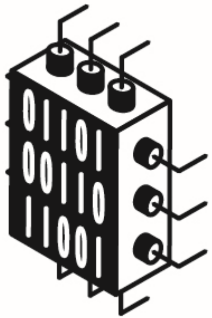
(b) Tweezers short-circuiting DQ_0 and V_{SS}.

Fig. 2: Fault injection with the help of syringe needles.

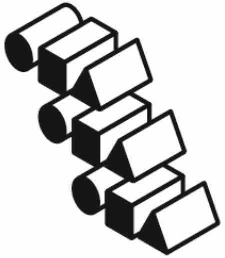
Proposition 2. *The ECC value of a data word with a single bit asserted on a specific position is equal to the syndrome obtained when that specific bit is faulted.*

In the presence of an error $e = (e_1, e_2, \cdots, e_{k+r})$ with $e \neq 0_{1,k+r}$, $v' = v + e$, and because $S(v) = 0$, we can rewrite the syndrome as:

$$\begin{aligned} S(v+e) &= (v+e) \cdot H^T \\ &= v \cdot H^T + e \cdot H^T \\ &= S(v) + e \cdot H^T \\ &= e \cdot H^T \\ &= e \cdot ([-P^T|I_r]^T) \\ &= e \cdot ([-P^T|0_{r,r}]^T + [0^T_{k,r}|I_r]^T) \end{aligned} \tag{3}$$



DRAM security



microarchitural security

OS security

peripheral security

What about courses?

learn about and tackle this complexity in Computers and Networks by

- **analyzing** them
- **designing**, **building** and **operating** them
- **breaking** them apart and **securing** them.

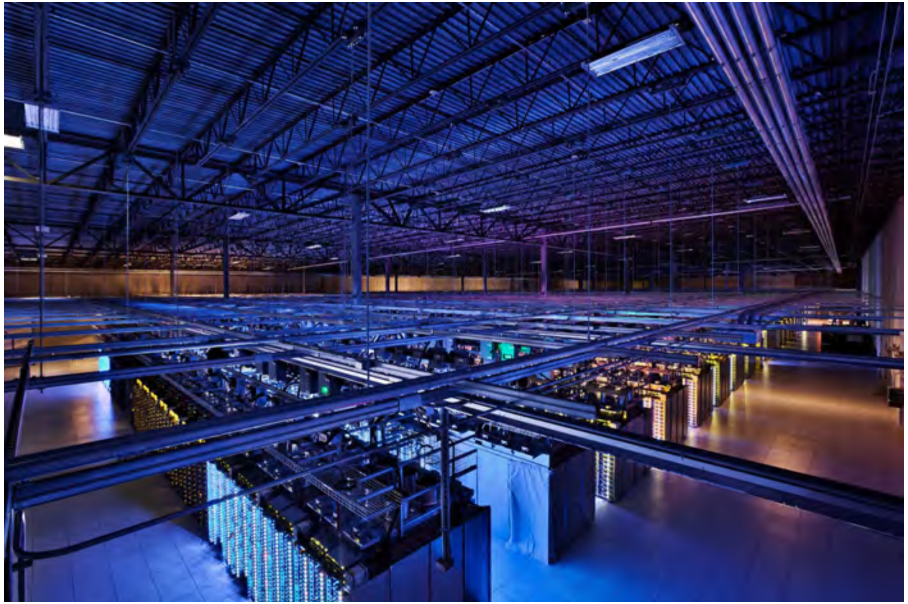
Bachelor (3rd year)

Autumn	Discrete Event Systems
	Communication Systems
Spring	Communication & Detection Theory
	Communication Networks
	Embedded Systems

Communication Networks

Understand how the Internet works and why

from your network plug…



to Google’s data centers

By building your own Internet!

Master (core subjests)

Autumn	Hardware Security Network Security Hardware/Software Codesign Advanced Topics in Communication Networks System Security Low-Power System Design
Spring	Principles of Distributed Computing

+ 20 recommended subjects/specializations

Hardware Security: build the attacks yourself!

What do you do with a
Master in Computers and Networks?

Plenty!

Work for top tech companies

Create your own startup

BITSPLITTERS

Get Your Guide

uepaa! SWISS ALPINE TECHNOLOGY

SYNVO Synthetic Voices

STREAM FORGE

You do a PhD! (hopefully with us)

~50 PhD candidates

~7 PhD theses per year

~90,000 citations

Computer Engineering and Networks Laboratory (TIK)

Lothar Thiele

Roger Wattenhofer

Laurent Vanbever

Kaveh Razavi

Come work with us!

Specialization Area:

Electronic and Photonic Materials and Devices

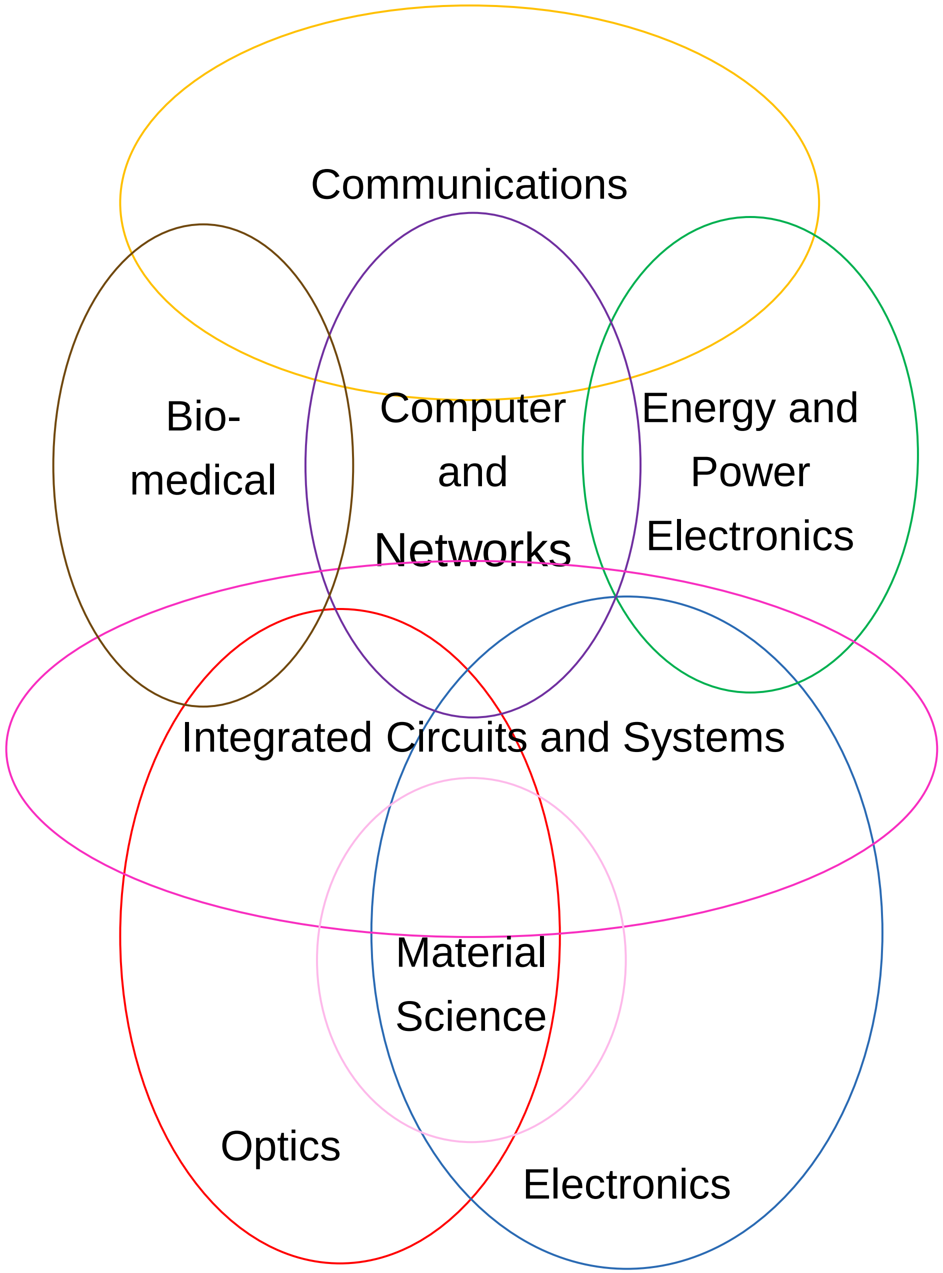
My Advise

Mathematics

System

Circuit

Physics & Material Science



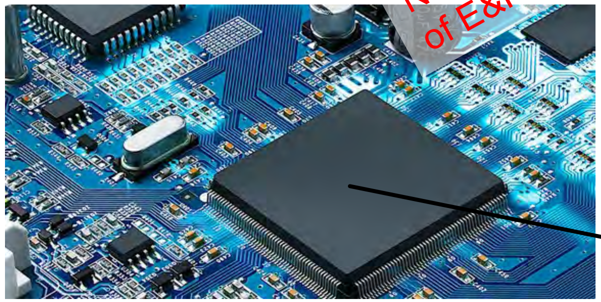
What is “Electronics and Photonics” About?

This is a full fledged biomedical apparatus

Not strength of E&P!

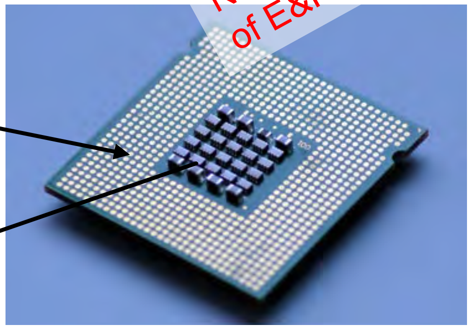
Powerful Integrated circuits

Not strength of E&P!

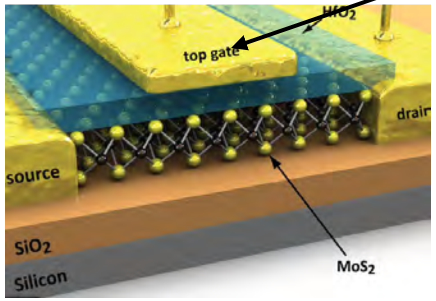


Electrical chip

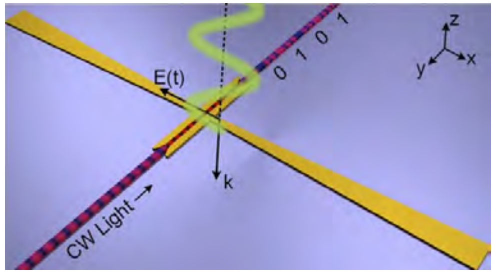
Not strength of E&P!



Latest electrical device



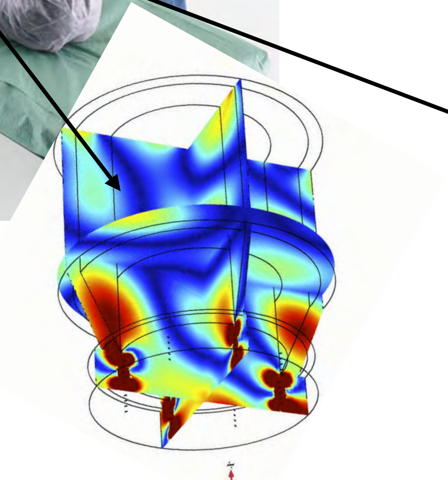
Novel sensors – enabled by latest nanoscale technology



New algorithm

Not strength of E&P!

3D Electromagnetic field simulations



What is “Electronics and Photonics” About?

- It is the “smart stuff” that drives the world of tomorrow

Novel display – quantum engineered materials

Flexible Electronics

Integrated circuits

Ultra-dense battery

On-chip-optical interconnected

Network-on-chip

High-speed wireless link

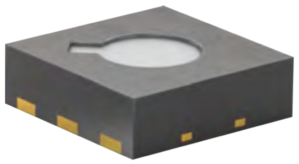
Novel sensors – enabled by latest nanoscale technology

What is “Electronics and Photonics” – It is about Components

Others build the car

ublox

II-VI

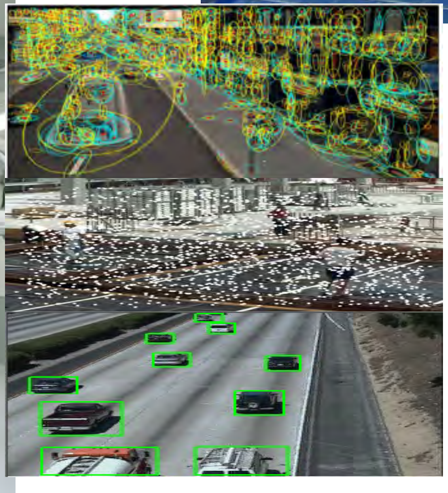


SENSIRION
THE SENSOR COMPANY

The Components may go Anywhere

Energy Harvesting

Communications: Wired and wireless



Traffic

Medical Apparatus

Getting the fundamentals: Fall 2021 and Spring 2022

Foundation Core Courses:

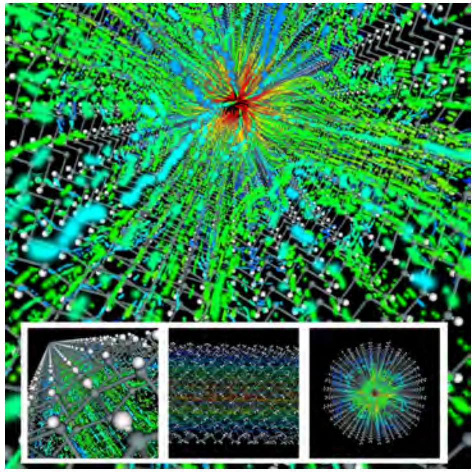
- **VLSI 1: HDL based design for FPGAs**
- **VLSI 2: Design of Very Large Scale Integration Circuits**
- **Analog Integrated Circuits**
- **High-Speed Signal Propagation**.
- **Solid State Electronics and Optics**
- **Optics and Photonics**.
- **Electromagnetic Waves: Materials, Effects, and Antennas –** Optical and RF-fields
- **Fundamentals of Physical Modeling and Simulations**

Many complementary courses found in Circuits & Integrated Systems, Communications, Computers and Networks, Energy and Power Electronics, and Biomedical Engineering and Neuroinformatics.

A Selection of Lectures 2021 and beyond…

Example Courses for 6th, 7th and 8th Semesters:

- Quantum Transport for Engineers
- Nano-Optics
- Organic and Nano Optoelectronics
- Nonlinear Optics
- Optical Communications Fundamentals

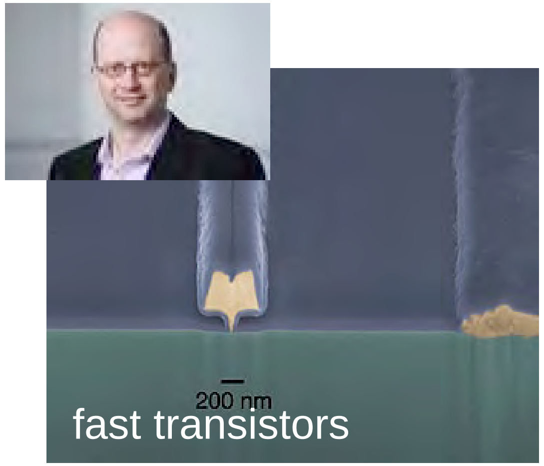


Where do electrons go?

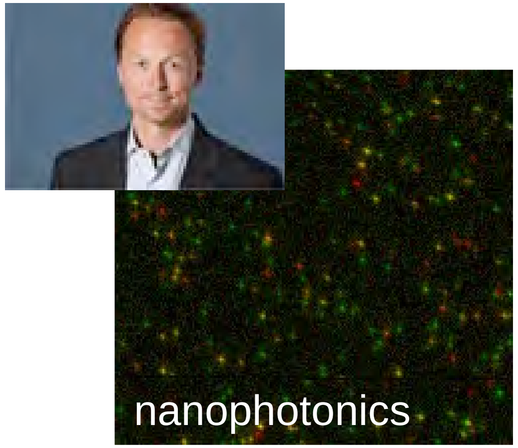
OLEDs, QLEDs

Who is who?

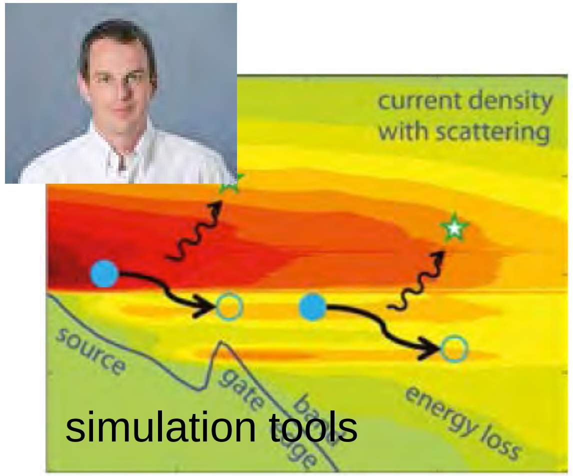
Prof. Colombo Bolognesi



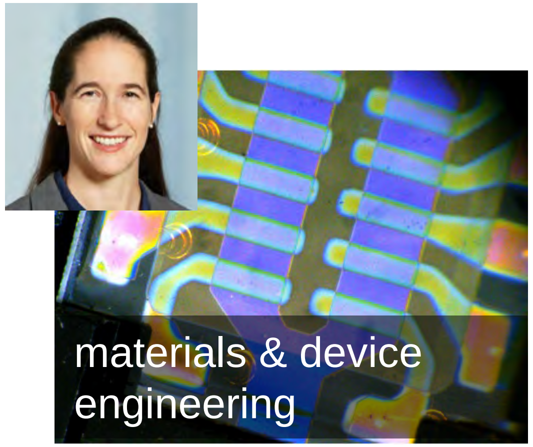
Prof. Lukas Novotny



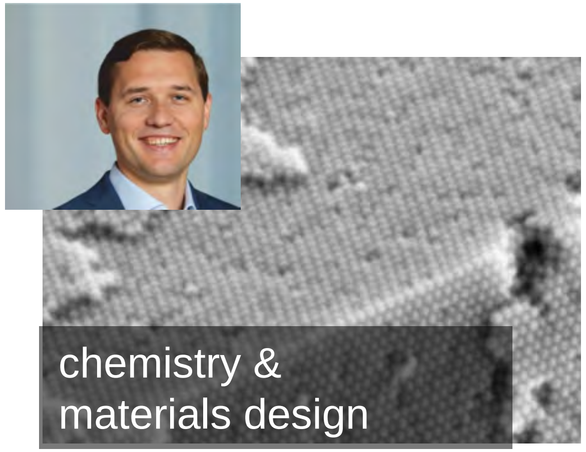
Prof. Mathieu Luisier



Prof. Vanessa Wood



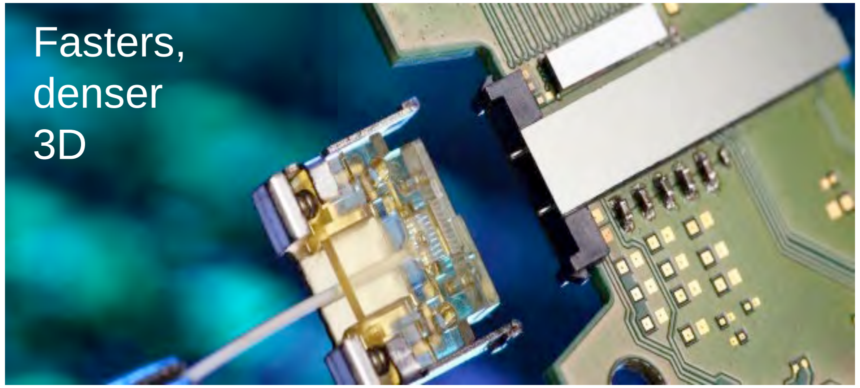
Prof. Maksym Yarema



Prof. Jürg Leuthold

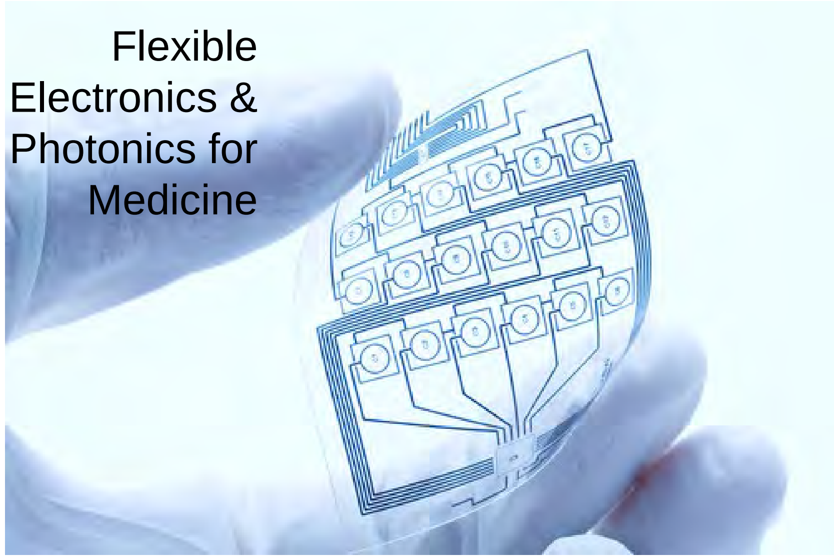
ETH zürich

What will electronic and photonics research enable in 10 to 20 years?



Fasters, denser 3D

Next generation solar

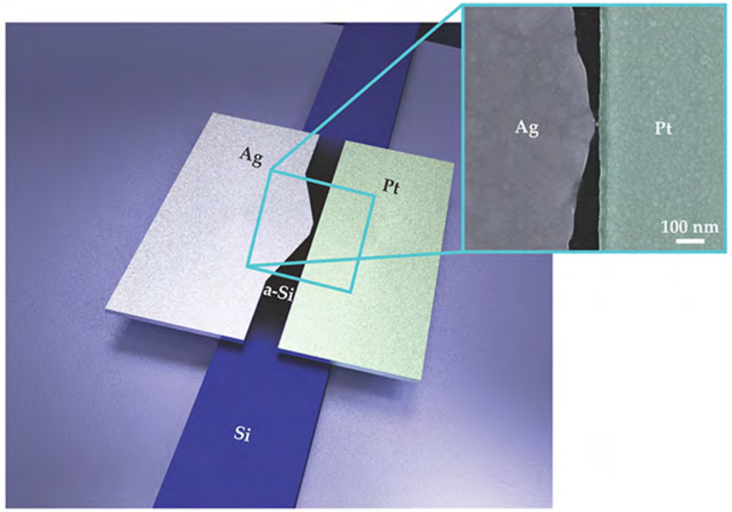


Flexible Electronics & Photonics for Medicine

Next generation computing

Electronics and Photonic Reesarch

Opportunities in theory, simulation, and experiments ranging from electronics, optics, material and device development and characterization



World's smallest integrated optical switch

Ultrafast light sources driven by quantum tunneling

Memristors
Phase change memory
Single photon sources

Neuromorphic computing

Quantum computing

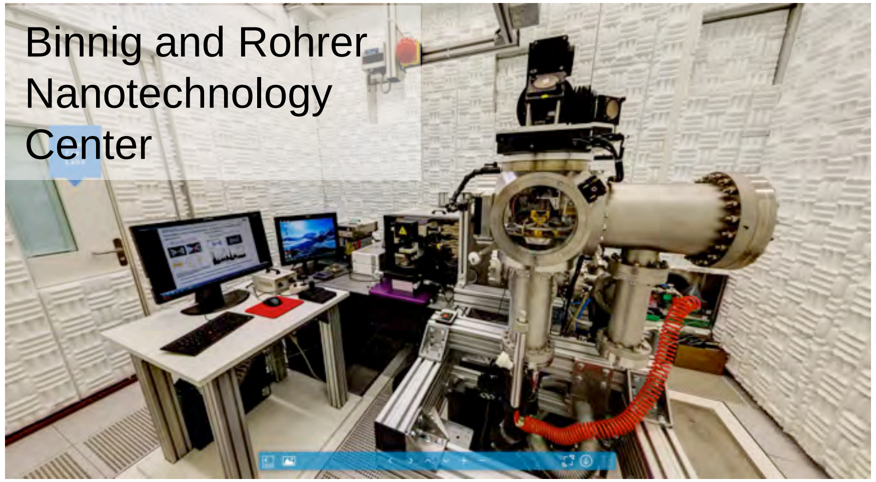
Batteries

Devices for sensing and detection

Optical & Wireless Communications

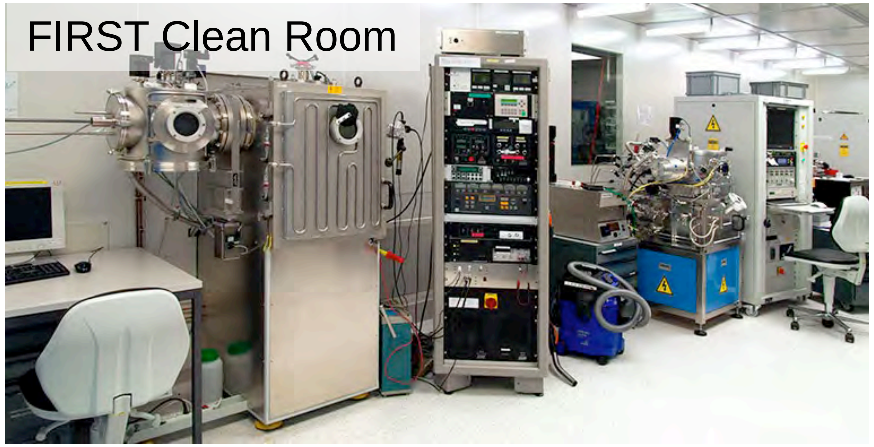
State of the Art Facilities

Integrated into coursework (Praktika, Gruppenarbeit, ….)



Binnig and Rohrer Nanotechnology Center

CSCS



FIRST Clean Room

The Jobs

Internships, thesis projects, collaborations …

ETH zürich

Vertiefungsrichtung

«Energietechnik und Leistungselektronik»

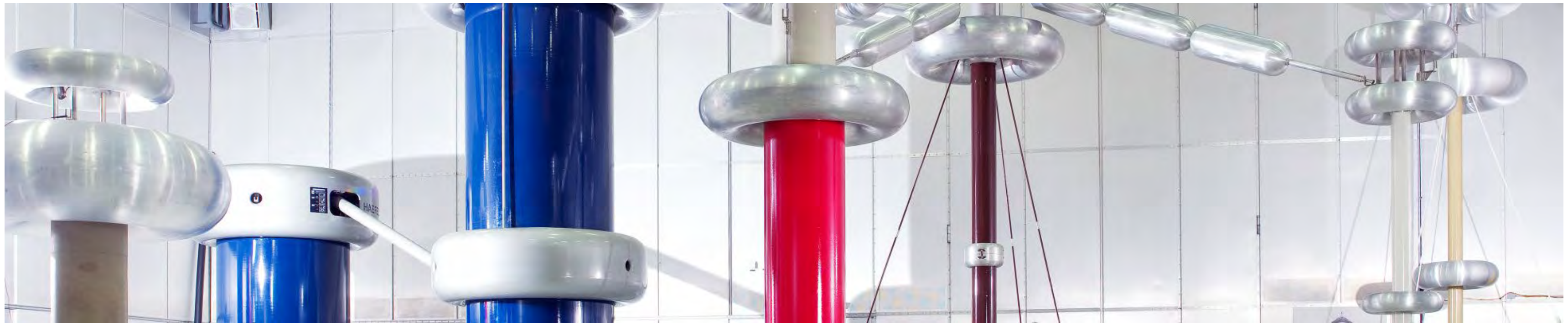
Ulrike Grossner

Two of the «Top 15 Global Challenges»: Energy & Environment

Wir sind am Beginn eines grundlegenden Wandels unseres Energiesystems:

Erneuerbare statt fossile (und nukleare) Brennstoffe; starker Fokus auf Energieeffizienz!

Die elektrische Energietechnik hat hierbei eine Schlüsselrolle!



Energietechnik am D-ITET

J. Biela: High Power Electronics / Solid State Pulsed Power — HPE Laboratory for High Power Electronic Systems

Ch. Franck: High Voltage Engineering / Power Transmission Technology — HVL High Voltage Laboratory

U. Grossner: Advanced Power Semiconductors, Packaging — APS

G. Hug: Electric Power Systems — PSL Power Systems Laboratory

J. Kolar: Power Electronic Systems / Mechatronics — PES Power Electronic Systems Laboratory

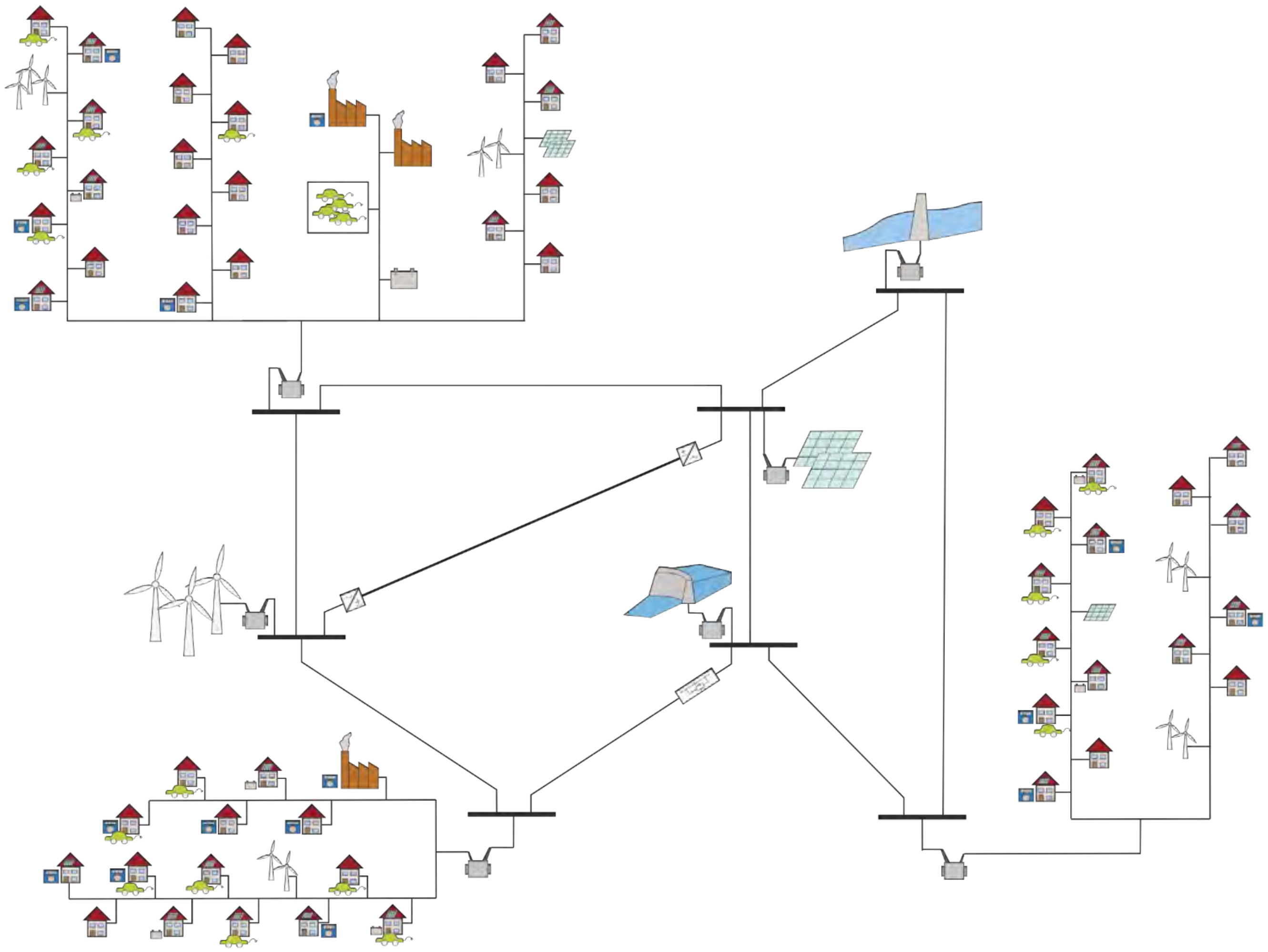
- Anwendungsorientierte und interdisziplinäre Projekte
- Intensive Industriekollaboration

Forschungsbeispiel – Management von Verteilten Ressourcen

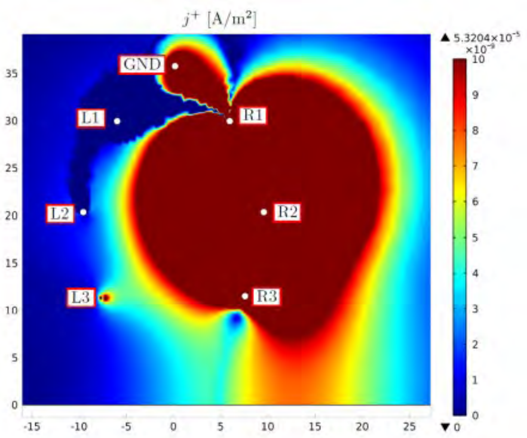
Ziel:
Flexibilität verteilter Ressourcen zum Balancieren von erneuerbaren Energien nutzen

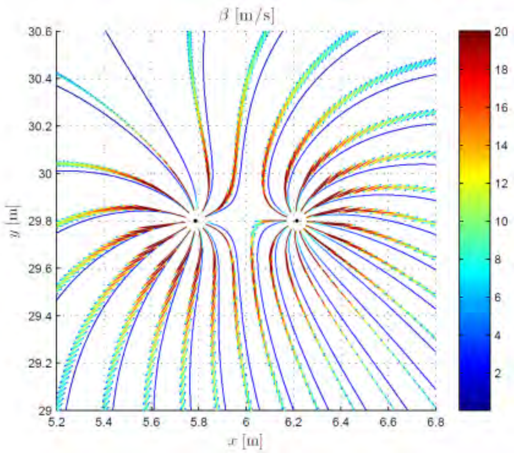
Komponenten:
Demand Response, elektrische Autos, Speicher, erneuerbare Energien (bulk und verteilt), Speicher, HVDC, FACTS

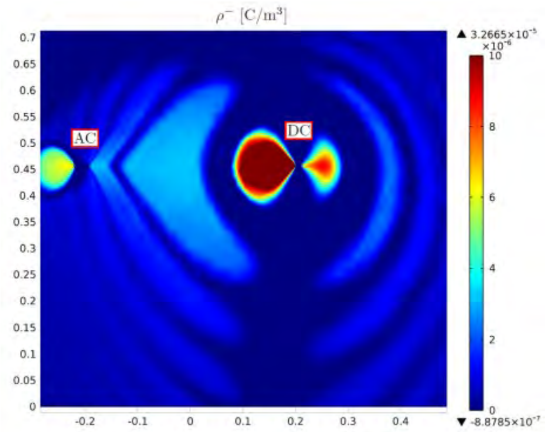
Methoden:
Koordination von Ressourcen anhand verteilter, aber koordinierter Intelligenz mit Einbezug von Kommunikation; inklusive Integration in Märkte



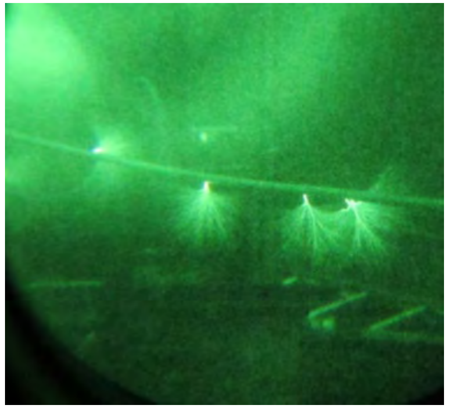
Forschungsbeispiel – Hybride AC/DC Freileitungen

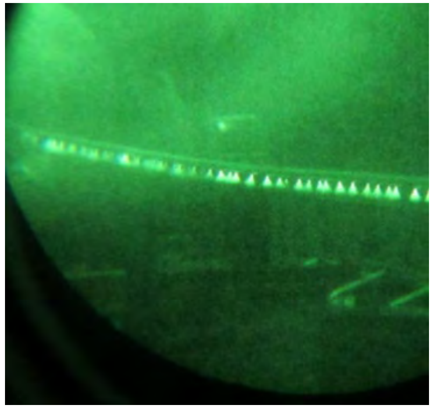






Berechnung der gegen-
seitigen Beeinflussung der
Systeme





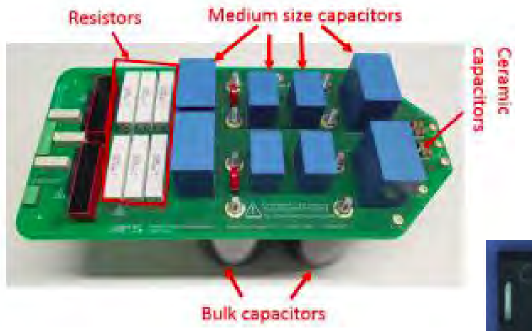
Verifikation der
Simulationsmodelle
im Labor

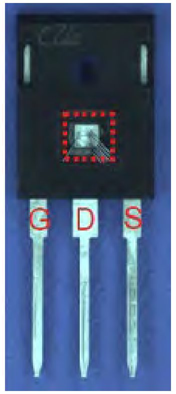
Forschungsbeispiel – Induktives Laden von E-Fahrzeugen

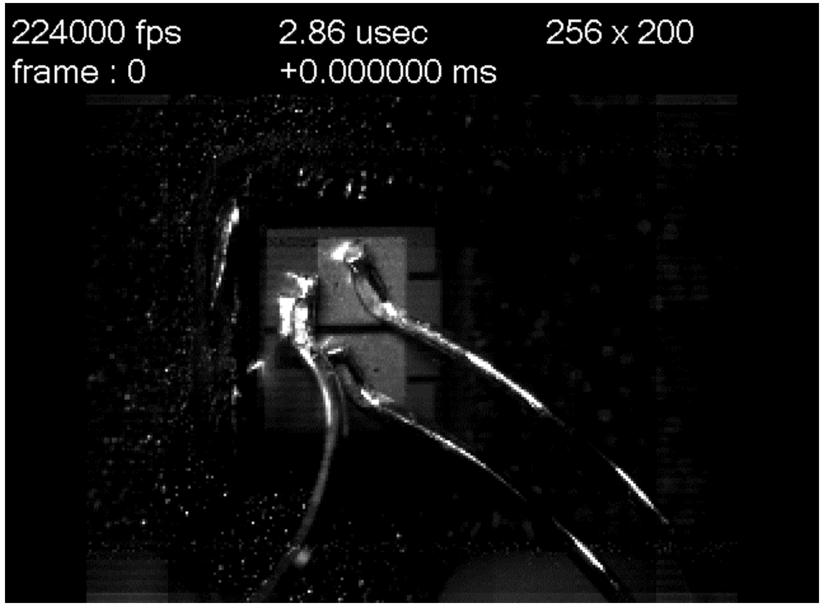
- Maximize Efficiency
- Minimize Weight of On-Board System
- Interact with the Grid (Storage)!

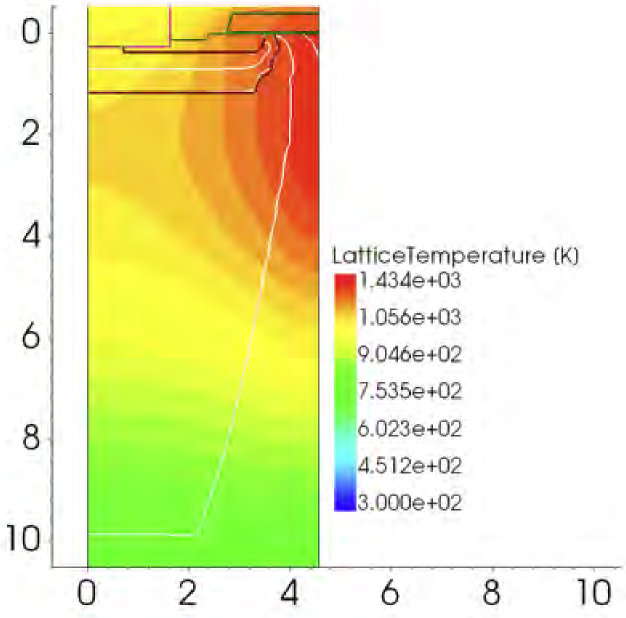
★ η_{DCDC} = 95.8% @ 50kW / ICNIRP @ 800mm

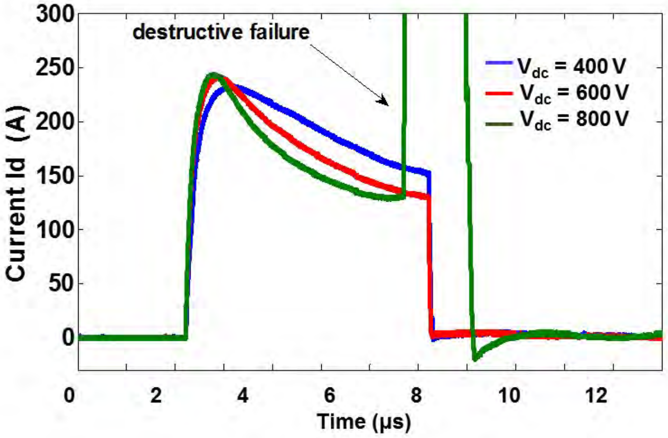
Forschungsbeispiel – Kurzschlussfestigkeit von SiC MOSFETs











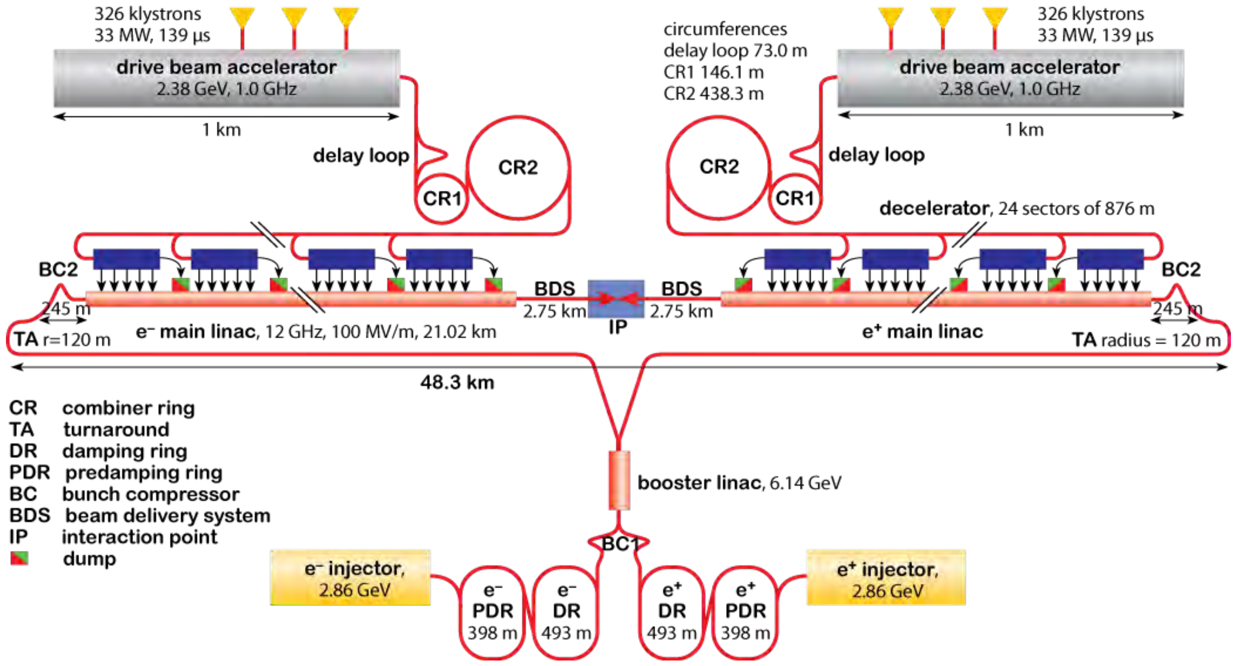
Experimentelle und theoretische Beschreibung von Kurzschluss in SiC MOSFETs

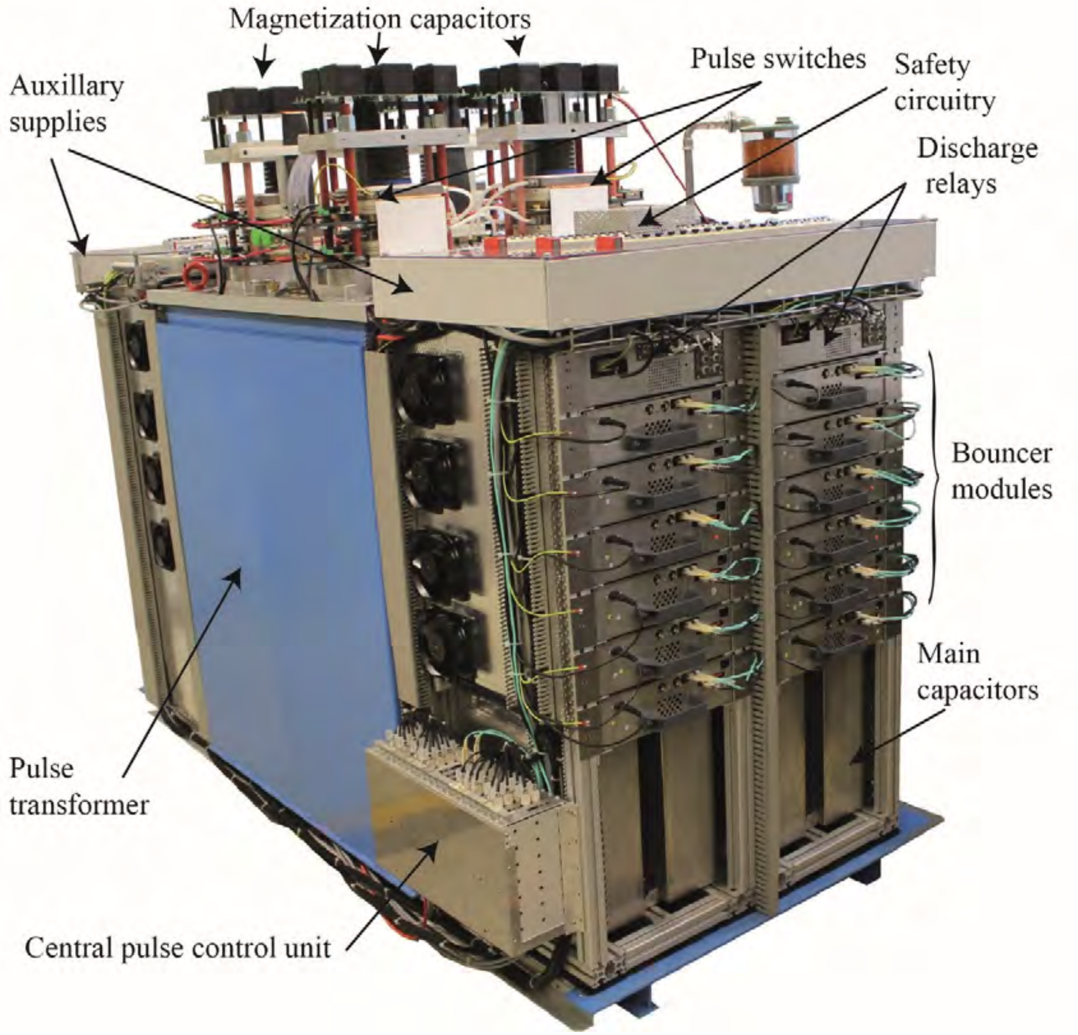
Korrekte Beschreibung in Simulation

Vorschläge für verbessertes «device design»

Forschungsbeispiel – «Ultra High Precision Klystron Modulators»

- Anwendung am CERN
  - Energy in klystron in case of arc < 10J (without cable)
  - System efficiency » 90%
  - Peak power 33MW (35MW)
  - Pulse voltage 150kV - 180kV





→ **Compact Linear Colliders (CLIC)**

Forschungsbeispiel – «Mechatronik»

- Laser Measurement Technology
- Active Damping of Air Bearings
- Satellite Attitude Control

World Record !
★ 500‘000 rpm

→ Ultra High Speed Magnetically Levitated Drive Systems

Typische Vorlesungen

5. Semester:

Leistungselektronik
Einführung in die Theorie und Technologie elektrischer Energieübertagungssysteme

6. Semester:

Hochspannungstechnik
Power Semiconductors
Mechatronik

Master- Semester- Gruppenarbeiten:

- Hardware und/oder Programmierung bzw. Simulation
- Forschungsnahe Projekte (Publikationen) oder industrienahe Projekte

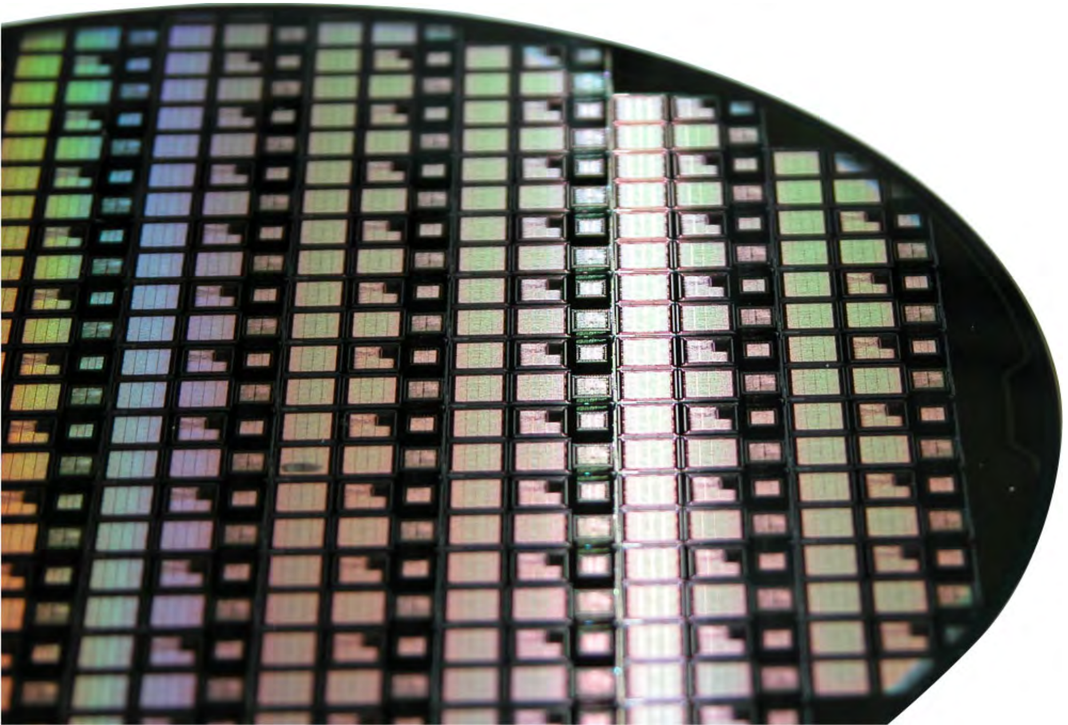
Starker Bedarf an Energietechnik-Ingenieuren:

…. and many more!

ETH zürich

Integrated Circuits and Systems

Research and Student Project Introduction

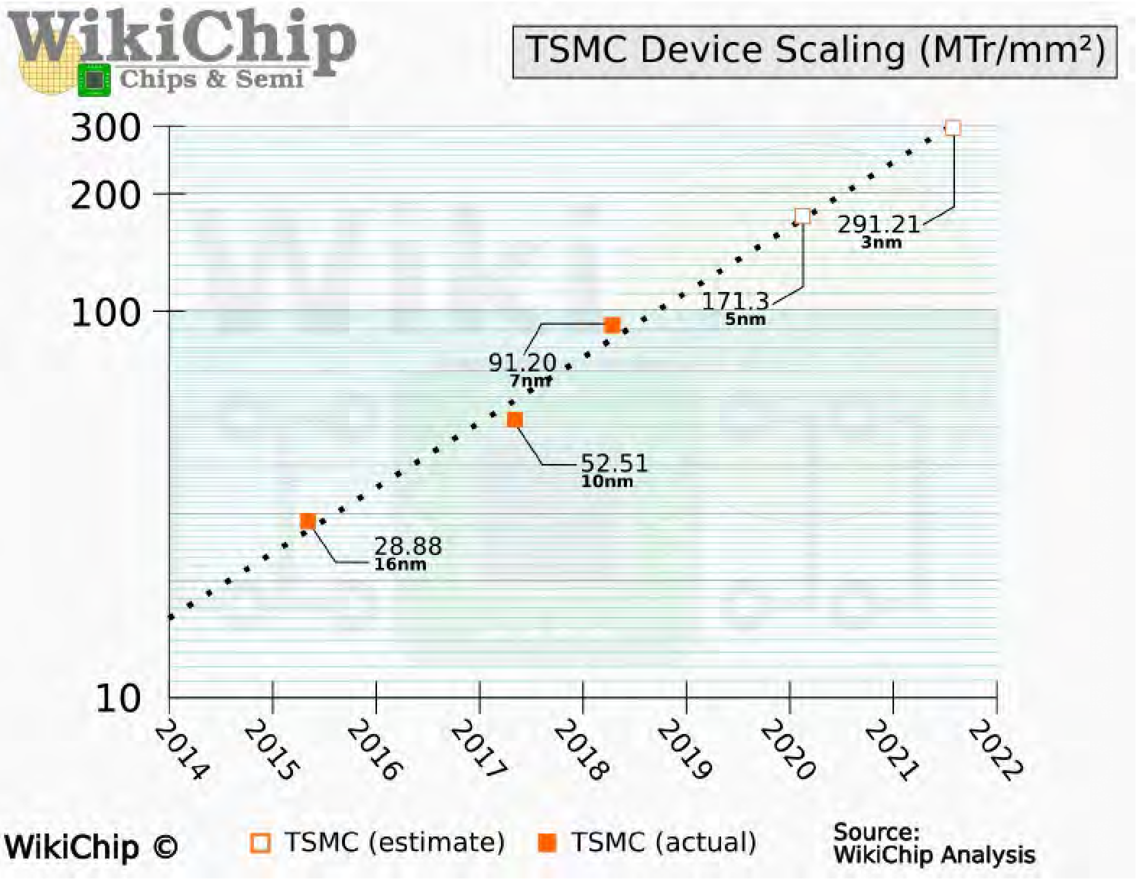


1 June 2021

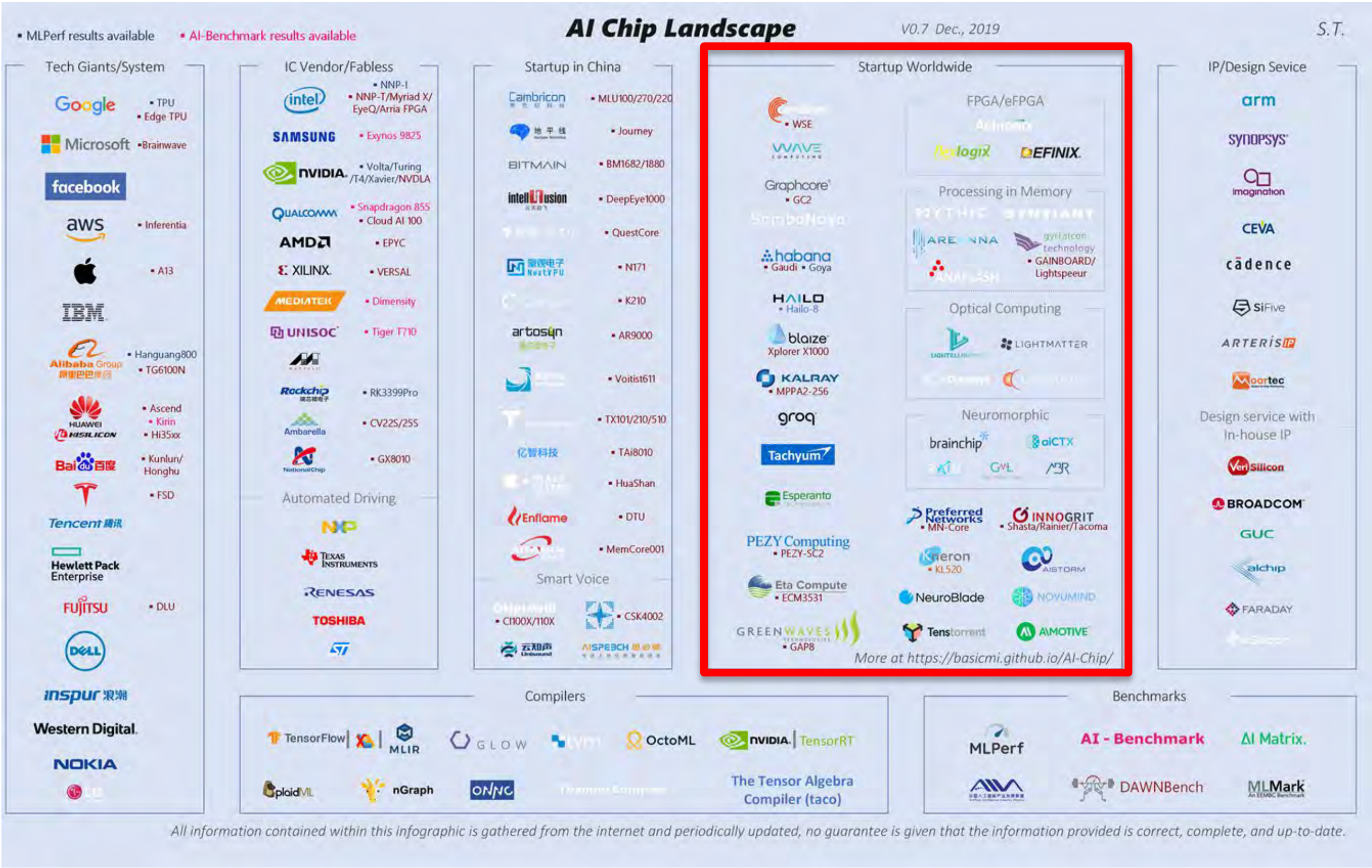
Prof. Qiuting Huang
Prof. Luca Benini
Prof. Christoph Studer
Prof. Taekwang Jang
Prof. Hua Wang

IC Design is Hot!

Moore's Law's still there



Huge new Markets: AI, 5G, Self-driving Cars



Overall Offers

- **Analog Integrated Circuits**
  - 5th semester specialization course on analog IC design
- **Communication Electronics**
  - 6th semester specialization course on RF electronics
- **Analog Signal Processing and Filtering**
  - Master level specialization course
- **Analog to Digital Converters**
  - Master level specialization course (Spring)
- **Energy Efficient Analog Circuits for IoT Systems**
  - Master level specialization course (Spring)
- **The new Digital VLSI Sequence**
  - In 3 semesters, 5 classes (VLSI I, II, III, IV, SoCs for Data Analytics & Machine Learning) → "**from idea to SoC**"
  - Learn to design: microcontrollers, processors, accelerators for machine learning… on FPGA or in dedicated silicon
  - All interested students given the opportunity to specify, **design, test their own chip**

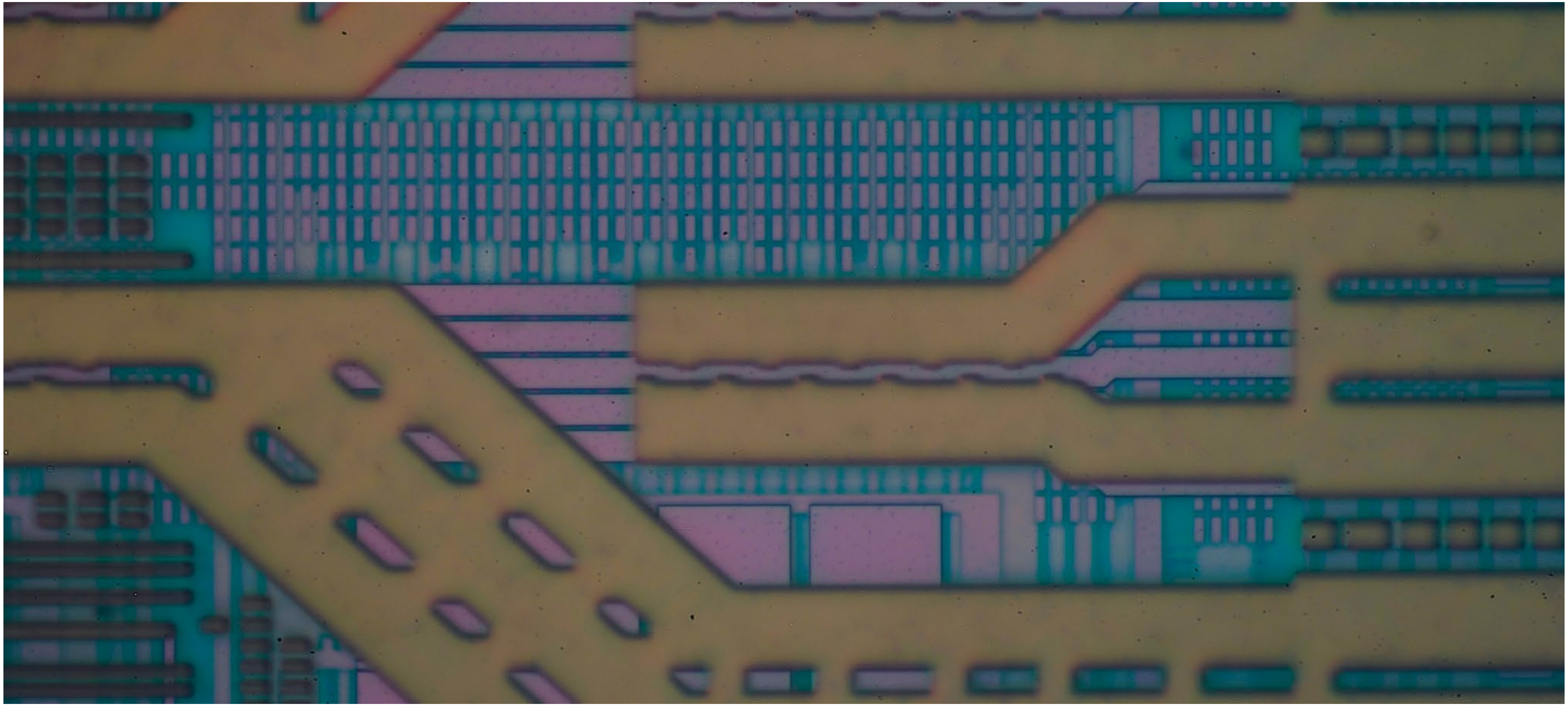
Bachelor Recommendation

- **Analog Integrated Circuits**
  - 5th semester specialization course on analog IC design
- **Communication Electronics**
  - 6th semester specialization course on RF electronics
- **VLSI I: From Architectures to VLSI Circuits & FPGAs**
  - 5th semester introduction course with focus on FPGA design
- **VLSI II: Design of Very Large Scale Integration Circuits**
  - 6th semester course on practical ASIC design

- **Discrete-Time and Stochastic Signal Processing**
  - 5th semester specialization course
- **Communication Systems**
  - 5th semester specialization course
- **High Speed Signal Propagation**
  - 5th semester specialization course

Student Projects – Analog Group

Prof. Q. Huang

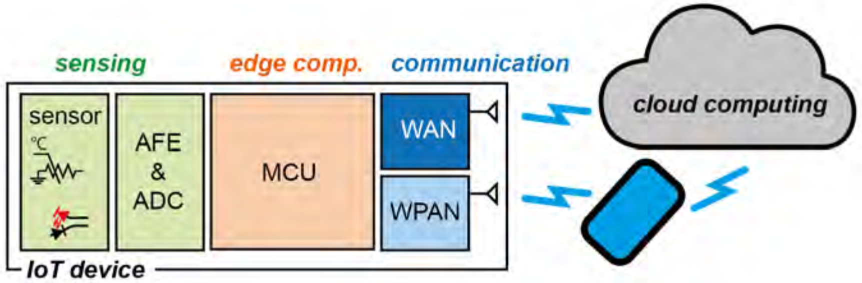


The Internet-of-Things (IoT)

[1] https://iot-analytics.com/state-of-the-iot-update-q1-q2-2018-number-of-iot-devices-now-7b

IoT Applications demand for highly integrated System-on-Chips

- Sensing
- Computing
- Transmission



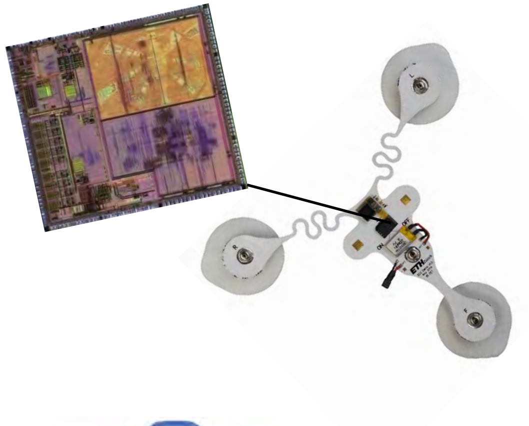
mobile Health System-on-Chip & Applications

***VivoSoC*: universal platform**

- Sensor front-ends (ExG, PPG, BioZ, temperature, AUX)
- Power management (DC/DC, LDOs, Bat. Chrg., ...)
- Processing (PULP)

Available Projects:

- Applications (i.a.)
  - Signal processing / feature extr.
  - PCB design for wearables
- Analogue IC design
  - Sensor circuits, ADC, DAC, audio-amp, voltage regulators, ...
- Digital IC design
  - Interfaces, data management, ...

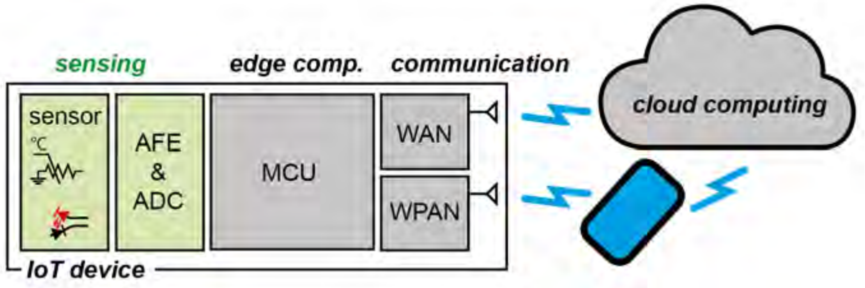


ECG Patch

- VivoSoC-3 based
- 6 ch ECG
- 6.20 g
- Bluetooth con. to Android app.

SpO2 Earbud

- VivoSoC-3 based
- 2 ch PPG
- Bluetooth
- Audio?



RF-System-on-Chips for the Internet of Things

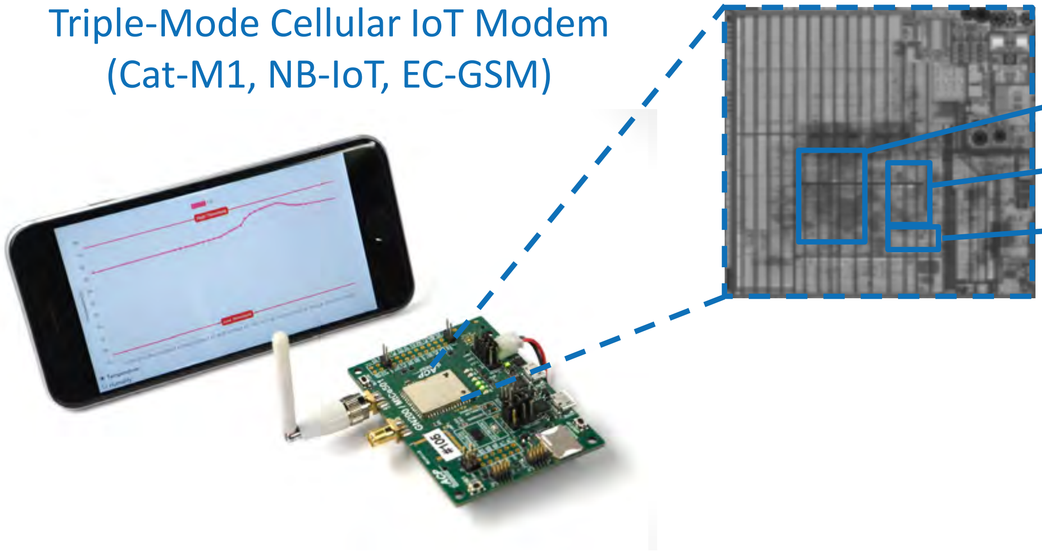
Communication systems build the bedrock of the IoT

- Contribute to cutting-edge IoT modems

Available projects

- Digital Baseband Algorithms and Implementation for **5G NR-Light**
- Channel Decoders for **5G Ultra-Reliable Low-Latency Communication**
- **5G RF Transceiver** Design
- Low-Cost, Low-Power Indoor & Outdoor **Positioning for the IoT**
- High-Speed Channel Estimation & Tracking for **V2X Communications**

Triple-Mode Cellular IoT Modem
(Cat-M1, NB-IoT, EC-GSM)

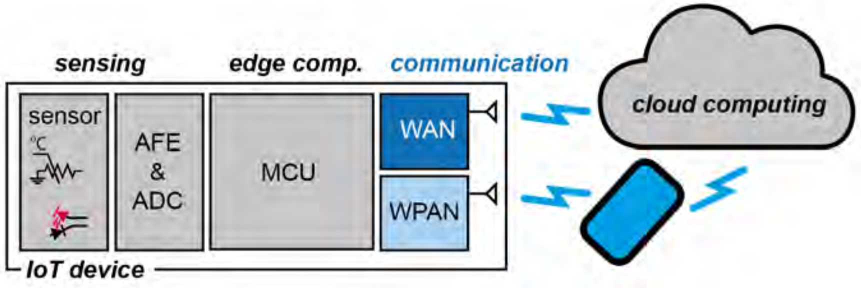


Former Student Projects

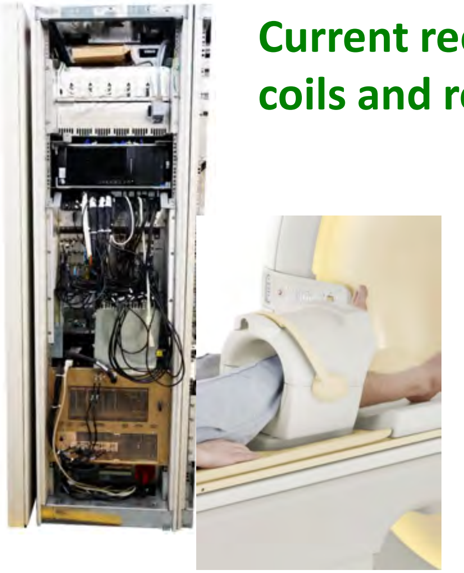
"Shared Correlation Accelerator for an RF SoC"

„An Energy Efficient Turbo Decoder for the IoT "

„Mixed Radix FFT Core Generator"



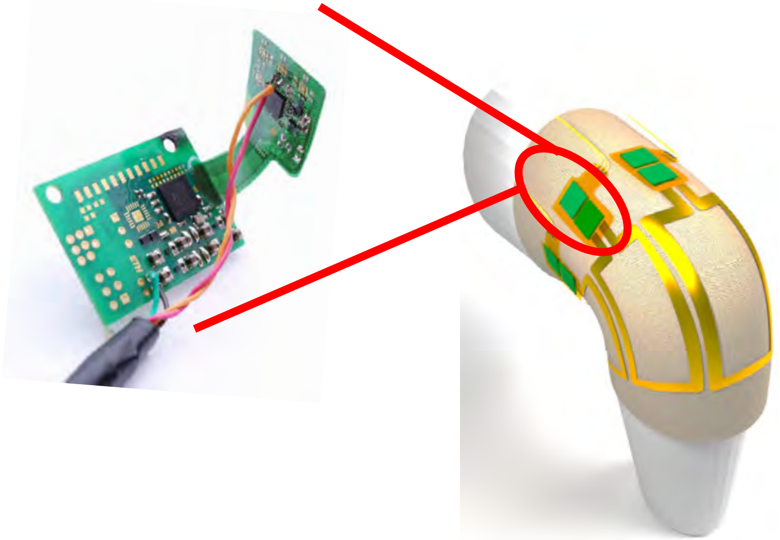
Integrated Receiver System for MRI



Current receiver coils and receiver

Project goal

Wearable MRI



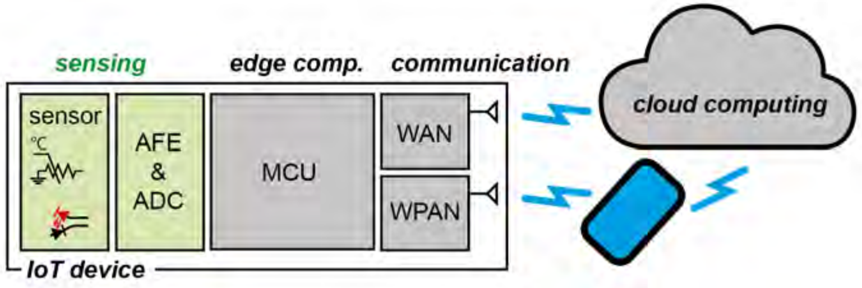
Biomedical application MRI

- Advancing state-of-the-art by wearable receiver board

Available projects

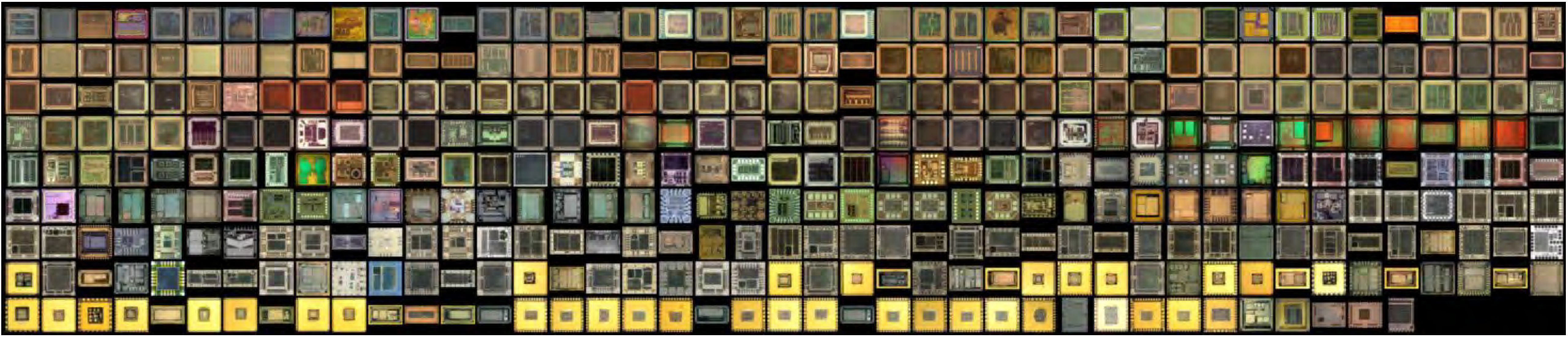
- Receiver circuit design and layout
- Frequency synthesizer design and layout

Opportunity to actually fabricate and measure your circuits



Student Projects – Digital Group

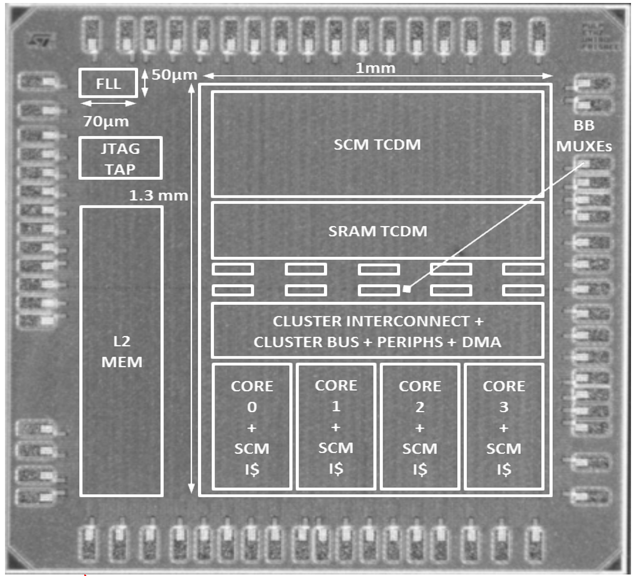
Prof. L. Benini



Open Source Parallel ULP computing

3pJ/op computing platform

PULP
Parallel Ultra Low Power



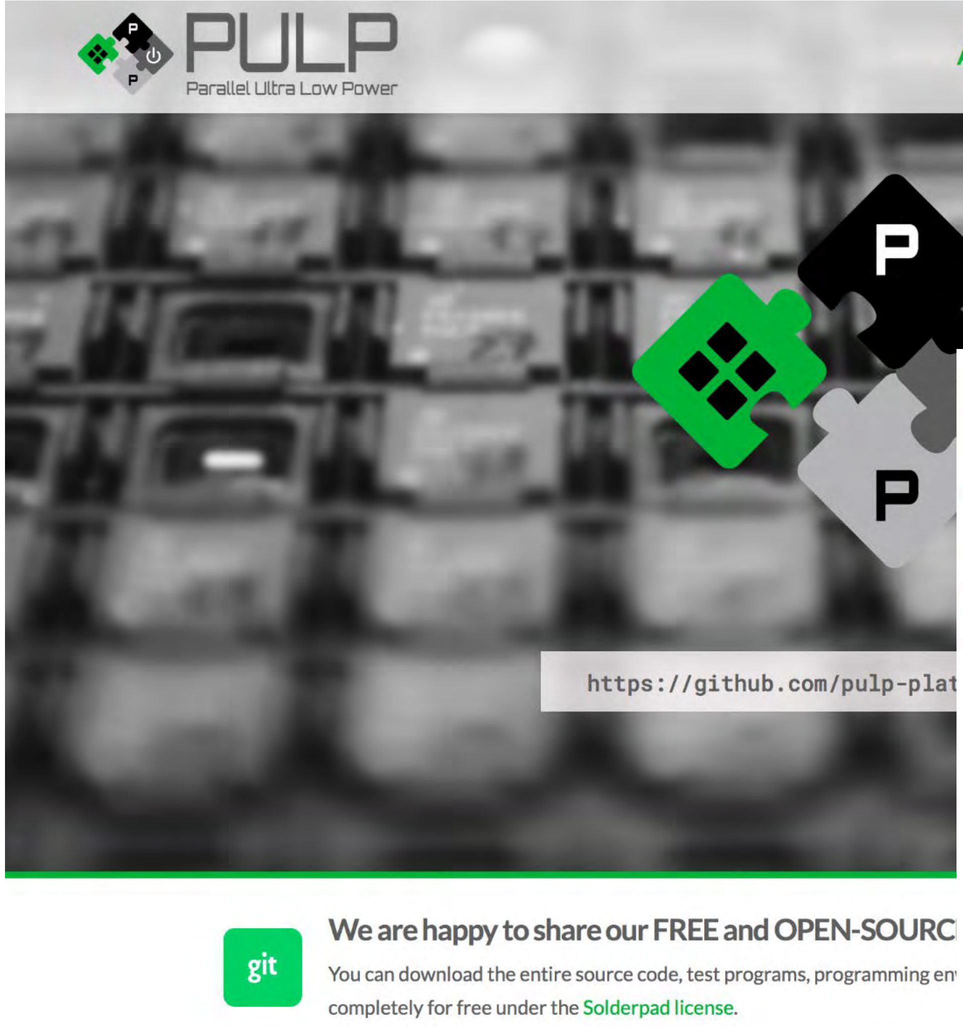
40 PULP chips produced in our group

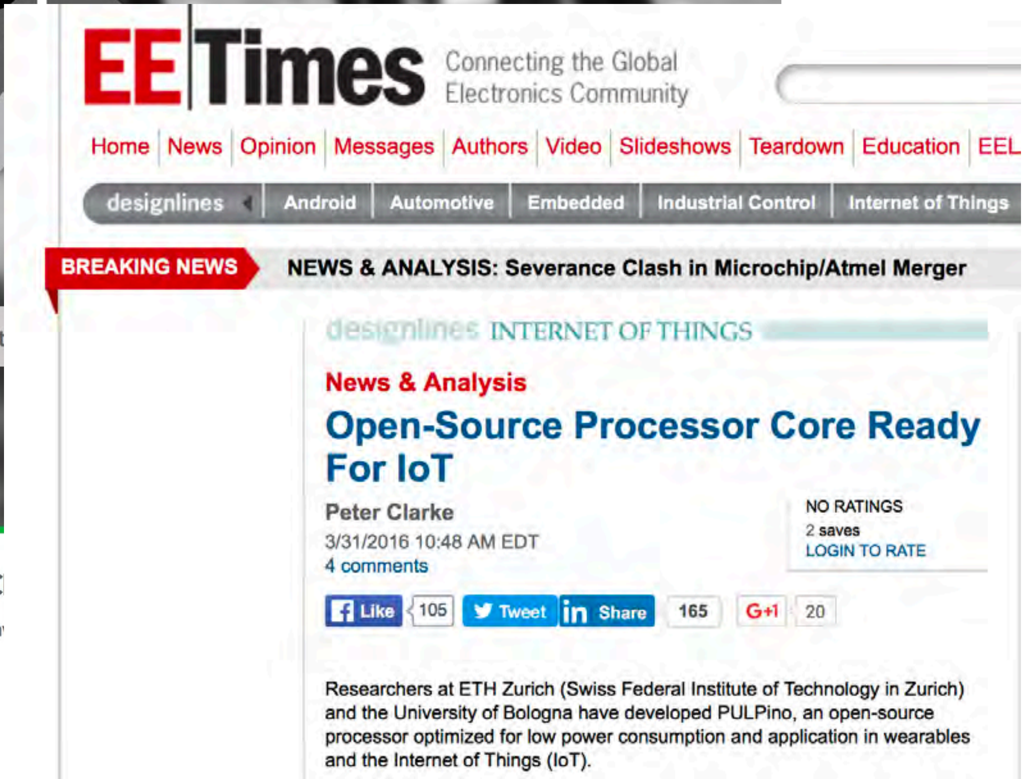
RISC-V → GCC / LLVM COMPILER INFRASTRUCTURE → freeRTOS → OpenMP, ONNX, PyTorch

Processor & Hardware IPs | Compiler Infrastructure | Virtualization Layer | Programming Model

Our open HW is Used by Micron, NXP, IBM, Google, NVIDIA, STM, SiLabs ....

Largest OS HW initiative in Europe!





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BREAKING NEWS NEWS & ANALYSIS: Severance Clash in Microchip/Atmel Merger

designlines INTERNET OF THINGS

News & Analysis

Open-Source Processor Core Ready For IoT

Peter Clarke
3/31/2016 10:48 AM EDT
4 comments

NO RATINGS
2 saves
LOGIN TO RATE

Like 105 Tweet Share 165 G+1 20

Researchers at ETH Zurich (Swiss Federal Institute of Technology in Zurich) and the University of Bologna have developed PULPino, an open-source processor optimized for low power consumption and application in wearables and the Internet of Things (IoT).

OPENHW GROUP
PROVEN PROCESSOR IP

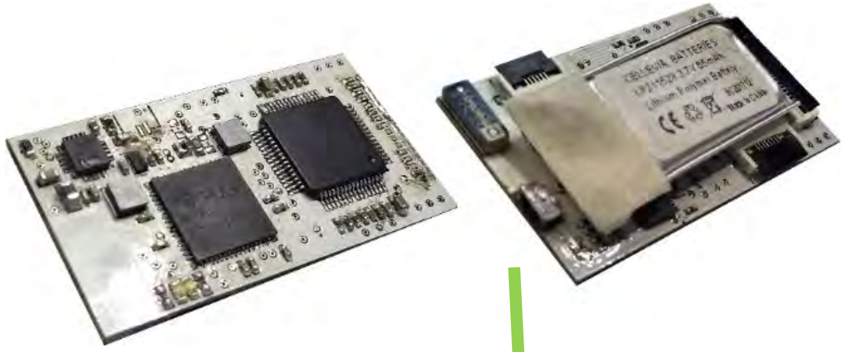
lowRISC

FOSSi Foundation

pulp-platform.org

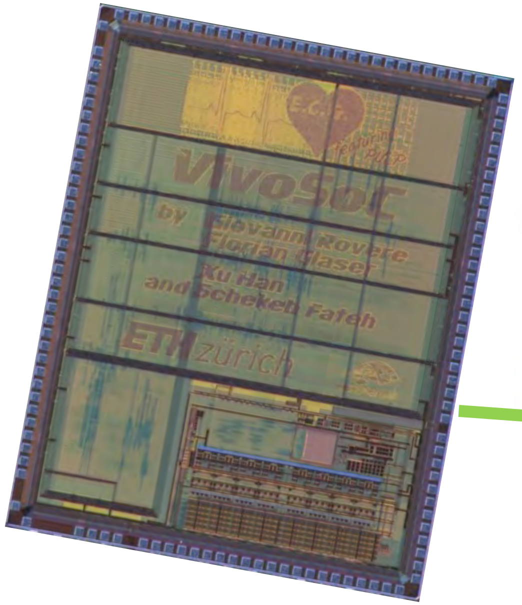
Wearable Biomedical Devices

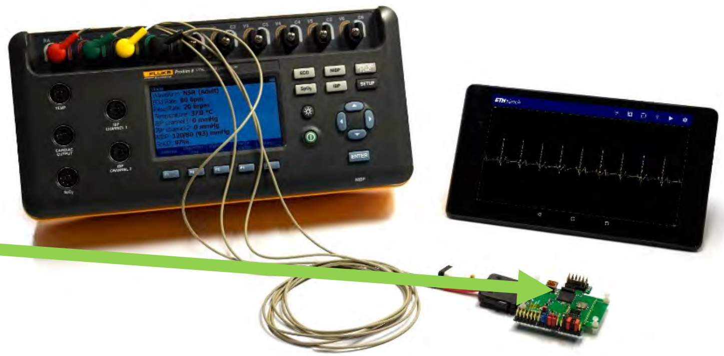
Chip → PCB + package

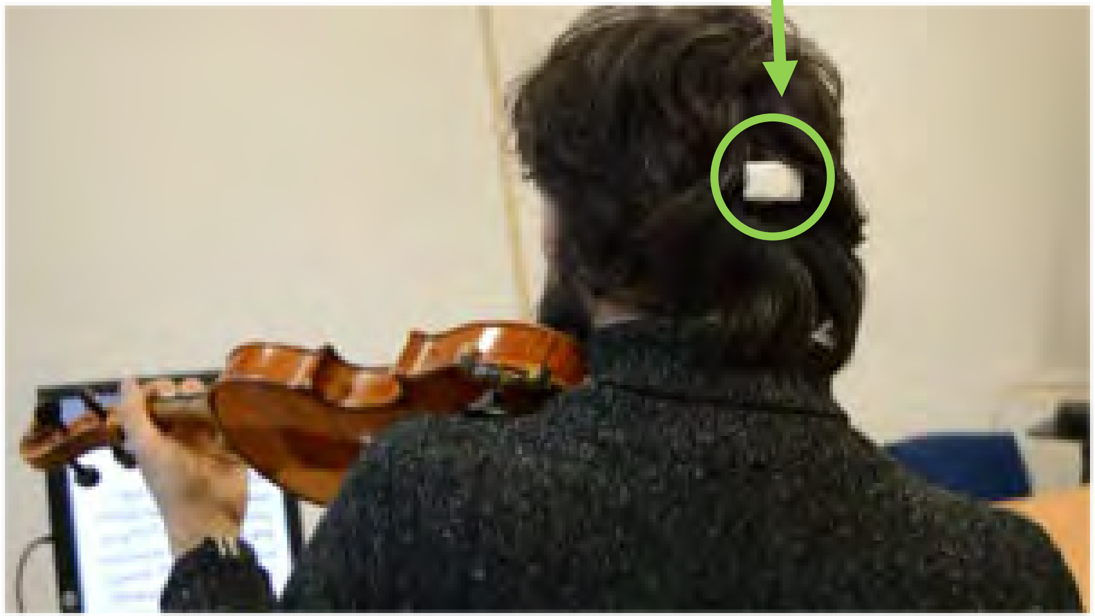


Usage example (brain monitoring patch)

- **Cooperation within IIS – Analog+Digital**
- **Project Goal:**
  - System-on-Chip and miniaturized electronics capable of acquiring a multitude of vital signs
  - Enabling new medical experiments
  - Improving health monitoring, therapy







Accelerators for Machine Learning

- **Brain-inspired (deep convolutional networks) systems are high performers in many tasks over *many domains***

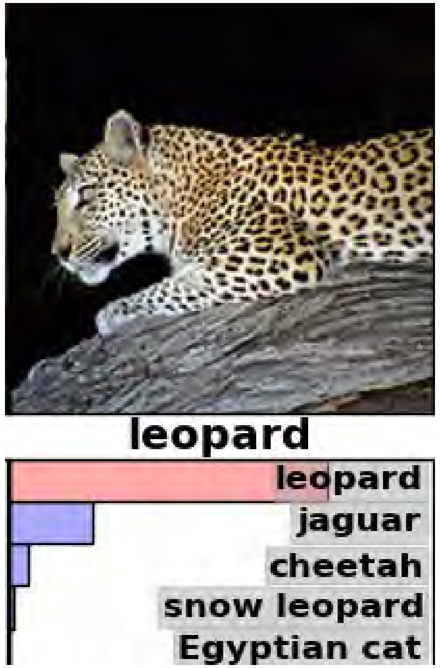
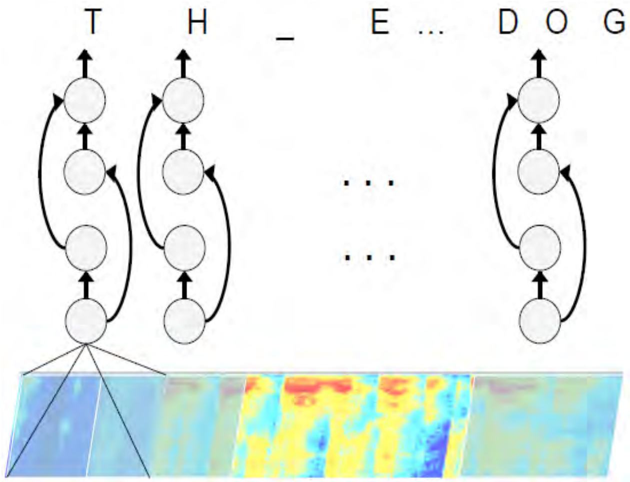


Image recognition



Speech recognition

Accelerators for
Quantized NN
Spiking NN
On-chip learning

Build the most Energy-Efficient AI chips for the IoT

Student Projects:
Integrated Information Processing Group

Prof. C. Studer

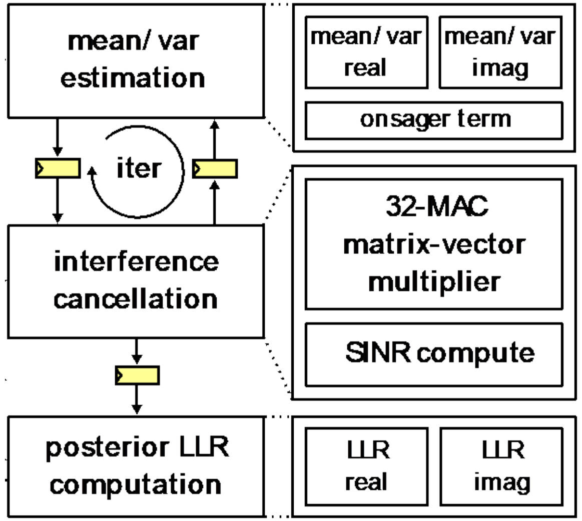
Applications → **Theory & Algorithms** → **Architectures** → **Integrated Circuits**

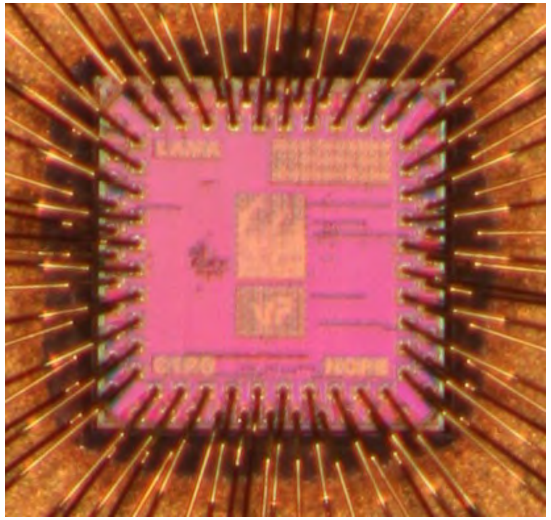
Algorithm 1. *Suppose that* $\mathbf{H}$ *satisfies (A1) and [30, Lem. 5.56] holds. Then, the* complex Bayesian AMP (cB-AMP) *algorithm performs the following steps for each iteration* $t = 1, 2, \ldots,$:

$$\hat{\mathbf{s}}^{t+1} = \mathsf{F}(\hat{\mathbf{s}}^t + \mathbf{H}^{\mathrm{H}}\mathbf{r}^t, N_0^{\mathrm{post}}(1+\tau^t))$$
$$\mathbf{r}^{t+1} = \mathbf{y} - \mathbf{H}\hat{\mathbf{s}}^{t+1}$$
$$+ \frac{\beta\mathbf{r}^t}{2}\langle(\partial_1\mathsf{F}^{\mathrm{R}} + \partial_2\mathsf{F}^{\mathrm{I}})(\hat{\mathbf{s}}^t + \mathbf{H}^{\mathrm{H}}\mathbf{r}^t, N_0^{\mathrm{post}}(1+\tau^t))\rangle$$
$$- i\frac{\beta\mathbf{r}^t}{2}\langle(\partial_2\mathsf{F}^{\mathrm{R}} - \partial_1\mathsf{F}^{\mathrm{I}})(\hat{\mathbf{s}}^t + \mathbf{H}^{\mathrm{H}}\mathbf{r}^t, N_0^{\mathrm{post}}(1+\tau^t))\rangle \quad (8)$$
$$\tau^{t+1} = \frac{\beta}{N_0^{\mathrm{post}}}\langle\mathsf{G}(\hat{\mathbf{s}}^t + \mathbf{H}^{\mathrm{H}}\mathbf{r}^t, N_0^{\mathrm{post}}(1+\tau^t))\rangle,$$

where the functions $\partial_{\{1,2\}}\mathsf{F}^{\{\mathrm{R},\mathrm{I}\}}(x+iy,\tau)$ *are defined as*

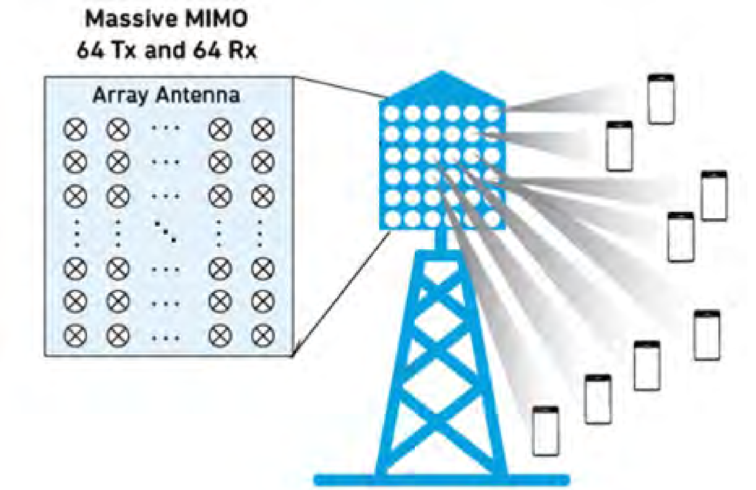
$$\partial_1\mathsf{F}^{\mathrm{R}} \triangleq \frac{\partial\mathrm{Re}\{\mathsf{F}(x+iy,\tau)\}}{\partial x}, \quad \partial_2\mathsf{F}^{\mathrm{R}} \triangleq \frac{\partial\mathrm{Re}\{\mathsf{F}(x+iy,\tau)\}}{\partial y},$$
$$\partial_1\mathsf{F}^{\mathrm{I}} \triangleq \frac{\partial\mathrm{Im}\{\mathsf{F}(x+iy,\tau)\}}{\partial x}, \quad \partial_2\mathsf{F}^{\mathrm{I}} \triangleq \frac{\partial\mathrm{Im}\{\mathsf{F}(x+iy,\tau)\}}{\partial y},$$

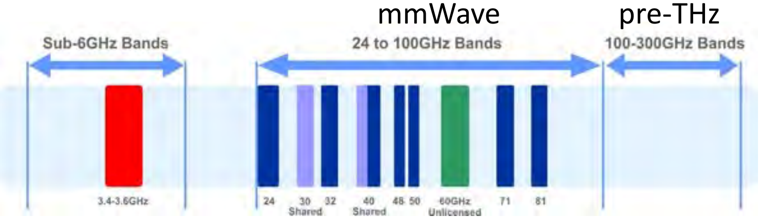




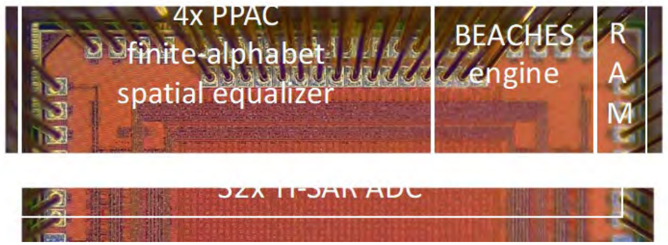
Student Projects: Accelerators for 6G

- Beyond 5G! **6G wireless systems will use new communication technologies:**
  - Massive multiuser MIMO (thousands of antennas)
  - Millimeter-wave (mmWave) and terahertz (THz) communication (extremely high frequencies)
- **Signal processing with thousands of antennas at 10GHz of bandwidth is currently infeasible**
  - Requires new theory, algorithms, hardware architectures, application-specific integrated circuits (ASICs), and hardware/FPGA prototypes





First Mixed-Signal IC for 6G

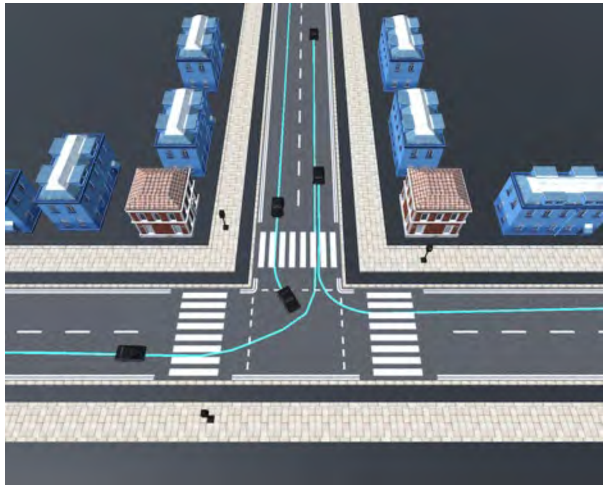


ComSenTer COMMUNICATIONS SENSING TERAHERTZ

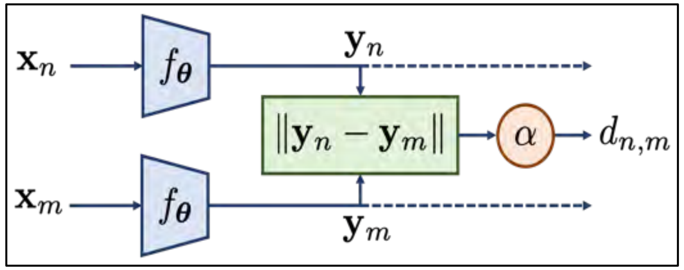
ERICSSON

Student Projects: Wireless Positioning

- **Indoor and Outdoor Positioning of Wireless Devices where GPS is Unavailable/Unreliable**
  - Currently no satisfactory solution available
  - Machine learning to the rescue!
- **Available projects:**
  - ML-based localization from wireless measurements
  - Self-supervised localization: localization without the user's consent (and novel adversarial attacks to avoid that...)
  - Imaging and object tracking from RF measurements
  - Ultra-wideband (UWB) localization and sensing in collaboration with Zurich-based startup 3dB Access

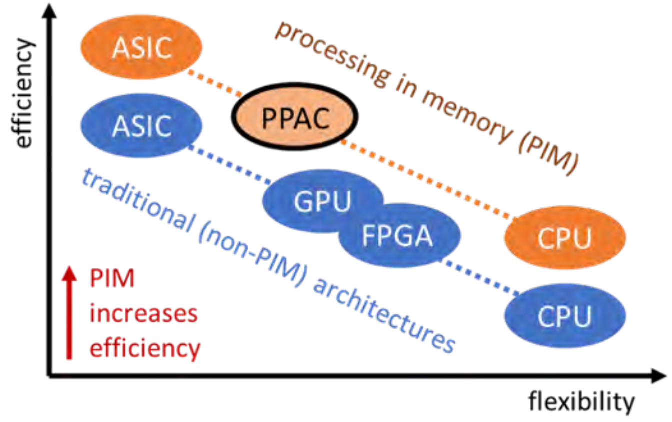


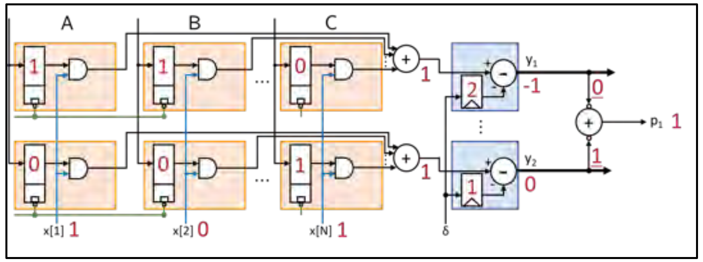
Siamese Neural Network for Localization

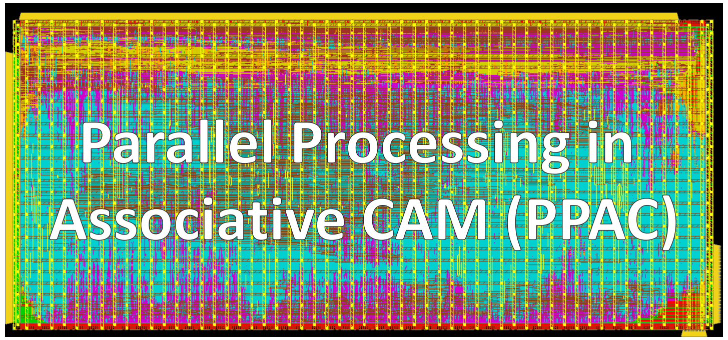


Student Projects: Processing-in-Memory (PIM)

- **Processing-in-Memory moves computation into memories to improve energy-efficiency**
  - Data movement between memory and processing engines can dominate power consumption
  - Existing PIM accelerators are custom made (hand layout) and single-purpose (e.g., for ML acceleration)
- **Available projects:**
  - All-digital & synthesizable PIM accelerator design
  - Multi-purpose PIM accelerator design → PPAC
  - Semi-custom PIM with customized standard-cells
  - Integration of PIM into PULP and application design

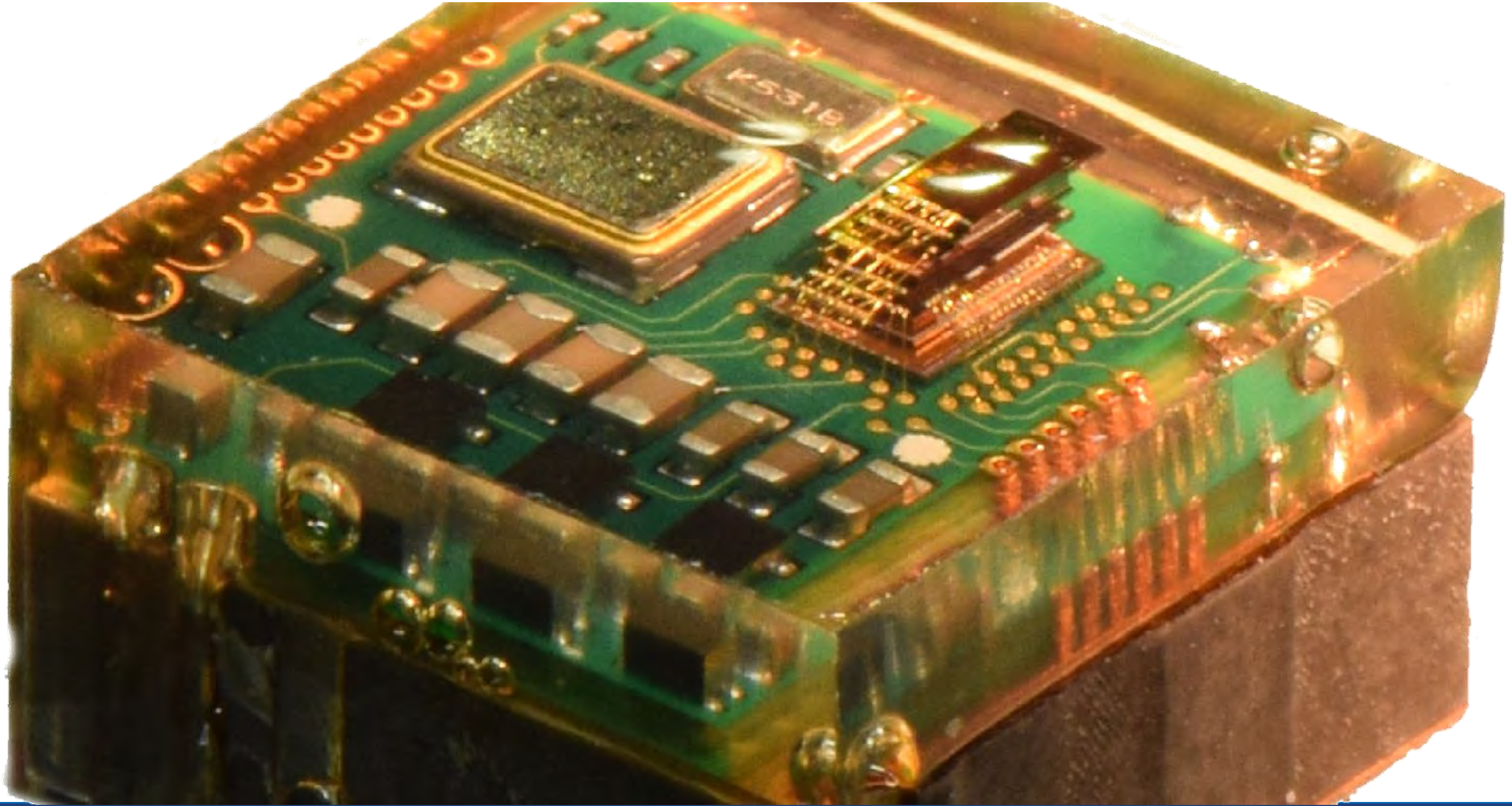






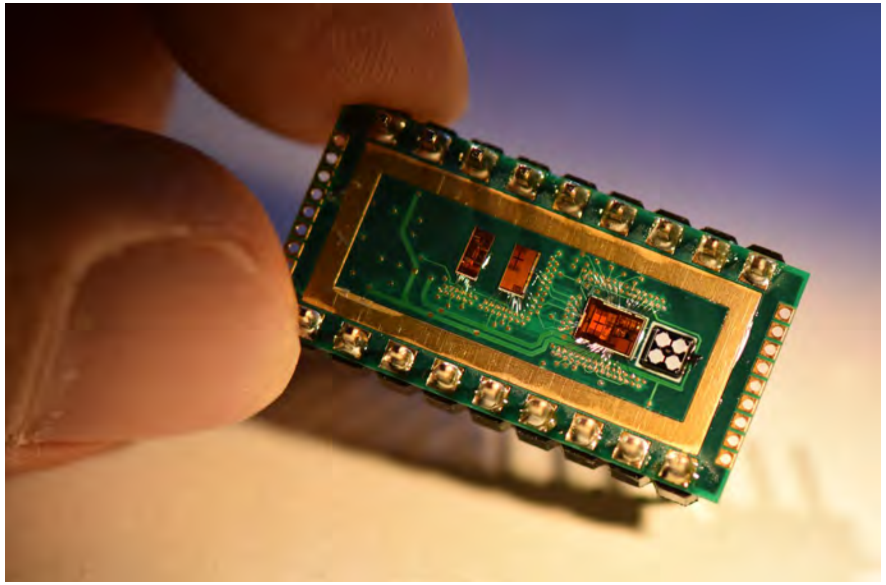
Student Projects – Energy Efficient Circuits and IoT Systems Group

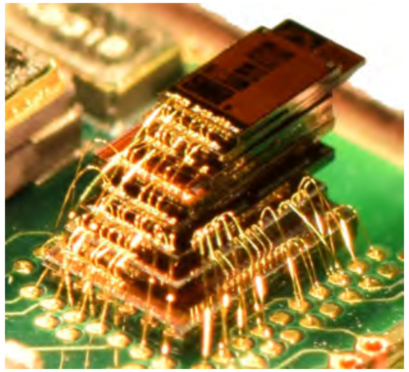
Prof. Taekwang Jang

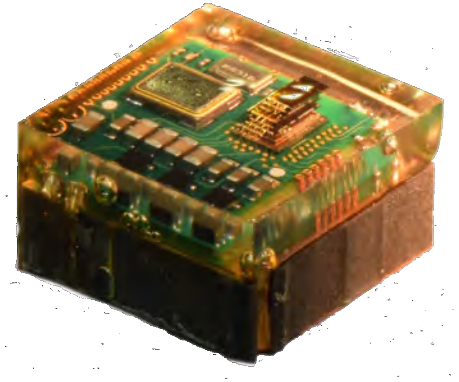


Key Building Blocks for Miniaturized Computers

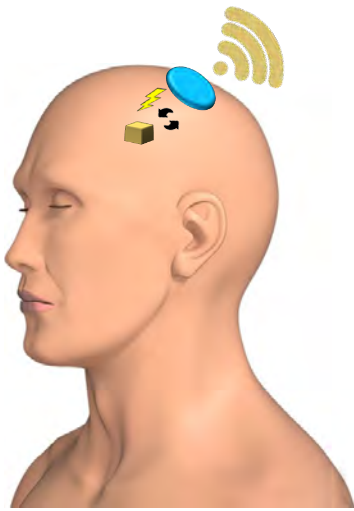
- **Ultra-low power miniaturized systems**
  - Micro-processor
  - Analog sensing interface
  - Energy harvester
  - RF communication
  - Optical communication
  - Flash memory
  - Power management
  - Frequency generation



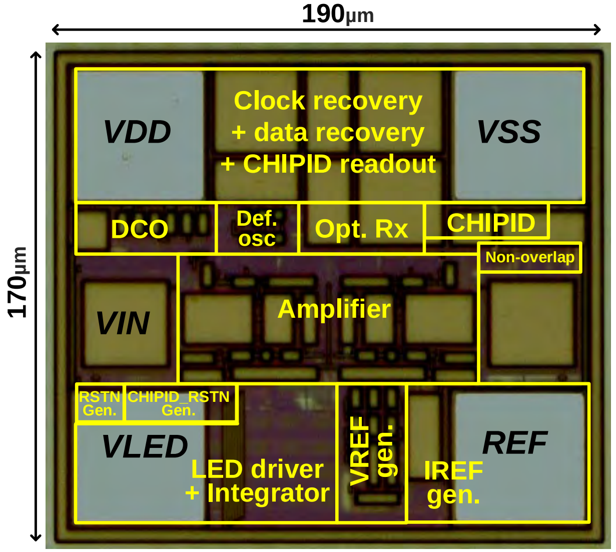


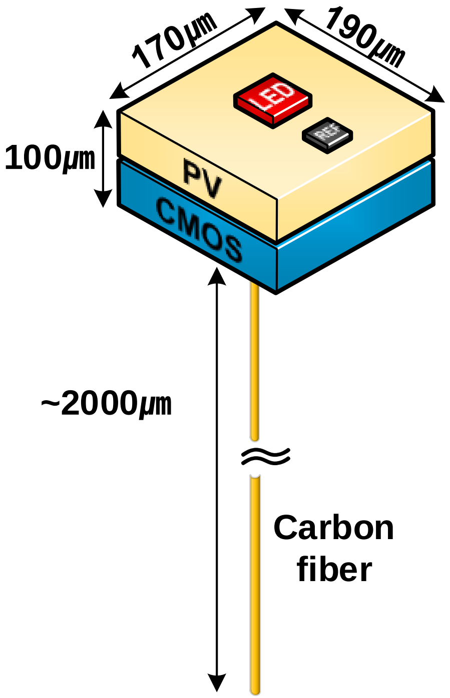


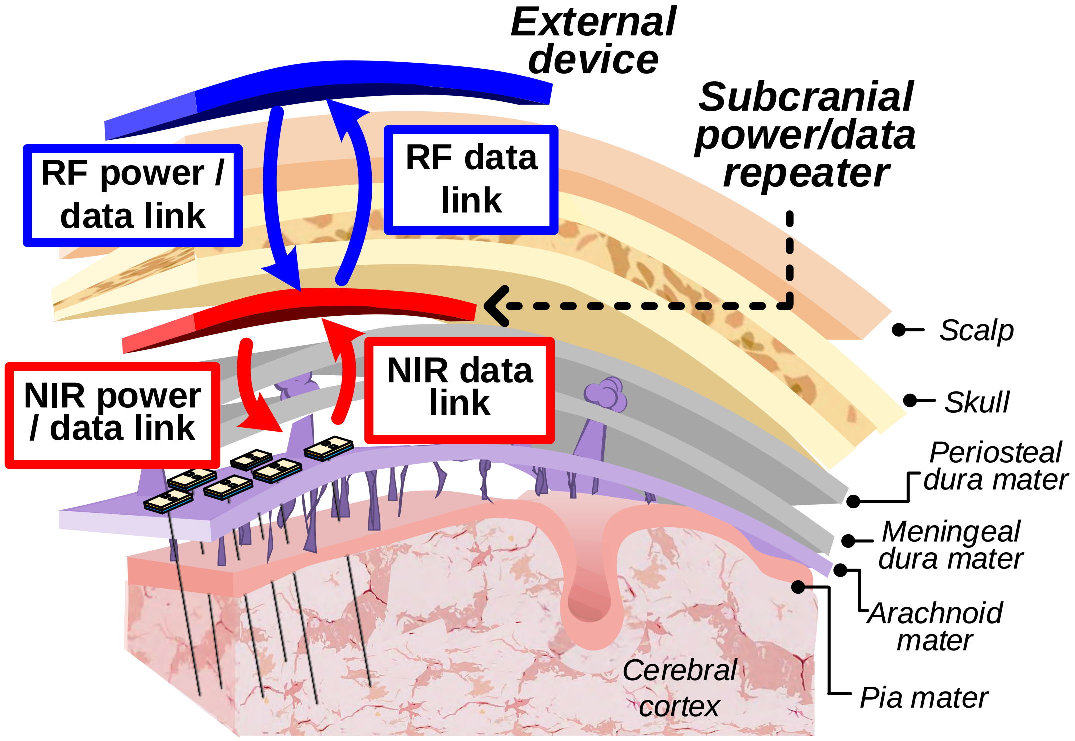
Student Project: Wireless Neural Recording



- **Fully wireless neural recording**
  - Implantable wireless power transfer circuit
  - Energy efficient neural recording front-end
  - RF/optical communication circuit
  - Spike sorting & inference



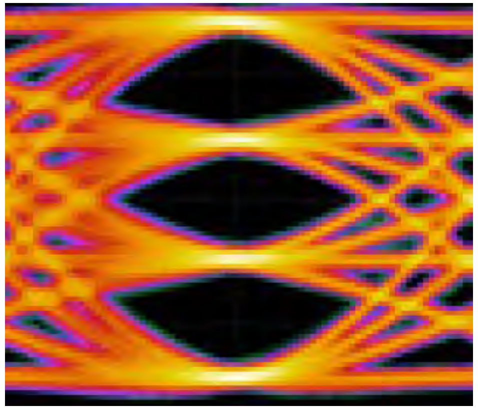


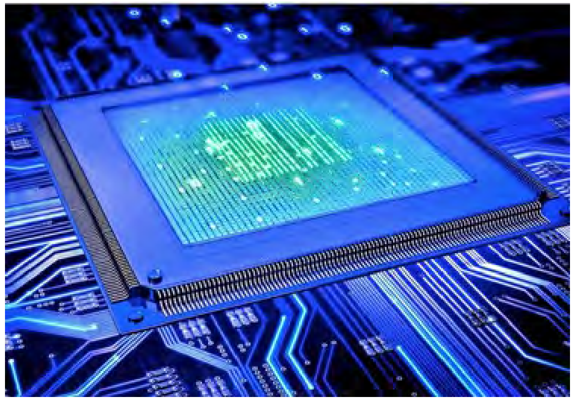


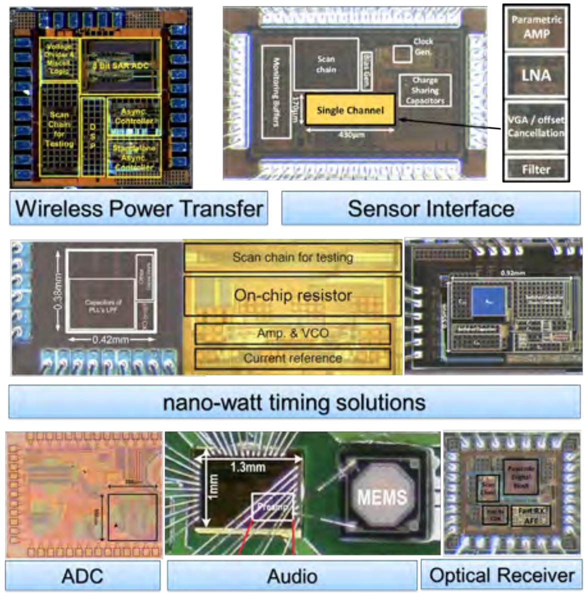
Student Project: Miniaturized IoT Devices

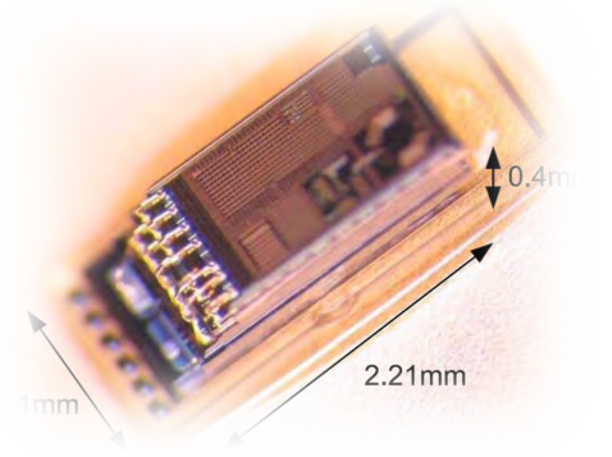
- Palm size chip NMR probe
- Epilepsy control system
- Nano-watt circuits for mm-scale devices

Insite, http://www.in-sitesolutions.com/









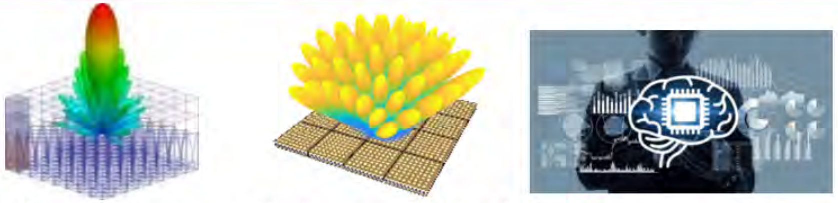
Student Projects:
Integrated Electronics and Hybrid Systems Group

Prof. Hua Wang

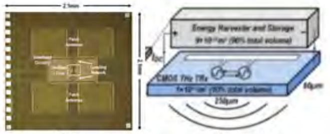
1. 5G/6G RF, Mm-Wave and THz Integrated Circuits and Systems — "Circuits and Up"

Theme: Intelligently generate, manipulate, and receive electromagnetic signals by heterogeneous platforms

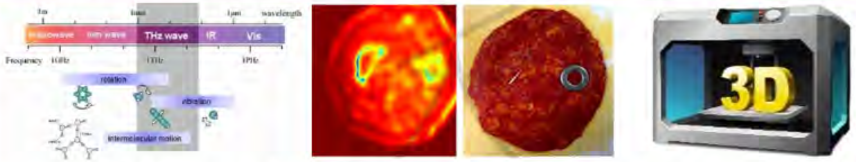
5G/6G RF/Mm-Wave/Sub-THz Wireless with Intelligence



MIMO Architectures (Autonomy, Ultra-Low Latency, and Security)



THz Pico-Sized Radios and "Invisible" Sensors Nodes

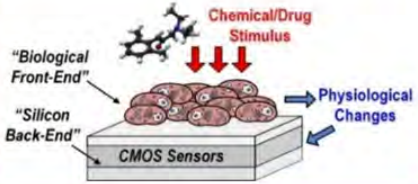


THz Hyperspectral Imaging and Spectroscopy

Quantum Computing + Si Photonics

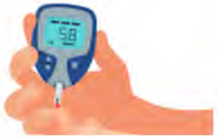
2. Hybrid Biosensors and Bioelectronics — "Circuits and Down"

Theme: "Integrate" living biology with non-living electronics



Drug Screening

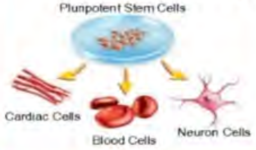
PoC/LoC Devices



Synthetic Biology

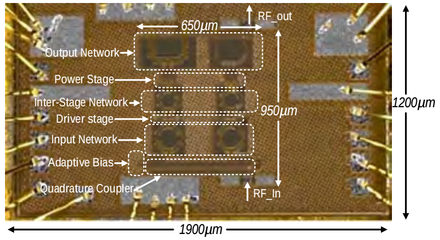
Molecular Electronics

Cell Manufacturing



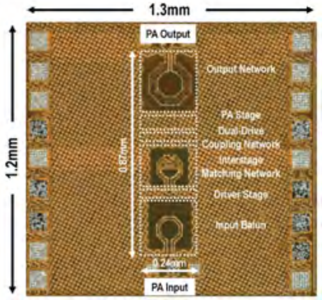
Student Projects: 5G/6G Mm-Wave/THz Frontend and Antennas

- **5G/6G Mm-Wave/THz Frontends:**
  - High-Efficiency Wideband Power Amplifiers and Power Generations
  - Low-Noise High-Linearity Receiver Frontend
  - THz Source and Detector Arrays for Imaging and Radar
- **Antenna-Electronics Co-Designs:**
  - Hybrid Multi-Feed Antennas and Electronics for Sub-Wavelength Radiation Modulation
  - Full-Duplex Wireless Systems
- **On-Chip/In-Package Electromagnetics Designs:**
  - Low-Cost Printed Electromagnetic Band-Gap (EBG) structures for Mm-Wave/THz Radiation Enhancement



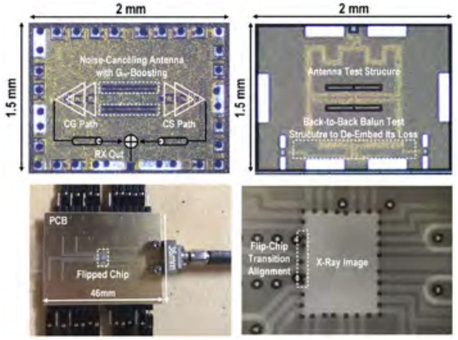
A 26-to-60GHz Continuous Coupler-Doherty Linear Power Amplifier

ISSCC 2021



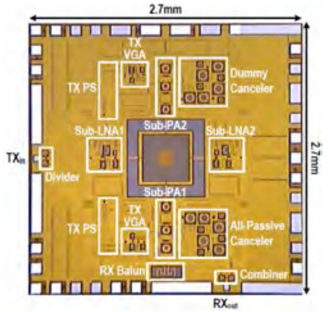
A Novel Class-W "Wang" Mm-Wave Power Amplifier for Wideband High-Efficiency/Linearity MIMOs

ISSCC 2021



A 75-85GHz Antenna-LNA Front-End with On-Antenna Noise Cancellation and Gain Boosting

ISSCC 2020



A 64GHz Full-Duplex Transceiver Front-End with On-Chip Multi-Port SIC Antenna

ISSCC 2018, JSSC 2018

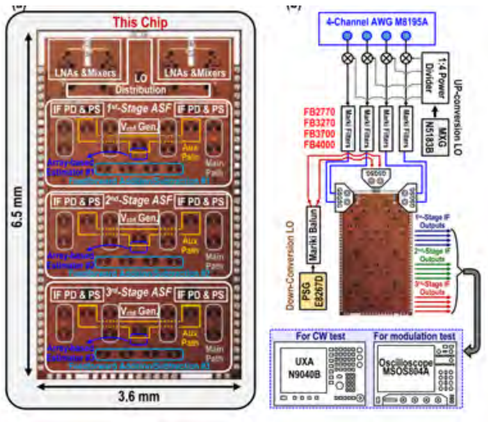
intel MITSUBISHI ELECTRIC tsmc Georgia Tech PACKAGING RESEARCH CENTER SRC Semiconductor Research Corporation

Student Projects: Novel MIMO Concepts and Operations

- **Novel MIMO Array Architectures BEYOND Phased Arrays**
  - Spatiotemporal Modulated Arrays
  - Frequency Diversity Arrays
  - Retrodirective/Autonomous Beamforming Arrays
  - Non-Coherent/Hyperspectral THz Imaging Arrays
- **New Array Operations**
  - Rapid Beam Finding/Locking/Tracking in Dynamic, Unknown, and Fast-Changing Wireless Environments
  - One-Shot Mm-Wave Source Localization
  - Concurrent Multi-Beam MIMOs
  - Electromagnetic Physical Layer Security

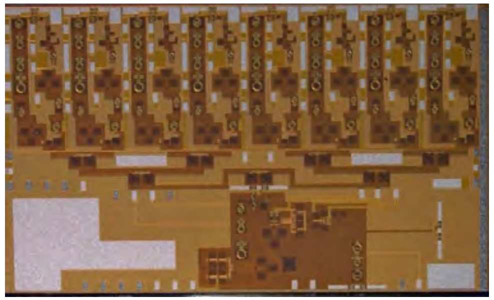
27-41GHz 1 × 4 MIMO RX array with full-FoV autonomous hybrid beamforming

ISSCC 2019 and JSSC 2019



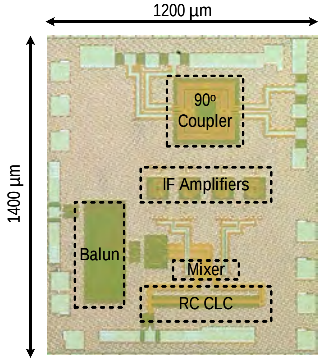
A 24-42 5G 1 × 8 MIMO TX/RX array with hybrid beamforming in GFUS 45nm CMOS SOI

RFIC 2019 and JSSC 2020



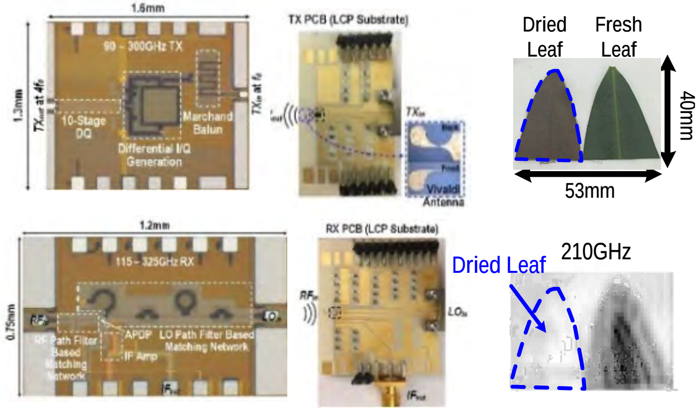
40-100GHz RX frontend in GFUS 22nm CMOS SOI

CICC 2020 and JSSC 2020 (invited special issue)



A Packaged 100-300GHz CMOS TRX with Vivaldi Antenna for Full-Band CW THz Hyperspectral Imaging

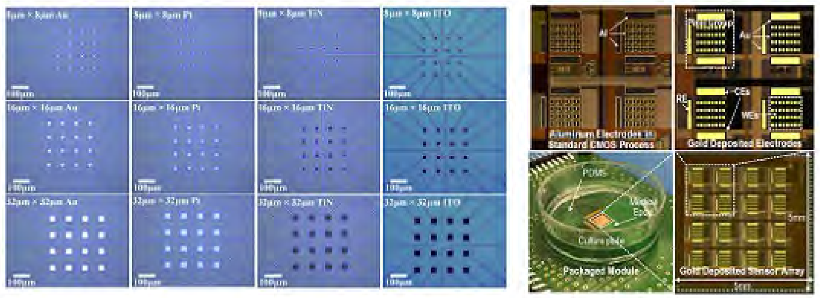
ISSCC 2017

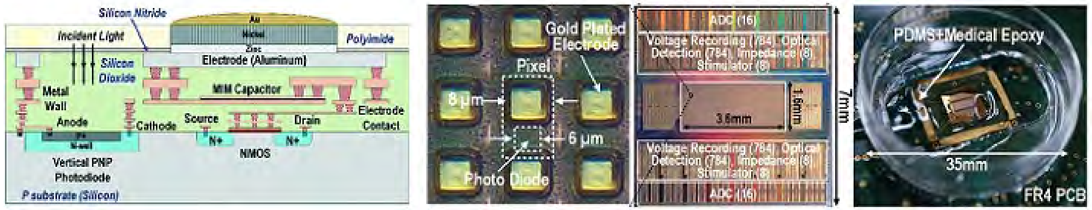


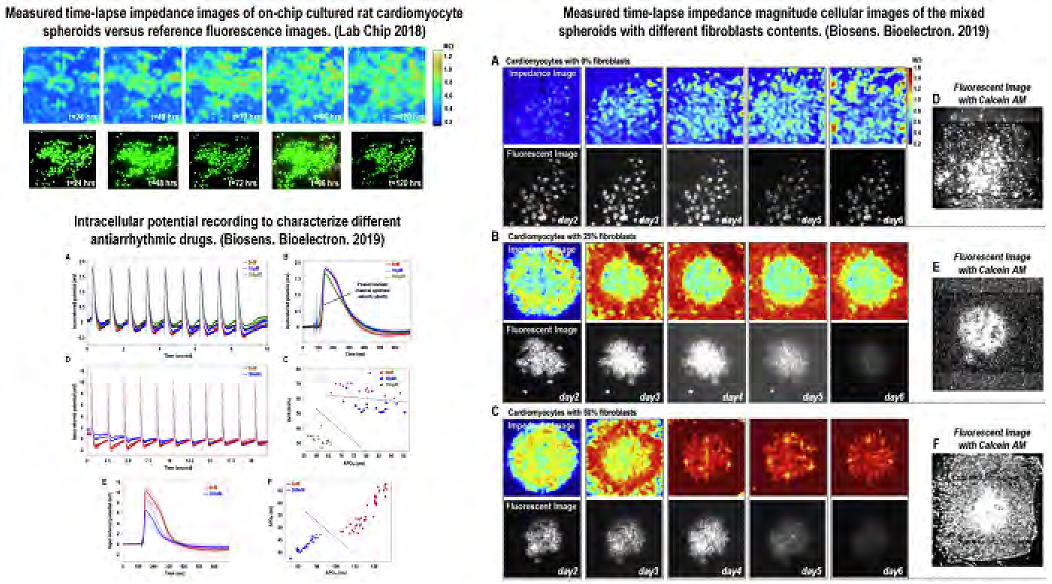
Qualcomm ANALOG DEVICES GLOBALFOUNDRIES qorvo

Student Projects: Multi-Modal LoC/PoC Biosensing Platform

- **Multi-Modal Lab-on-Chip (LoC) or Point-of-Care (PoC) Biosensing Platforms**
  - Mammalian Cell-based Assays LoC for New Drug Development
  - Mammalian Organ-on-Chip for Drug and Pathogen (Bacteria and Virus) Studies
  - Point-of-Care (PoC) Biosensor Devices
  - Synthetic Biology Screening
- **Biocompatible Packaging and Electronics Interface**
  - CMOS-Compatible Interface Electrodes Designs, Fabrication, and Characterization
  - Ultra-Low-Drift Reference Electrode Designs
  - CMOS-Microfluidics Co-Designs and Packaging

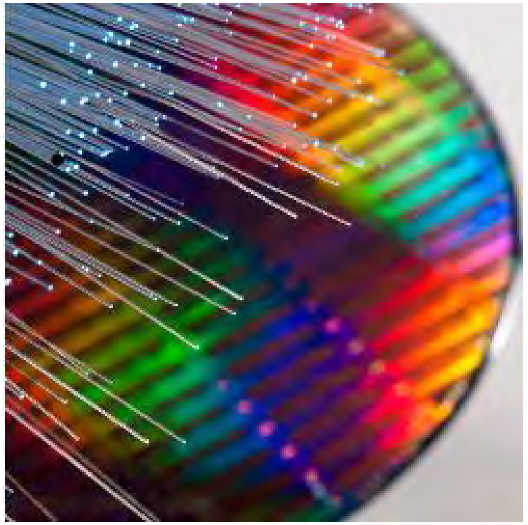


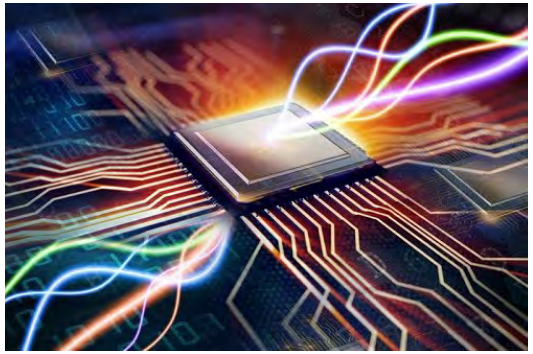


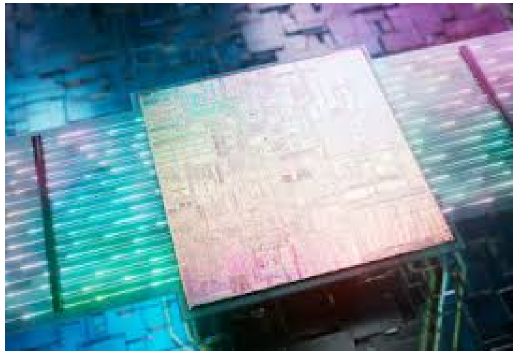


Student Projects: Hybrid Electronics-Photonics Systems

- **Silicon Photonics and Electronics Components and Sub-Systems**
  - On-Chip silicon photonics grating couplers, waveguides, resonators, modulators
  - Silicon photonics fully integrated interferometers
  - High-speed high-efficiency modulator drivers
- **Hybrid Silicon Photonics and Electronics Systems**
  - Silicon photonics and cryo-CMOS for quantum computing
  - Silicon photonics arrays for LIDAR imaging and ranging
  - "Auto-Focusing" photonics imaging arrays
  - Joint Electronics-Photonics signal processing







GLOBALFOUNDRIES

ETH zürich | University of Zurich[UZH]

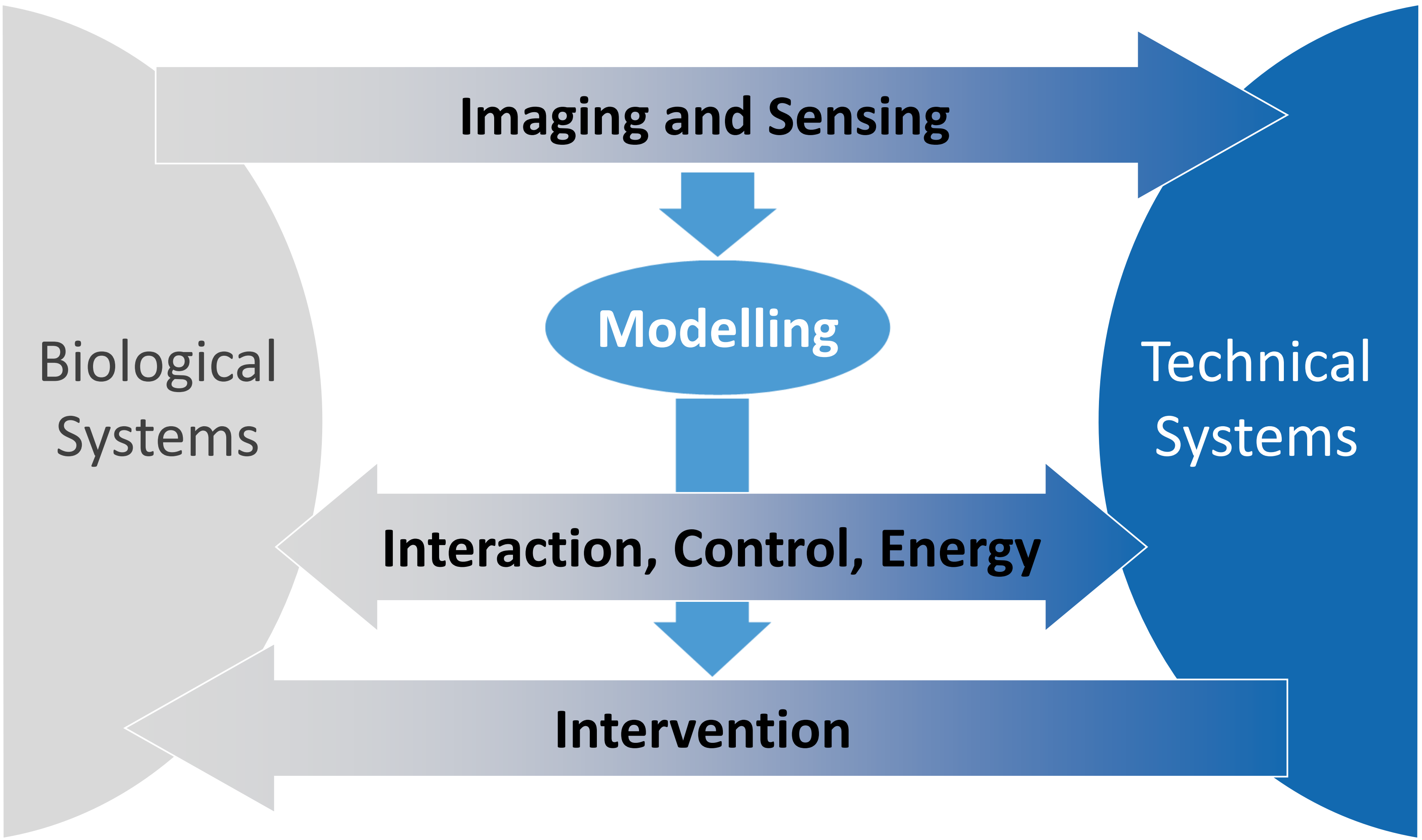
Biomedical Engineering

Research Topics and Core Courses

Institute for Biomedical Engineering (IBT), ETH Zurich and University Zurich

www.biomed.ee.ethz.ch

Bridging Biological and Technical Systems

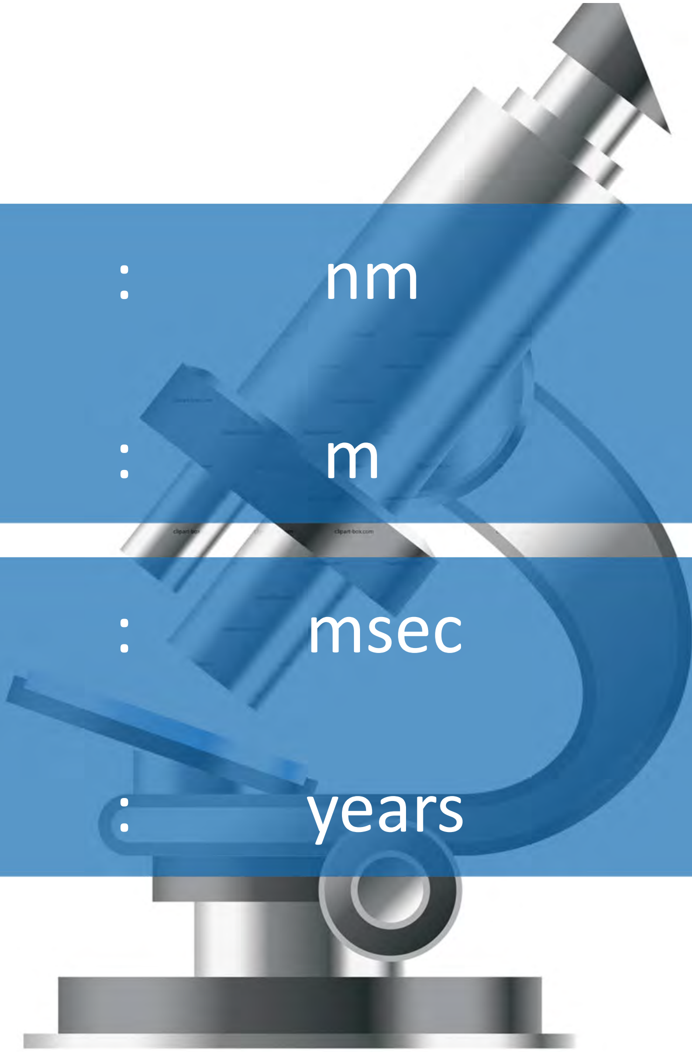


Biomedical Engineering

Engineering
embrace complexity,
play by rules of biology

Biology and Medicine
embrace reductionism,
get modular and quantitative

Challenges

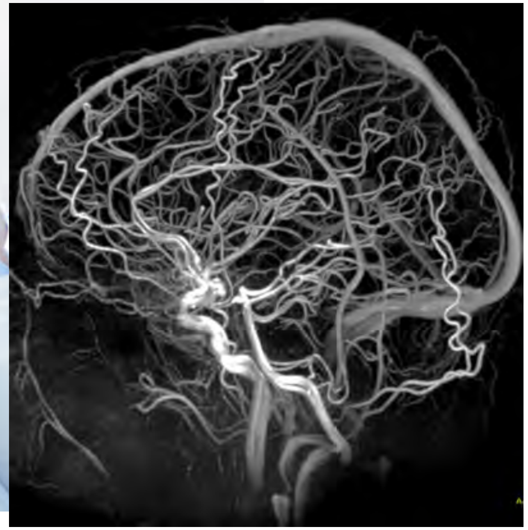


Proteins	:	nm	$1 : 10^9$
Body	:	m	
Synapse	:	msec	$1 : 10^{10}$
Life	:	years	

ETH zürich | University of Zurich[UZH]

Biomedical Imaging

Prof Klaas Pruessmann

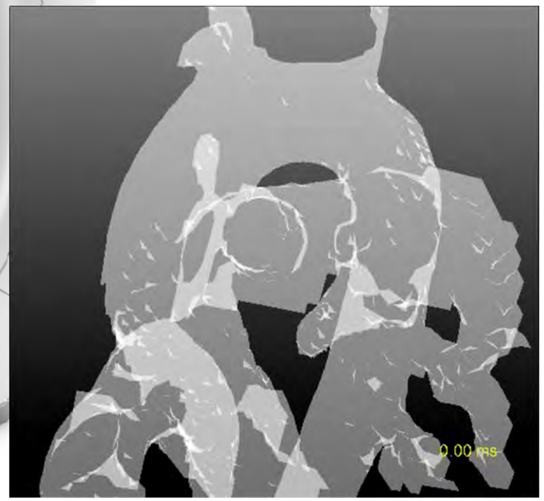


“Advancing Magnetic Resonance instrumentation and methods at very high magnetic fields for human applications.”

ETH zürich | University of Zurich[UZH]

Biomedical Imaging

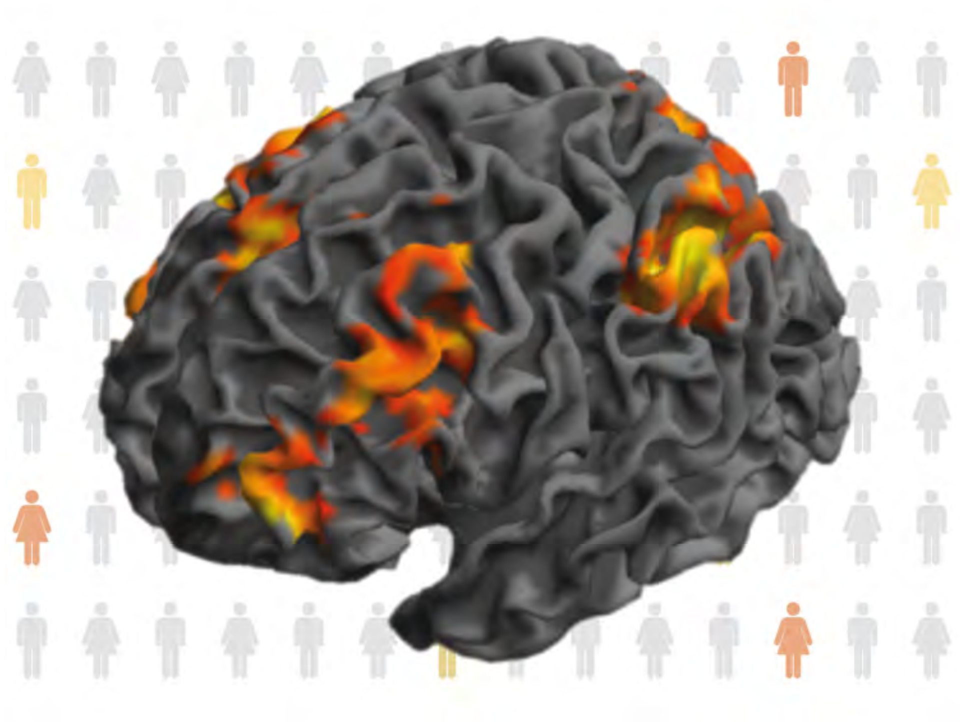
Prof Sebastian Kozerke

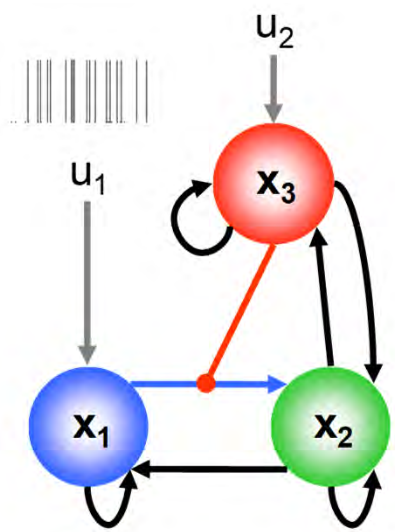


“Developing Magnetic Resonance imaging and spectroscopy methodology to diagnose cardiovascular diseases.”

Neuromodeling

Prof Klaas Enno Stephan

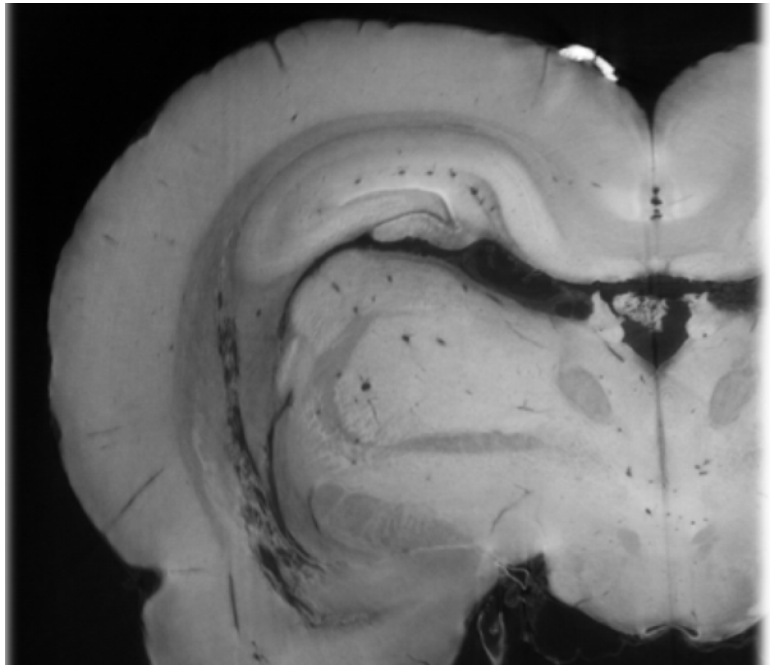


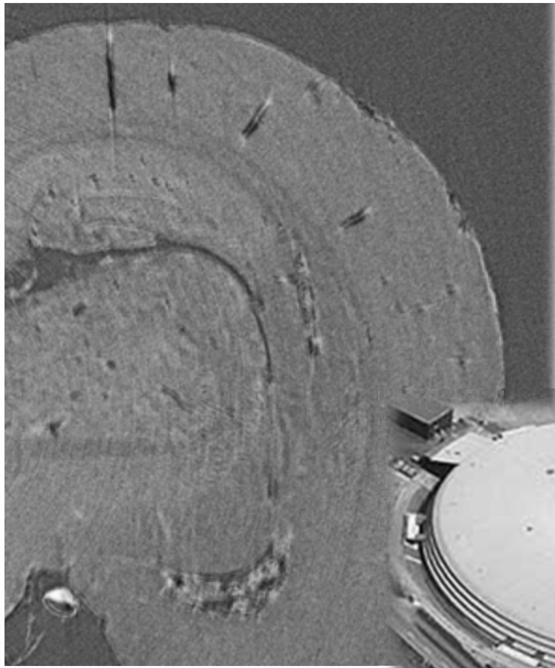


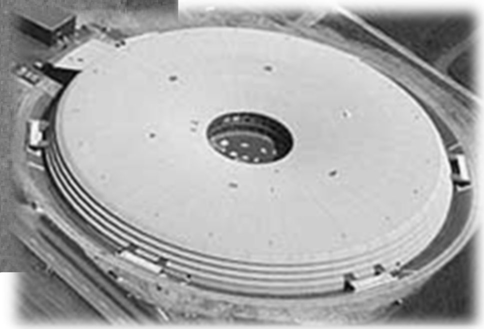
"Designing computational assays of individual disease mechanisms to provide new patient-specific diagnostic tools."

X-Ray Imaging

Prof Marco Stampanoni





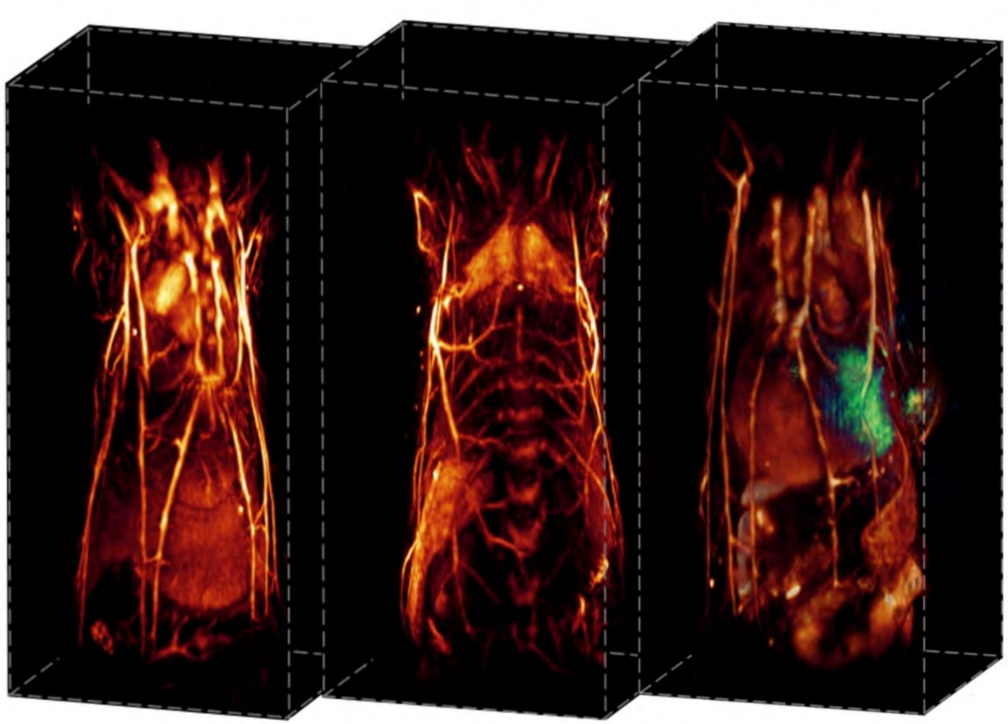


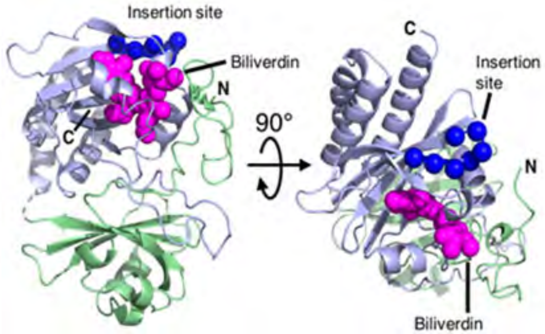
"Engineering of X-ray imaging technology, methods and applications for synchrotron and clinical imaging."

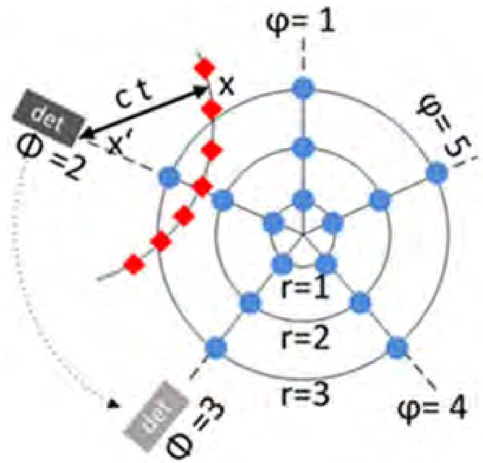
ETH zürich | University of Zurich UZH

Functional and Molecular Imaging

Prof Daniel Razansky



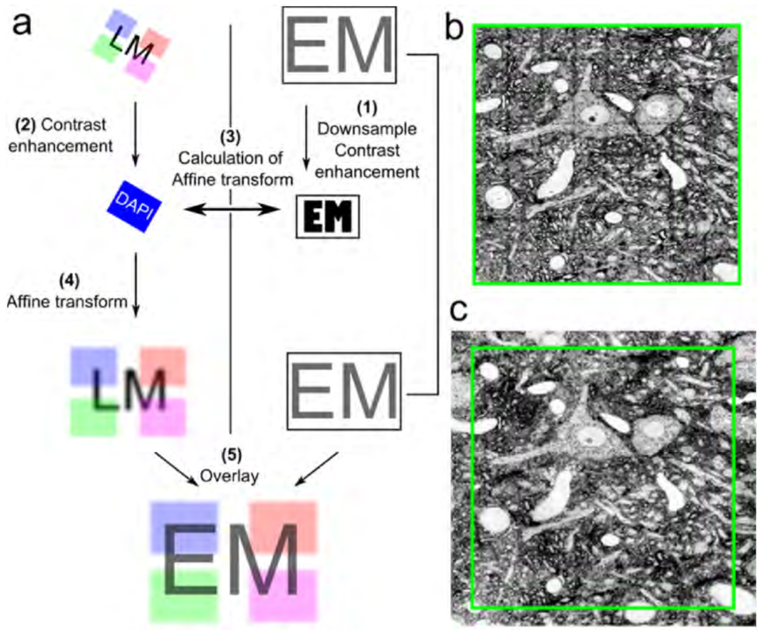


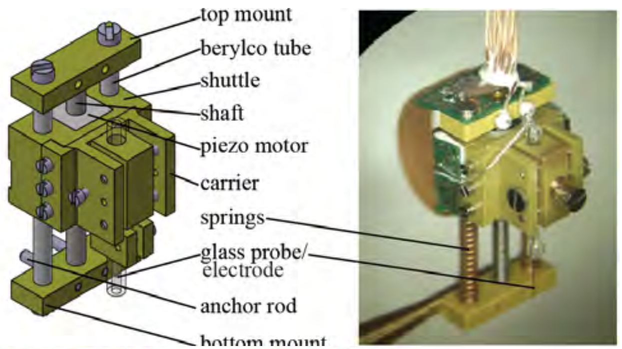


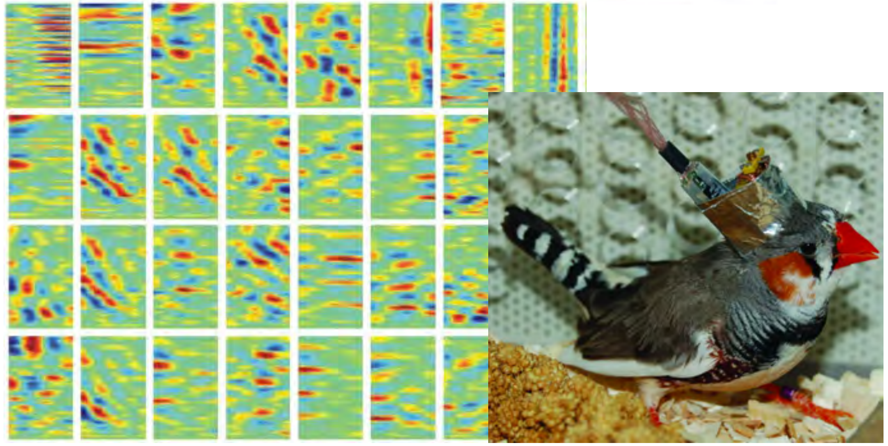
“Developing new generation imaging technologies to tackle key challenges in biology and medicine”

Neural Information Processing

Prof Richard Hahnloser



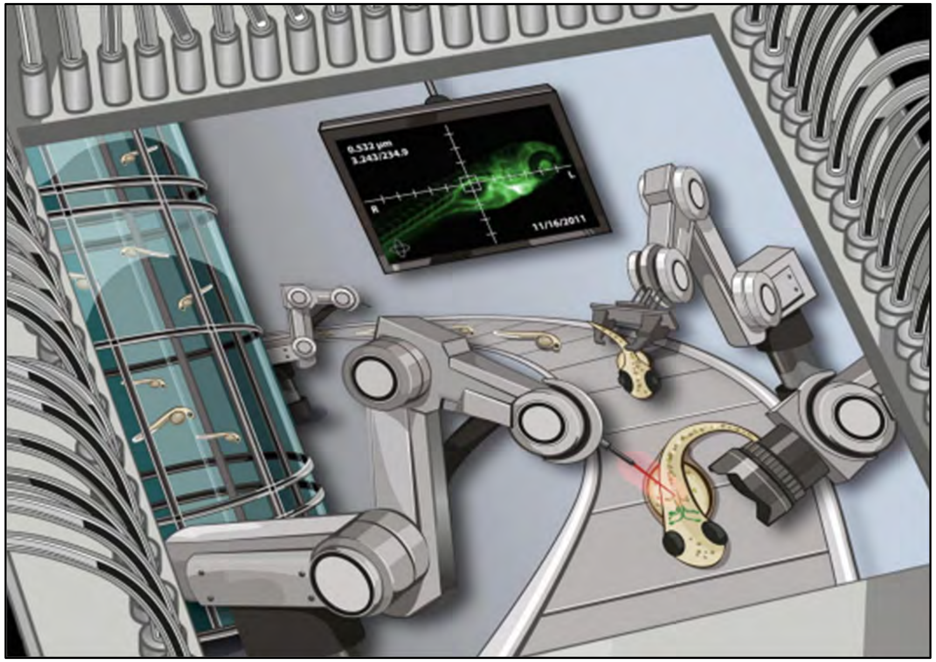


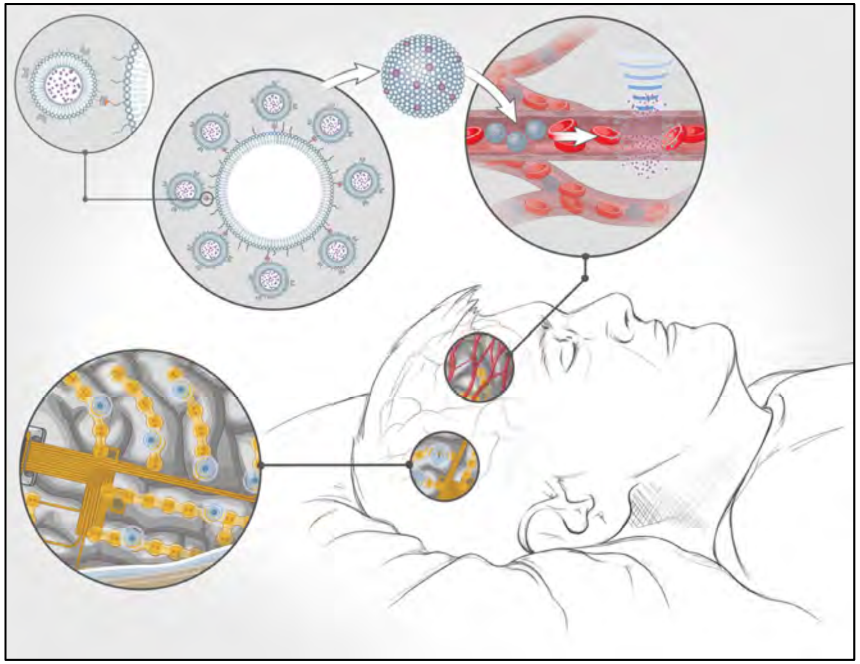


"Discovering neural code of behavior in freely moving animals and reconstructing and simulating neural circuits."

Neurotechnology

Prof. M. Fatih Yanik





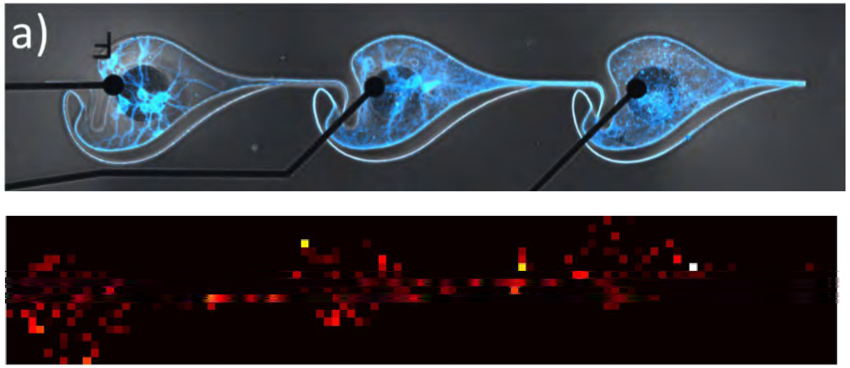
“Developing brain machine interfaces to decode and manipulate brain circuits and cognitive behavior.”

ETH zürich | University of Zurich

Prof. Janos Vörös

D-ITET, Laboratory of Biosensors and Bioelectronics

Neurons on a chip



Point-of-need diagnostics

"Developing biosensors and bioelectronic devices to diagnose and treat diseases and answer fundamental neuroscience questions."

ETH zürich | University of Zurich

Core Courses

Autumn

Biomedical Imaging
Kozerke, Pruessmann (6 ECTS)

Bioelectronics and Biosensors
Vörös, Yanik (6 ECTS)

:

Spring

Neural Systems
Hahnloser, Yanik (6 ECTS)

:

Core Courses

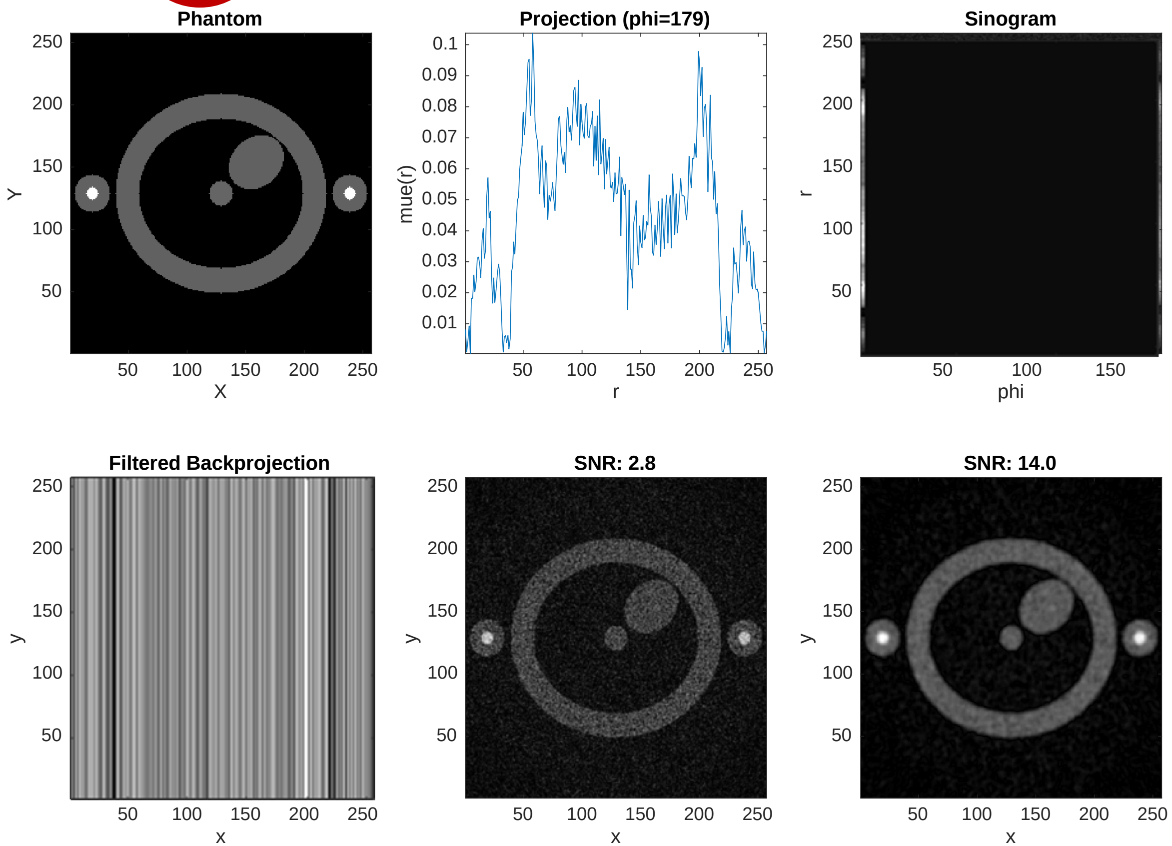
Biomedical Imaging
Lectures: 2V + 3U (Matlab)

- **Signal theory and processing**
- **X-rays – projections and computed tomography**
- **Nuclear imaging – single photon and positron emission**
- **Magnetic Resonance imaging**
- **Ultrasound imaging**

Core Courses

Biomedical Imaging

Lectures: 2V + 3U (Matlab)



Core Courses

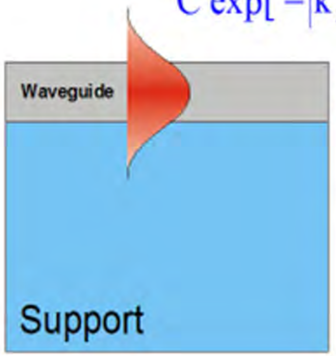
Bioelectronics and Biosensors
Lectures: 2V + 2U

- **Fundamentals of various biosensing modalities**
- **Biomeasurements with photons**
- **Bioelectric potentials and electron transfer**
- **Electronics of neurons**
- **Functional electric stimulation and recording**
- **Neural networks memory and learning**

Core Courses

Bioelectronics and Biosensors

Lectures: 2V + 2U

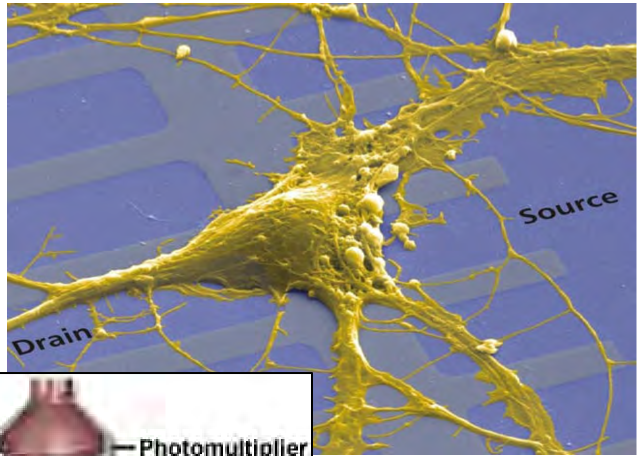


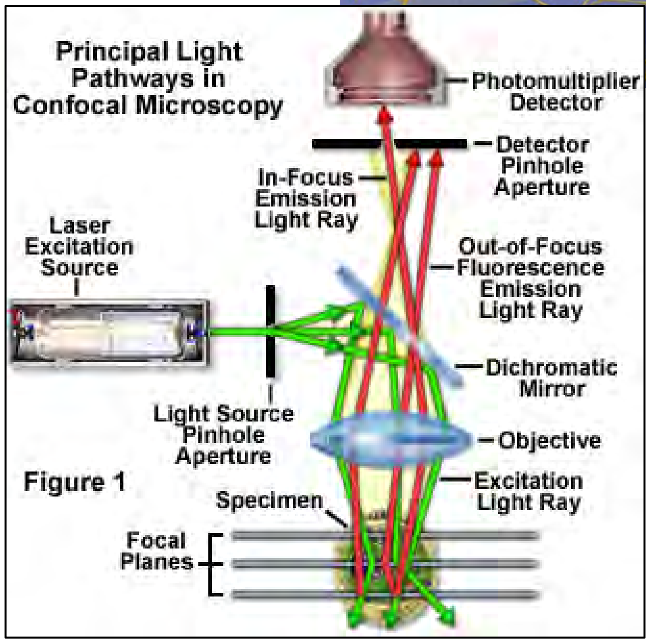
$$C \exp[-|k_{z,c}|(z - d_F/2)]$$

$$B \exp(ik_{z,F} z) + A \exp(-ik_{z,F} z)$$

$$D \exp[|k_{z,s}|(z + d_F/2)]$$

$$\sigma \sim \frac{\lambda}{2\pi} \frac{1}{\sqrt{N^2 - n_C^2}}$$





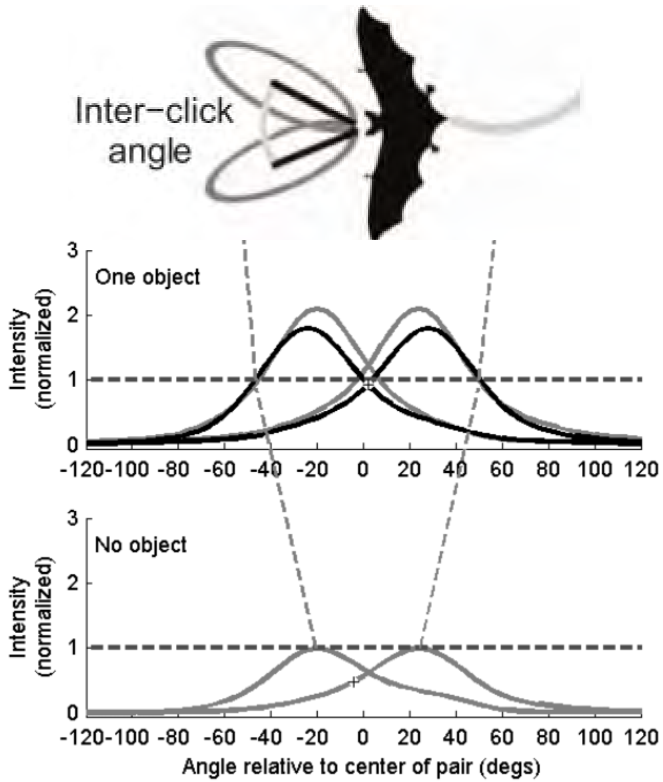
Core Courses

Neural Systems
Lectures: 2V + 2U

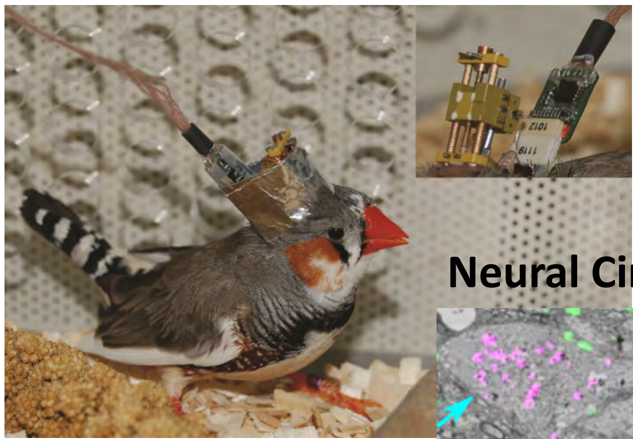
- **Microscopy Techniques for Neural Circuit Analysis**
- **The Neural Code of Behavior in Freely Moving Animals**
- **From Synaptic Plasticity to Deep Neural Networks**
- **Principles of Visual and Auditory Processing**
- **Imitation Learning and Motor Control**
- **Neural Integrators and Sequence Generators**

Core Courses

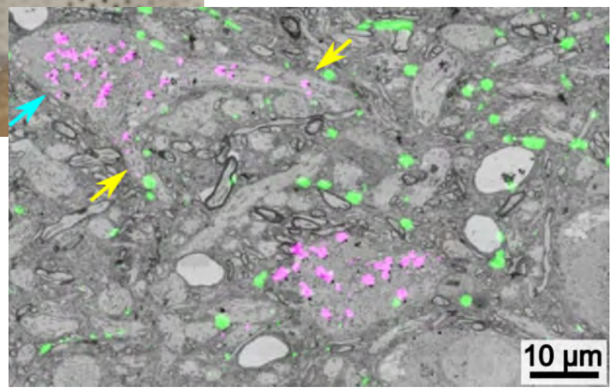
Neural Systems
Lectures: 2V + 2U



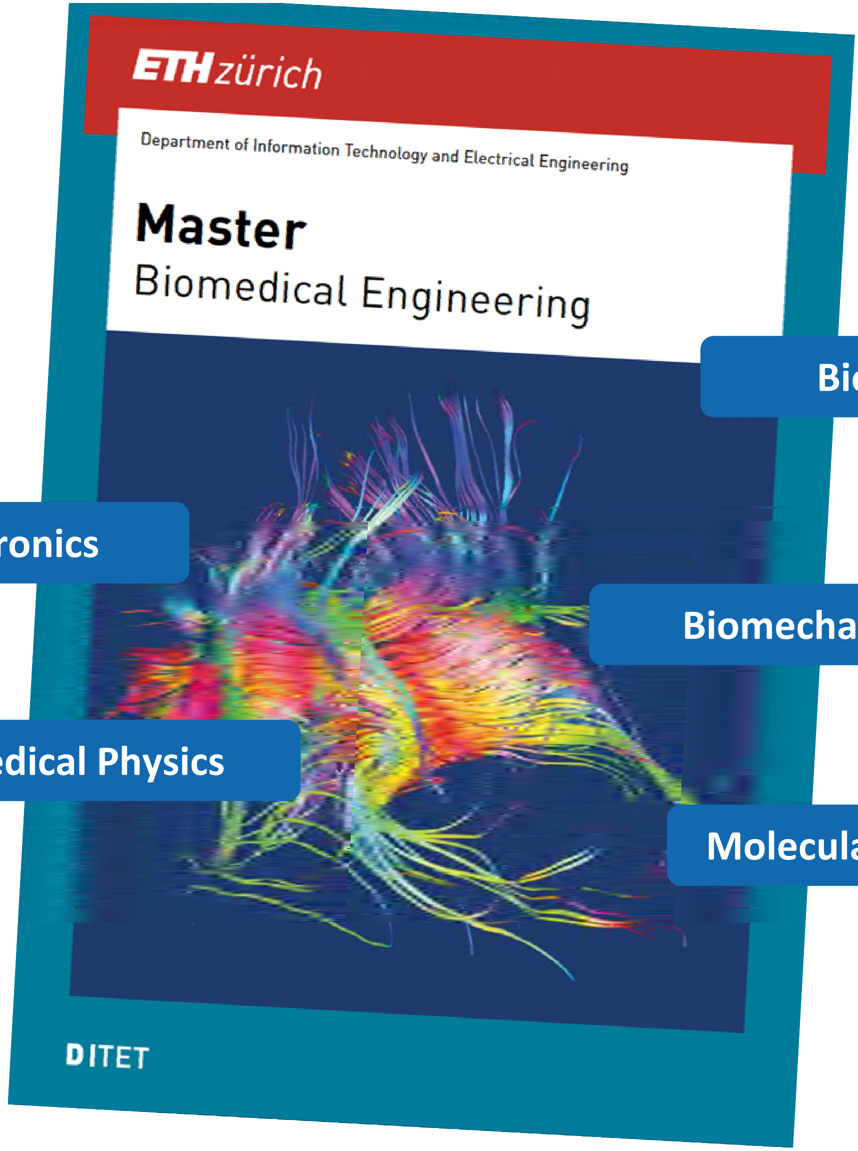
Neural Codes



Neural Circuit Reconstruction

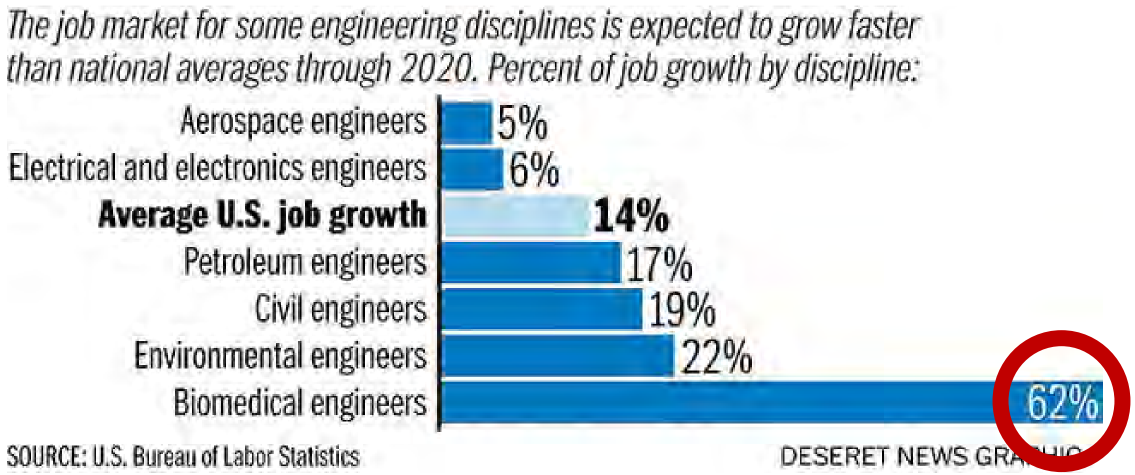


Master in Biomedical Engineering



- Bioimaging
- Bioelectronics
- Biomechanics
- Medical Physics
- Molecular Bioengineering

Career Outlook



Student Projects

Find group work, semester and Master projects:
www.biomed.ee.ethz.ch/studentprojects.html

Contact

Institute for Biomedical Engineering
Janos Vörös
janos.voros@biomed.ee.ethz.ch
ETZ F82, 044 632 5903