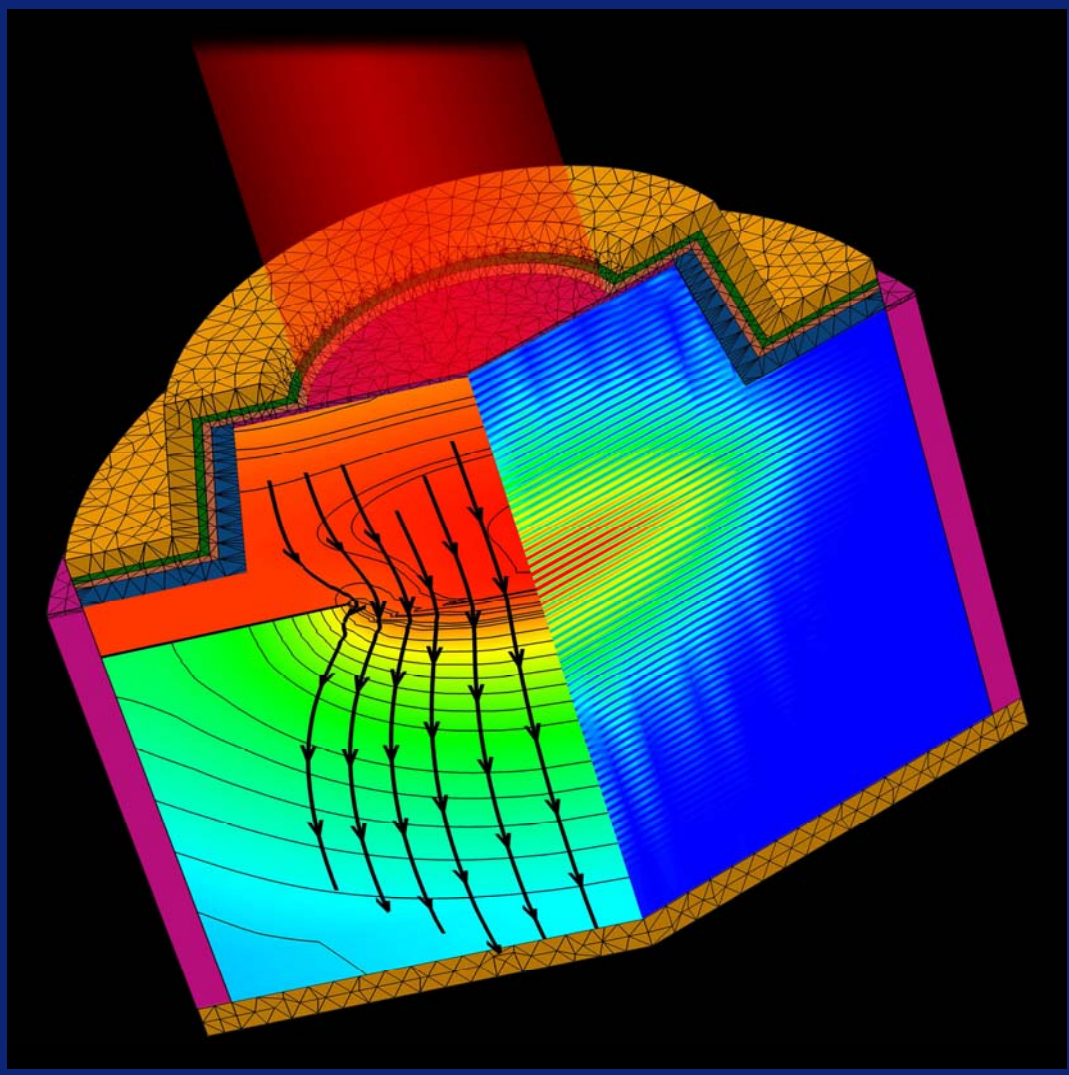
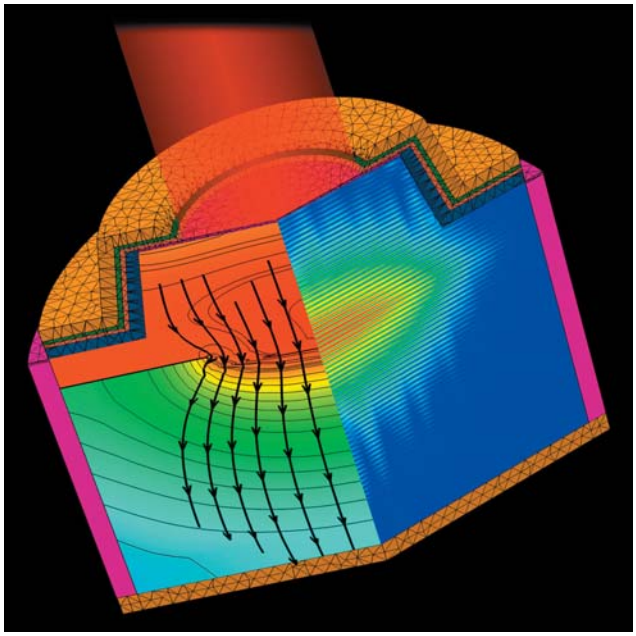
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Integrated Systems Laboratory
Microelectronics Design Center

Research Review 2004



Cover Image:
Simulation of a Vertical-Cavity Surface-Emitting Laser (VCSEL) with Physics-based Models



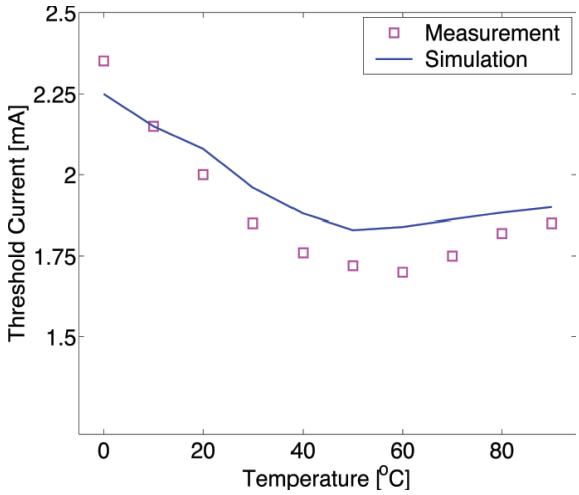
The cover image shows results from a simulation of a vertical-cavity surface-emitting laser (VCSEL). The VCSEL is a single mode device with an oxide aperture emitting at a wavelength of 850 nm.

The simulation has been performed with a two-dimensional model that exploits the cylindrical symmetry of the device structure. It solves the coupled electronic, optical and thermal equations in a self-consistent fashion. The right face of the illustration shows the fundamental mode of the optical intensity obtained from a solution of the complex vectorial Helmholtz equation. The left face shows the temperature profile at an operation point above threshold, and streamlines of the total electrical current. As a result of the low thermal conductivity of the oxide (black horizontal line), the main temperature rise is in the top mesa and in the center of the active region. This so-called self heating affects the device performance considerably.

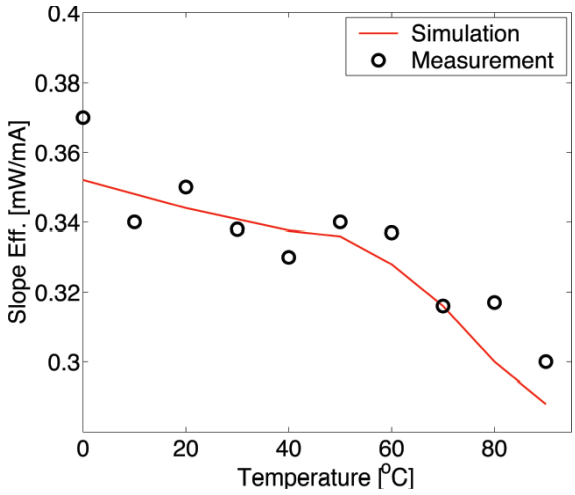
This simulation model has been calibrated extensively with measurements from an existing device. Comparisons are shown below for typical terminal characteristics. Calibrated, physics-based models enable predictive design studies using computer-aided design. For further information see pages 63 (right) and 64.

The TCAD based VCSEL design and the development of the simulation software is done in a joint project with Beam-Express SA, Avalon Photonics, Synopsys Switzerland LLC (formerly ISE AG), and LPN EPF Lausanne.

This project is funded by KTI (Commission for Technology and Innovation).



Threshold current versus ambient temperature, simulation and measurement.



Optical external efficiency versus temperature, simulation and measurement.

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Research Review 2004

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Hubert Kaeslin Norbert Felber Dölf Aemmer

Calibration of Physical Models for Silicon up to Very High Temperatures

The design of robust electrostatic discharge (ESD) protections of microcircuits is one of the major issues in microelectronics. The coupling of electrostatic discharges to integrated circuits results in high-current transients, which may lead to the failure of the device as a consequence of thermal runaway phenomena within the semiconductor. The development of appropriate predictive simulation tools to ensure the necessary level of robustness for the device requires an accurate characterization of the main physical parameters of silicon up to local temperatures approaching the melting point. This goal has been pursued in the framework of the European research project DEMAND, where the impact ionization coefficient (IIC), the bulk mobility, and the surface mobility of electrons and holes in silicon have been measured up to temperatures, which have never been reached before. The dedicated test structures selected for the measurement of the multiplication factor were Static Inductance Transistors (SIT, see inset in Figure 1), Bipolar Junction Transistors (BJT), and Vertical DMOS transistors all designed to cover a large interval of the electrical field. Figure 1 shows the (electron) current collected at the gate of a p-SIT, which arises due to the impact generation and carrier separation along the channel. These data are used to calibrate the compact model for the IIC of holes as a function of the electric field and of the temperature. The University of Bologna model (UNIBO) for the IIC of electrons calibrated up to a temperature of 773 K and extrapolated to a temperature of 1000 K is presented in Figure 2. This model has been validated for fields in the 40 – 500 kV/cm range. The maximum temperature, which can be reached by these test structures is limited by the dominance of thermal carrier generation over impact generation. The operating range of conventional junction-isolated van der Pauw structures for the characterization of the Hall carrier mobility in silicon as a function of the temperature is limited to 400 K by several parasitic effects.

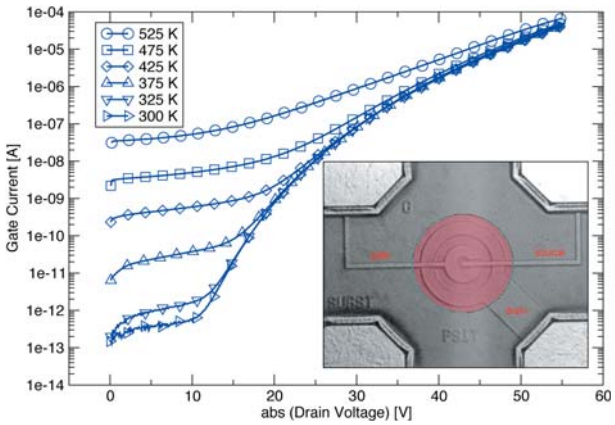


Fig. 1 The measurement of the gate current of the p-SIT (inset) as a function of the drain voltage is used to extract the IIC of holes as a function of the temperature

This limit can be extended up to about 700 K by a proper design of the structures and by the application of a reverse bias to the isolating junction. Nonetheless, alternative structures are needed to reach the temperature range of interest. Figure 3 shows the measurement up to 973 K of the Hall bulk mobility of electrons carried out by unipolar van der Pauw structures using a dedicated metallization scheme. Figure 4 shows the improvements in the prediction of the snap-back behavior of an ESD diode submitted to reverse transmission line pulses, when using the newly calibrated electron impact ionization model.

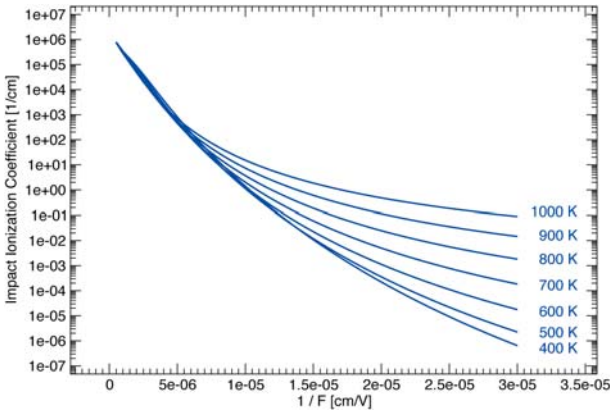


Fig. 2 IIC of electrons as a function of the electric field implemented according to the Bologna model calibrated with the present measurements

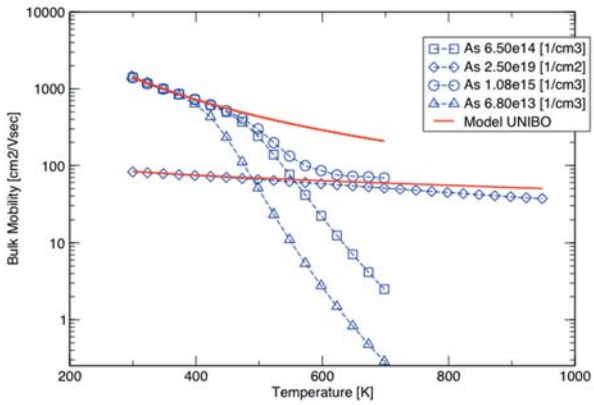


Fig. 3 Comparison of the measured bulk mobility of electrons for different doping concentrations (symbols) with the UNIBO model (red lines) prior to calibration.

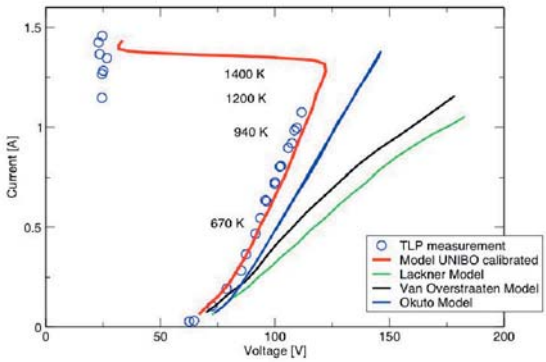


Fig. 4 Measurement and simulation of the characteristics of an ESD diode submitted to a reverse high-voltage pulse from the breakdown to the thermal failure. With the newly calibrated model (UNIBO), the prediction is correct up to 1200 K

More information on this project can be found on pages 71 and 72 (left), and in the conference paper “Measurement of the Silicon Resistivity at Very High Temperature with Junction Isolated Van der Pauw Structures” by C. Corvasce et. al., referenced on page 136.

Contents

Preface

Introduction

This is a report on the academic and research activities of the Integrated Systems Laboratory (IIS) and the Microelectronics Design Center (DZ) at the Department of Information Technology and Electrical Engineering (D-ITET) of the Swiss Federal Institute of Technology in Zurich (ETH Zurich) for the year 2004.

The IIS staff includes three professors, six research associates, eleven post docs, forty nine (49) PhD students, three computer system administrators, three secretaries, and five technicians.

Research topics in digital, mixed, and analog integrated circuit (IC) design range from sensitive sensor interfaces to GHz RF circuits on the analog side, over analog-to-digital converters to the digital field covering projects from low-power design methodologies to complex systems-on-a-chip (SoC). Technology CAD (TCAD), technology and device development, computational optoelectronics, physical characterization, and bio-electromagnetics complement the research fields of IIS towards professional tools for modeling and optimizing micro-electronic and opto-electronic devices and technologies in the deep-submicron and nanometer range as well as bio-electromagnetic systems.

Microelectronics Design Center

The Microelectronics Design Center, headed by Dr. H. Kaeslin, with four staff members, is a service organization of the Department of Information Technology and Electrical Engineering. It is closely co-operating with IIS and other D-ITET and ETH Zurich laboratories in their design research and teaching activities for VLSI, analog, and system electronics (see page 128).

Research Projects and Funding

Following the trends of earlier years, our co-operation with national and international partners is at the center of our activities. In 2004, one new European (funded by BBW, Swiss Federal Office for Education and Science), two new KTI (Swiss Commission for Technology and Innovation), three new industrial, and one new research projects funded by ETH Zurich have started in the fields of semiconductor process and device development and simulation, complex digital systems on chip, computational optoelectronics, and bio-electromagnetics. Overall, IIS was involved in a total of 30 research projects. Four of them were EU projects funded by BBW, eleven by KTI, four by ETH Zurich, one by SNF, three by TOP NANO 21, and seven by industry in Switzerland, Europe, USA, and Japan.

A total of 42 job positions at IIS was financed by third-party projects, which, in relation to the 25 ETH positions, and in comparison with other laboratories of ETH Zurich, is a sign of the quality of research performed by our staff.

PhD Students and Honorary Professor

In 2004, eleven PhD students finished their doctoral thesis successfully. IIS offers an excellent and highly stimulating research environment that permits PhD students to work on very attractive topics and, nevertheless, to finish their thesis in a comparatively short time. However, it is still an ambitious challenge to find very qualified PhD students from all over the world. We try the best to overcome this situation by an appropriate salary policy and by focusing the student activities on scientific work in order to reduce the administrative and educational overhead.

PD Dr. Andreas Schenk was honored with the Titularprofessor (honorary professor) of ETH Zurich for his outstanding contributions to theory and physics based modeling of semiconductor devices in the nanometer regime.

Analog and Mixed Signal Group

For the Analog and Mixed Signal Integrated Circuit Design (AMIC) Group of Prof. Huang, the year 2004 has shown a continuation of work around the group's focus in the field of RF and base-band circuit design for telecommunications applications.

In 2004 the group´s research efforts were rewarded with 3 papers at the International Solid-State Circuits Conference (ISSCC), all in the converter design area. On the ADC side, the group presented a delta-sigma modulator that offers 10 MHz (VDSL compatible) bandwidth at very high resolution. On the DAC side both the delta-sigma technique with semi-digital postfiltering leading to excellent resolution and linearity at moderate bandwidth as well as a high-speed technique based on current sources with background calibration have been published.

In 2004 the AMIC group has been partner in several Swiss and international projects with research focus in advanced circuit design for wireless applications and implementation in deep-submicron CMOS technologies at the 130nm node and beyond. The group´s spin-off company ACP has participated 2004 in the EU-project "End-to-End Reconfigurability", a big European effort to make wireless telecommunication equipment more versatile and hence saving development cost.

IC and System Design and Test Group

The research on multi-antenna (MIMO) communications systems in close collaboration with the Communication Theory Group of Prof. Helmut Bölcskei became the major activity of the digital design group. Lifely scientific interest in our real-time MIMO-OFDM Testbed has been evinced. Significant results are two Sphere Decoder VLSI implementations - among the first and the most powerful worldwide. The second industrial collaboration on MIMO has been initiated with a Swiss company.

Further activities of the group led to lower-power hearing aid circuits, a prototype system for medical communication over the human body, progress of Globally-Asynchronous Locally-Synchronous (GALS) systems on chips towards industrialization, and Differential-Power-Attack resistant Crypto ASICs.

Technology CAD Group

The Device Physics Group continued to study quantum and ballistic effects in ultra-small electronic devices with focus on the first-principle modeling of transport parameters, correlation functions, and noise sources close to and far from thermodynamic equilibrium, respectively, on correlation effects on the silicon bulk mobility, and on the impact of quantization and remote Coulomb scattering on the channel mobility in silicon MOSFETs.

The new simulation package SimnIC has been accomplished which contains a 2D full-band Monte Carlo simu-

lator (one-particle and ensemble) and a finite-element based energy-balance simulator for silicon devices. The Monte Carlo code allows to compute exact solutions of any moment of the inverse scattering operator of the Boltzmann equation as well as exact transport parameters for the drift-diffusion and energy-balance models in a given point of 1D or 2D devices for ambient temperatures between 50 K and 500 K. The theoretical base was found by a proof of the existence and uniqueness of moments of the inverse scattering operator of the Boltzmann equation and by a general discretization scheme to actually compute these moments by iteration.

The multi-subband scattering matrix approach developed for the SIMNAD quantum mechanics simulator was improved and applied to the simulation of quantum-ballistic currents in nanodevices. The exchange of realistic doping profiles was enabled in the self-consistent coupling scheme between SIMNAD and the device simulator DESSIS. SIMNAD was extensively used in the EU-IST project SINANO (Silicon-based Nanodevices) to study performance limits of double-gate silicon-on-insulator devices and silicon-based resonant tunneling diodes. Work has started on the self-consistent NEGF (Non-equilibrium Green's Function) modeling of quantum transport. A fast recursive algorithm for 1D simulations of RTDs including first-principle self-energies from elastic scattering has been developed and implemented.

Activities in process simulation included the elaboration of a complete deactivation model for group V donors and the evaluation of possible co-dopants for n-type silicon. Moreover, a thorough analysis was conducted of the migration mechanisms and energetics of the self-interstitial atom and the lattice vacancy in silicon. All of these investigations were conducted making use of static and dynamic ab initio simulations. In addition, a kinetic Monte Carlo drift-diffusion solver with charged defects and Fermi level effects was developed.

The parallel iterative linear solver for shared memory multiprocessor has been integrated into the device simulator. The performance was improved further and the solver is fully parallel now. Especially the parallel efficiency increased a lot. The computational costs for large scale 3D problems reduce dramatically compared to preliminary used linear solvers.

The mixed-mode device simulator has been extended by a harmonic balance analysis module, enabling a physics-based understanding of harmonic distortion phenomena in nonlinear devices important for large signal RF applications. The constituting frequency domain harmonic balance equation is solved by a Newton-like procedure which has been coupled both to a direct solver as well as to a very efficient memory-free preconditioned iterative solver.

Computational Optoelectronics Group

The COE group has focused on the development of new simulation models and TCAD based device analysis. The microscopic laser noise model has been extended to include phase noise, and the gain table loader allows, for the first time, to couple many body gain to an electro-opto-thermal simulator. In collaboration with our industrial partners, several substantial design improvements have been achieved using simulation, e.g. the use of a sophisticated chirped quantum well design resulted in a superluminescent LED with doubled bandwidth. With the aid of multi-dimensional simulation, the full tuning map of an integrated, broadly tunable laser has been analyzed. Finally, the OptoLab has been inaugurated, and numerous experiments from the COE group and its partners have contributed to the model and device improvement.

Physical Characterization Group

The activities of the Physical Characterization Group covered four main fields: the characterization of the electrical properties of silicon at very high temperatures, the extraction of doping profiles by scanning probe techniques, the simulation and the experimental assessment of ESD protection circuits and floating gate memory cells, and the demonstration of fast procedures for the electro-thermal simulation of power units for automotive applications. Particular focus has been set on the investigation of the complementarity of Scanning Capacitance (SCM) and Scanning Spreading Resistance Microscopy (SSRM). For the first time the performance in terms of dopant profiling and imaging capabilities of both techniques have been compared with dedicated test structures designed and integrated in the framework of an European network including nine different laboratories. In addition, the development of a new experimental setup enabled the calibration of the theoretical models for the bulk mobility and for the impact ionization up to 973 K and 873 K, respectively.

Bio-Electromagnetics Group

IT'IS, the "Foundation for Research on Information Technologies in Society" (headed by ETH adjunct Prof. Niels Kuster), a non-profit research institution supported by ETH Zurich, established its scientific and technical work in close collaboration with our laboratory. The research activities of IT'IS are in the domain of the interaction of electromagnetic radiation with biological organisms, in advanced measurement equipment for electromagnetic radiation, and health risk assessment. A growing number of research projects and PhD students at IIS is funded by the global wireless communications industry, several governmental agencies, and the Commission of the European Union. It turned out that this collaboration with IT'IS is very fruitful and a benefit for both institutions (see page 129).

Education

Next to research, teaching occupies a central role in our activities. Our staff is responsible for several core lectures in Information Technology and Electrical Engineering as well as in other departments (see page 118). The chapter on student projects (page 89) gives an overview on the manifold diploma theses and semester projects. The unbroken attraction of IC design projects is complemented by a rising interest for the optoelectronics research of our lab. The outstanding semester project on page 38 (left) and the excellent Diploma Theses on page 95 (left) and 42 (right) have been presented at international conferences (see Presentations, page 130).

Department of Information Technology and Electrical Engineering

Prof. Fichtner was Head of the Department of Information Technology and Electrical Engineering until November 2004.

Spin-off ISE AG acquired by Synopsys, Inc.

In 1993 ISE Integrated Systems Engineering AG was founded as spin-off of IIS in the field of Technology CAD (TCAD). Main business activities were software development, application and customer support in microelec-

tronics, optoelectronics and nano technologies. ISE AG's business was successful, it became TCAD market leader and had subsidiaries in Silicon Valley and Tokyo with 120 employees worldwide.

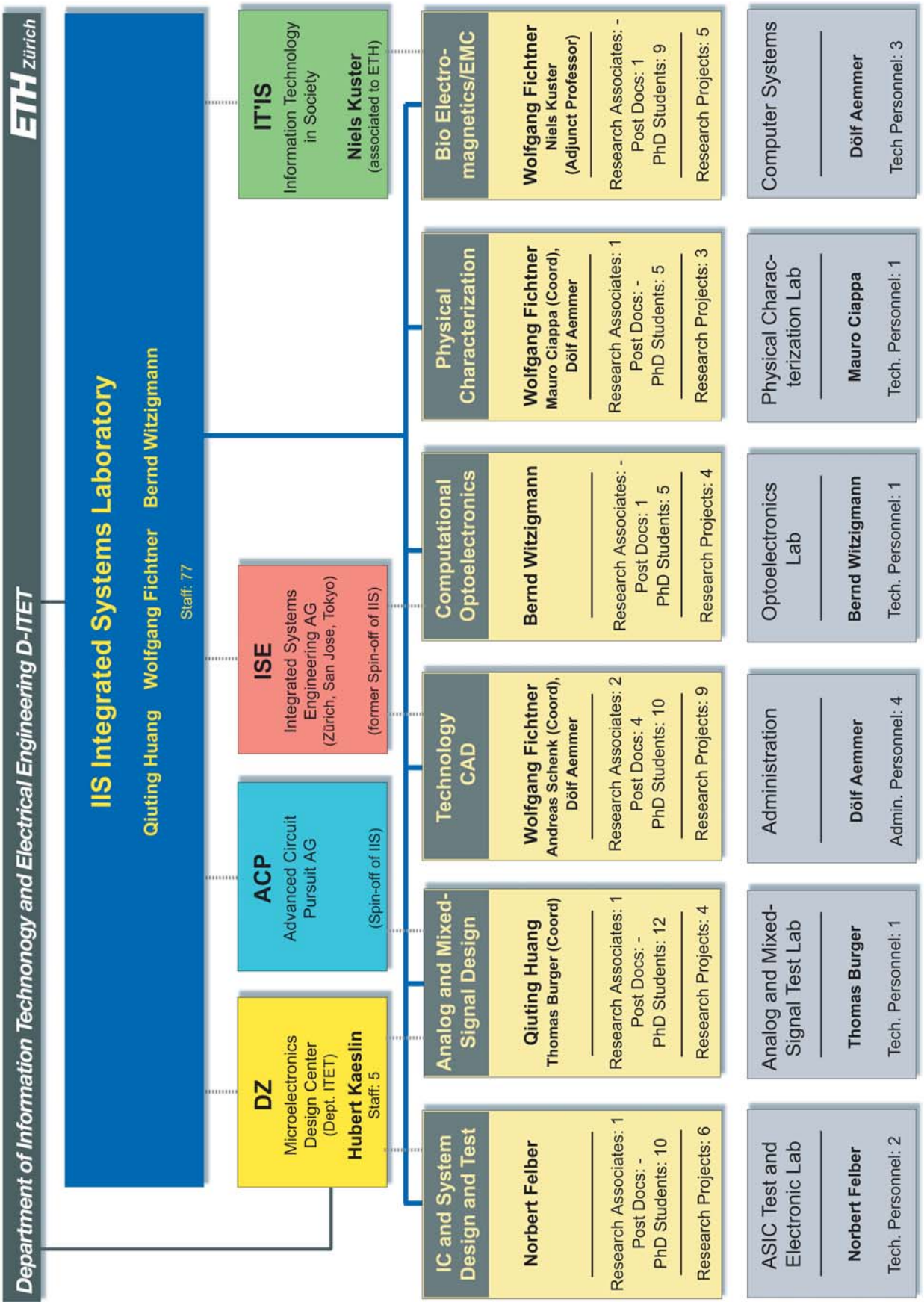
In October 2004 ISE AG was acquired by Synopsys (www.synopsys.com). Synopsys, Inc. is a world leader in semiconductor design software and develops software that companies use to design systems-on-chips (SoCs) and electronic systems. Synopys existing TCAD business unit was merged with the ISE group to Synopsys TCAD Business unit under the direction of Prof. Wolfgang Fichtner. ISE's TCAD tools like DESSIS (device simulation) or FLOOPS (process simulation) belongs to the major products of Synopsys TCAD with high priority regarding scientific and technical innovation. ISE AG (Zurich) became Synopsys Switzerland LLC, it is a Swiss based subsidiary and the headquarter of Synopsys TCAD activities. It is still partner in ISE's European and national research projects and will intensify TCAD related research activities in cooperation with worldwide, European and national microelectronics industry and academia.

Partners and Funding Agencies

The activities of our laboratory were only possible through the support from the governing board of our university, and several national and international institutions and industrial parties. Special thanks go to our school, to the computing services of ETH Zurich, as well as to the Department of Information Technology and Electrical Engineering and its services and administration.

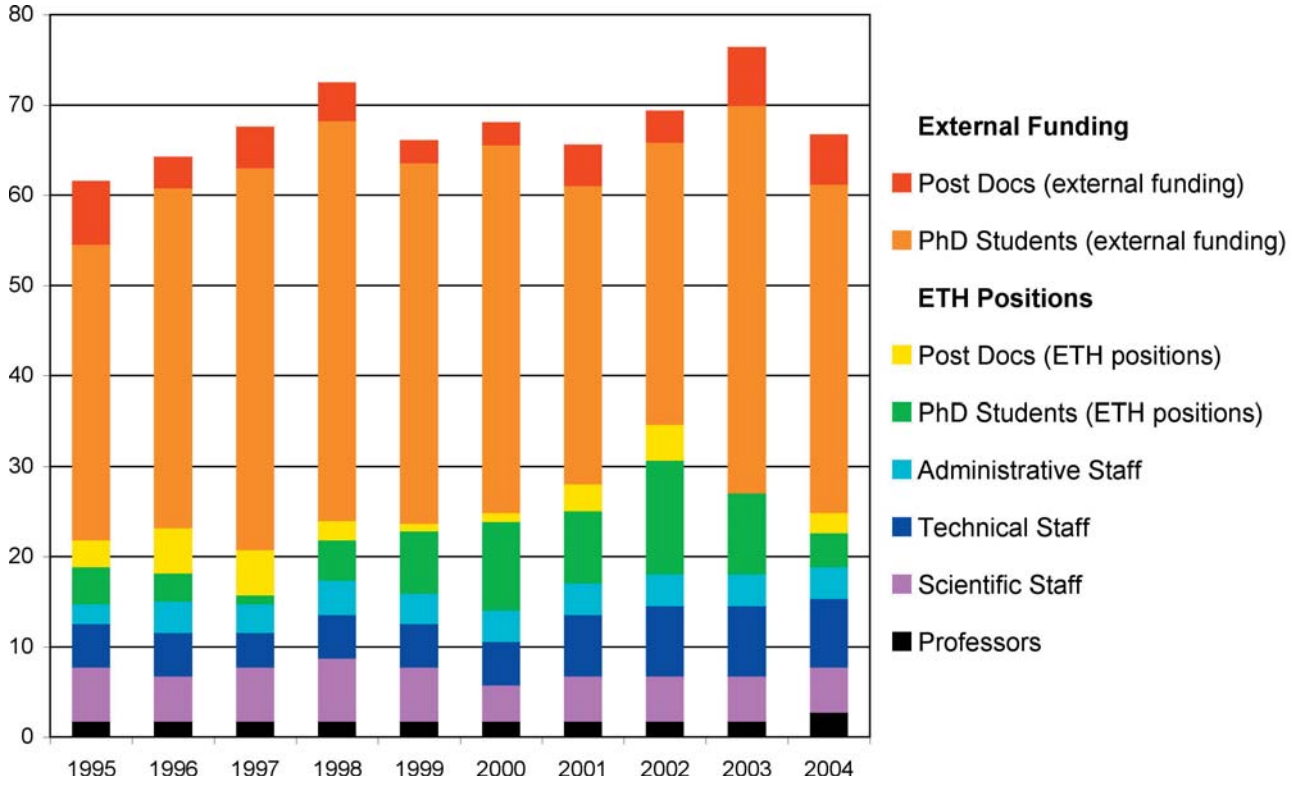
Finally, we would like to express our gratitude to the Swiss Commission for Technology and Innovation (KTI), the Swiss National Science Foundation (SNF), the Swiss Federal Office for Education and Science (BBW), the Swiss program TOP NANO 21, and the Commission of the European Union for their financial support. Just as much we would like to thank our partners ACP, Albis Optoelectronics, austriamicrosystems Austria, Avalon Photonics Switzerland, BeamExpress Switzerland, Bernafon Switzerland, Bookham Switzerland, Bosch Germany, BridgeCo Switzerland, CNR-IMETEM Italy, EPFL Switzerland, Exalos Switzerland, FNM Switzerland, Fraunhofer-Gesellschaft Germany, Fujitsu Japan, IBM Research Switzerland, IMEC Belgium, IMMS Germany, Infineon Germany, INRIA France, ISE Integrated Systems Engineering AG Switzerland (now Synopsys Switzerland LLC), IT'IS Foundation Switzerland, Miromico Switzerland, Philips Semiconductors Zurich Switzerland, Philips Research Belgium, Philips NATLAB Netherlands, Siemens Germany, SIGMA-C Germany, SPEAG Switzerland, ST Microelectronics Italy and France, Synopsys Switzerland LLC (former ISE Integrated Systems Engineering AG), TDC Switzerland, Toshiba Japan, Toyota Japan, Technical University Wien Austria, University of Basel Switzerland, University of Bologna Italy, University of California Santa Barbara USA, University of Kassel Germany, University of Linz Austria, University of Padova Italy, University of Pisa Italy, WIAS Germany, and the ETH Zurich laboratories IfE, IFH, IKT, IWR, MATH, and TIK for the fruitful cooperation in research projects as well as for their financial support.

Organization



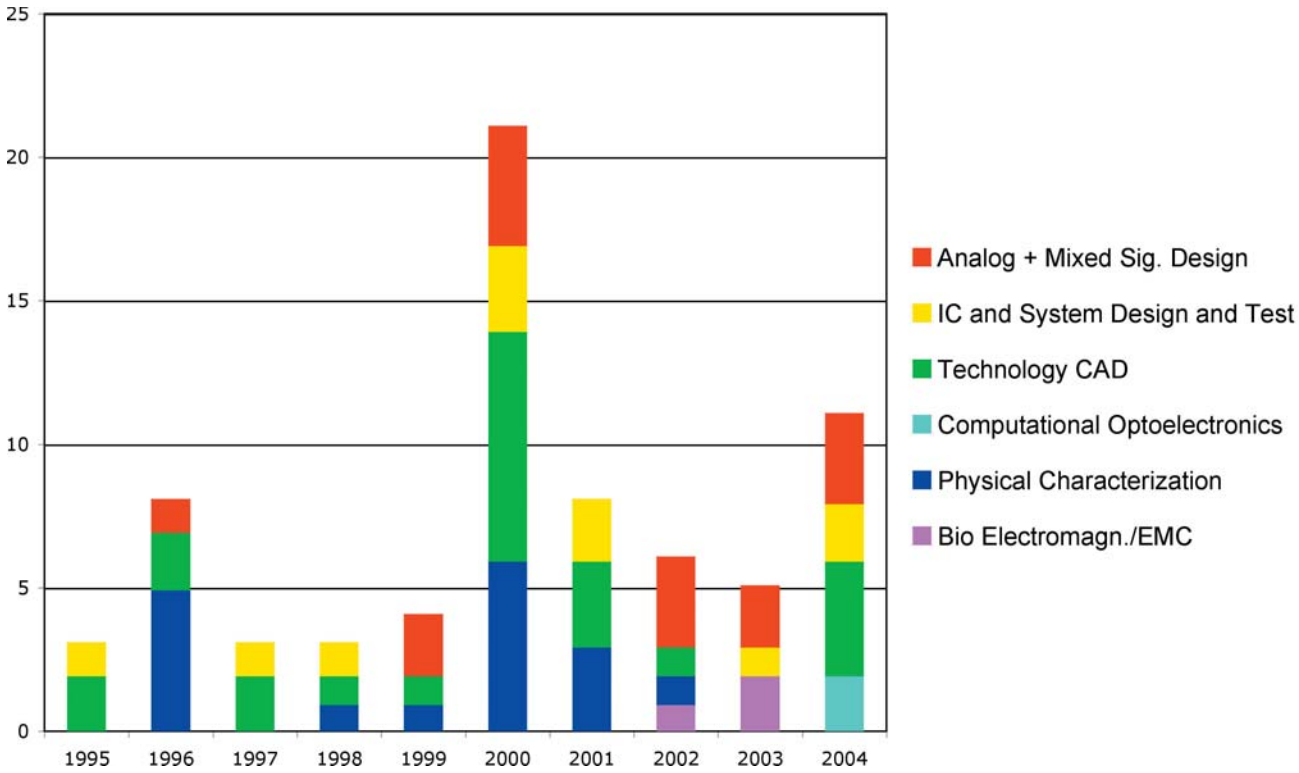
Representative Figures

Staff



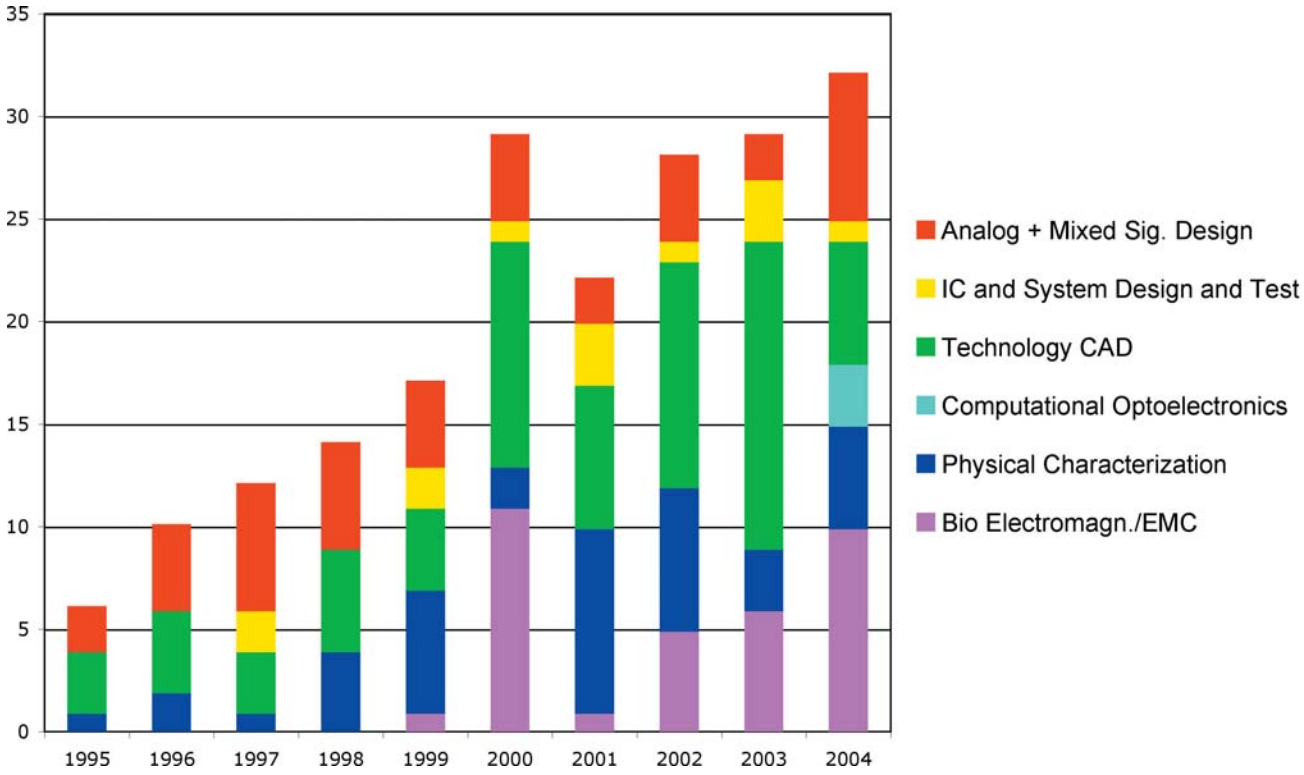
Number of full job positions at the Integrated Systems Laboratory from 1995 to 2004.

PhD Theses



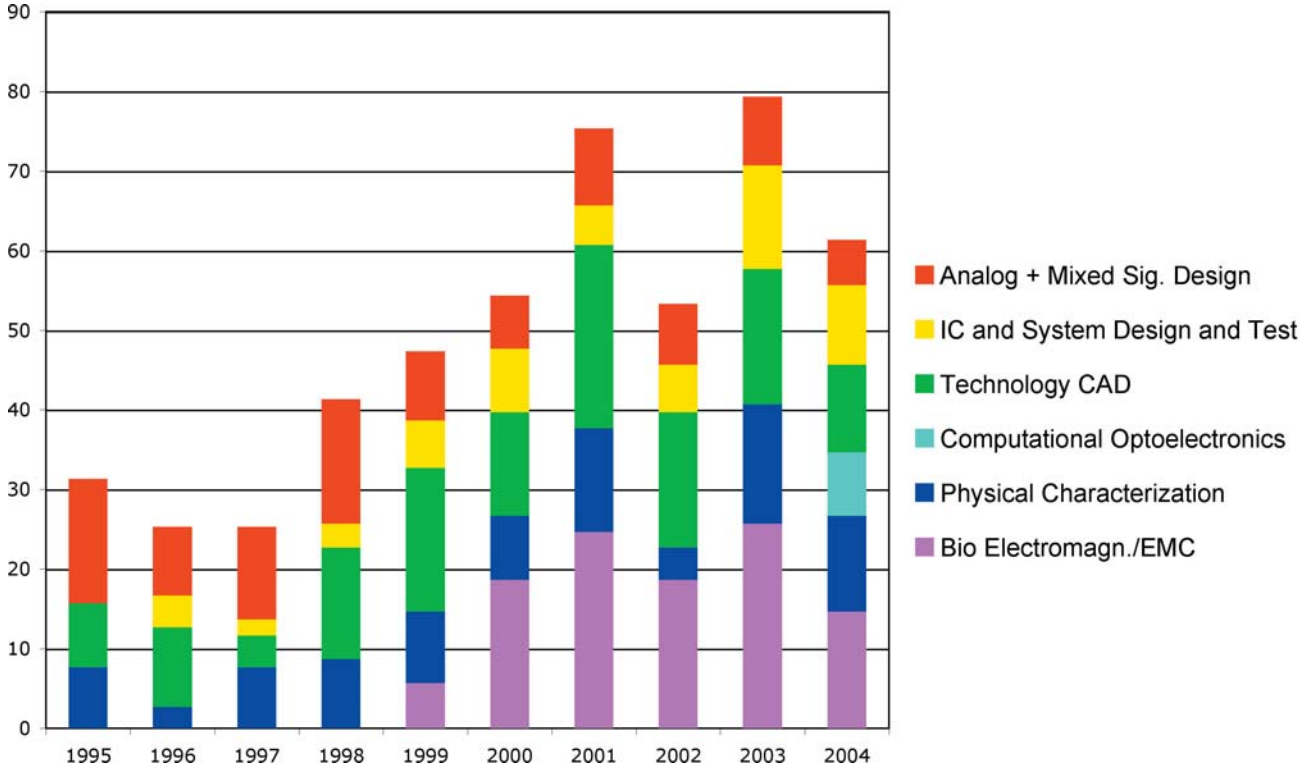
Number of completed PhD theses per year at the Integrated Systems Laboratory from 1995 to 2004. Abstracts of PhD theses: see page 108.

Journal and Book Publications



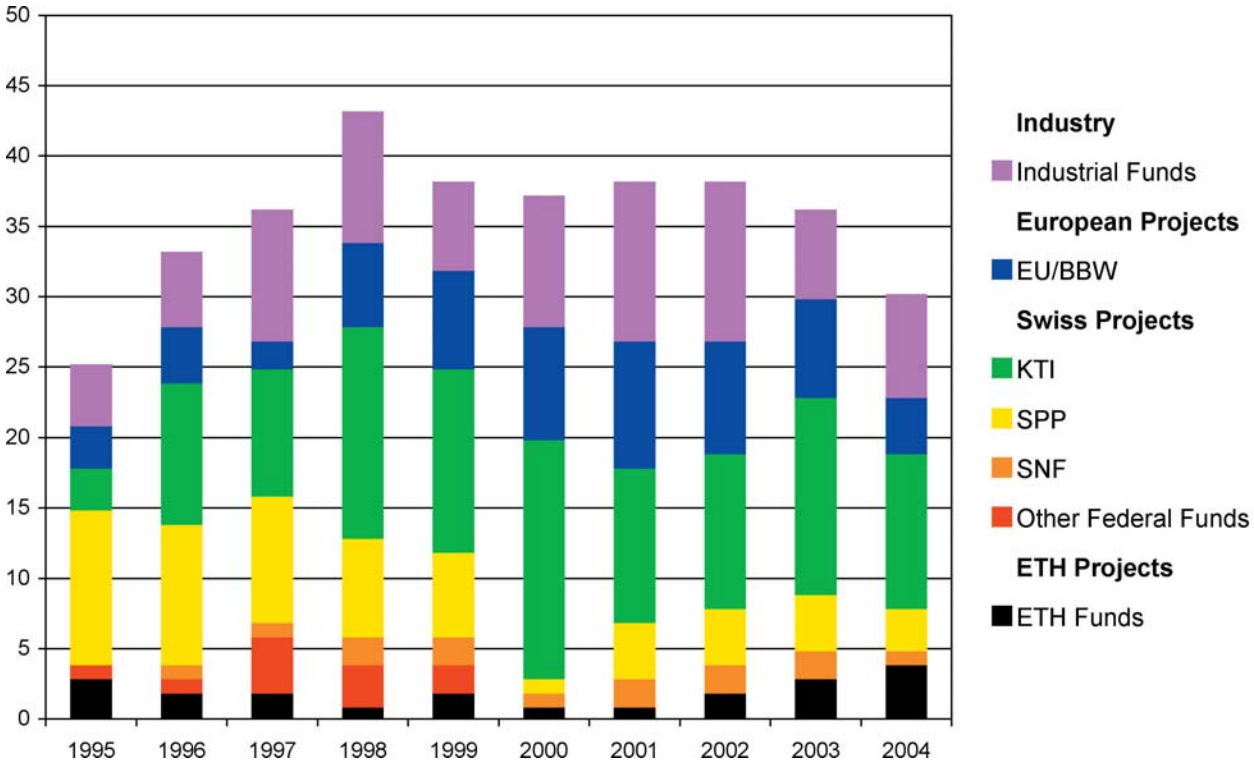
Number of journal and book publications by the Integrated Systems Laboratory from 1995 to 2004. References: see page 135.

Conference and Workshop Presentations



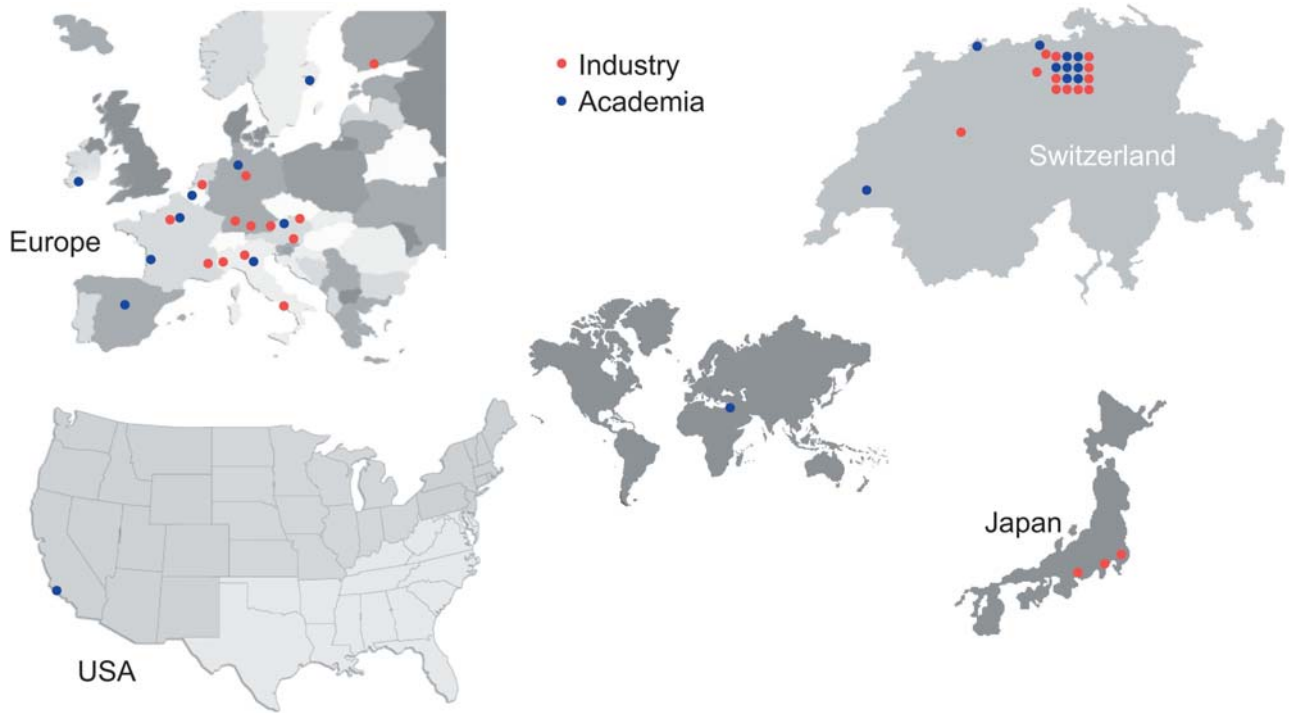
Number of conference and workshop presentations by the Integrated Systems Laboratory. References: see page 130.

IIS Research Projects



Number of research prijects with external funding at the Integrated Systems Laboratory from 1995 to 2004. Overview of research projects: see page 124. Partners and funding agencies: see page 20.

Research Partners of IIS



	CH	Europe	USA	Japan	Others	World
Industry	15	13	0	3	0	31
Academia	17	8	1	0	2	28

Research partners of the Integrated Systems Laboratory in Switzerland (CH), Europe, and worldwide. Addresses of partners: see page 20.

Staff

Professors

Fichtner Wolfgang, Dr., Professor for Electronics	since	1 Sept	1985			
Huang Qiuting, Dr., Professor for Electronics, Head	since	1 Jan	1993			
Schenk Andreas, Prof., Dr., Dipl.-Phys., Senior Scientist	since	1 Aug	1991			
Witzigmann Bernd, Dr., Professor for Optoelectronics	since	5 Feb	2004			

Microelectronics Design Center

Kaeslin Hubert, Dr., Dipl. El.-Ing. ETH, Head	since	1 Jan	1986			
Brändli Matthias, Dipl. El.-Ing. ETH	since	1 May	2001			
Camarero Francisco, Dipl. Ing.		1 Jun	2002	–	31 Dec	2004
Köppel Rudolf, FEAM	since	1 Apr	1995			

Scientific Staff

Aemmer Dölf, Dr., Dipl. Phys. ETH, Senior Scientist	since	1 Sept	1985			
Alonso Eduardo, Dr., Industrial Engineer	since	1 Oct	2004			
Bäcker Alexandra, Dipl.-Ing.	since	1 July	2000			
Balmelli Pio, Dr., Dipl. El.-Ing. ETH		1 Apr	1998	–	30 Jun	2004
Barlini Davide, Electronic Eng.	since	1 Oct	2002			
Benkeser Christian, Dipl. El.-Ing. ETH	since	14 Jun	2004			
Berdinas Veronica de Jesus, M. Sc. Physics-Electronic	since	15 Oct	2002			
Benkler Stefan, Dipl. Rech. Wiss. ETH	since	15 Oct	2002			
Bösch Thomas, Dr., Dipl. El.-Ing. ETH		1 Apr	2000	–	31 Mar	2004
Brenna Gabriel, Dr., Dipl. El.-Ing. ETH		1 Mar	2000	–	31 Mar	2004
Brugger Simon, Dipl. El.-Ing. ETH	since	17 Jan	2001			
Burg Andreas, Dipl. El.-Ing. ETH	since	6 Nov	2000			
Burger Thomas, Dr., Dipl. El.-Ing. ETH	since	1 Oct	1994			
Bürgin Felix, Dipl. El.-Ing. ETH	since	1 Jun	2003			
Carbognani Flavio, Telecommunications Eng.	since	1 Dec	2002			
Centoni Scott, Dr., Materials Science		1 May	2003	–	30 Apr	2004
Chen Xinhua, M. Sc. EE	since	1 Sep	2001			
Chen Yihui, M. Sc. EE	since	1 Aug	2003			
Chen Zhiheng, Dr., M. Sc. EE	since	1 Aug	2003			
Ciappa Mauro, Dr., Dipl.-Phys.	since	1 Jan	1998			
Corvasce Chiara, Dipl.-Phys.	since	8 Apr	2002			
Eberli Stefan, dipl. El.-Ing. ETH	since	1 Dec	2003			
Ebert Sven, Dipl.-Phys.	since	15 May	2000			
Eom Sang Jin, M. Sc. EE		3 Jul	2002	–	31 Oct	2004
Felber Norbert, Dr., Dipl. Phys. ETH, Senior Scientist	since	1 July	1987			
Francese Pier-Andrea, Dipl. El.-Ing.	since	1 Sep	2000			
Geelhaar Frank, Dr., Dipl.-Phys.		1 Oct	1998	–	31 Oct	2004
Glaser Ulrich, Dipl.-Phys.	since	1 Oct	2002			
Gürkaynak Frank, Dipl. El.-Ing.	since	15 Sept	2000			
Häne Simon, Dipl. El.-Ing. ETH	since	1 June	2002			
Heinz Frederik, Dr., Dipl. Phys. ETH		25 Apr	2000	–	30 Sep	2004
Hertle Jürgen, Dr., Dipl. Ing. Elektrotechnik		2 Mar	1998	–	29 Feb	2004
Höhr Tim, Dipl.-Phys.	since	15 Mar	2001			
Jacob Biju, Dr., MTech.		1 Sep	2002	–	31 Dez	2004
Kaplan Vassili, M. Sc. Mathematics		1 Dec	2003	–	30 Jun	2004
Köksoy Sinan, M. Sc. EE	since	12 Jul	2004			
Kouchev Ilian, M. of Science	since	1 Sep	2000			
Laino Valerio, Electrical Eng.	since	1 Oct	2002			

Loeser Martin, Dipl. Ing.	since	1	Sep	2003			
Luisier Mathieu, Dipl. El.-Ing. ETH	since	1	Apr	2003			
Lüthi Peter, Dipl. El.-Ing. ETH	since	1	Nov	2003			
Martelli Chiara, Dipl. El.-Ing.	since	17	Jan	2001			
Müller Christoph, Dr., Dipl. Phys. ETH	since	1	June	2000			
Müller Peter, M. Sc. E. E.	since	1	Jan	2004			
Neufeld Esra, Dipl. Natw. ETH	since	14	Jun	2004			
Nikoloski Neviana, M. Sc. Engineering Physics	since	15	Nov	2002			
Odermatt Stefan, Dipl. El.-Ing. ETH	since	15	Mar	2003			
Oesch Walter, Dipl. Natw. ETH	since	15	Aug	2000			
Oetiker Stephan, Dipl. Informatik-Ing. ETH	since	1	May	2001			
Olszewska Joanna, Dipl. El.-Ing. EPFL		1	Dec	2003	–	31 Oct	2004
Papadopulos Dimitris, M. Sc. EE	since	1	July	2003			
Perels, Dipl. El.-Ing. ETH	since	1	Feb	2001			
Pfeiffer Michael, Dr., Dipl.-Phys.		1	Oct	1999	–	31 Mar	2004
Rogin Jürgen, Dr., Dipl. El.-Ing. ETH		1	Apr	1999	–	31 Mar	2004
Röllin Stefan, Dr., Dipl. Math. ETH	since	1	Apr	2000			
Roth Eric, Dr., Dipl. El.-Ing. ETH		5	Apr	2000	–	31 Mar	2004
Ruiz Gallego Ivan, Dipl. El.-Ing. ETH	since	15	Nov	2003			
Sahli Beat, Dipl.-Phys.	since	1	June	2000			
Schaldach Markus, Dipl.-Ing.		1	Mar	2000	–	29 Feb	2004
Schmithüsen Bernhard, Dr., Dipl.-Mathematiker	since	27	May	1996			
Schneider Lutz, Dipl. Phys. ETH	since	7	May	2001			
Sponton Luca, M. Sc. Electronic Engineering	since	1	Mar	2004			
Stangoni Maria, Dipl. El.-Ing.	since	15	Feb	2001			
Streiff Matthias, Dr., Dipl. El.-Ing. ETH	since	7	Feb	2000			
Treichler Jürg, Dipl. El.-Ing. ETH	since	1	May	2003			
Tschopp David, Dipl. El.-Ing. ETH		1	Mar	2000	–	29 Feb	2004
Villiger Thomas, Dr., Dipl. El.-Ing. ETH		1	May	1999	–	30 Abr	2004
Wegmüller Marc, Dipl. El.-Ing. ETH	since	1	Oct	2003			
Witzig Andreas, Dr., Dipl. El.-Ing. ETH	since	1	Aug	1997			
Yuan Chenghao, Dr., M. Sc. EE		15	Nov	2003	–	15 Nov	2004
Computer Staff							
Böhm Anja, Dipl. Geologin (80%)	since	1	Apr	2001			
Richardet Christoph, Oberstufenlehrer	since	10	May	2000			
Wicki Christoph, Dipl. El.-Ing. ETH	since	1	Oct	1985			
Technical Staff							
Balmer Christoph, Dipl. El.-Ing. HTL	since	1	Aug	1989			
Gisler Hansjörg, Industriespengler (80%)	since	1	Sept	1989			
Illien Fritz, Dipl. El.-Ing. HTL		1	May	1998	–	31 Dec	2004
Mathys Hanspeter, Elektromonteur	since	15	Dec	1991			
Rheiner Rudi, Dipl. El.-Ing. HTL	since	15	Nov	1996			
Administrative Staff							
Boksberger Margit (50%)	since	1	Jan	2000			
Bucher Gina-Lisa (30%)		15	Nov	2003	–	31 Aug	2004
Fischer Bruno, Dipl. El.-Ing. HTL	since	14	Apr	1992			
Haller Christine, Betriebsökonomin HWV (95%)	since	8	Mar	1993			
Plank Eva (50%)	since	1	July	1998			
Roffler Verena (50%)	since	1	Sept	1999			

Former PhD Students

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Dr. H. Schlueter	TRUMPF Photonics Inc., Cranbury, NJ, USA	8 Jan 2004
M. H. Yabuhara	Toshiba Corp., Process Research Center Corporate Manufacturing Engineering Center Yokohama, Japan	9 Jan – 12 Jan 2004
Dr. N. Finger	ARC Seibersdorf research GmbH, Vienna, Austria	13 Jan 2004
Dr. M. Tuma	Academy of Sciences, Prague, Czech Republic	19 Jan – 21 Jan 2004
F. Becheiraz	Philips Semiconductors AG, Zurich, Switzerland	27 Jan 2004
Dr. St. Gappisch	Philips Semiconductors AG, Zurich, Switzerland	27 Jan 2004
K. Hasegawa	Matsuhita Electric Industrial Co., Ltd., Kyoto, Japan	29 Jan 2004
Dr. K. Shimizu	Matsuhita Electric Industrial Co., Ltd., Kyoto, Japan	29 Jan 2004
M. Shindo	Matsuhita Electric Industrial Co., Ltd., Kyoto, Japan	29 Jan 2004
Prof. A. Fiore	Institute de micro- et optoelectronic, EPFL, Lausanne, Switzerland	13 Feb 2004
Dr. K. Shimizu	Matsuhita Electric Industrial Co., Ltd., Kyoto, Japan	2 Mar 2004
Dr. T. Akiyama	Toshiba Corporation, Yokohma, Japan	15 Mar – 19 Mar 2004
U. Hofmann	Integrated Systems Engineering, Inc., San Jose, USA	16 Mar – 19 Mar 2004
T. Hori	ISE Integrated Systems Engineering Japan Ltd. Tokyo, Japan	15 Mar – 21 Mar 2004
H. Kakinuma	Toshiba Corporation, Kawasaki, Japan	18 Mar 2004
S. Komatsu	Toshiba Corporation, Kawasaki, Japan	16 Mar – 19 Mar 2004
Y. Nakajima	Toshiba Corporation, Kawasaki, Japan	15 Mar – 19 Mar 2004
K. Shimai	ISE Integrated Systems Engineering Japan Ltd. Tokyo, Japan	15 Mar – 21 Mar 2004
K. Shirai	Toshiba Corporation, Yokohma, Japan	16 Mar – 18 Mar 2004
T. Yoshida	ISE Integrated Systems Engineering Japan Ltd. Tokyo, Japan	15 Mar – 21 Mar 2004
A. Kumar	Dayanda Mahavidiyalya (D.A.V. Degree College) Varanasi,India	15 Mar – 15 Sep 2004
Prof. Dr. G. Baccarani	Universita degli Studi di Bologna, Bologna, Italy	2 Apr 2004
M. Denison	Infineon Technologies AG, Munich, Germany	2 Apr 2004
E. Gnani	Universita degli Studi di Bologna, Bologna, Italy	2 Apr 2004
G. Groos	Infineon Technologies AG, Munich, Germany	2 Apr 2004
N. Jensen	Infineon Technologies AG, Munich, Germany	2 Apr 2004
S. Reggiani	Universita degli Studi di Bologna, Bologna, Italy	2 Apr 2004
Prof. Dr. M. Rudan	Universita degli Studi di Bologna, Bologna, Italy	2 Apr 2004
Dr. M. Stecher	Infineon Technologies AG, Munich, Germany	2 Apr 2004
Dr. A. Benvenuti	ST Microelectronics Srl, Agrate Brianza, Italy	7 Apr 2004
Dr. C. Lombardi	ST Microelectronics Srl, Agrate Brianza, Italy	7 Apr 2004
Dr. A. Marmiroli	ST Microelectronics Srl, Agrate Brianza, Italy	7 Apr 2004
Dr. L. Zullino	ST Microelectronics Srl, Cornaredo, MI, Italy	7 Apr 2004
Dr. Ch. Vélez	Exalos AG, Zurich, Switzerland	5 May 2004
Prof. Y. Danto	University of Bordeaux, Bordeaux, France	13 May 2004
Dr. G. Groesenecken	IMEC, Leuven, Belgium	13 May 2004
Prof. N. Labat	University of Bordeaux, Bordeaux, France	13 May 2004
Prof. J. Møltoft	Technical University of Denmark, Lyngby, Denmark	13 May 2004
Prof. T. Mouthan	University of Twente Twente, The Netherlands	13 May 2004
Dr. J. Höck	TOP NANO 21, Managment	1 Jun 2004
Dr. H.-J. Muhr	TOP NANO 21, Managment	1 Jun 2004
Dr. C.-A. Berseth	Beam Express SA, Lausanne, Switzerland	9 Jun 2004
Dr. M. Moser	Avalon Photonics, Zurich, Switzerland	9 Jun 2004
Prof. E. Kapon	Institute de micro- et optoelectronic, EPFL, Lausanne, Switzerland	9 Jun 2004
Dr. A. Gehring	TU Wien, Vienna, Austria	19 Jun – 30 Jul 2004

Prof. J. Katzenelson	Technion, Israel Institute of Technology, Haifa, Israel	1 Jul – 31 Dec 2004
T. Eberle	Avalon Photonics Ltd., Zurich, Switzerland	28 Jul – 29 Jul 2004
Dr. S. Eitel	Avalon Photonics Ltd., Zurich, Switzerland	28 Jul – 29 Jul 2004
R. Hoevel	Avalon Photonics Ltd., Zurich, Switzerland	28 Jul – 29 Jul 2004
Dr. P. Royo	Avalon Photonics Ltd., Zurich, Switzerland	28 Jul – 29 Jul 2004
Dr. M. Achtenhagen	Institute de micro- et optoelectronique, Département de Physique, Lausanne, Switzerland	28 Jul – 29 Jul 2004
J. Boucart	Institute de micro- et optoelectronique, Département de Physique, Lausanne, Switzerland	28 Jul – 29 Jul 2004
Dr. Y. Hattori	Toyota Central R&D Labs., Inc., Yokomichi, Japan	29 Jul 2004
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M. Matsumara	Sony Corporation, Kanagawa, Japan	29 Jul 2004
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Dr. R. Kaufmann	CSEM, Zurich, Switzerland	17 Aug 2004
Dr. B. Schmidt	Bookham (Switzerland) AG, Zurich, Switzerland	27 Aug 2004
Dr. M. Blaser	Albis Optoelectronics AG, Rüschlikon, Switzerland	31 Aug 2004
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Dr. T. Hatakeyma	Toshiba Corporation, Kawasaki, Japan	6 Sep 2004
T. Hori	ISE Integrated Systems Engineering Japan Ltd., Tokyo, Japan	6 Sep 2004
Dr. H. Yoshimura	Toshiba Corporation, Yokohama, Japan	6 Sep 2004
Dr. V. Jungnickel	Fraunhofer Institut Nachrichtentechnik, Heinrich-Hertz-Institut, Berlin, Germany	7 Sep 2004
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BBW	Bundesamt für Bildung und Wissenschaft (Federal Office for Education and Science, a Swiss Government Agency) Wildhainweg 9, CH-3001 Bern, Switzerland
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EU-RTN	Community Research in the Fifth Framework Programme “Improving human research potential and the socio-economic knowledge base: Research Training Networks (RTN)” of the European Union
Exalos	Exalos AG Technoparkstrasse 1, CH-8005 Zürich, Switzerland
FhG-IIS-B	Fraunhofer-Institut für Integrierte Schaltungen Bauelementetechnologie Schottkystrasse 10, D-91058 Erlangen, Germany
FNM	Forschungskoperation Mobilkommunikation c/o Institut für Feldtheorie und Höchstfrequenztechnik (Laboratory for Electromagnetic Fields and Waves) ETH Zürich, Gloriastrasse 35, CH-8092 Zürich, Switzerland
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Infineon	Infineon Technologies AG Otto-Hahn-Ring 6, D-81730 München, Germany and Infineon Technologies AG Balanstrasse 73, D-81609 München, Germany
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KTI	Kommission für Technologie und Innovation (Commission for Technology and Innovation, a Swiss Government Agency) Effingerstrasse 27, CH-3003 Bern, Switzerland
MATH-ETHZ	Forschungsinstitut für Mathematik (Research Institute for Mathematics) ETH Zürich, Rämistrasse 101, CH-8092 Zürich, Switzerland
Miromico	Miromico AG Technoparkstrasse 1, CH-8005 Zürich, Switzerland
Philips Belgium	Philips Research Leuven B-3001 Leuven, Belgium
Philips NATLAB	Philips Research Laboratories Professor Holstlaan 4, NL-5656 AA Eindhoven, The Netherlands
Philips Nederland	Philips Electronics Nederland B.V. Professor Holstlaan 4, NL-5656 AA Eindhoven, The Netherlands

Philips Zurich	Philips Zürich AG, Semiconductors Binzstrasse 44, CH-8045 Zürich, Switzerland
PSI	PSI Paul Scherrer Institut CH-5332 Villingen, Switzerland
Siemens Bocholt	Siemens AG Information and Communication Mobile Frankenstrasse 2, D-46393 Bocholt, Germany
Siemens München	Siemens AG Hoffmannstrasse 51, D-81359 München, Germany
SIGMA C	SIGMA C GmbH Software Thomas-Dehler-Strasse 9, D-81737 München, Germany
SINANO Consortium	France Innovation Scientifique et Transfert S.A., FIST, Paris, France Centre National de la Recherche Scientifique, CNRS, Paris, France Technische Universität Wien - Institut für Festkörperelektronik, TUW FKE, Wien, Austria Technische Universität Wien - Institut für Mikroelektronik, TUW IME, Wien, Austria The University of Warwick, WARWICK, Coventry, United Kingdom Universite Catholique de Louvain, UCL, Louvain la Neuve, Belgium Rheinisch-Westfälische Technische Hochschule Aachen, RWTH, Aachen, Germany Alma Mater Studiorum - Universita di Bologna, ARCES, Bologna, Italy AMO GmbH, AMO, Aachen, Germany The University of Birmingham, BU, Birmingham, United Kingdom Commissariat a l'Energie Atomique, CEA, Paris, France Chalmers University of Technology AB, CHALMERS, Göteborg, Sweden Technische Universiteit Delft, DELFT, Delft, the Netherlands Ecole Polytechnique Federal de Lausanne, EPFL, Lausanne, Switzerland Eidgenössische Technische Hochschule Zürich, ETH, Zürich, Switzerland Forschungszentrum Juelich GmbH, FZJ JUELICH, Jülich, Germany The University of Glasgow, GLASGOW, Glasgow, United Kingdom Göteborgs Universitet, GOETEBORG, Göteborg, Sweden Universidad de Granada, GRANADA, Granada, Spain Fraunhofer-Gesellschaft E.V., IISB, München, Germany Interuniversitair Micro-Electronica Centrum VZW, IMEC, Leuven, Belgium National Center for Scientific Research "Demokritos", IMEL, Aghia, Greece Infineon Technologies AG, INFINEON, München, Germany Kungliga Tekniska Högskolan, KTH, Stockholm, Sweden The University of Liverpool, LIVUNI, Liverpool, United Kingdom NMRC - University College of Cork, NMRC, Cork, Ireland University of Newscastle upon Tyne, NU, Newcastle upon Tyne, United Kingdom Universita degli Studi di Pisa - Dpt Ingegneeeria Dell Informazione, PISA, Pisa, Italy The University of Southampton, SOTTON, Southhampton, United Kingdom ST Microelectronics SA, ST, Montrouge, France Technische Universität München, TUM, München, Germany Linköpings Universitet - Institute of Technology, LINKOPING, Linköping, Sweden The University of Cambridge, UCAM, Cambridge, United Kingdom Universita degli Studi di Udine, UDINE, Udine, Italy Universitetsstudiene Pa Kjeller, UNIK, Kjeller, Norway Universitat Rovira i Virgili, URV, Tarragona, Spain Universität Stuttgart, USTUTT, Stuttgart, Germany Eberhard Karls Universität Tübingen, UTU, Tübingen, Germany Uppsala Universitet, UU, Uppsala, Sweden Politechnika Warszawska, WUT, Warszawa, Poland Institute of Semiconductor Physics - National Academy of Science, ISP, Kyiv, Ukraine Puslaidininkiu Fizikos Institutas, SPI, Vilnius, Lithuania
SNF	Swiss National Science Foundation Wildhainweg 20, CH-3012 Bern, Switzerland
SPEAG	Schmid & Partner Engineering AG Zeughausstrasse 43, CH-8004 Zürich, Switzerland
ST Microelectronics	ST Microelectronics Via Carlo Olivetti 2, I-20041 Agrate Brianza (MI), Italy and ST Microelectronics Via Tolomeo 1, I-20010 Cornaredo (MI), Italy and

	ST Microelectronics 850 rue Jean Monnet, F-38921 Crolles, France
Synopsys	Synopsys Switzerland LLC (Former ISE Integrated Systems Engineering AG) Affolternstrasse 52, CH-8050 Zürich, Switzerland and Synopsys Inc. 700 East Middlefield Road, Mountain View, CA 94043, USA
TAU	Tel-Aviv University (TAU) Department of Physical Electronics Tel-Aviv University, Ramat Aviv, IL-69978, Israel
TDC	TDC Switzerland AG Thurgauerstrasse 60, CH-8050 Zürich, Switzerland
TIK-ETHZ	Institut für Technische Informatik (Computer Engineering and Network Laboratory) ETH Zürich, Gloriastrasse 35, CH-8092 Zürich, Switzerland
TOP NANO 21	Swiss Technology Oriented Program NANO 21 Universität Basel Institut für Physik Klingelbergstrasse 82, CH-4056 Basel, Switzerland and Themas AG Egnacherstrasse 69, CH-9320 Arbon, Switzerland
Toshiba	Toshiba Corporation 1-1. Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan and Toshiba Corporation 2-5-1, Kasama, Sakae-ku, Yokohama 247-8585, Japan and Toshiba Corporation 1, Komukai, Toshibacho, Saiwai-ku, Kawasaki 210, Japan
Toyota	Toyota Central R&D Labs. Inc. Nagakute-cho, Aichi-gun, Aichi 480-1192, Japan
TU Graz	Graz University of Technology Institute for Applied Information Processing and Communications (IAIK) Inffeldgasse 16a, A-8010 Graz, Austria
TU Wien	Technical University Vienna Institute for Microelectronics Gusshausstrasse 27–29, A-1040 Wien, Austria
UCSB	University of California ECE Department Santa Barbara, CA 93106-9560, USA
Uni Basel	Universität Basel Departement für Computer Wissenschaften CH-4000 Basel, Switzerland
Uni Bern	Universität Bern Universitätsklinik Inselspital CH-3010 Bern, Switzerland
Uni Bologna	Universita degli Studi di Bologna Dipartimento di Elettronica Informatica e Sistemistica Via Zamboni 33, I-40126 Bologna, Italy
Uni Cagliari	Universita degli Studi di´Cagliari Dipartimento di Ingegneria Elletricae et Elettronica Piazza D‘ armi, I-09123 Cagliari, Italy
Uni Canberra	Australien National University Engineering Canberra 0200 ACT, Australia
Uni Hamburg	Universität Hamburg Institut für Angewandte Physik Jungius-Strasse 11, D-20335 Hamburg, Germany
WIAS	Weierstrass-Institut für Angewandte Analysis und Stochastik Mohrenstrasse 39, D-10117 Berlin, Germany

Awards

Andreas Schenk

received the

Titularprofessor (Honorary Professor)

of the Swiss Federal Institute of Technology (ETH) Zürich.

Prof. Wolfgang Fichtner

received the

ISPSD Conbributory Award

for outstanding contributions to the growth of ISPSD into a world-leading international symposium, May 25, 2004.

Silvio Dragone

received the

First Plateau
Invention Achievement Award

in appreciation and recognition of creative contributions to IBM progress, April 2004.

Gabriel Brenna

received the

“ETH Medal” of the Swiss Federal Institute of Technology

for his excellent Ph.D. thesis
“The Design of Direct-Conversion CMOS Radio Transmitters”.

Matthias Streiff

received the

“ETH Medal” of the Swiss Federal Institute of Technology

for his excellent Ph.D. thesis
“Opto-Electro-Thermal VCSEL Device Simulation”.

Andreas Witzig

received the

“ETH Medal” of the Swiss Federal Institute of Technology

for his excellent Ph.D. thesis
“Modeling the Optical Processes in Semiconductor Lasers”.

Mathieu Luisier

received the

“ETH Medal” of the Swiss Federal Institute of Technology

for his excellent diploma thesis
“Simulation of Semiconductor Lasers”.

Markus Wenk and Martin Zellweger

received the

“Prix du Jeune Entrepreneur 2004”

of the Section Suisse des Conseillers du Commerce Extérieur de la France
for their excellent semester thesis “SphereDEC”.

Patents

Title:	**Method for Detection of a Timeout of Elements in an Element Processing System**
Owner:	IBM Corporation
Inventors:	Silvio Dragone, Andreas Döring
Patent No.:	CH920030081EP1

Title:	**Method and Apparatus for Using FPGA Technology with a Microprocessor for Reconfigurable, Instruction Level Hardware Acceleration**
Owner:	IBM Corporation
Inventors:	Andreas Döring, Silvio Dragone, Andreas Herkersdorf, Charles E. Kuhlmann, Richard G. Hofmann
Patent No.:	RPS920030110US1, RPS920030110JP1

Title:	**Coupling a General Purpose Processor to an Application Specific Instruction Set Processor and Processor Configuration Therefore**
Owner:	IBM Corporation
Inventors:	Silvio Dragone, Andreas Döring
Patent No.:	CH920030050EP1

Title:	**Method and Device for Synchronizing a Processor and a Coprocessor**
Owner:	IBM Corporation
Inventors:	Andreas Döring, Silvio Dragone
Patent No.:	CH920030033US1, CH920030033EP1

Title:	**ESD-Schutzvorrichtung für eine Halbleiterschaltung mit einer mit einem Substrat- oder Guard-Ring-Kontakt kontaktierten ESD-Schutzschaltung**
Owner:	Infineon Technologies AG
Inventors:	Ulrich Glaser, Harald Goßner, Jens Schneider, Martin Streibl, Silke Bargstätt-Franke
Patent No.:	DE 102004007655

History of the Integrated Systems Laboratory (IIS)

1985 Appointment of Wolfgang Fichtner, Professor for Electronics, Department of Electrical Engineering, ETH Zurich.
Formation of the research group “VLSI” in the Electronics Laboratory.
First research project (2D device simulation, funded by KTI).
Installation of 3 minicomputer DEC VAX-11/785 (1 CPU, 16 MBytes memory).

1986 Foundation of the “Integrated Systems Laboratory” by merging of the research groups of Prof. Wolfgang Fichtner (Department of Electrical Engineering) and Prof. Martin Morf (Department of Computer Science).
Start of the lecture “Electronics Systems” (undergraduate EE students).
Start of the lecture series “Design of Integrated Circuits I, II, III” (graduate EE, CS, and physics students).
Summer school “VLSI Design” in Beatenberg/Switzerland (2 weeks, 85 participants from Europe and Switzerland), organization as well as scientific and technical responsibility by IIS. 15 invited talks by well known experts from USA, Europe, and Switzerland, presentations and hands-on experience on workstations.

1987 Leaving of Prof. Martin Morf.
Appointment of Marco Annaratone, assistant professor for Parallel Computing, Department of Computer Science, ETH Zurich.
Start of the lecture “Digital Design and Processor Structures” (undergraduate CS students).
Design and integration of the first student ICs (20 MHz, 7 000 transistors).
Installation of the HILEVEL TOPAZ 50 ASIC test system (50 MHz, 96 I/O channels).
Installation of a mini-supercomputer Alliant FX/80 (6 CPUs, 112 MBytes shared memory).
Introduction of the first professional CAD tool for IC design in teaching and research (VLSI Technology Inc., later Compass Design Automation Inc.).
Installation of the parallel computer Sequent Symmetry (26 CPUs, 160 MBytes shared memory).

1988 Foundation of the Microelectronics Design Center (Department of Electrical Engineering, associated to the Integrated Systems Laboratory).
First PhD thesis of a computer science student at IIS.
Design and integration of the first VLSI chip (Viterbi decoder, 35 000 transistors).

1989 First European research project (parallel computer architecture).
First PhD thesis of a physics student at IIS.
2nd prize “Seymour Cray Competition” Switzerland for “Multi-Dimensional Semiconductor Device Simulation” to members of scientific staff of IIS.
First “Intensive Course on ASIC Design and Test” with ETH-internal and -external participants.
First functional 2D simulation program for semiconductor devices developed by IIS scientific staff.

1990 First PhD thesis of an electrical engineering student at IIS.
Start of the lecture “Semiconductor Devices: Technology and Modeling”.
CEI-Europe Elsevier course “VLSI Process and Device Simulation” in Davos/Switzerland. Organization as well as scientific and technical responsibility by IIS (1 week, 35 participants).
Start of the project “Education and Research in Microelectronics”, generous funding by the board of ETH Zurich for IC integration and measurement equipment.
Evaluation of the Department of Electrical Engineering of ETH Zurich and the laboratories of the department by a group of international experts. Qualification of the research at the Integrated Systems Laboratory compared at the international level:
• process and device simulation: outstanding.
• VLSI design: very efficient.
• parallel computer architectures: very good ideas, realization has to be proven.
Prof. Wolfgang Fichtner elected IEEE Fellow for the “application of numerical modeling to device scaling and submicron transistor optimization”.

1991 Leaving of Prof. Marco Annaratone.
4th International Conference on “Simulation of Semiconductor Devices and Processes – SISDEP’91”, ETH Zurich/Switzerland (3 days, 200 participants), organization by IIS, Conference Co-Chairman Prof. Wolfgang Fichtner, 3 invited papers, 44 regular papers, 18 poster presentations.
Start of the national program “Microswiss” to support microelectronics in Swiss SMEs and education. Microelectronics Design Center acts as a support center.
Presentation of the IIS activities in “Modeling of Microelectronic Devices” at CEBIT’91 exhibition Hannover/Germany, as a winner of the competition “Technology Location Switzerland 1991”.
Installation of the IMS XL60 Mixed Signal ASIC Verification System (60 MHz, 96 I/O channels).

1992 Start of the Swiss priority program “LESIT – Power Electronics, Systems, Information Technology”, 11 research projects in the module “Silicon Power Device Technology” (module coordinated by Prof. Wolfgang Fichtner).
Start of the first European ESPRIT project (“DESSIS – Device Simulation for Smart Integrated Systems”).
Start of a European JESSI project (Circuits for Communication Technology).
Design and integration of a high-speed data encryption IC (177 Mbit/s, 250 000 transistors).
First functional 3D grid generation program developed by IIS scientific staff.

1993 Appointment of Qiuting Huang, assistant professor for Analog Integrated Circuits, Department of Electrical Engineering, ETH Zurich.
Foundation of the IIS spin-off “ISE Integrated Systems Engineering AG” Zurich by IIS members (scope of business: software and application support in Technology CAD). Location for the first one and a half years at IIS with support of ETH Zurich.
Start of the lecture “Analog Integrated Circuits” (graduate EE students).
First functional 3D simulation program for semiconductor devices developed by IIS scientific staff.

1994 “6th International Symposium of Power Semiconductor Devices & ICs – ISPSD’94”,
Davos/Switzerland (3 days, 195 participants), organization by IIS, symposium chairman Prof. Wolfgang Fichtner, 3 invited presentations, 29 regular papers, 41 poster presentations.
Planning phase of the Swiss priority program MINAST, designated program director Prof. Wolfgang Fichtner (1994/95), provisional program direction established at IIS.
Installation of the HP83000 ASIC Verification System (660 MHz, 128 I/O channels).
Microelectronics Design Center also assumes responsibility for PCB support.

1995 Completion of the Swiss priority program LESIT with outstanding scientific results and efficient transfer of research to industry.
First functional simulation program for semiconductor processes developed by IIS scientific staff.
Move of spin-off ISE AG from ETH Zurich location to Technopark Zurich.
First course “Getting started with VHDL Synthesis” with ETH-internal and -external participants.
Installation of the parallel computer IBM SP2 (6 CPUs, 4.5 GBytes distributed memory).

1996 Start of the Swiss priority program “MINAST – Micro and Nano System Technology”, program director Prof. Wolfgang Fichtner (1996–1997), program direction established at IIS, total 56 Mio CHF granted by Swiss authorities and more than 60 Mio CHF contributions from Swiss industrial enterprises; IIS research projects: two in the module “Integrated Microsystems Technology”, four in the module “Design, Simulation and Engineering of Microsystems”, and one in the module “Microsystems Applications”.

1997 Postdoctoral thesis (habilitation) of PD Dr. Andreas Schenk for the subject “Advanced Physical Models for Silicon Device Simulation”.
Public workshop “3D Semiconductor Simulation” of the European ESPRIT Project “PROMPT II – Process Optimization in Multiple Simulations for Semiconductor Technology II” (3 days, 56 participants), Monte Verità Ascona/Switzerland, 8 presentations as well as demonstrations and hands-on experience, organization by IIS and spin-off ISE AG.
Installation of the first parallel computer DEC Alphaserver (4 CPUs, 2 GBytes shared memory).

1998 Promotion of Qiuting Huang to Professor for Electronics, Department of Electrical Engineering, ETH Zurich.
Accommodation of the research group “Physical Characterization”, including well known experts and advanced equipment from the former Reliability Laboratory at the Department of Electrical Engineering, ETH Zurich.
Start of three new European research projects.
Two patents on telecommunication ICs, inventors: IIS scientific staff, owner: Siemens Schweiz AG.
Migration to Synopsys and Cadence EDA systems for IC design in teaching and research.
First functional simulation program for electromagnetic fields developed by IIS scientific staff.

1999 Accommodation of the research group “Bioelectromagnetics/EMC” from the Electromagnetic Fields and Microwave Electronics Laboratory at the Department of Electrical Engineering, ETH Zurich.
Election of Prof. Wolfgang Fichtner as head of the Department of Electrical Engineering Oct 1999 – Sept 2001.
Start of the lecture “Electrical Engineering I” (undergraduate mechanical and process engineering students).
Completion of the Swiss priority program MINAST with outstanding scientific results and efficient transfer of research to industry.
Public workshop “ESD Protection Design Methodology” of the ESPRIT Project ESDEM as an open meeting of the “EMC ’99 Zurich Symposium”, (1 day, 86 participants), ETH Zurich/Switzerland, 5 invited talks by well known experts from USA and Europe, demonstrations of the methodology, organization by IIS and spin-off ISE AG.
Design and integration of a high-quality video image processor (100 MHz, 1.8 Giga Ops/s, 2.7 Mio transistors).
Establishment of the “Foundation for Research on Information Technologies in Society IT’IS” (Zurich, director Dr. Niels Kuster). Associated to ETH Zurich and a close research partner of the IIS research group Bio Electromagnetics/EMC.

2000 Graduation of no less than 21 PhD students at IIS due the conclusion of the 4th framework program of the European Union as well as the Swiss priority program MINAST.

IEEE Andrew S. Grove Award of the Year 2000 to Prof. Wolfgang Fichtner “for outstanding contributions to semiconductor device simulations”.

World’s first chip of relevant complexity in GALS (Globally Asynchronous Locally Synchronous) technique, a SAFER SK-128 cipher implementation.

Ultra low offset (200 nV) chopper amplifier.

First functional simulation program for semiconductor lasers by IIS scientific staff.

Simulation platform SEMCAD for design and optimization of antennas in complex environments by IIS and IT’IS scientific staff.

Evaluation of the Department of Electrical Engineering ETH Zurich by a group of international experts with high scientific reputation. Overall qualification: “The international standing of Integrated Systems Laboratory regarding its core activities is definitely among the best of the world.”

Introduction of a new organization structure of ETH Zurich with autonomous departments and global budget.

2001 Prof. Qiuting Huang elected IEEE Fellow for outstanding contributions to integrated circuits for wireless communications.

Re-election of Prof. Wolfgang Fichtner as head of the Department of Information Technology and Electrical Engineering Oct 2001 – Sept 2003.

Start of the lecture “Semiconductor Devices” (undergraduate EE students).

Start of the lecture “Communications Electronics” (undergraduate EE students).

Start of the lecture series “Optoelectronic Devices” (graduate EE students).

Three contributions from IIS to the new Project Oriented Work program (undergraduate EE students).

Configurable hardware optimization and timing recovery for the first multimedia chip of the research partner company BridgeCo AG.

13.5 mW 185 MSample/s Delta-Sigma Modulator for UMTS/GSM Dual-Standard IF Reception.

Completion of the European research project SUBSAFE with excellent review results.

First functional optical eigenmodes solver for Vertical-Cavity Surface-Emitting Lasers (VCSELs).

ESPRIT-Project MADBRIC One-Day “Workshop on A/D Converters for Telecommunication” in Pfäffikon, Switzerland with 42 participants from 12 different countries.

Pilot User Workshop “Simulation of Semiconductor Laser Devices” at ETH Zurich/Switzerland (2 days, 29 participants from Europe, USA, and Japan), 3 invited talks by well known experts from USA and Europe, 5 talks, 1 tutorial, computer lab, organization by IIS.

2002 Start of a close collaboration with the new Communication Theory Group of Prof. Helmut Bölcskei (Communication Technology Laboratory, IKT) in the field of multiple-antenna (MIMO) research. A large, ETH-funded project on MIMO research has been approved by the board of ETH.

Successful completion of the European project LEMON on the design and implementation of a UMTS transceiver in deep sub-micron CMOS technology.

14 bit, 1 MHz Bandwidth Delta-Sigma A/D converter with lowest power consumption published so far.

The new Monte Carlo simulator SPARTA for stable and efficient self-consistent simulations of contemporary MOSFETs was included in the release 8.0 of ISE Integrated Systems Engineering AG.

Self-consistent coupling of opto-electro-thermal equations in device simulation of Vertical-Cavity Surface-Emitting Lasers (VCSEL).

Three accepted papers resulting from Master student theses to international conferences were presented by the students.

First Linux-cluster for physical simulations in Technology CAD (22 PCs with 2.2 GHz CPUs).

“International Conference on Numerical Simulation of Semiconductor Optoelectronic Devices NUSOD-02”, 25–27 September 2002, organized by IIS at ETH Zurich, 111 participants from Europe, USA, and Japan, 13 invited talks by well known experts from USA and Europe, 19 talks, 10 posters, and 5 company presentations.

2003 ETH Zurich established the assistant professorship Computational Optoelectronics. Dr. Bernd Witzigmann was elected and has taken up this position at the Integrated Systems Laboratory on 1 March 2004.

Re-election of Prof. Wolfgang Fichtner as head of the Department of Information Technology and Electrical Engineering Oct 2003 – Sept 2005.

Audio clock recovery circuit and reconfigurable processor resulting from PhD theses are integrated into an industrial Multimedia chip.

First 10 MHz bandwidth delta-sigma modulator with more than 80 dB signal to noise ratio, published at ISSCC‘04.

The new Monte Carlo simulator NOISE has been developed to enable the computation of noise phenomena in microelectronic device simulation.

2004 The research group Computational Optoelectronics was founded under the direction of Assistant Professor Bernd Witzigmann. The research group consists of 2 Postdocs and 5 PhD students, it is engaged in 3 research projects with public funding.

The Optoelectronics Laboratory (OptoLab) was founded as a common research instrument between IIS-ETHZ, IfE-ETHZ and IFH-ETHZ to support scientific work in fundamental and applied research projects with industrial partners.

Spin-off ISE AG was acquired by Synopsys, Inc. and became Synopsys Switzerland LLC. It is a Swiss based subsidiary and the headquarter of Synopsys TCAD activities. It is partner in ISE's and in future European and national research projects.

Start of the lecture series "Advanced Optoelectronics" (graduate EE students).

The world's first and fastest Sphere Decoder VLSI implementations for 4th generation mobile phones.

First coupling of Many-Body Gain Model to full Electro-Opto-Thermal VCSEL simulation.

Acquisition of a lightwave component analyzer (Agilent 86030A, equipment installed in the OptoLab).

Installation of an AMD-64Bit compute-cluster (40 AMD Opteron CPUs, 2.4 GHz, 200 GB memory).

"15th European Symposium Reliability of Electron Devices, Failure Physics and Analysis (ESREF) 2004", 4-8 October 2004, organized by IIS at ETH Zurich, 234 participants from Europe, USA, and Far East, 7 invited talks by well known experts from Europe, Far East, and USA, 52 talks, 40 posters, and an exhibition with 16 companies.

IC and System Design and Test

Coordinator:

Norbert Felber

VLSI Implementation for MIMO Communications

Personnel: Andreas Burg, David Perels, Simon Häne, Peter Lüthi

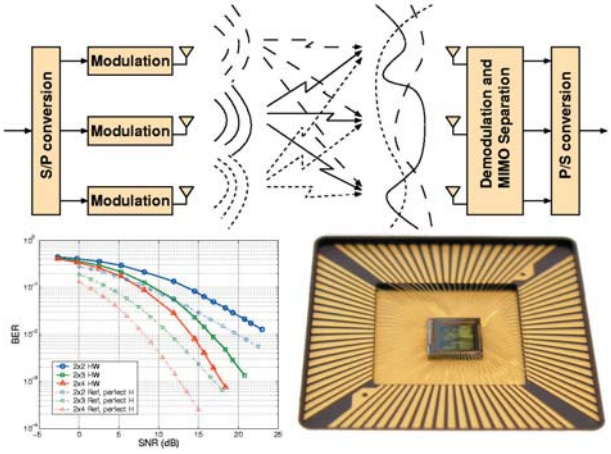
Funding: ETHZ TH-602-2 MIMO OFDM, Siemens Bocholt

Partners: IKT-ETHZ, Siemens Bocholt

The fast growth of mobile communications and wireless computer networks (WLAN) increases the demand for bandwidth-efficient wireless access solutions providing high-speed and high-quality data transmission. The idea of communication systems with multiple antennas at both transmitter and receiver (MIMO) has attracted considerable attention in the past 10 years. From an information-theoretical point of view the application of multiple antennas allows to drastically improve the channel capacity compared to single antenna systems. This implies that higher data rates and improved link reliability can be achieved without increasing neither the transmit power nor the occupied bandwidth. Unfortunately, the MIMO gains are achieved at the expense of increased receiver algorithm complexity which might become prohibitively large for practical VLSI implementation.

The research activity at the IIS in the field of MIMO communications aims towards the development of hardware-efficient receiver algorithms. Feedback is provided to algorithm designers by analyzing and modifying the suggested algorithms (that are optimal from a theoretical perspective) with respect to their suitability for hardware implementation. Aspects such as the effect of finite-word-length arithmetic, potential for hardware reuse, regularity of dataflow and control overhead are taken into account. Ideally, the modified algorithms allow for drastic reduction in hardware complexity at the expense of a small performance penalty.

The most promising algorithms are implemented on FPGA-based rapid prototyping platforms for proof-of-concept and for real-world performance measurement before being manufactured as ASICs.



From theory to silicon: block diagram of a 3x3 MIMO wireless communication system for increased data rates, real-world performance measurements using a rapid prototype and photograph of a communications ASIC.

Real-Time MIMO-OFDM Testbed

Personnel: Simon Häne, David Perels, Peter Lüthi

Funding: ETHZ TH-602-2 MIMO OFDM

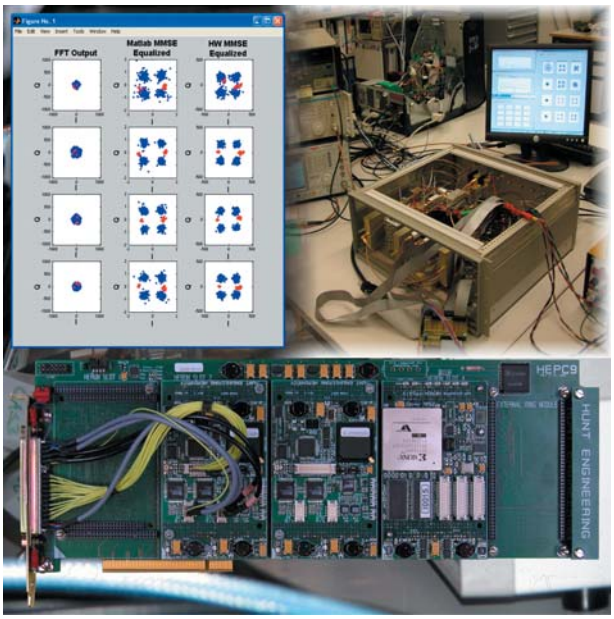
Partners: IKT-ETHZ

While multiple-input, multiple-output (MIMO) systems offer grear opportunities to make better use of bandwidth, they pose immense challenges to the algorithm and hardware development. A testbed with excessive calculation resources and high development flexibility is therefore of ultimative importance for prototyping MIMO systems.

This project, a close collaboration between IIS and the Communication Technology Laboratory (CTL), has the main goal of developing a real-time testbed demonstrating MIMO-OFDM wireless data transmission. The research topics are in the fields of algorithm development for optimal MIMO gain, hardware-efficient VLSI implementation and channel measurement and modeling.

The testbed is primarily developed to investigate a MIMO extension of the 802.11a single-antenna wireless LAN standard and is running on an FPGA-based rapid prototyping platform. Commercial frontend components are employed for the conversion of the baseband signals into the 2.4 GHz RF channels. Antenna configurations of up to four antennas at both transmitting and receiving side are supported.

All required receiver algorithms such as automatic gain control (AGC), frequency offset estimation and compensation, timing synchronization, FFT, channel estimation, and MIMO separation are implemented in hardware.



The testbed setup is presented on the top right. The analog frontend in the foreground and the digital baseband processing host PC in the background. On the bottom image the rapid prototyping platform is shown.

MIMO Testbed: Network-Based MATLAB-Hardware Co-Simulation

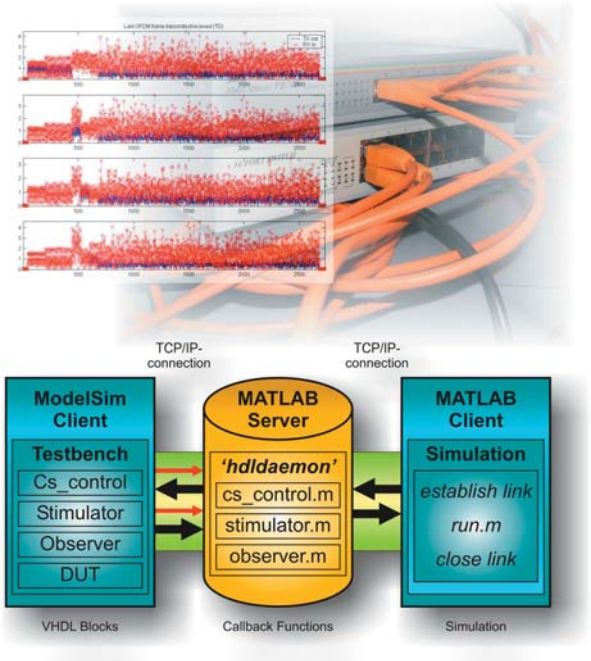
Personnel: Peter Lüthi

Funding: Siemens Bocholt

Partners: IKT-ETHZ

The evaluation of design parameters for a new digital hardware block is sometimes a tedious work, especially if the block is part of a large digital system. When optimizing the performance of the entire system, the contributions from individual blocks may be hard to determine. With this MATLAB-ModelSim™ co-simulation, single or multiple hardware description language (HDL) components can be integrated and run as part of a large MATLAB simulation. Once there is a MATLAB reference simulation with quasi-infinite precision available, a certain MATLAB sub-function can be replaced with the corresponding HDL block. Since hardware blocks are usually employing fixed-point arithmetic, the afiliated degradation in mathematic precision may affect the performance of the entire system.

By replacing MATLAB sub-functions with their corresponding HDL components in the co-simulation environment, the numeric imprecision of hardware components are introduced into the simulation. The impact of hardware-related quality trade-offs such as quantization, limited dynamic range, saturation, and overflow can be directly assessed and visualized. It is now possible to evaluate and adjust the design parameters of dedicated HDL components such as to satisfy the overall performance requirements or other quality metrics.



MATLAB-ModelSim™ co-simulation environment for direct assessment of hardware-related performance trade-offs.

Linear/SIC Receivers for MIMO Communications

Personnel: Peter Lüthi, Andreas Burg, Simon Häne, David Perels

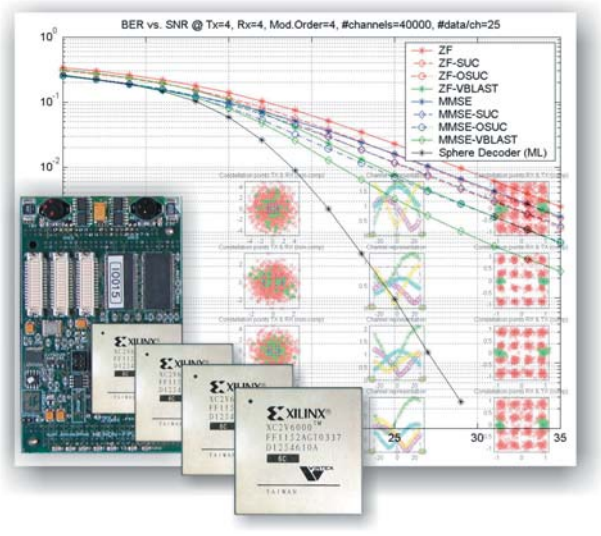
Funding: Siemens Bocholt

Partners: IKT-ETHZ

Separation of spatially multiplexed data streams is one of the most computationally complex tasks in multiple-input multiple-output (MIMO) systems. Different receiver algorithms allow for tradeoffs between hardware complexity and bit error rate (BER) performance of the system. Linear and successive interference cancellation (SIC) receivers have moderate complexity and are applied in high-rate systems, where optimal maximum-likelihood detection is no longer feasible. However, especially in wideband OFDM systems even these schemes are on the edge of what is currently feasible with integrated circuits.

Prominent examples of linear/SIC algorithms are zero-forcing (ZF) and minimum mean-squared error (MMSE) detection, with or without interference cancellation, and the so called V-BLAST scheme. They differ in their BER performance, their complexity, and their regularity. Moreover, a number of different implementation strategies exist for each of these algorithms with often very different numerical requirements and significant differences in the number and type of operations. This wide range of tradeoffs makes designspace exploration a challenging and important task that is addressed in this project.

Besides the comparison of algorithms, new hardware architectures and algorithms are proposed for their implementation. In particular, a novel MMSE detector implementation based on the matrix inversion lemma has been developed and integrated into the ETHZ real-time MIMO-OFDM testbed.



Simulation results for MIMO-OFDM and performance comparison of different MIMO detectors, together with a picture of an FPGA system on which the receiver algorithms are implemented in the ETHZ MIMO-OFDM testbed.

Sphere Decoder ASIC for MIMO Communications

Personnel: Markus Wenk, Martin Zellweger (students); Andreas Burg, Marc Wegmüller

Funding: ETHZ

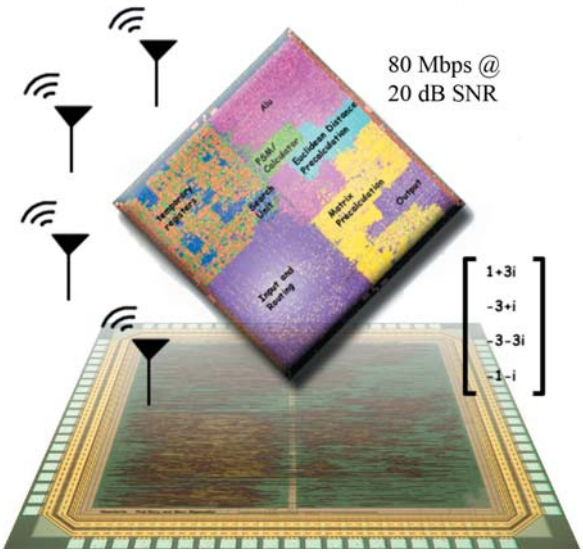
Partners: IKT-ETHZ

Maximum likelihood (ML) detection can be used to achieve optimum bit error rate (BER) performance in multiple-input multiple-output (MIMO) communication systems and in a variety of other problems in wireless communications. Unfortunately, the complexity of a straightforward implementation with an exhaustive search grows exponentially with rate and quickly becomes prohibitive.

Sphere decoding (SD) is an algorithm that significantly reduces the average complexity of the ML detection problem. So far, only DSP implementations of the algorithm have been reported which can not achieve sufficient throughput to meet the requirements of wideband MIMO communication systems.

In this project, the worlds first VLSI implementation of the algorithm has been realized. The ASIC performs MIMO detection in a 4x4 system with 16-QAM modulation and achieves a throughput of 80 Mbps at 20 dB SNR, outperforming other MIMO detection ASICs in terms of throughput and BER performance. The key contributions of this work are an innovative high-level architecture that is optimized for the tree-pruning procedure that is used in the SD algorithm, and adaptations of the original algorithm to reduce the critical path of the circuit.

The project was awarded the “Prix du Jeune Entrepreneur” of the “Section Suisse des Conseillers du Commerce Extérieur de la France”.



Layout and micrograph of the sphere decoder ASIC.

Enhanced Sphere Decoder ASIC for MIMO Communications

Personnel: Andreas Burg

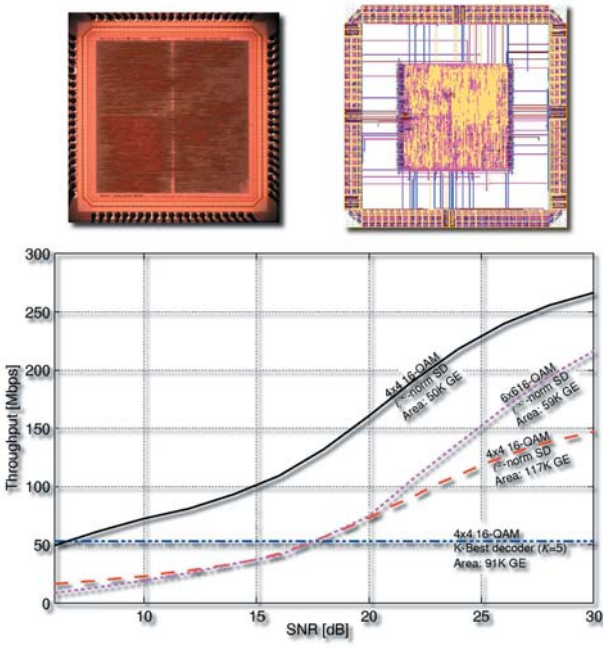
Funding: ETHZ

Partners: IKT-ETHZ

Sphere decoding (SD) has recently been recognized as a means to greatly reduce the complexity of maximum likelihood (ML) detection in multiple-input multiple-output (MIMO) systems. While the algorithm has attracted significant attention, most optimizations have been performed with DSP implementations in mind. Only little is known about its VLSI implementation which calls for completely different implementation tradeoffs and new hardware architectures.

The first ASIC implementation of SD was realized in a student project for a 4x4 MIMO system with 16-QAM modulation (see left column). Further optimizations on the algorithmic, architectural and circuit level led to a second ASIC implementation which more than doubles the throughput of the original implementation and requires less than half of its silicon area. The design outperforms all other currently reported MIMO detection ASICs with close-to-ML performance.

To examine the scalability of the proposed scheme to higher rates, the algorithm has also been implemented for systems with 64-QAM modulation and with up to six antennas. Current work addresses the problem of obtaining soft-information from sphere decoding which promises further improvements of the bit error rate performance in MIMO communication systems.



Two generations of sphere decoder ASICs for 4x4, 16-QAM MIMO systems (top) and throughput comparison of different implementation architectures for sphere decoding with different transmission rates (bottom).

Generic Hardware Prototyping Platform for Wireless Communication Systems

Personnel: Reinhard Bischoff, Jonas Biveroni (students); Andreas Burg, David Perels, Simon Häne

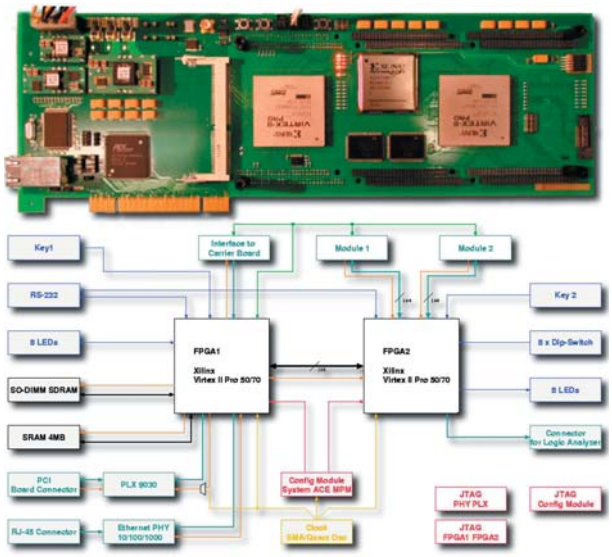
Funding: ETHZ

Partners: IKT-ETHZ

Rapid prototyping is an important step in the development and verification of complex wireless communication systems. The goal is to replace time-consuming simulations based on abstract models of the wireless channel with real-time experiments under real-world conditions. New receiver algorithms and hardware architectures are thereto first implemented in real-time testbeds using programmable logic devices.

In this project a rapid prototyping platform was developed. The core are two XILINX Virtex-2 Pro FPGAs, each of which contains two PowerPC processors, up to 328 multipliers and 74K programmable logic cells. To ease automatic partitioning of very large designs among the two devices, they are interconnected with more than 240 IO-pins. A fast 4 MByte SRAM and up to 256 MBytes of SDRAM provide sufficient storage for most applications. High-speed communication with the outside world is handled via a PCI and a Gigabit Ethernet interface. Two extension ports are available to communicate with the radio boards in wireless communication systems.

Compared to other prototyping platforms the system offers abundant resources on a single board. This avoids problems with clocking and synchronization and reduces communication bottlenecks between the system components. The manufacturing cost is less than one fifth of a comparable commercially available product.



Picture of the generic prototyping board (top) and a high-level block diagram showing its major components and interfaces (bottom).

Measurement System for the Characterization of the Human Body as a Communication Channel at Low Frequency

Personnel: Marc Wegmüller, Norbert Felber; IT'IS: Jürg Fröhlich; Miromico: Michael Oberle, Robert Reutemann

Funding: KTI 6454.3 ULTRACOM, Miromico

Partners: IT'IS, Miromico, Uni Bern

Investigations on some of the most challenging questions considering data communication through the human body will be enabled with a new measurement system developed as part of the ULTRACOM project. First attempt is the characterization of the human body as a transmission medium for electrical current and its propagation paths, secondly the usage of the human body as a communication channel at low frequency for biomedical parameter monitoring. The development of such a specific measurement system is driven by high sensitivity requirements and full decoupling from all other electronic devices.

A data transfer is established between a sender and a receiver unit using the human body as transmission channel to which signals are coupled galvancically. Both units are battery powered and linked to a standard computer by an optical link. The patient and the sensor units are therefore entirely electrically decoupled from any power lines. Based on the safety limitation (peak current of 2 mA, limited frequency range) and parameters of interest, standard tests are grouped as sessions for gathering information on: Signal attenuation in a frequency sweep over the window of interest (10 kHz to 1 MHz), dual frequency scan (relative shift comparing two different frequencies and making assumptions to influences of specific tissue layers), reachable SNR, and finally, basic data transmission schemes (FSK and BPSK modulation).

The safety of the patient has the highest priority. The injected current is 10 times below the maximum allowed contact current and even more than 25 times below nerve stimulation. The new technology will show its feasibility in clinical trials organized by the university hospital in Bern.

Sender, receiver and optical interface (middle) boards of the ULTRACOM measurement system for low frequencies.

Two-Phase Clocking for Low-Power Hearing Aid Circuits

Personnel: Felix Bürgin, Flavio Carbognani

Funding: KTI-6695.2 Micropower, Bernafon

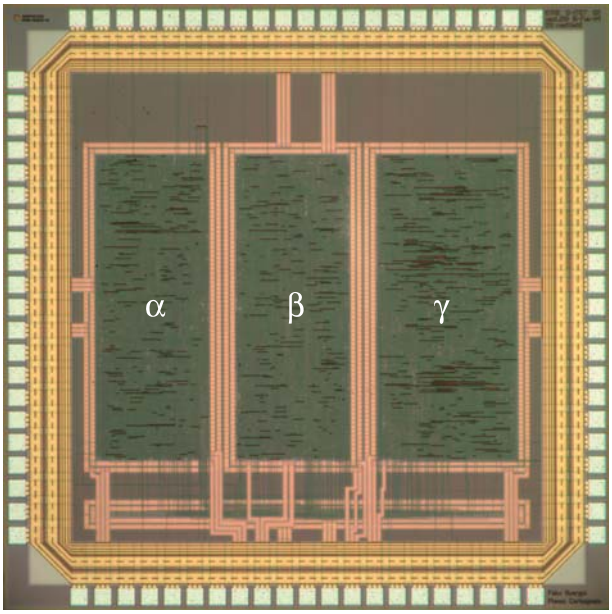
Partners: Bernafon

Energy efficiency is of primary importance in CMOS circuits intended for the portable market. Replacing the widely used one-phase single-edge-triggered (SET) clocking strategy by a two-phase level-sensitive counterpart in low-frequency applications (e.g. low-rate audio processing, as in hearing aids) makes it possible to do without strong and, hence, energy-consuming clock buffers. While this seems an attractive option, there are trade-offs and limitations.

To study the impact of the clocking strategy on the overall power dissipation, three versions of the same high-order general-purpose FIR filter have been designed and merged on the same die (see figure):

- α: One-phase design with clock gating.
- β: Two-phase design with clock gating.
- γ: One-phase design without clock gating.

The results of the measurements point out that γ dissipates around 5 times more than the others, demonstrating the energy efficiency of the clock gating technique. Design α represents the state-of-the-art of low-power, fully exploiting traditional low-power strategies, such as scaled supply voltage, clock gating and latch-based memories. Two-phase clocking enables a 20% energy savings of β compared to the one-phase design α. Yet, this energy efficiency is limited by the supply voltage.



Die photo: Three versions of the same high-order general-purpose FIR filter are merged on the same chip. Each design has its own power ring to enable accurate power measurements.

Resonant Clocking for Low-Power Hearing Aid Circuits

Personnel: Flavio Carbognani, Felix Bürgin

Funding: KTI-6695.2 Micropower, Bernafon

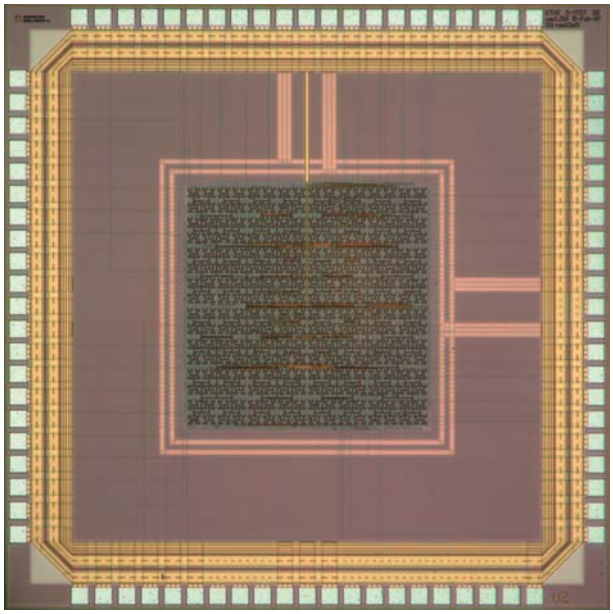
Partners: Bernafon

The fundamental cause of CMOS dynamic power dissipation is the organization of the energy transport in the circuit. Charging and discharging an internal node capacitance requires an energy injection from the driver proportional to the load and to the square of the supply voltage. Hence, to decrease the dissipation in standard CMOS circuits, the designer must minimize the switching events, reduce the node capacitance, decrease the voltage excursion, or apply some kind of combination of these methods. The problem is particularly critical inside the clock network of the design, where up to 40% of the total energy are dissipated.

Yet, when timing is not a major issue, *resonant clocking* can represent an efficient alternative to standard clocking. This technique allows the recycling of the energy from the large capacitance of the clock net, which is put in resonance with a small external inductance.

In the frame of this project, a high-order general-purpose FIR filter for low-rate audio application with a fully *resonant clocking* strategy has been designed. Among the features of this 110k-transistors design, probably the largest ever realized with such a clocking strategy, are:

- Latch-based coefficient and data memories;
- H-clock-tree to minimize the effect of clock skew even in absence of clock-tree buffers.



Die photo: FIR filter design applying *resonant clocking* strategy. The H-clock-tree inside the chip appears very neatly.

Industrial GALS Application

Personnel: Frank K. Gürkaynak, Stephan Oetiker

Funding: ETHZ

Partners: Philips NATLAB

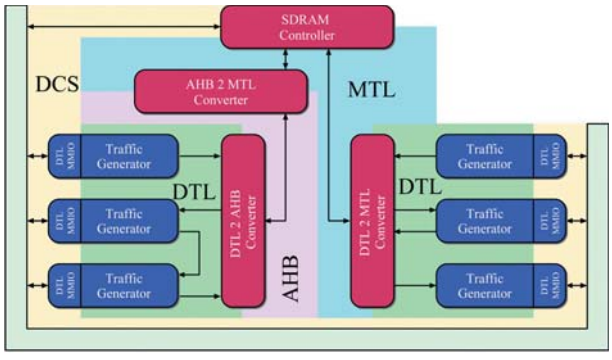
The IIS has been on the forefront of *Globally-Asynchronous Locally-Synchronous* (*GALS*) research for more than 5 years and has established a reputation especially for practical realization of *GALS* circuits. While the industry has been supporting this research, all implementations have so far been academic test chips.

The goal of this project is to implement the *GALS* solutions developed at the IIS for the past years in an industrial design environment. Among the challenges of this project are:

- Developing customized asynchronous controllers for the specific interfaces used within the design flow of the industrial partner.
- Providing satisfactory solutions for mission-critical aspects such as production testing and functional verification for *GALS* implementations.
- Making the necessary customizations to the *GALS* design flow so that it can be integrated within the established EDA tool chain of the industrial partner.
- Finding a suitable benchmark design.

At the moment, a new set of *GALS* asynchronous controllers suited to a proprietary interface have been developed and verified successfully.

The figure below shows an early study of a benchmark design providing interfaces to various protocols. DCS, DTL and MTL are proprietary protocols, while AHB is a common bus architecture. This design represents the present structure of System-on-Chip designs as implemented by the industrial partner.



The figure shows a benchmark design, that incorporates a range of different industrial interface protocols (DTL, MTL, AHB, DCS).

Adjustable Local Clock Oscillator for GALS Systems

Personnel: Stephan Oetiker, Frank K. Gürkaynak

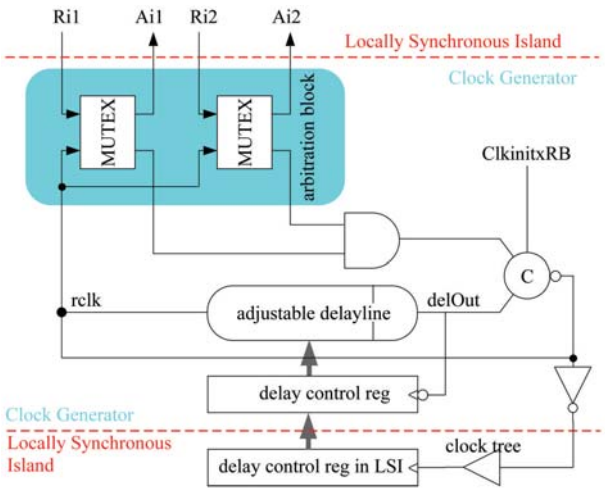
Funding: ETHZ

Partners: Philips Zurich

In this project a clock generator for crypto applications which use the GALS design approach has been developed and simulated. In addition to the functionality required by a Locally Synchronous Island (LSI) (pausability of the oscillator to avoid meta-stability during data transfers) it incorporates a mechanism to adjust its frequency at run-time. This clock, which is capable of variable clock periods, will be used to develop cryptographic hardware that offers substantially more security against Differential Power Attacks.

A year ago, a self-calibrating oscillator for GALS was implemented which was able to calibrate itself at run-time. It used two delay lines: one was being calibrated while the other one was used for the oscillator. The two delay lines introduced a big area overhead, and in some situations the switching between the two delay lines was not possible without introducing a small delay to the oscillators' period. The frequency adjustment mechanism which was developed for the crypto oscillator could now also be used for this self-calibrating oscillator.

The idea is simple: In order to enable delay adjustments at run-time without introducing glitches in the clock, the delay line has to be empty (input of the delay line is zero and the value has propagated through the delay line making the output zero as well) and stable. Only then is it possible to change the delay control value and switch to a different delay slice. To guarantee this condition, the falling edge coming from the delay line can be used to clock in the new delay control value.



Simplified overview of the pausable oscillator. The delay control signal to adjust the clock period at run-time comes from the Locally Synchronous Island and is clocked into the oscillator with the falling edge coming from the delay line.

Methods for Designing Secure Crypto Chips

Personnel: Frank K. Gürkaynak

Funding: ETHZ

Partners: KU-Leuven, TU-Graz

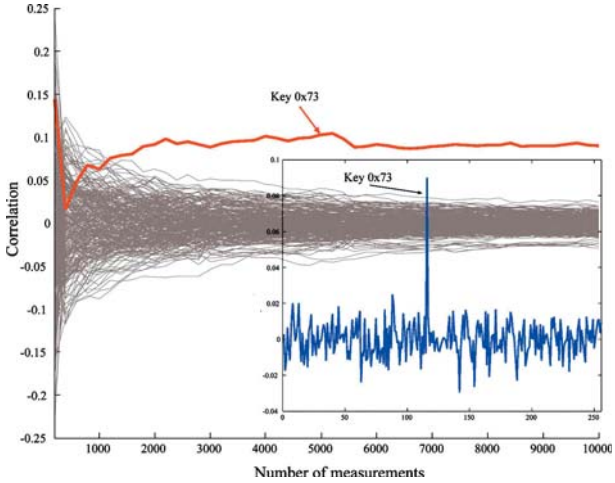
The so-called digital society can not be realized without the aid of cryptology. Most people tend to think about government secrets and espionage when talking about cryptology. While it certainly has uses in keeping government secrets safe, systems developed by cryptologists are required to (among others) ensure that digitally stored documents are not modified (integrity) and users accessing a digital service claim who they are (authentication).

Such crypto-systems are based on a number of cryptographic algorithms, and the overall success of this system depends on the security of each of its components.

While the (relative) security of a cryptographic algorithm is known, its implementation in hardware and/or software results in additional weaknesses that are difficult to quantify. By observing physical properties of the device performing the cryptographic algorithm, successful attacks can be launched against a system using this algorithm.

The aim of this project is to quantify the relative security of implementations of cryptographic algorithms in hardware and develop methods for relatively more secure ASIC implementations.

This project is a collaboration between the IIS, the IAIK of the TU-Graz (Austria) and COSIC of the KU-Leuven (Belgium).



Measurement results from a DPA attack. The correlation of each individual guess is compared against data collected by measurements. The correct guess (0x73) shows a higher correlation than the other keys.

DPA Resistant Crypto ASIC

Personnel: Norbert Pramstaller (student);
Frank K. Gürkaynak, Simon Häne

Funding: ETHZ

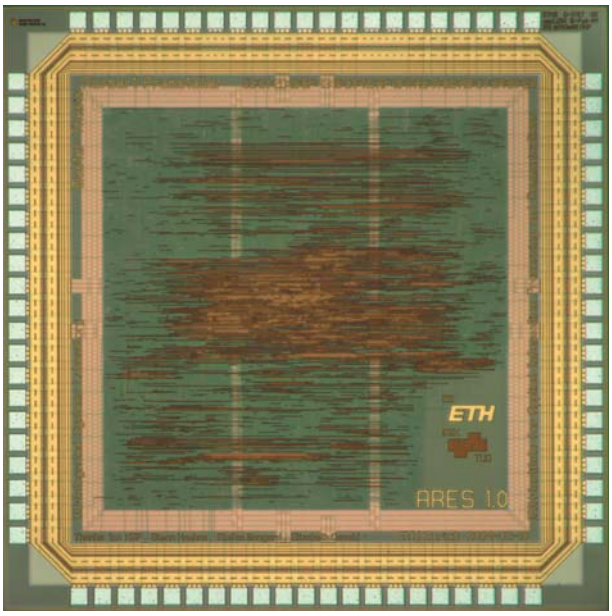
Partners: TU-Graz

Differential Power Analysis is a very efficient method of attacking hardware implementations of cryptographic algorithms. In such attacks the power consumption of a device implementing the algorithm is observed over many operations. The power consumption of a standard CMOS circuit is dependent on its operators. The attacker makes use of this property and compares the measurement results to a set of pre-computed power curves.

Each power curve is calculated using a simple model of the device and a different key assumption. In a successful attack the power curve generated using the correct portion of the key will exhibit a higher correlation to the measurement result.

In this project a specific family of countermeasures, known as masking methods, have been implemented and evaluated for the Advanced Encryption Standard (AES) algorithm. The masking method prevents direct operations between data and key within the device. The data is 'masked' by a random sequence of numbers prior to any operation involving the key. A specialized parallel computation unit is used to calculate the *correct* value of the mask so that it can be removed after the operation.

The chip implemented in this project uses two different masking methods, one reported in the literature and the other one developed as part of this project. The implementation occupies roughly the same area of a comparable design (*Fastcore*), but has a throughput that is around 40 % lower.



The chip photograph of the DPA-resistant cipher chip named ARES.

Coprocessor Prototyping Platform for SoCs

Personnel: Silvio Dragone

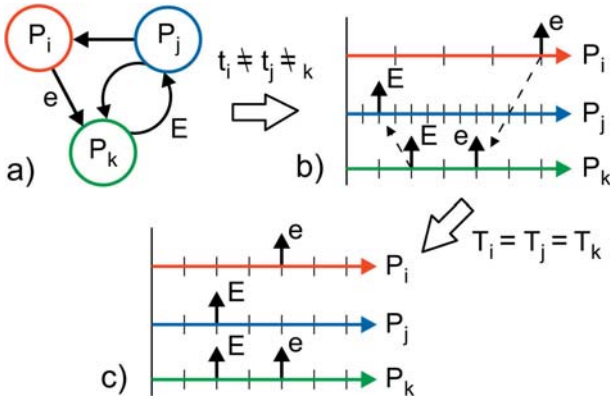
Partners: IBM Research

The performance of software-based verification strategies is not keeping up with the increasing complexity of modern System-on-Chip (SoC) designs. Therefore, modular prototyping platforms are proposed to validate SoC designs. Most of these platforms consist of real processors combined with programmable logic, e.g. FPGAs, which communicate through a board-level interconnect system.

Usually, the programmable logic and the interconnect system do not run at the target clock speed of the future design. Hence, the emulated processes of the prototyping platform have to be synchronized in order to provide an accurate system validation.

Most synchronization concepts are only able to synchronize the process data flows if data is time-independent. In this project an event-based prototyping platform is developed, which emulates events cycle-accurately, even though the processes operate in different scaled clock domains.

The figure illustrates the basic idea of the event-based prototyping platform. Part a) shows a communication example between processes running on the emulated SoC. Each process may be allocated to a separate module, each with a different physical clock. The space-time diagram in part b) shows the relative shift of the events, the emulated SoC runs with a differently scaled clock. To restore the proper event order across the entire system, the platform provides a global logical clock *T*. It does this without changing the local physical clocks.



a) A communication example between processes.
b) Space-time diagram of events with local physical clocks.
c) Space-time diagram of events with a global logical clock.

Analog and Mixed-Signal Design

Coordinator:

Qiuting Huang

High Resolution Digital-to-Analog Conversion using Over-Sampled $\Delta\Sigma$–Modulation

Personnel: Pier Andrea Francese

Funding: KTI-5731.1 OTRACOM, Philips Zurich

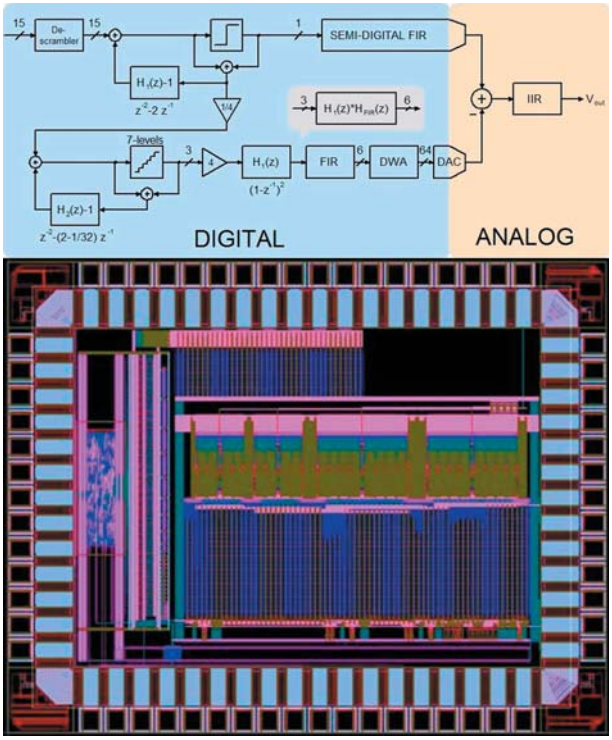
Partners: Philips Zurich

As the demand for higher data tramission rates over telephone lines is steadily increasing VDSL (Very High Speed Digital Subscriber Line) has become the standard of choice for transceiver development. A key component in the VDSL modem is the Digital-to-Analog Coverter (DAC) where a resolution in the range of 12 to 14 bits, within a signal bandwidth of several MHz are required.

This project aims at the realization of a DAC fulfilling this level of specifications in one of the newest CMOS technologies available at the moment, that features a drawn gate length of 90 nm and a power supply of only 1.2 V.

The architecture chosen is the evolution of an innovative scheme that was already implemented and successfully characterized in a previous CMOS technology node featuring a gate length of 0.18 μm.

The circuit implements a cascaded digital sigma-delta modulator followed by an analog reconstruction filter that is realized in switched-capacitor (SC) technique. The filter includes a semi-digital finite-impulse-response (FIR) filter plus it digital replica and a high-order infinite-impulse-response (IIR) filter.



The DAC includes a descrambler at the digital input to avoid signal dependent distortion at the board level. The entire chip occupies an area of roughly 2 mm² including the pads.

High-speed Pipelined A/D Converters in Deep-Submicron CMOS Technology

Personnel: Jürg Treichler

Funding: KTI-6171.2 CITE, Philips Zurich

Partners: Philips Zurich

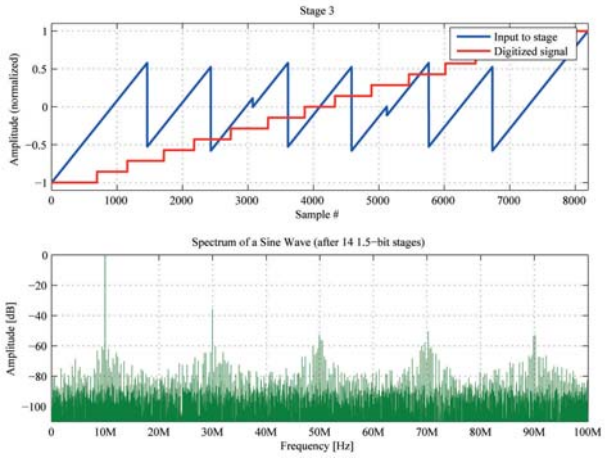
Recent developments in wireless and wire bound communication systems have created a growing demand for analog-to-digital converters (ADCs) featuring medium resolutions combined with high throughput. These ADCs must be producible in mainstream deep-submicron technologies together with digital circuitry, for example digital signal processors (DSPs), as systems-on-a-chip.

Pipelined ADCs have the potential to fulfill the aforementioned requirements. Recent publications underline the growing capabilities of the pipelined architecture, as there are designs available with excellent spurious free dynamic range (SFDR) characteristics combined with sampling rates well above 20 MS/s.

A major limit to the performance of pipelined ADCs is the mismatch among different components with nominally equal sizes, which is intrinsic to every manufacturing process.

In past publications, several schemes have been introduced which intend to counter the effects of component mismatch. Such schemes include passive error averaging, double sampling, as well as digital background calibration.

The goal of this project is to develop a pipelined analog-to-digital converter which satisfies the initially mentioned requirements. One or more of the published schemes will be used to counter the effects of component mismatch. The system will run at very low voltage (1.2 V) and be fabricated in a modern deep-submicron process.



Harmonic distortion of a sine wave caused by capacitor mismatch in the multiplying DACs of a pipelined ADC. The mismatch is greatly exaggerated for demonstration purposes.

Folding and Interpolating A/D Converters in Deep-Submicron CMOS Technology

Personnel: Yihui Chen

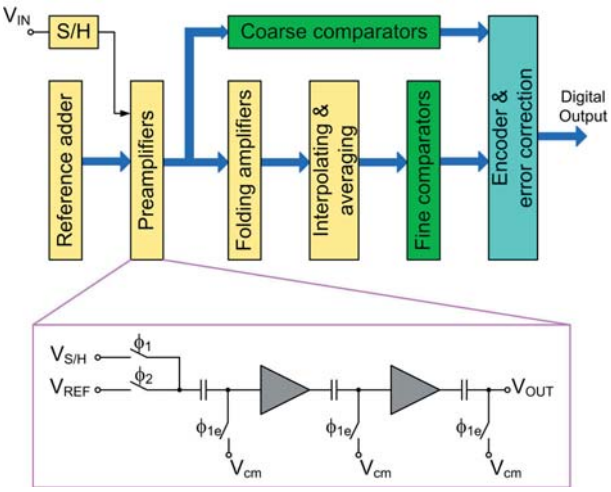
Funding: KTI-6171.2 CITE, Philips Zurich

Partners: Philips Zurich

High speed Nyquist analog-to-digital converters (ADCs) are key elements in modern digital communication systems. Although the flash architecture has been used to implement the highest speed ADCs, the exponential growth of power, area, and input capacitance of flash converters as a function of resolution makes them impractical for resolutions above 8 bits. Folding and interpolating have been proved beneficial to alleviate these problems while maintaining the one-step nature of the architecture.

However, ever since the elegant solution of folding migrated from bipolar to CMOS technologies, folding has been plagued by the higher mismatches of CMOS differential pairs. Although averaging techniques can be used to improve matching performance, fairly large MOSFET device sizes are still needed to maintain reasonable offsets, which compromises the goal to maximum the conversion speed.

In this project, in order to boost the accuracy of folding ADCs to 10 bits, two preamplifier stages are inserted before folding amplifiers. The offset voltages of these amplifiers are fully canceled by utilizing open loop offset storage. In addition, these preamplifiers provide sufficient gain to overcome the offset voltages contributed by the following folding amplifiers and comparators. As a consequence, small devices can be used in the differential pairs, which help to increase the conversion rate for limited power consumption.



Architecture of folding and interpolating A/D converter and simplified circuit diagram of preamplifiers.

Multi-Standard A/D Converter for Wireless Receivers

Personnel: Thomas Christen

Funding: BBW 03.0465-2 End-to-End Reconfigurablility, ACP

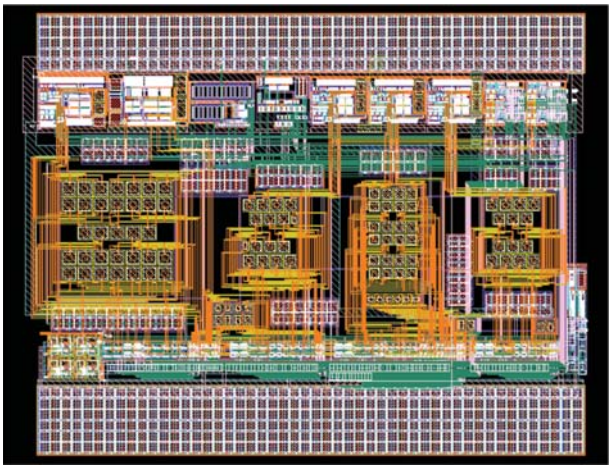
Partners: ACP, E2R Consortium

Wireless communication is witnessing tremendous growth. The proliferation of different standards covering wide, local and personal networks requires designs that work across multiple wireless standards. The current trends call for designs that allow convergence of wireless services allowing access to different standards from the same wireless device and cost effective design solutions for intercontinental roaming. For space and cost reasons, hardware has to be shared as much as possible.

As advances in technology provide increasingly faster and less expensive digital hardware, more of the traditional analog functions of radio receivers will be replaced with software or digital hardware. Trends in receiver design have evolved this goal by incorporating digitazation closer and closer to the receive antenna. The A/D converter in the receive path has therefore become one of the key elements in such a device.

An attractive converter architecture for such a multi-standard receiver is the ΣΔ converter, since speed can be traded for resolution. Nethertheless, covering multiple cellular and WLAN standards is a challenge, because the spread of bandwidth and resolution between the different standards is very high.

The goal of this project is to develop a multi-standard ADC covering multiple celluar and WLAN standards featuring maximum resource share and low power consumption, since users will excpect performance (battery life, size and weight, ease to use) to be at least as good as for current single-standard devices.



Layout of a multi-standard ΣΔ ADC in 0.18 μm CMOS.

Multi-Standard RF Front-Ends for Mobile Communications

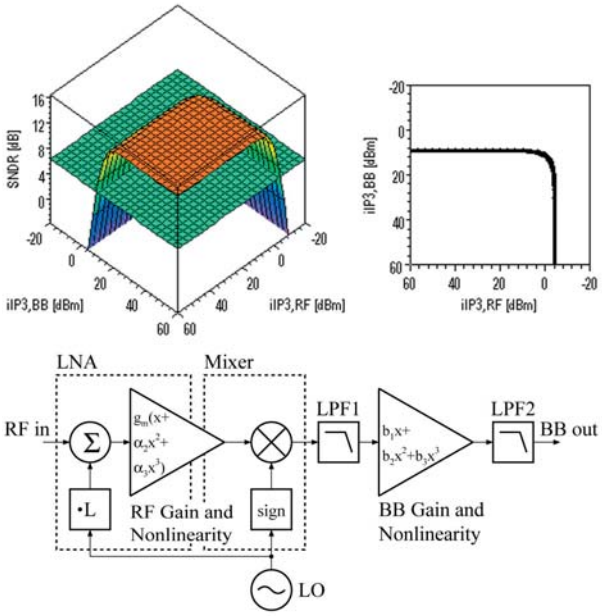
Personnel: Thomas Dellsperger

Funding: BBW 03.0465-2 End-to-End Reconfigurablility

Partners: ACP, E2R Consortium

The idea of a multi-standard RF front-end is to accommodate a certain set of mobile communication standards in a single RF front-end by reconfiguration of its elements. Such a reconfigurable RF front-end can be expected to allow a substantially lower bill of materials (BOM) through intelligent resource sharing. Though the “ideal” RF front-end - in which the RF signal is fed into the analog to digital converter (ADC) right after the antenna - is not realizable today for cellular phone standards, the ADC should be moved as close to the antenna as possible to make a receiver amenable for software-defined radio (SDR).

This project investigates the requirements on a multi-standard RF front-end supporting well-known cellular phone standards (GSM/DCS/PCS and W-CDMA) and a wireless LAN standard (IEEE 802.11b/g). A direct conversion receiver (DCR) architecture realized in CMOS technology has been identified as a versatile architecture for broadband systems (W-CDMA, WLAN), but suffers from flicker-noise and DC-offset for narrow-band systems like GSM. A major challenge is therefore to overcome the flicker-noise and DC-offset issues by an appropriately modified down-conversion mixer design. Alternatively, the same DCR architecture can be adapted to a very-low IF architecture for narrow-bandwidth systems requiring only low adjacent channel rejection. Since GSM is the bottleneck of a multi-standard RF front-end if a DCR architecture is employed, this standard is the primary focus of this project.



SNDR for the GSM AM suppression test as a function of the RF section iIP3 and the BB section iIP3 (top left), its intersection with the min. SNDR for reference performance (top right), and DCR model used for calculations (bottom).

Design Study of a Digital Receiver for UMTS Mobiles

Personnel: Chiara Martelli, Christian Benkeser

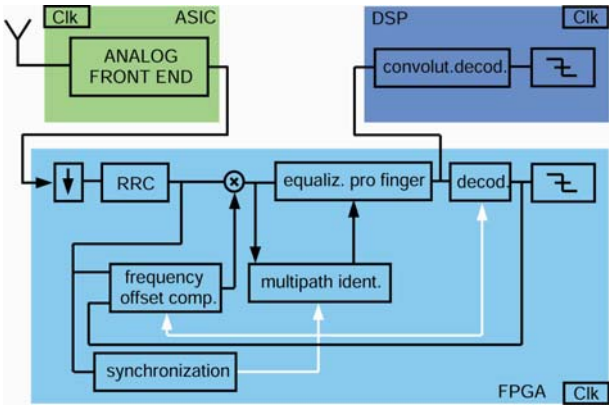
Funding: KTI6767.1 OREMO, ACP

Partners: ACP

Receiver design for mobile communications has to handle the characteristics of a mobile radio signal such as wide dynamic range, time, delay and frequency variation in a chain of sub-sequent building blocks. To achieve that, the radio signal is processed such that all unwanted signal components like adjacent channel signals or unrelated blockers are eliminated and the wanted signal is made ready for decoding.

Known mobile receivers have been implemented with one or multiple receiver front-end ICs which passed their analog base-band output signals to A/D-converters located on a large digital base-band IC. Receiver front end ICs were usually realized in Bipolar or BiCMOS technologies, base-band circuitry on CMOS technologies. The advent of modern deep sub-micron CMOS processes has lead to the noble implementation of the whole receiver chain in CMOS, allowing new trade-offs to be made, especially across the previous boundary of the A/D converter.

In preceding projects a wide-band code division multiple access (WCDMA) RF front end and a suitable A/D converter, both in CMOS technology, with a digital front end have been realized. They incorporate a new front end with a digital interface to base-band signal processing. This project will complement this set-up with a digital rake receiver, required of passing the WCDMA type approval tests, after 3GPP specifications. It will be first implemented on an FPGA and DSP system, to easily check the fulfillment of the requirements. Afterwards it will be implemented on a digital VLSI, in 0.13μm CMOS technology. The digital rake receiver handles frequency offset compensation, symbol synchronization as well as channel impairments equalization, i.e. time and phase shifts and gain imbalances due to multiple fading environment. The convolutional and turbo decoding of the wanted signal is lead on an external DSP, easily re-programmable by the user.



Block diagram for the WCDMA receiver.

Frequency Synthesis for UMTS Transmission

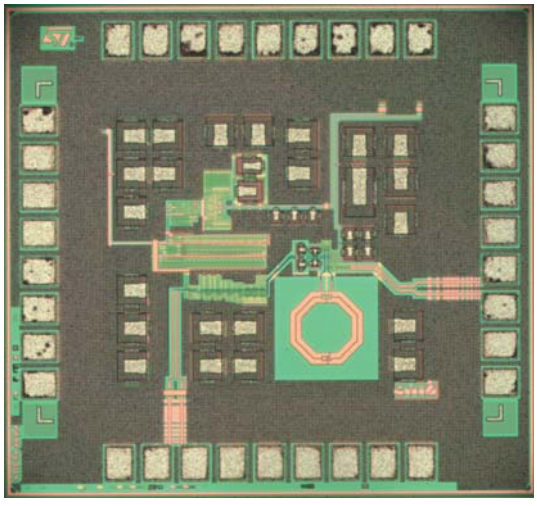
Personnel: Xinhua Chen

Funding: KTI-6148.1 CMOS-SOI, ACP

Partners: ACP

Third-generation cellular radio networks based on Wideband Code Division Multiple Access (WCDMA) are growing rapidly and believed to dominate the market in the next few years. Given the substantial amount of digital signal processing, fine line CMOS technologies with gate lengths of 0.13 µm or even below is preferred to realize low power, cost effective solutions. A RF front-end in the same technology simplifies the technology mix for the wireless chip set and offers a potential for higher integration level. Recently much research has been carried out on the low voltage and low power CMOS design of WCDMA transmission. However, the progress of the corresponding frequency synthesizers is slow. This is probably due to the difficulties in achieving good phase noise voltage-controlled oscillator (VCO) and high speed prescaler with limited supply voltage which is the key aspect to meet the stringent WCDMA specifications.

In this project, an integer-N frequency synthesizer, including an on-chip VCO, has been successfully implemented in 0.13 µm standard CMOS technology. The overall performance meets the UMTS specifications with low power consumption which is a result of careful design and layout of the individual building blocks. A compact layout has been obtained, which forsters the inclusion of synthesizers for single chip UMTS transceiver to maximize the level of integration and also contradict the argument that synthesizers take up too much space in a complete solution, hence making it too costly.



Chip photograph of the frequency synthesizer.

Deep Sub-micron CMOS Quadrature Modulator and Translational Loop for DCS 1800 MS Transmitter

Personnel: Zhiheng Chen

Funding: ETHZ

Partners: ACP

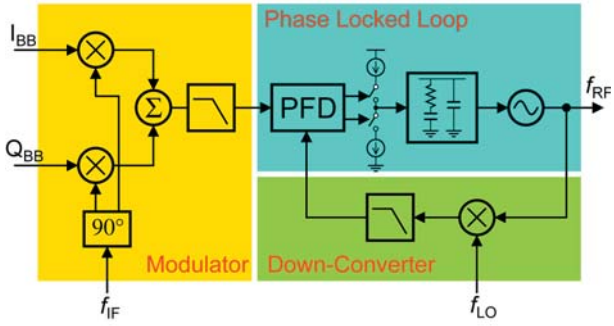
Although the third generation (3G) wireless services have already been launched, 2G and 2.5G systems are expected to continue to flourish for a long period. A single handset enabling the user to choose the most appropriate service is thus the trend of development. Multi-mode operation covering both the GSM/GPRS and WCDMA air interfaces will resolve most of the evolution issues of the GSM system. Research works of recent years have confirmed the interest.

This project aims at a translational-loop-based CMOS modulator/up-converter for GSM/GPRS mode and DCS 1800 band operation of mobile stations (MSs). It is an interim step toward an integrated multi-band multi-mode CMOS mobile transceiver.

The translational loop (or offset PLL) is a proven modulation/up-conversion architecture for narrow band phase-modulated systems. The spectrum purity of the output signal is guaranteed by the filtering nature of the PLL and thus no duplexer is needed. This saves the efficiency of the power amplifier, minimizes the form factor, and lowers the cost. What makes this project challenging is low voltage (1.2 V) yet still low power operation.

At the first phase of this project, the GSM(DCS)/GPRS system is studied at the system level, with the focus on the performance specs of radio transceivers. An in-depth analysis of the translational loop follows, which addresses key transmitter specifications and translates them into design parameters of corresponding building blocks. A behavioral model has also been developed to verify the analysis and gain design insights.

In the next research stage, the emphasis will be shifted to the circuit side.



An overview of the transmitter with its functional building blocks highlighted.

Research Projects

Technology CAD

Coordinators:

Wolfgang Fichtner
Andreas Schenk
Dölf Aemmer

Silicon-based Nanodevices (SINANO)

Personnel: Andreas Schenk

Funding: BBW, EU-IST-2004-506844 SINANO

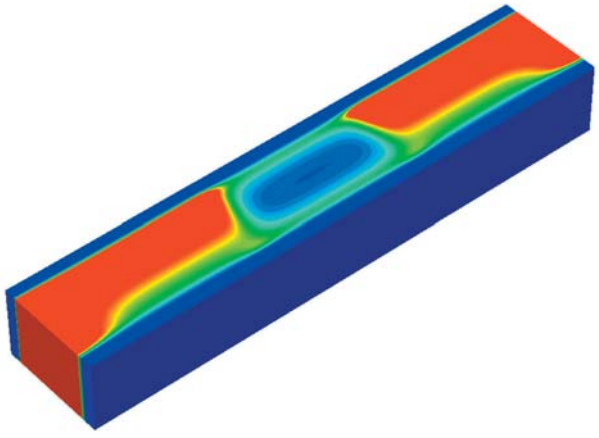
Partners: SINANO Consortium

The aim of the SINANO project is to study the potential of conventional CMOS (*Complementary Metal Oxide Semiconductor*), alternative CMOS as SOI (*Silicon On Insulator*), SON (*Silicon On Nothing*), FinFET, and post-CMOS devices, like SET (*Single-Electron Transistor*), SEM (*Single-Electron Memory*), and RTD (*Resonant Tunnelling Diode*), in view of the challenges and predictions set by the *International Technology Roadmap for Semiconductors* for the 45 nm node and beyond (> 2008), to propose innovative designs by simulating exploratory devices and structures, and to integrate the partners' modelling capabilities by validation and benchmarking of the modelling tools and strategies against template devices.

Simulation activities are bundled in work package 4 of the project, comprising five tasks:

- Building up a common platform of benchmark devices
- Study of the transport models most suitable for predictive simulation of CMOS devices from the 50 nm node down to the ultimate limit (both bulk and SOI)
- Study of the performance and reliability of conventional (SiO_2) and high-k thin insulator gate stacks for sub-50 nm MOSFETs
- Lumped and compact models for sub-50 nm MOSFETS and post-CMOS devices
- Modelling of post-CMOS devices (SET, SEM, RTD, carbon nanotubes)

The contribution of ETHZ during the first year involved quantum-ballistic simulations of template devices, computation of quantum-V_T shifts with different codes, a comparative study of template MOSFETs using all available mobility models, and the simulation of sequential and coherent tunneling through a SiO_2-Si-SiO_2 RTD.



Quantum-mechanical electron density distribution in a 25 nm DGSOI nMOSFET with realistic doping profile. Coupled *SIMNAD-DESSIS* simulation.

Simulation of Post-CMOS Devices

Personnel: Andreas Schenk

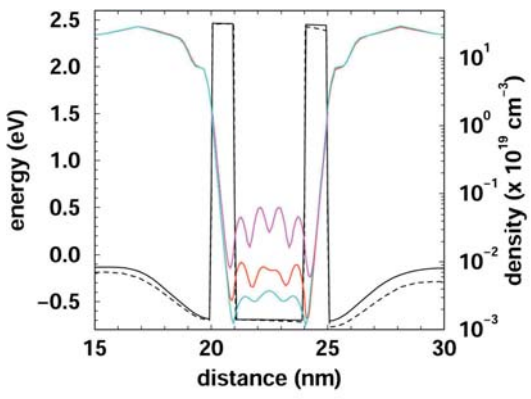
Funding: BBW, EU-IST-2004-506844 SINANO

Partners: SINANO Consortium

Study of the potential of post-CMOS devices, in view of the challenges and predictions set by the International Technology Roadmap for Semiconductors beyond the 45 nm node is part of work package 4 of the SINANO project with the aim to develop new theoretical and modelling approaches to the simulation of the fundamental properties (density of states, scattering rates, etc.) and the electrical characteristics (conductance, etc.) of individual quantum dots (QDs), interacting quantum dots, single electron transistors (SETs), resonant tunneling diodes (RTDs), resonant tunneling transistors (RTTs), and carbon nanotubes (CNTs). Main topics are:

- Simulation of capacitance and conductance of SETs in the near-equilibrium limit
- Comparison of different SET geometries and conclusions on the impact of the geometry on device parameters
- Investigation of the behaviour of SiO_2-Si-SiO_2 RTDs
- Identification of the most crucial problems for a realistic modelling and for potential applications
- Variation of critical device parameters.

Based on well-defined template devices which are, on one hand, realistic enough to yield all the essential physics and which are, on the other hand, simple enough to enable as many partners as possible to participate in the simulations, the development of adequate simulation tools and the improvement and extension of already existing in-house tools is stimulated. The comparison of simulation results for a given template device between different groups reveals the reliability of a certain tool, the necessary refinement of physical models, and puts forward a scientific assessment of the underlying methodologies.



Band edge and electron density profiles in a SiO_2-Si-SiO_2 RTD. Coherent quantum-ballistic charge injection at low forward bias between the third and fourth resonance level.

Hierarchical Physics-based RF Noise Modeling for Silicon Devices

Personnel: Simon Brugger, Andreas Schenk

Funding: Fujitsu, Synopsys (ISE AG)

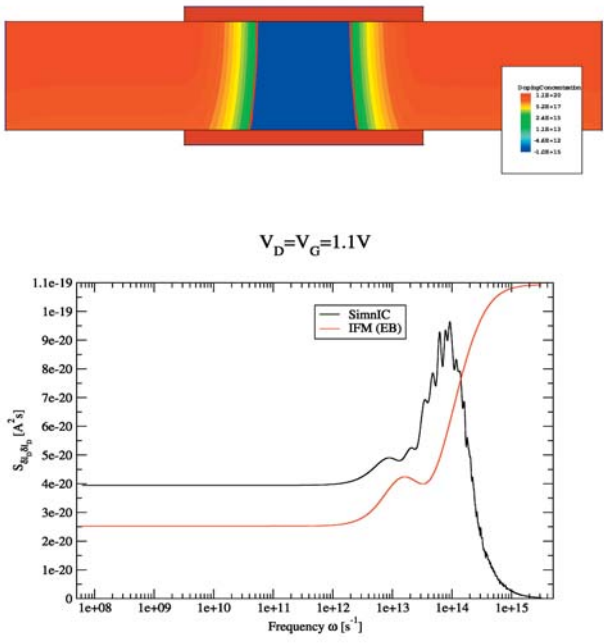
Partners: Fujitsu, Synopsys (ISE AG)

Nowadays different methods are available to compute noise figures of merit for semiconductor devices.

In an effort to compare all those methods with each others a device simulator for noise computation called SimnIC was developed and validated.

SimnIC is a simulator for silicon devices which can compute both the steady states and small signal behaviors using the drift-diffusion, energy-balance, one-particle and many-particle Monte Carlo (MC) methods. It is, therefore, not only able to compute noise figures using the impedance field method (IFM) coupled with MC generated- or thermodynamic noise sources, but also using the one-particle and many-particle MC methods. The simulator is fully parallelized and can run on many processors on shared memory architecture. It is therefore possible to simulate millions of particles in a reasonable amount of CPU time.

SimnIC enables to determine the cases where the IFM breaks down and offers, in those cases, alternative ways to compute the needed figures of merit.



Top: Double gate SOI-MOSFET. Bottom: Comparison of the autocorrelation function of the fluctuation of the terminal drain current computed using the many-particle Monte Carlo method (black) and using the IFM (red).

Quantum-mechanical Modeling of the Low-field Mobility in Ultra-small MOS Transistors

Personnel: Timm Höhr, Andreas Schenk

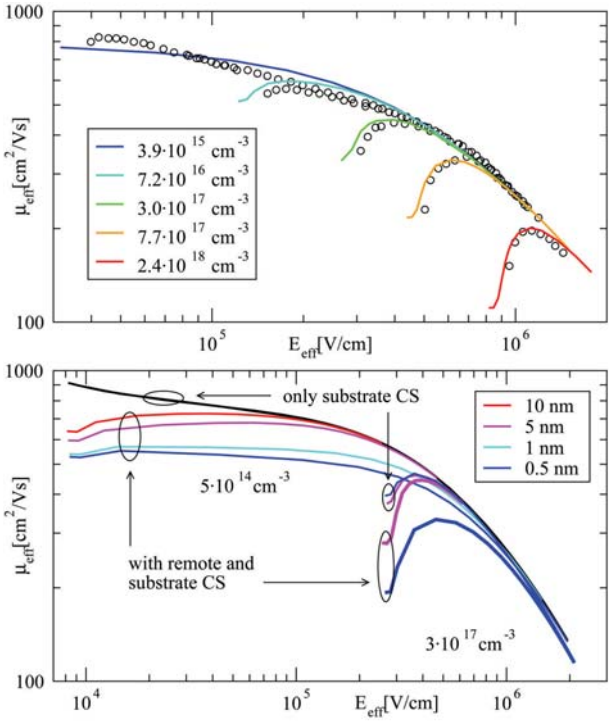
Funding: ETHZ, Fujitsu

Partners: Fujitsu

Simulation of state-of-the-art transistors requires quantum-mechanical modeling to obtain realistic inversion layer densities. Many devices such as standard bulk, SOI or double gate transistors, feature one-dimensional quantum confinement perpendicular to the transport direction.

In this project the eigenstates of the channel electrons are obtained from a 1D-Schrödinger-Poisson-Solver in the *DESSIS* simulator and fed into a quantum-mechanical model for the low-field drift mobility taking into account phonon, surface roughness and Coulomb scattering from ionized impurities. The mobility model was fit to the universal curve that is obtained from measurements on long-channel bulk MOSFETs. Towards low effective fields, i.e. for weak screening by the inversion layer density, Coulomb scattering at ionized impurities in the substrate causes deviations from the universal behavior, the so-called *Coulomb roll-off* (upper graph).

By including scattering at the impurities in the poly silicon gate depletion zone (i.e. unscreened by majority carriers) the mobility further degrades. This *remote charge scattering* (RCS) effect is shown for different oxide thicknesses and two substrate dopings ($5\cdot10^{14}$ and $3\cdot10^{17}$ cm^{-3}) in the lower graph.



Calculated effective mobility (lines) vs. the normal effective field for NMOS structures: upper part: results for different dopings compared to the Takagi measurements (circles), lower part: RCS degradation for a gate doping of 10^{20} cm^{-3}.

Quantum Transport Models Study

Personnel: Mathieu Luisier

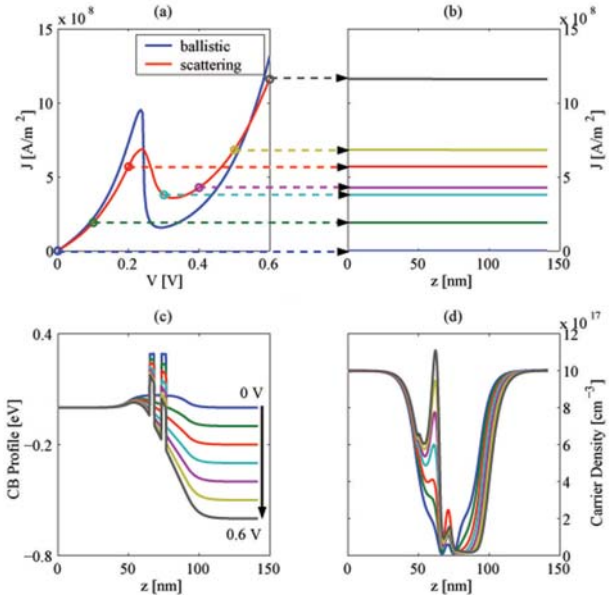
Funding: ETHZ

The modeling of quantum transport for semiconductor nanostructures has gained a lot of attention during the ten last years due to the progress obtained in the fabrication technology. Many quantum mechanical theories has been investigated to handle this complicated problem: among possible candidates, the nonequilibrium Green's functions introduced by Kadanoff and Baym in the 1960's (NEGF), the density matrix approach based on the Heisenberg equation of motion, the quantum Monte Carlo simulation of particles, and the resolution of the Pauli master equation take up the first places.

All these methods describe the same quantum mechanical problem but with different approximations and levels of complexity. However, they all enable the separation of the global particle transport into a ballistic or coherent part and into a scattering part.

The main challenge consists in selecting and implementing an efficient quantum mechanical method from the list proposed above. It should allow an adequate treatment of the scattering mechanisms for one-, two-, and three-dimensional structures with arbitrary potential shape in order to get a more realistic description of quantum transport than in the ballistic case.

For stationary situations, the nonequilibrium Green's functions seem to be the best solution because scattering interactions are easily included in the theory.



One dimensional simulation of a resonant tunneling diode (RTD) using Green's functions. (a) Current versus voltage with/without scattering. (b) Current conservation through the device. (c) Conduction band profile. (d) Carrier density.

Integration of Kinetic Monte Carlo Module in Continuum Process Simulator

Personnel: Eduardo Alonso

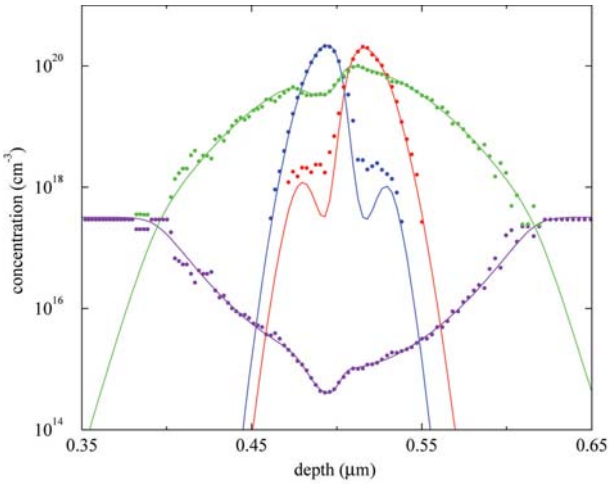
Funding: TOP NANO 21 5779.2 MOLDYN

Partners: Synopsys (ISE AG)

The kinetic Monte Carlo (KMC) code ATOMISE developed in the MOLDYN project has been integrated as a module into the process simulator FLOOPS. Its TCL interface allows for the implementation of diffusion and oxidation models at user level. ATOMISE is a diffusion solver based on the KMC method with charged defects and Fermi level effects, that can now substitute the diffusion processing steps in FLOOPS. Like in FLOOPS, different diffusion models can be constructed in ATOMISE without modifying the source code.

During the coupling stage, the FLOOPS supported diffusion models have been implemented in ATOMISE. Direct comparisons between finite element simulations by FLOOPS and KMC by ATOMISE have been conducted in order to assess the charges implementation. The results have been very encouraging since the agreement between continuum and atomistic simulations has been excellent, while performance has not been affected. Further work geared towards extending the coupling between FLOOPS and ATOMISE to all the processing steps, such as etching and oxidation, are planned. In this manner, the whole atomistic picture can be conserved throughout the entire process simulation.

The example below shows the effect of charges on the annealing of a boron and an interstitial spike, after carefully choosing the charging parameters, forcing boron interstitial-pairs (BI) to be negatively charged. BI's are therefore repelled by boron (blue), which leads to a trough in the BI concentration at the boron peak. The violet line represents the electron density, with a minimum at the boron peak.



Direct comparison between the five stream model in FLOOPS (solid lines) and atomistic simulations with ATOMISE (circles). The blue line depicts boron, interstitials are displayed in red and boron-interstitial pairs in green.

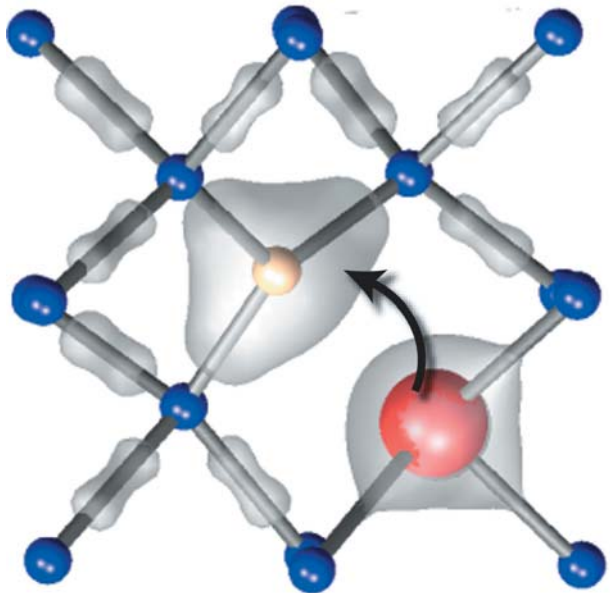
Co-doping Strategies for Donors in Silicon

Personnel: Christoph Müller

Funding: ETHZ

Deactivation of donors in heavily doped silicon is one of the predominant problems that CMOS technology has to deal with in connection with the down-scaling of semiconductor devices. In nanoelectronics technologies, source, drain, and channel regions of transistors need to feature doping concentrations in excess of the respective solid solubility limits. Unfortunately, a large percentage of up to 90 % of the donors introduced are compensated during the wafer manufacturing process. Co-doping is considered to be one method that could potentially forestall donor deactivation. Prerequisite for its investigation is a deep understanding of the deactivation mechanisms in silicon on atomistic level.

Based on ab initio calculations, the effectiveness of various Group I, II, and IV elements as possible co-dopants has been evaluated. A co-dopant should exhibit a high binding energy with both vacancies and donor-vacancy complexes. At the same time, the co-dopant should reduce the number of acceptor states of such a complex. The isovalent impurities C and Ge are found to be unsuited for the intended purpose of clustering inhibition. Lithium and Magnesium, on the other hand, both bind strongly to vacancies while reducing the number of deep acceptor levels of compensating complexes in the band gap. Magnesium seems to be the most promising co-doping candidate for both Phosphorus and Arsenic.



An Arsenic (red)-Carbon (white) pair in the Silicon lattice: The charge density plot reveals the charge transfer (arrow) of the strongly localized donor state of As, mainly centered around the C atom. The co-dopant pair is hence neutral and electrically inactive.

Vacancy Diffusion in Silicon

Personnel: Beat Sahli

Funding: TOP NANO 21 5779.2 MOLDYN, Synopsys (ISE AG)

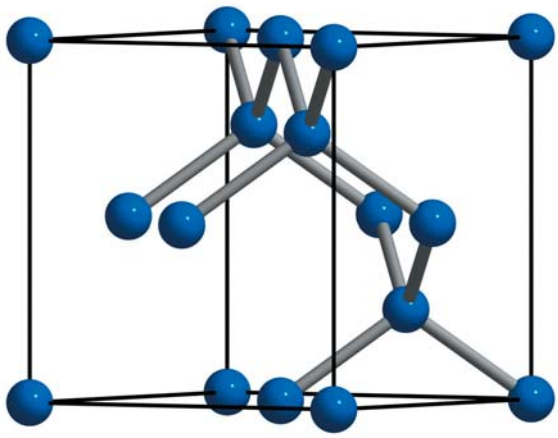
Partners: Synopsys (ISE AG)

In a previous project phase the diffusion coefficient of the self-interstitial was calculated for different temperatures with ab-initio molecular dynamics simulations. The method worked well and indeed proved to be indispensable. In the current phase the same method is applied to the diffusion of the vacancy in silicon.

The vacancy and the self-interstitial are the two intrinsic point defects in silicon. It is necessary to know their properties for modeling dopant diffusion in silicon and for modeling silicon crystal growth with the Czochralski method. But their diffusion coefficients and many other of their properties are very difficult to measure. Accordingly, many studies have tried to determine the diffusion coefficients of the vacancy and the self-interstitial with theoretical methods. But the required amount of computing power to do this with an accurate potential energy function and without additional assumptions about the defect dynamics has only recently become available.

The simulations are done with the *Vienna Ab-initio Simulation Package (VASP).* The required computing time is collected with the *Condor* high throughput computing system which makes it possible to use all workstations at our institute when the user is absent and no other batch job is running. Many independent simulations are necessary and the simulations need a lot of CPU time but only a small amount of memory. Running the simulations on a cluster of workstations is therefore the optimal solution.

The particle trajectories produced by the molecular dynamics simulations are analyzed in order to determine the trajectory of the defect in the simulation cell. From the defect trajectory the diffusion coefficient is calculated. The procedure is repeated for several different temperatures and a prefactor and a migration energy are extracted by fitting to an Arrhenius curve.



This picture shows a vacancy in the silicon crystal lattice: One silicon atom is missing.

The Harmonic Balance Module in DESSIS

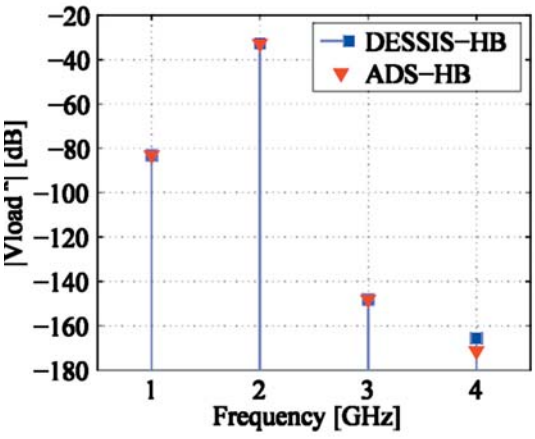
Personnel: Bernhard Schmithüsen, Ivan Ruiz Gallego

Funding: KTI-6378.1 LASSIS, Synopsys (ISE AG)

Partners: Synopsys (ISE AG)

The harmonic balance analysis (HB), a well known frequency domain method in circuit simulation to solve (almost-)periodically excited systems for nonlinear HF and microwave applications, has been implemented for the mixed-mode device simulation platform DESSIS. The analysis enables efficient simulations of harmonic distortion effects for systems and devices under large signal conditions. It is beneficially applied for simulation cases with intrinsic time constants ranging over several orders of magnitude, and extends the existing transient and small signal (AC) analysis capabilities of the simulator.

The device-level HB module enables a physics-based distortion analysis of nonlinear semiconductor devices. Compared to compact modeling, the generation of distortion can be spatially localized within the device. Optimization processes for standard RF figures of merit, like compression points or interception points, become feasible while the geometrical structure and material properties are completely taken into account, and the effect of physical models on distortion characteristics can effectively be studied. The implementation of the HB module includes so far the excitation with a single harmonic excitation for mixed-mode simulation. The solution procedure consists of a Newton-like iteration process utilizing either direct or iterative linear solvers.



A comparison of the output voltage spectra of a varactor frequency doubler computed by mixed-mode HB (DESSIS-HB) and by circuit-level HB simulations with ADS-HB after compact model parameter extraction of the diode.

Iterative Solution Procedures for the Harmonic Balance Equation in Device Simulation

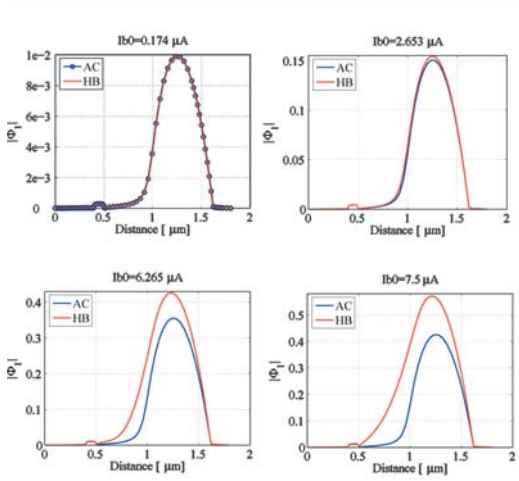
Personnel: Bernhard Schmithüsen

Funding: KTI-6378.1 LASSIS, Synopsys (ISE AG)

Partners: Synopsys (ISE AG)

The Fourier transformation of the differential equation describing periodically excited electronic systems leads, using truncated Fourier series, to the harmonic balance (HB) equation, a very large nonlinear algebraic equation containing the Fourier coefficients of the solution variables as unknowns. Compared to DC simulations, with typical system sizes of several ten thousand variables, the number of unknowns grows linearly with the number of approximating harmonics. The use of iterative linear solvers becomes indispensable.

Within our mixed-mode device simulation platform DESSIS Newton-like solving methods for the HB equation have been coupled to the standard parallel linear iterative solver ILS, to the parallel direct solver PARDISO, and a novel block-band preconditioned GMRES solver with memory-less matrix assembly. Experimental simulations show that well established incomplete-LU-factorization-based preconditioners are hardly feasible for the HB problem, while, astonishingly enough, a physically motivated block-band preconditioner for GMRES iterations lead to reasonable convergence even under large signal operation. Compared to Newton-direct methods, the novel Newton-BBP-GMRES iteration scheme requires more Newton steps but reduces significantly the memory consumption of the simulation and enables the use of a larger number of approximating harmonics.



HB simulation example using the Newton-direct method: comparison of linear AC and HB fundamental electrostatic potential over depth for a simple bipolar transitor showing increasing deviations for large signal operation.

Physics-based Simulation of RF Devices and Systems

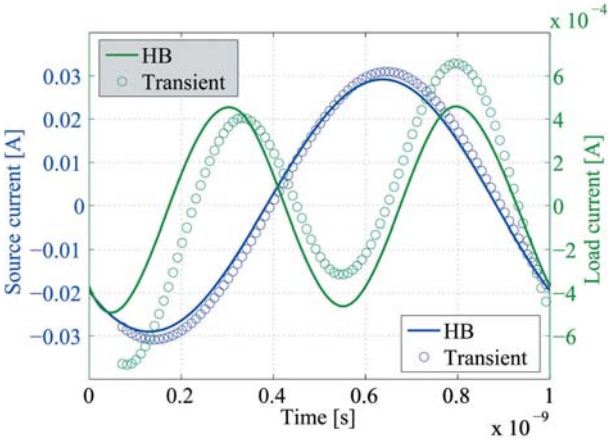
Personnel: Ivan Ruiz Gallego, Bernhard Schmithüsen

Funding: KTI-6378.1 LASSIS, Synopsis (ISE AG)

Partners: Synopsis (ISE AG)

The harmonic balance analysis (HB) is the standard steady-state analysis technique in circuit simulation for analysis, design and optimization of HF circuits operated under large-signal conditions. In circuit simulators semiconductor devices are taken into account by means of compact models. Even if such models are computationally efficient and allow very short design cycles, their significance concerning the analysis of physical phenomena leading to distortion is very limited. The recently implemented HB algorithm in the device simulator DESSIS (DESSIS-HB) together with its mixed-mode simulation capabilities allows the physics-based simulation of HF systems and can be used for device and circuit co-optimization of the nonlinear performance of large-signal circuits.

Both stand-alone devices and simple large-signal circuits have been analyzed with DESSIS-HB. The large-signal operation of a PN-diode, a 0.3 μm polysilicon emitter RF bipolar transistor and a 150 nm N-channel MOSFET have been successfully simulated. Additionally, to simple test circuits, a 1 GHz varactor-based harmonic frequency doubler and a bipolar small-signal amplifier have been simulated. Compact models have been extracted for the varactor and the RF bipolar transistor. The DESSIS-HB simulation results have been verified by comparison with physics-based transient analysis and HB circuit simulation.



Current through source and load of a 1 GHz varactor-based frequency doubler circuit. Comparison between DESSIS transient and DESSIS-HB.

From Process Technology to Statistical Circuit Simulation

Personnel: Luca Sponton, Yisuo Li;
Synopsys (ISE AG): Sathya Krishnamurthy, Gerhard Braun, Lars Bomholt

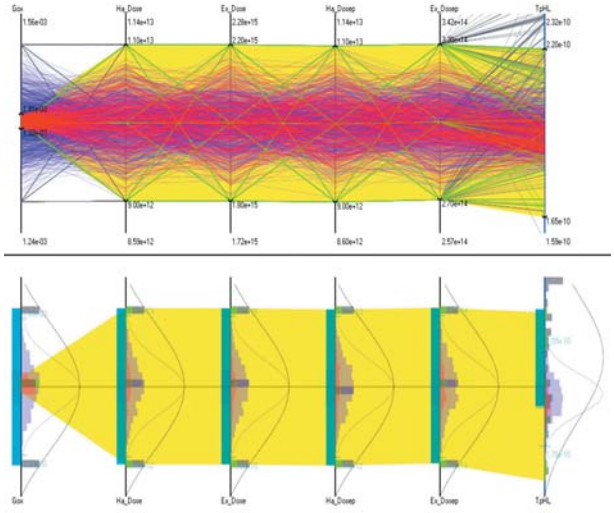
Funding: KTI 6650.2 PARA TCAD, Synopsys (ISE AG)

Partners: Synopsys (ISE AG)

In the increasingly important field of design-for-manufacturing (DFM), TCAD tools play an important role in giving an insight into the causes of variability of circuit performance and its dependencies. As process simulation is not affected by random effects, it can be used to explain the part of systematic yield problems that is becoming more important in the current and future technology nodes.

As part of a project between Synopsys and ETH, in this work the impact of several process parameters and lithography effects on circuits are investigated. Starting from screening experiments in order to determine the parameters having the most significance, an appropriate design of experiment (DOE) is then developed. TCAD process and device simulation, automated SPICE parameters extraction, and circuit simulation are used to build process compact models (PCMs), which are computationally inexpensive models obtained by regression analysis. Particular care is taken to avoid the introduction of non-physical effects to guarantee a reliable model.

These PCMs can be used for feed-forward analysis in order to correct run-time processes or to investigate variability sources (reverse analysis) beyond the possibilities of metrology.



Parallel coordinates plot of a model obtained from a 3 level full factorial DoE on 5 parameters of a 90nm CMOS process. The Response Surface Model (RSM) describes the fall time behaviour of a generic NAND cell with process variations.

Algorithmic DoE for High Dimensional Process Control Factor Space Modeling

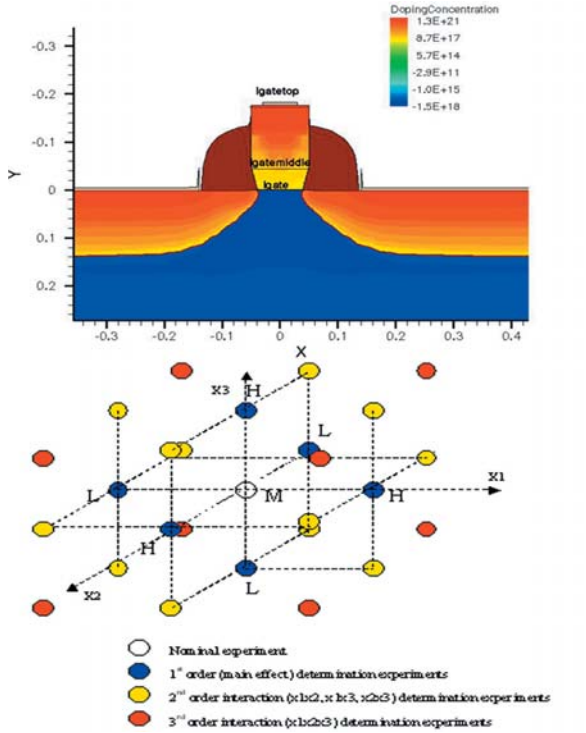
Personnel: Yisuo Li, Luca Sponton;
Synopsys (ISE AG): Sathya Krishnamurthy, Gerhard Braun, Lars Bomholt

Funding: KTI 6650.2 PARA TCAD, Synopsys (ISE AG)

Partners: Synopsys (ISE AG)

Due to the increase of complexity and the extreme scaling, modern semiconductor processes have more critical process control factors and noise factors than in the past. While simulation is an ideal tool to explore and characterize process variability steps and its impact on device performance, the TCAD simulations are very compute intensive. To understand and explorer variations of manufacturing process, simplified behavioral models called Process Compact Models (PCMs) are used. Such PCMs can have further use for process optimization, yield analysis and process control in semiconductor manufacturing.

PCMs are extracted by applying regression analysis to results from a systematic Design of Experiments (DoE). The exploration of a high-dimensional process factor space requires in principle design of experiments of factorial complexity, i.e., the effort grows extremely fast with a higher number of factors. We therefore investigate efficient ways of creating PCMs that cover all interesting effects such as nonlinearity and factor interaction, and yet keep the number of experiments small. Different methodologies for algorithmic DoEs are being studied, which implement methodologies to explore process factor space. An added advantage of simulation over experimental DoE methods is that the absence of external noise in simulation allows sequential strategies.



90nm CMOS process with 3 process control factors, lgatetop, lgatemiddle and lgate and its algorithmic DoE design illustration.

Optimized Parallel Incomplete LU-Factorizations for Shared-Memory Multiprocessors

Personnel: Stefan Röllin

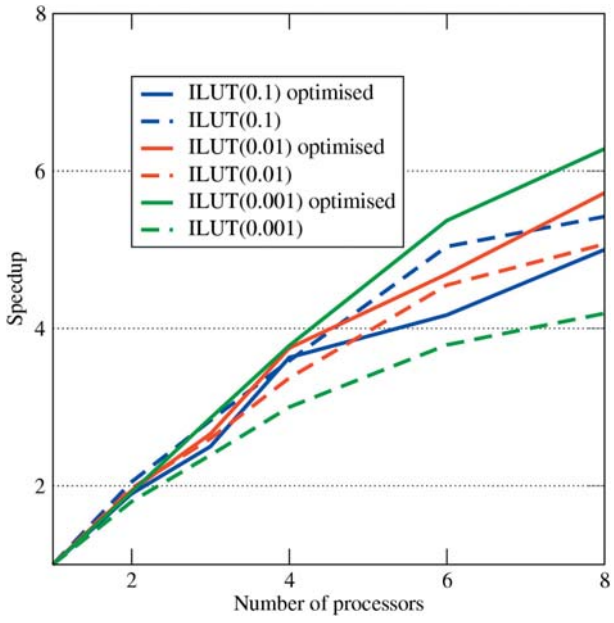
Funding: CSE-SEP ETHZ

Partners: Synopsys (ISE AG)

During a semiconductor device simulation a lot of large sparse linear systems have to be solved. The best choice for large 3D simulations to solve these linear systems are iterative solvers. The time and memory requirements are much smaller compared to direct methods. For example a simulation with about 320,000 unknowns requires about 12.5 GB of memory, whereas an iterative solver only needs 3.2 GB. Moreover, the simulation time is reduced by a factor of 6 compared to the direct solver.

The wall-clock time for the solution of the linear systems can further be reduced with the use of parallel computers. Most of the time in the iterative solver is spent for the computation of the preconditioner and the iterative method, e.g. BiCGStab. The existing parallel implementation for these parts gave satisfactory results, but there was room for improvements. An optimized version has therefore been implemented, which divides the computation of the Schur complement among the involved processors. As a drawback, one has to take into account slightly increased memory demands and a higher algorithmic complexity.

The realized implementation has been tested on several shared-memory multiprocessor architectures for different drop tolerances, i.e., parameters for the factorization. The results show that the performance of the optimized parallel incomplete ILUT factorization scales quite well. With eight processors, speedups up to 6.3 have been measured.



Speedups for the optimised incomplete ILUT factorization compared with an older implementation. The performance is significantly increased, especially with a small drop tolerance.

Maximum-Weighted Matching Strategies and the Application to Symmetric Indefinite Systems

Personnel: Stefan Röllin
Uni Basel: Olaf Schenk

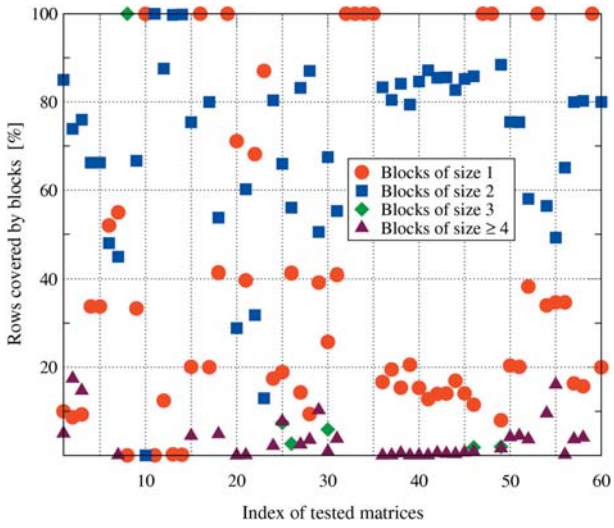
Funding: CSE-SEP ETHZ

Partners: Uni Basel

It is commonly known that maximum-weighted bipartite matching algorithms greatly enhance solvers for large sparse unsymmetric linear systems. The idea is to place large entries on the diagonal using unsymmetric permutations and scalings. One obtains a matrix that is better scaled and more diagonally dominant. This preprocessing has a beneficial impact on the accuracy of the linear solver. It also leads a reduction of the required pivoting steps during the factorization process.

These maximum-weighted matchings are also applicable to symmetric indefinite systems, but the symmetry of the indefinite systems is lost. However, the matching strategies can be adapted for these systems such that the symmetry of the matrix is preserved. Instead of permuting the large entries onto the diagonal, they are permuted to diagonal blocks with the help of a symmetric permutation. There are several possibilities to choose the sizes of these blocks. There is a trade-off between the accuracy and the fill-in. Large diagonal blocks result in more accurate factorizations, since there is more freedom for pivoting. However, the factorization is much more expensive regarding computational time than it is for smaller block sizes.

In this project, several strategies have been implemented for the direct solver PARDISO. They have been compared with the static Bunch and Kaufmann pivoting method. The results show that the novel strategies are very effective at the cost of a slightly higher factorization time.



Distribution of the natural sizes of the diagonal blocks for the tested matrices. Depending on the strategy, the diagonal blocks are split up into smaller pieces. Most of the blocks are of size one or two.

Computational Optoelectronics

Coordinator:

Bernd Witzigmann

3D Multimode Simulation of *DFB* Laser

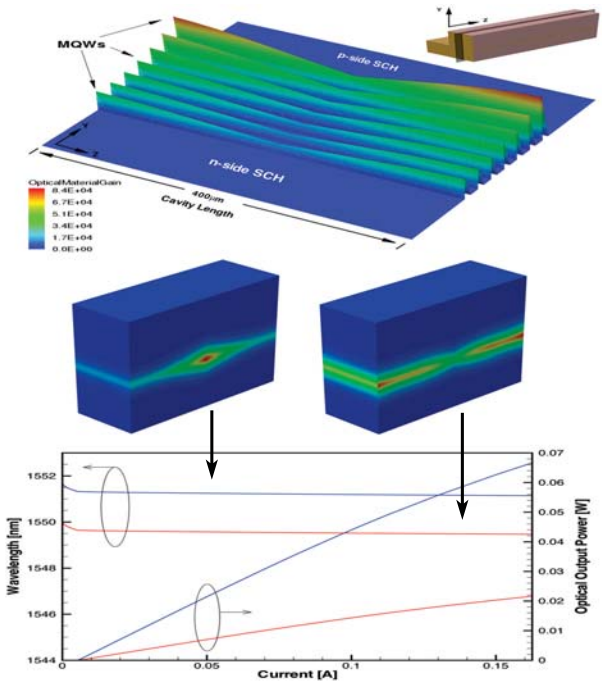
Personnel: Lutz Schneider

Funding: TOP NANO 21 5785.1 MQW, ISE AG

Partners: Synopsys (ISE AG)

In this project an antireflection coated ridge-waveguide *DFB* laser has been used as a benchmark structure for the implementation of a full 3D multimode device simulator.

DFB lasers with a phase shift in the center of the device are characterized by a strong peak of the fundamental mode. In order to analyze both transverse and longitudinal spatial hole burning effects 3D device simulation is indispensable. A longitudinal cut through the active region perpendicular to the quantum well plane displays two limiting factors for the output power: Accumulation of holes in the p-side quantum wells and longitudinal spatial hole burning. Since a high sidemode suppression ratio is critical for many *DFB* laser applications a robust and efficient multimode tracking feature has been implemented in the device simulator *DESSIS*.



Simulation Results. Top: Optical material gain profile obtained from transverse cut through device. Bottom: Wavelength and optical power vs. current characteristics for competing lasing modes along with mode profiles.

Wavelength Tuning Behavior of Sampled-Grating *DBR* Laser

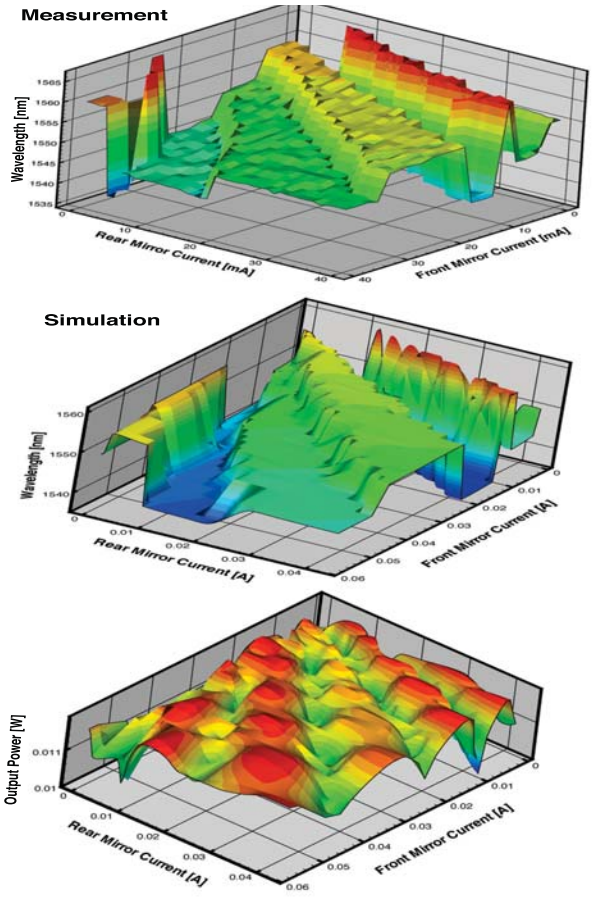
Personnel: Lutz Schneider

Funding: TOP NANO 21 5785.1 MQW, ISE AG

Partners: Synopsys (ISE AG), UCSB

Covering all the physical effects in widely-tunable sampled-grating *DBR* (*SGDBR*) lasers requires full 3D device simulation. In this project, the numerically challenging task of acquiring a wavelength tuning map through self-consistent electro-optical simulation has been mastered.

While tunable lasers such as *DFB* and three-section *DBR* lasers exhibit a smooth and continuous tuning behavior widely-tunable lasers with sampled gratings are known for their discontinuous wavelength jumps of up to more than 5 nm depending on the specific mirror design. A new approach had to be developed to deal with this particularity within the self-consistent device simulation framework. Comparison with experimental data shows very good agreement. Along with the fact that a typical tuning map can be simulated over night on a medium-size PC cluster the simulator proves to be an important tool for industrial device design.



Top: Measured wavelength tuning map. Center, Bottom: Simulated wavelength tuning map and variation of output power versus front and rear mirror tuning currents as obtained from 3D device simulation.

Spontaneous Emission From Single Quantum Dots in Microcavities

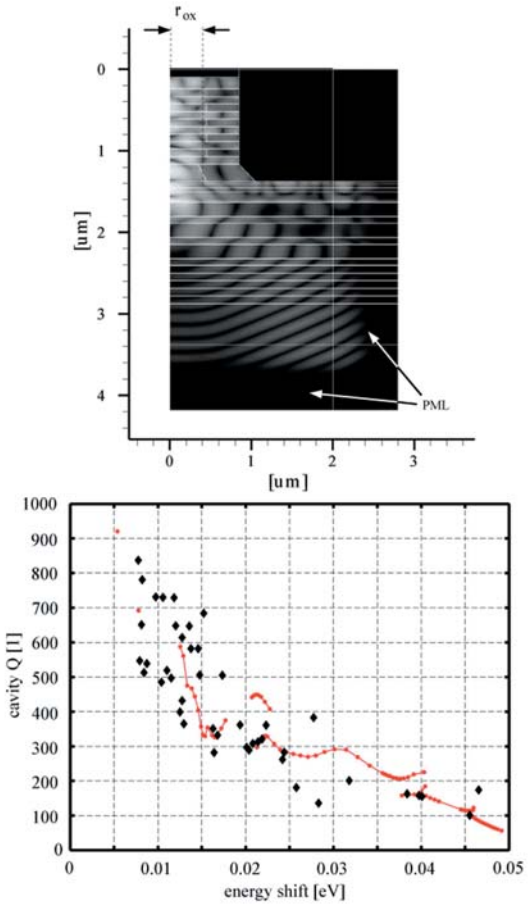
Personnel: Matthias Streiff;
EPFL: Carl Zinoni, Christelle Monat, Blandine Alloing, Andrea Fiore

Funding: ETHZ

Partners: EPFL

Advances in microfabrication techniques enable the construction of high quality semiconductor microcavities that can be used for solid-state cavity-quantum-electrodynamics (QED) experiments. Cavity QED phenomena may be used in the construction of high-efficiency light-emitting diodes, low-threshold lasers, and single-photon sources.

In this project the lumi2 optical mode solver software was employed to initially analyse and then design to specifications the spontaneous emission properties of quantum dots placed in optical, rotationally symmetric, resonant microcavities. The lumi2 simulator was first assessed with measured electroluminescence spectra. Subsequently, it was used to design an optical microcavity showing pronounced spontaneous emission enhancement for a narrow band source (Purcell effect).



Top: Oxide confined micropost cavity, absolute value of real part of HE11 type electric field is shown on logarithmic scale. Bottom: Simulation (red) versus measurement (black).

Analysis of Long-wavelength Vertical-Cavity Surface-Emitting Lasers

Personnel: A. Bäcker, S. Odermatt, M. Streiff; EPFL: M. Achtenhagen; BeamExpress: C. Berseth; Synopsys: A. Witzig

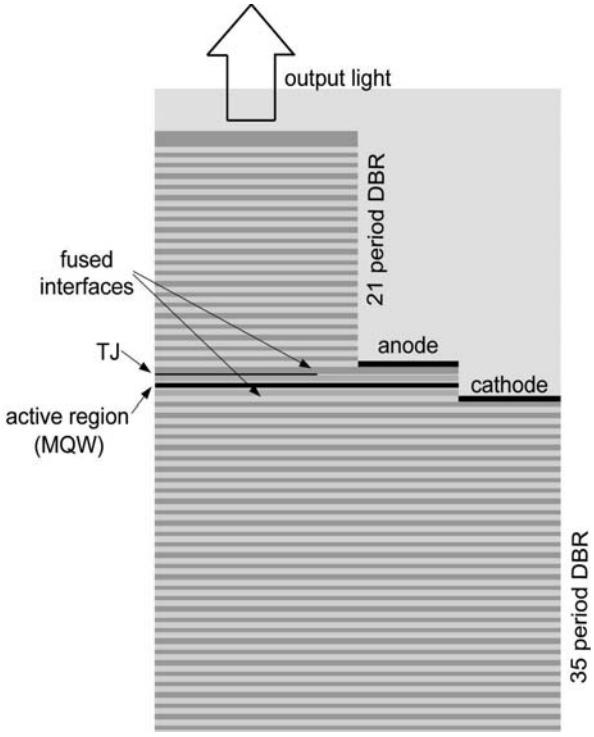
Funding: KTI 6941.2 VCSEL, Synopsys (ISE AG), Avalon

Partners: EPFL, BeamExpress, Synopsys (ISE AG)

Long-wavelength Vertical-Cavity Surface-Emitting Lasers (VCSELs) at 1310 nm and 1550 nm are a source for optical data communication. The IIS Computational Optoelectronics Group gained experience in short-wavelength VCSEL and preliminary work has been conducted in the long-wavelength regime.

Self-heating is a major challenge faced with long-wavelength VCSELs. Additionally, increased Auger recombination and carrier related optical losses pose fundamental problems. Hence, careful design is necessary which can be assisted by TCAD where electro-opto-thermal simulations enable the analysis and improvement of the VCSELs' performance.

As an example a top-emitting long-wavelength VCSEL structure is considered. It is formed by AlGaAs/GaAs distributed Bragg reflectors (DBRs) which are wafer-fused to both sides of the active cavity. The InP-based active cavity consists of a multi-quantum well (MQW) structure with intracavity contacts. The tunnel junction (TJ) leads to a substantially thinner p-type layer which results in higher efficiency as well as lower power consumption and lower threshold current.



Typical long-wavelength VCSEL device structure: Top and bottom distributed Bragg reflectors (DBRs), active region with multi-quantum well (MQW) structure, tunnel junction (TJ), intracavity contacts.

Simulation of Relative Intensity Noise in Laser Diodes

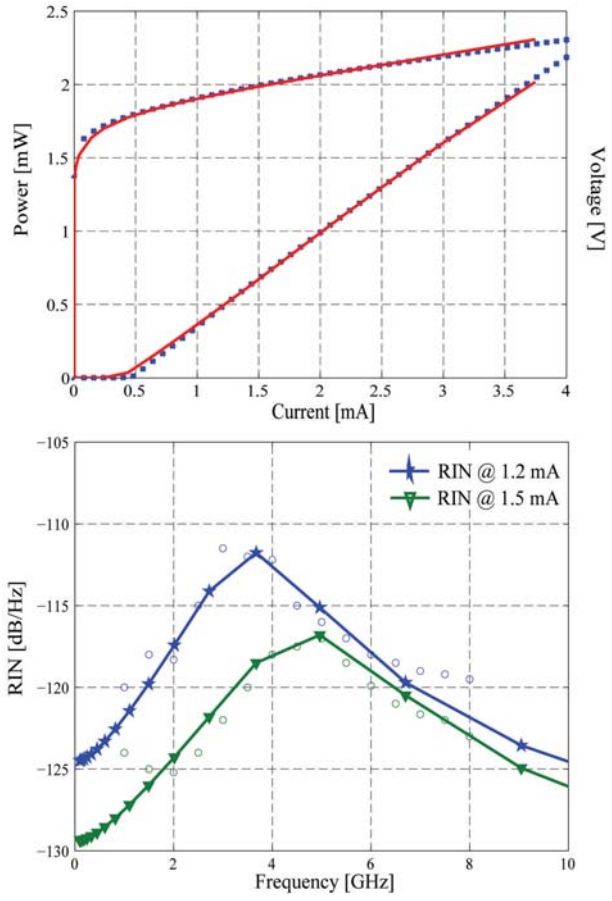
Personnel: Stefan Odermatt, Bernhard Schmithüsen; Avalon: Paul Royo

Funding: KTI 6941.2 VCSEL, Synopsys (ISE AG), Avalon

Partners: Avalon, Synopsys (ISE AG)

Relative intensity noise (RIN) is an important specification in high-speed optical communication and sensing systems. Noise in lasers is usually described theoretically by rate equations including Langevin noise sources that account for generation of the fluctuations. However, such analysis has been restricted to lumped rate equations. Design and optimization of optoelectronic communication systems require to minimize noise systematically.

In order to meet these requirements, a multidimensional physics-based RIN model has been developed and implemented into the device simulator DESSIS-Laser. The benefit of the model is twofold: First, it allows to investigate the noise properties that are important in datacom and sensing applications. Second, it allows to revise the static models since the models describe the behaviour only correctly if static and dynamic (noise) characteristics agree at the same time.



Top: Power-current and voltage-current characteristics of an VCSEL manufactured by Avalon Photonics (blue: measurements, red: simulation). Bottom: RIN at two different bias points (circles: measurements, solid: simulation).

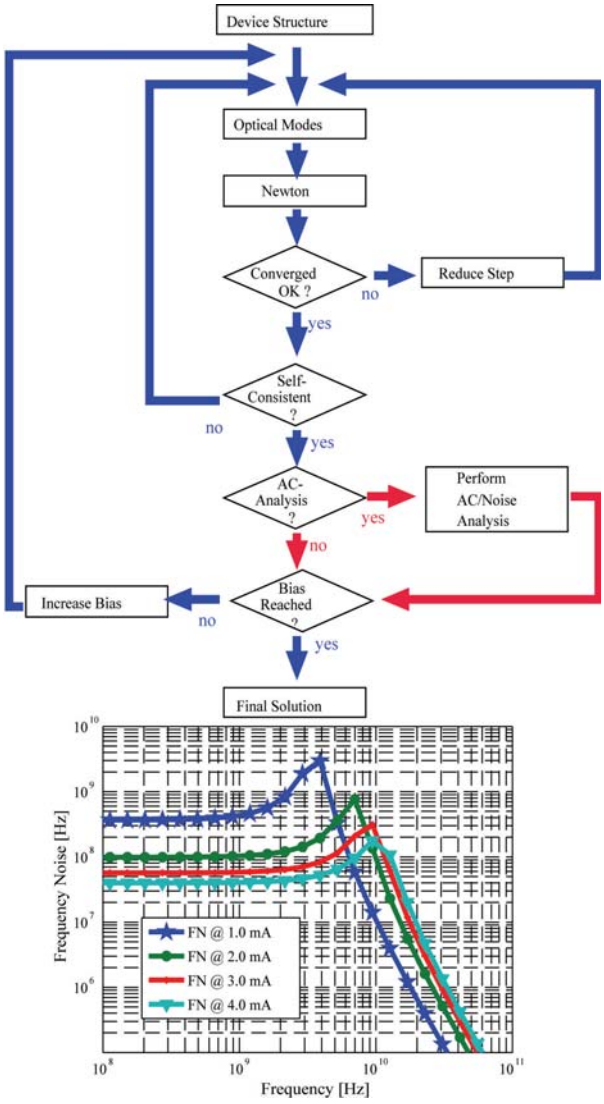
Simulation of Frequency Noise in Laser Diodes

Personnel: Stefan Odermatt, Bernhard Schmithüsen

Funding: KTI 6941.2 VCSEL, Synopsys (ISE AG), Avalon

Partners: Avalon, Synopsys (ISE AG)

In current and future data-com and sensing applications, very strong demands on the spectral purity of the signal source are made. This spectral purity in semiconductor lasers is characterized by frequency noise (FN). Since FN is caused by fluctuation in the photon phase, the multidimensional laser equations in the device simulator DESSIS-Laser have been completed by an equation for the photon phase of each mode. Noise is taken into account by spatially distributed Langevin forces and the correlation functions are described directly in the frequency domain assuming small signal noise source.



Top: Electro-opto-thermal simulation flow. After a self-consistent solution is achieved at a bias point, AC and noise analysis can be perfomed (red). Bottom: Simulated FN spectra for a VCSEL at different bias points.

Large Scale Eigenvalue Problems in Optoelectronic Semiconductor Lasers and Accelerator Cavities

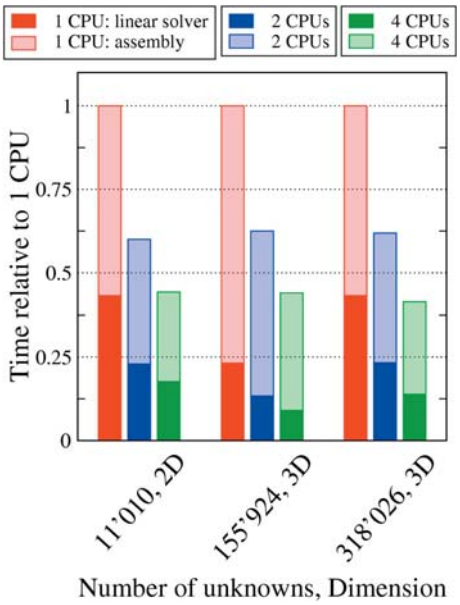
Personnel: S. Röllin, M. Streiff, B. Schmithüsen
IWR-ETHZ: P. Arbenz, M. Becka
Uni Basel: O. Schenk; PSI: H. Fitze

Funding: CSE-SEP ETHZ

Partners: IWR-ETHZ, Uni Basel, PSI

Solving large scale eigenvalue problems is a major task in the numerical simulation of optoelectronic semiconductor lasers, as well as of accelerator cavities. The discretization of the homogeneous Maxwell equations lead to generalized eigenvalue problems that have more than one million of unknowns and therefore are very challenging to treat. The Jacobi-Davidson eigensolver is used to solve these problems. In order to reduce the solution time, this method has been parallelised for distributed memory architectures. The most difficult part has been the parallelization of the two-level hierarchical preconditioner. The realized implementation shows very good speedups.

The solution of large sparse linear systems arising in the electronic part is another major computational part in a semiconductor laser simulation apart from the solution of the eigenvalue problems. The increasingly complex devices and the need to carry out 3D simulations lead to dozens of linear systems with more than 100,000 unknowns. Iterative solvers are the only viable solvers for these systems. In this part of the project, a fully parallel iterative solver has been implemented for shared memory architectures with the help of OpenMP. The numerical experiments on different architectures show that good speedups are achieved with a modest number of processors.



Wall-clock time for three different semiconductor simulations using different number of processors on a shared memory architecture. The times are scaled to the simulation with one processor.

Yield Improvement for Semiconductor Lasers Using Statistical Analysis

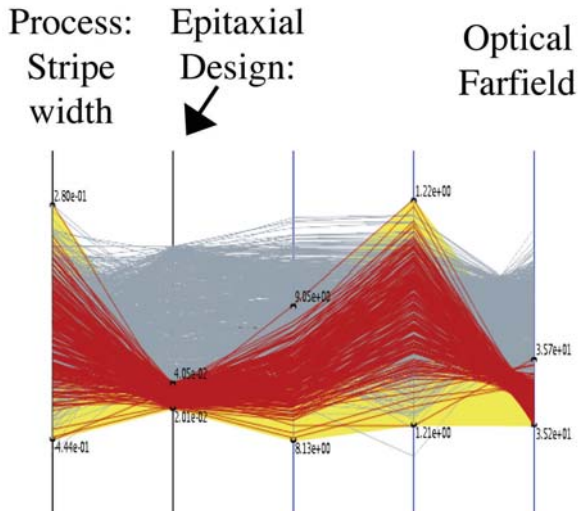
Personnel: Bernd Witzigmann, Valerio Laino,
Lutz Schneider;
Synopsys: Andreas Witzig

Partners: Synopsys (ISE AG)

Industrial semicondcutor laser design aims to find a specific design that meets the performance specifications. At least equally important, the design has to be manufacturable with high yield. Using capital intensive processing methods in the semiconductor industry, yield is a major factor for economic success. Therefore the device specifications of an ideal design should be immune against tolerances of the processing method. Predictive simulation tools for the process and the device performance can link process tolerances to specification tolerances, and with the aid of statistical tools, lead to a powerful TCAD design for manufacturing (DFM) methodology.

In this project, the goal is to demonstrate yield analysis by TCAD based DFM for semiconductor optoelectronics. As example, the terminal characteristics of a ridge waveguide laser are modeled using the microscopic device simulator DESSIS. The ridge etch process is modeled with the process simulator FLOOPS, and the statistical analysis is done in the GENESISe framework with the Process Explorer by Synopsys.

The picture illustrates how the laser stripe width tolerance due to the lithography and etching process causes a variation in the optical farfield. In order to keep the farfield narrow, a specific layer thickness in the epitaxial design is varied (which is a parameter with low tolerance). The red bands illustrate that for small layer thickness, the optical farfield parameter is kept small despite the stripe width variations introduced by the process. The right choice of layer thickness therefore results in substantial yield improvement, assuming a tight upper farfield boundary.



DFM analysis of a stripe width variation due to process tolerances. The grey band shows the total manifold of experiments, the red band shows the epitaxial design optimization reducing the farfield despite the stripe width tolerance.

Interfacing Gaintables with Drift-diffusion Model: The Finite Element Interpolator

Personnel: Valerio Laino

Funding: TOP NANO 21 5785.1 MQW, Synopsys (ISE AG)

Partners: Synopsys (ISE AG)

Accurate simulations of semiconductor laser characteristics require microscopic description of the mechanisms involved in the electron-hole radiative recombination (optical gain). GEBAS is a state-of-the-art simulator that describes optical gain with respect to carrier density, lattice temperature and photon energy, developed at our institute. Due to the complexity of the models used, up to 6 minutes are required to evaluate optical gain for a given condition, leading to unacceptable time requirements for an electro-opto-thermal coupled self consistent simulation.

The gaintable approach consists of evaluating the optical gain for a broad range of carrier densities, lattice temperatures and energies and store computed values in a table. Requests for the self-consistent solution of the device from the main electro-opto-thermal numerical simulator DESSIS, are satisfied interpolating available values of the optical gain.

We choose a finite element cubic interpolator, that combines ease of software implementation with great accuracy for both the interpolated value and the first derivative. In one dimension, finite element interpolation consists of the construction of a third order polynomial (basis function) and its evaluation for a given input. Polynomial coefficients are evaluated on points in the proximity of the requested value, for which the function is known. To ease the evaluation of the polynomial coefficients, the Lagrange polynomial has been chosen. Finite element formulation leads to an easy multidimensional extension.

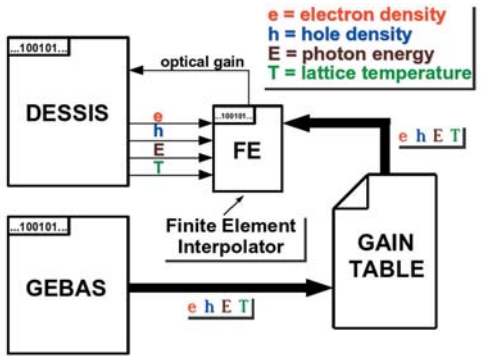


Illustration of the gaintable approach with the finite element interpolator.

Optimization of the Optical Emission Spectrum in Superluminescent LEDs

Personnel: Valerio Laino, Mathieu Luisier; Exalos: Lorenzo Occhi, Raffaele Rezzonico, Christian Velez

Funding: KTI 6429.1 SOA-SLED, Synopsys (ISE AG), Exalos

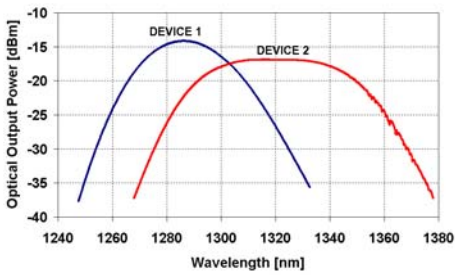
Partners: Exalos, Synopsys (ISE AG)

Superluminescent LEDs are manufactured by our partner Exalos for application including chromatic and polarization mode dispersion and passive component testing. The customer's requirement is to have broadband light sources covering a large range of wavelengths with high power densities. Our approach consists of using a multiple quantum-well edge-emitting Fabry-Perot semiconductor device. Each quantum well emits light at a wavelength defined by its thickness and material energy gap. Wells have different molefraction of the same semiconductor compound, to reduce manufacturing issues and lattice strain. Interaction between neighbor wells can be of two kinds: carrier capturing and cross photon absorption.

All wells share the same carrier reservoir due to the confinement structure. Further, photons generated by wells with higher energy gap can be absorbed by lower energy gap wells. Simulation of the carrier transport and capture has been used in order to fill all quantum wells with comparable carrier densities. Microscopic simulation of the optical gain has been used to evaluate the radiative recombination and the cross-well photon absorption.

These two effects can be partially balanced by proper device design. The compensation mechanism does not work for all polarization conditions, so that for lower driving currents the emission spectrum is shifted towards higher energy, while for high carrier densities the spectrum is dominated by the other wells.

This is at our knowledge the first known example where a microscopic simulation software has been successfully used to predictively evaluate optical properties of a semiconductor device. Measurement have confirmed simulations.



Comparison between measured emission spectra of the first (initial) and the second (optmized) SLED: the spectrum has doubled while the output power is almost unchanged.

Microscopic TCAD Modeling of Amplified Spontaneous Emission in Superluminescent LEDs

Personnel: Martin Loeser, Valerio Laino

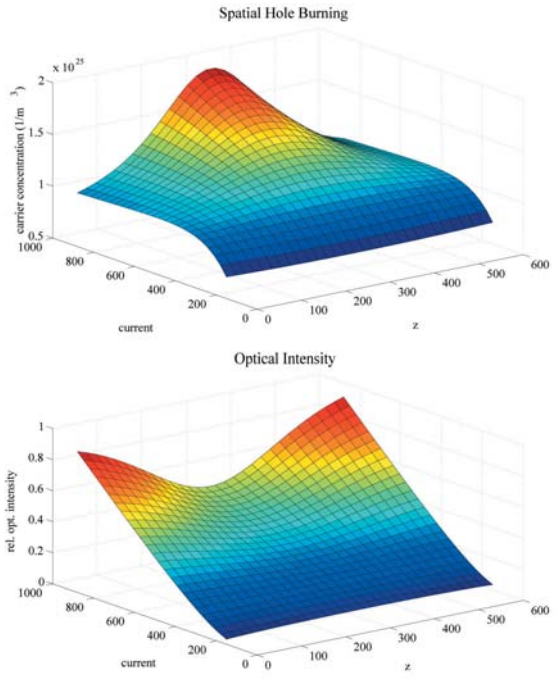
Funding: KTI 6429.1 SOA-SLED, Synopsys (ISE AG), Exalos

Partners: Exalos, Synopsys (ISE AG)

The recent years have seen a steady growth in the number of applications for both superluminescent light emitting diodes (SLEDs) and semiconductor optical amplifiers (SOAs). Applications range from test equipment to optical coherence tomography and optical sensors. The aim of this project is to provide a TCAD tool that allows to precisely predict the device's specific actions prior to processing. Thorough investigations based on predictive computer simulations can significantly accelerate the lengthy and cost intensive design process for novel devices. In detail this means that the extended simulation tool should provide the following features:

- Multi-dimensional (1D, 2D, 3D - depending on the problem) simulation
- Rigorous modeling of amplified spontaneous emission (ASE)
- Consideration of non-linear effects such as longitudinal spatial hole burning

The main challenges are to accurately describe ASE using the methods of quantum mechanics, and - based on these findings - develop and implement TCAD models that are computationally efficient. The simulation results obtained from these new models are then checked against experimental data provided by the industry partner Exalos.



The figure shows the impact of longitudinal spatial hole burning. The upper picture displays the carrier distribution, the lower curve shows the relative optical intensity.

Microscopic Gain Calculation and Comparison with Measurement

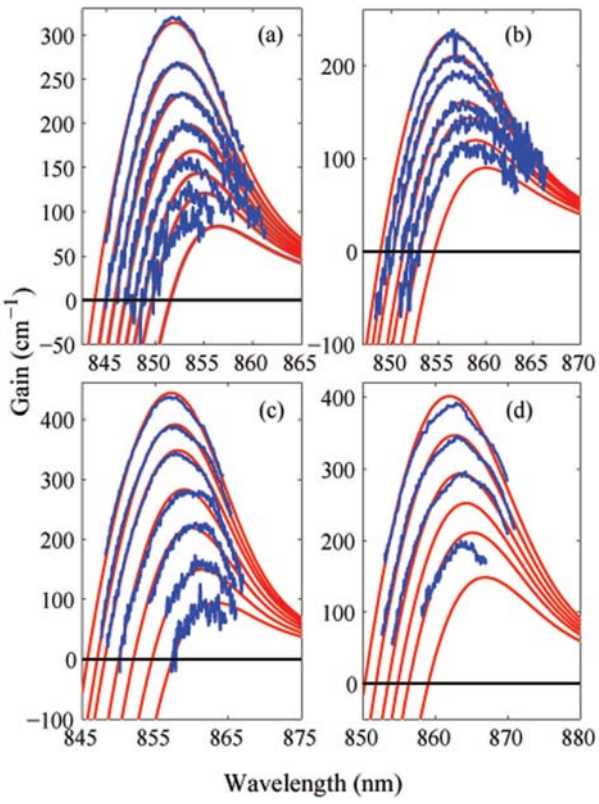
Personnel: Mathieu Luisier;
Avalon: Dominique Vez

Funding: KTI 6941.2 VCSEL, Synopsys (ISE AG), Avalon

Partners: Avalon, Synopsys (ISE AG)

The interest in simulating optoelectronics devices has considerably increased during the last few years, still requiring more accurate physical models like the optical gain of the active zone. With the Hakki-Paoli method gain spectra can be measured as function of the injected current and the ambient temperature but only below lasing threshold. However, for predictive simulations it is necessary to have an accurate gain model capable of matching measured gain curves and of extrapolating new ones for different current densities, temperatures, and designs.

The chosen gain model includes conduction-band nonparabolicity, valence-band mixing effects, Coulomb-induced intersubband coupling and correlation effects at the level of quantum kinetics. This leads to a homogeneously broadened gain, caused by carrier-carrier and carrier-phonon interactions. The variations of the quantum well thickness and material composition are taken into account via an inhomogeneous gain broadening.



Comparison between measured (blue) and calculated (red) gain curves for a GaAs-AlGaAs structure with three quantum wells as function of the carrier densities N, currents I, and temperature (a) 298 K (b) 313 K (c) 328 K (d) 343 K.

Single Mode Stability in Semiconductor Lasers: Effects of Temperature and Carrier Density

Personnel: Valerio Laino

Funding: KTI 6429.1 SOA-SLED, Synopsys (ISE AG), Avalon

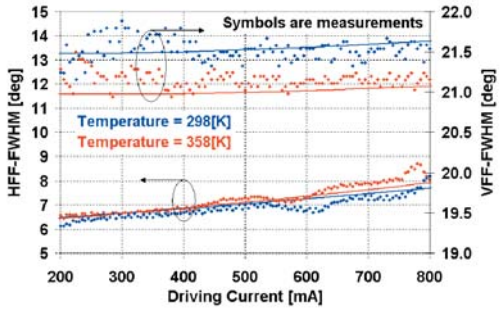
Partners: Bookham, Synopsys (ISE AG)

Single mode stability is a crucial requirement during the design of a single quantum well edge emitting semiconductor pump laser. To this purpose it is useful to observe modifications of the optical mode during device operation.

DESSIS-LASER evaluates the optical mode from the refractive index profile. Modifications to this are given by temperature and carrier density. Carrier effects on refractive index are related to band-filling and free carrier absorption. Bandgap shrinkage is included due to the many body effect. Changes in refractive index due to band filling are always negative and are particularly relevant in the active region during subthreshold regime, when the quantum well gets filled. Above threshold, induced changes are negligible due to the modest increase in carrier density. Free carrier absorption contributes to the refractive index always negatively. These effects are responsible for changes of the refractive index in the graded index carrier confinement structure (GRICC).

Refractive index temperature dependence is assumed linear; this effect is particularly important in the active region, just below the ridge, due to electron-hole recombination and Peltier effect. Temperature is maximum in the active region below the ridge and this induces a local increase of the refractive index.

All mentioned effects can be made compensating each other by proper device design, leading to an almost stable refractive index vertical profile at different driving currents. This can be experimentally evaluated by vertical far field measurements at different ambient temperatures.



Comparison between measured and simulated vertical (VFF) and horizontal (HFF) far-field full width half maximum (FWHM) for different ambient temperatures, with increasing driving current.

OptoLab Construction

Personnel: Matthias Streiff, Hansjörg Gisler, Fritz Illien, Anja Böhm

Funding: ETHZ, IfE-ETHZ, IFH-ETHZ, IIS-ETHZ

Partners: IfE-ETHZ, IFH-ETHZ

The development of predictive, physics-based simulation models requires accurate material and device characterization data. They support the determination of model parameters and serve as critical benchmark in TCAD model research.

In semiconductor optoelectronics, a wide variety of compound materials and device concepts are employed, and only consistent sets of both optical and electronic data for the specific device configuration allows for the development of state-of-the-art TCAD software.

The Optoelectronic Characterization Laboratory (OptoLab) is a joint effort of three institutes: Integrated Systems Laboratory, Electronics Laboratory, Electromagnetic Fields and Microwave Electronics Laboratory at the Department of Information Technology and Electrical Engineering. The purpose of the OptoLab is to provide all common setups for standard optoelectronics measurements of today, and to be able to develop novel measurement techniques as required by the three participating institutes.

As of end 2004, various DC and AC electro-optical measurements vertical cavity sufrace emitting lasers and PIN-photodiodes have been performed. Furthermore, a web-based administration tool has been established in order to schedule the inter-institutional use of the lab space and equipment efficiently.

Equipment of the new OptoLab.

Physical Characterization

Coordinators:

Wolfgang Fichtner
Mauro Ciappa
Dölf Aemmer

2D Dopant Profiling on 4H Silicon Carbide P⁺N Junction by Scanning Capacitance and Electron Microscopy

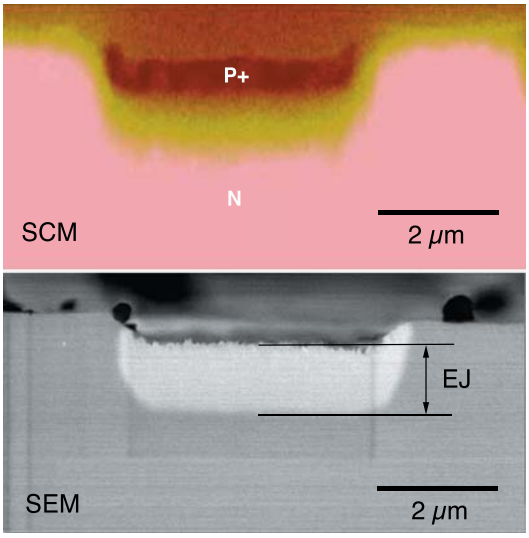
Personnel: Marco Buzzo, Mauro Ciappa

Funding: Infineon, BBW, EU-IST-2004-506844 SINANO

Partners: Infineon, SINANO Consortium

Silicon Carbide (SiC) is presently among the most promising semiconductors for power device applications due to its high operating temperature, high breakdown voltage and dynamic behavior. The availability of reliable dopant profiles is of key importance for both development and failure analysis of new devices. The common electrical dopant profiling techniques are not always suitable for this material due to its extreme physical properties. Scanning Capacitance Microscopy (SCM) is one of the leading techniques for 2D dopant profiling on silicon, however only few studies are reported on SiC. SCM measurements on SiC cross-sections are not straightforward. Due to its hardness, the conventional microsectioning techniques are inadequate to obtain a smooth surface. Furthermore, the slow oxidation kinetic leads to uncertainties when trying to grow a sufficiently thick and stable insulator layer as required by SCM.

In this project the suitability of the native oxide to play the role of the insulator in the metal-oxide-semiconductor structure underneath the SCM technique is investigated. The 2D dopant profile of a p⁺n-junction measured by SCM is compared with Scanning Electron Microscopy (SEM) potential contrast maps, demonstrating that SEM is as a powerful tool for quantitative junction delineation in SiC cross-sections, since it provides adequate contrast between differently doped regions.



SCM (top) and SEM potential (bottom) maps of a p⁺ well implanted in n-type substrate. The electrical junction (EJ) can be easily delineated in the SEM map.

2D Dopant Profiles of Proton Implanted High-Voltage Superjunction

Personnel: Marco Buzzo, Mauro Ciappa

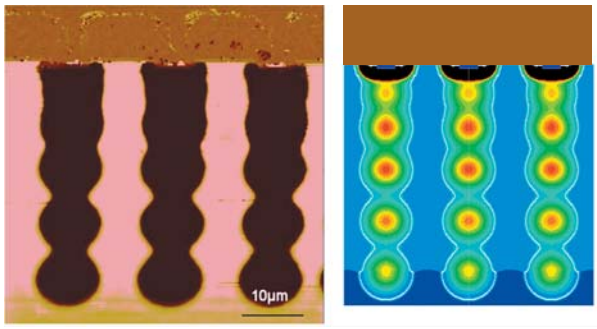
Funding: Infineon, BBW, EU-IST-2004-506844 SINANO

Partners: Infineon, SINANO Consortium

600 volt superjunction (SJ) transistors have been designed to reduce the on-state resistance by a factor of 10 compared to the state of the art power MOSFETs. The device concept relies on the charge compensation in the drift region of the transistor. The vertical n-type doping is increased and counterbalanced by the implementation of structured pillar-like columns of the opposite doping type. In blocking mode the full voltage sustaining capability is maintained, whereas in conducting mode the increased n-type doping results in extremely low on-resistances. The latest improvement of the SJ technology is based on the concept of proton implantation. Point defects created by hydrogen ion implantation in silicon are known to form hydrogen-related defect complexes. These complexes act as n-type donors and can be used to replace elementary n-type donors like phosphorous.

In this project an undoped wafer has been suitably masked and implanted to form p-type columns. The SJ device has been realized by a set of unmasked hydrogen implantations with a range of energies from a few hundred keV up to two MeV.

For the development and optimization of SJ devices it is crucial to access the distribution of the implanted species and their activated ratio after the annealing process. Secondary Ions Mass Spectroscopy is hindered by the low concentration of implanted Hydrogen. Furthermore, the ratio of activated hydrogen is low compared to total number of implanted hydrogen atoms. For the first time, 2D doping profiles have been measured by Scanning Capacitance Microscopy (SCM) and compared with process simulations results.



SCM image (left) of a standard SJ device showing the p-column (dark) into the n-type silicon (bright). The process simulation shows the corresponding isodoping curves for the vertical columns (right).

Thermal Transient Effects during Transmission Line Pulses

Personnel: Chiara Corvasce, Davide Barlini, Fridolin Illien, Mauro Ciappa

Funding: BBW, EU-IST-2000-30033 DEMAND

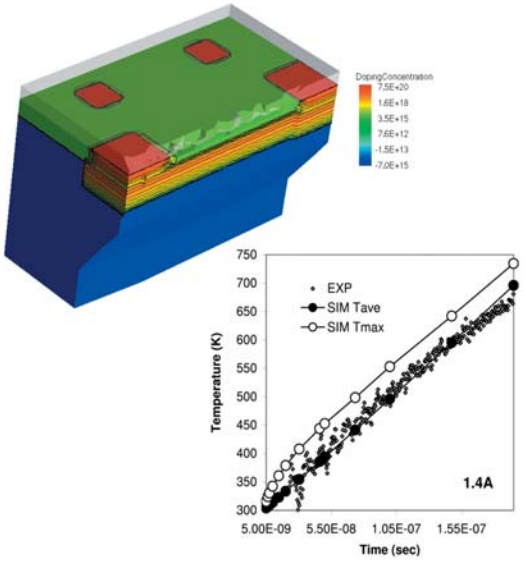
Partners: Infineon, TU Wien

The knowledge of the internal thermal behaviour of semiconductors is fundamental to estimate the robustness and to optimize the design of power devices and ESD protections, for which, due to the high current rating and/or the high blocking voltage, thermal effects are the main failure cause.

An experimental procedure is proposed here, which bases on the analysis of the time-dependency of the voltage drop across integrated silicon resistors when submitted to constant current Transmission Line Pulses (TLP).

As a consequence of the device self-heating the mobility degradation causes an increase of the resistance during the pulse that can be related to the average temperature on the condition to know the thermal regime within the device active area.

For this purpose electro-thermal transient 3D simulations have been performed that allowed the development of a phenomenological adiabatic-like model able to provide the estimation of the resistor temperature averaged over a volume of the active area from the instantaneous experimental resistance readings.



Section of the three dimensional model of a buried Kelvin resistor and example of the resistance conversion in temperature readings for 1.4A pulse.

Carrier Mobility in Silicon up to 1000 K

Personnel: Chiara Corvasce, Davide Barlini, Fridolin Illien, Mauro Ciappa

Funding: BBW, EU-IST-2000-30033 DEMAND

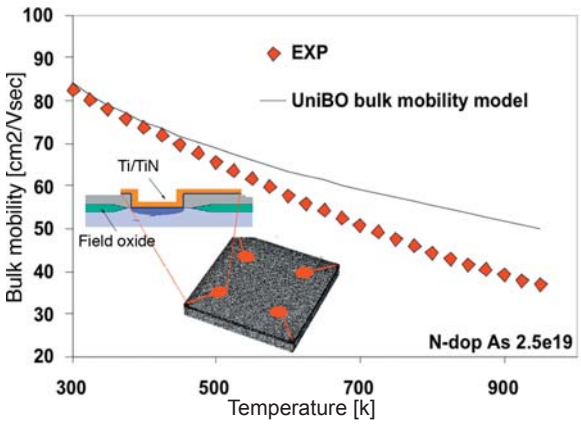
Partners: Infineon, Uni Bologna

The development of an integrated methodology to design devices with enhanced robustness by combining electrical measurements and TCAD simulations requires the experimental investigation of the device physics up to 1000 K and the model calibration over this temperature range that has never been explored before.

From the electrical measurements side the major problems to overcome are related to the high temperatures at which the physical parameters have to be extracted. The traditional approaches for silicon conductivity and mobility extraction make use of Van der Pauw (VdP) junction isolated resistors with standard Al metalization that are globally heated to high temperatures using an oven. Unfortunately two strong limitations arise: the parasitic effect related to the thermal carrier generation at the junction and the maximum operating temperature of the standard metallization stack that have been both demonstrated from the authors to fix the maximum operating temperature around 800 K.

In this work we have focused on the design of a new metalization scheme realized on a junction isolation free test structure. A single level Ti/TiN metalization has been demonstrated to operate reliably up to 1000 K in conjunction with bulk silicon samples of 3,000 μm x 3,000μm x 300 μm size. A traditional Hall-measurement system has beenmodified in order to achieve 1000 K in a temperature-controlled environment with a Hall voltage sensitivity of 10 μV at an inductance of 1 Tesla.

This enabled the extraction of the resistivity and mobility in a wide doping range up to 1000 K and the calibration of the bulk mobility model.



Bulk mobility as predicted by the Bologna model (solid line) and experimental data (dots) for a 2.5 10^{19} cm^{-3} As sample. The insert shows the layout of the bulk VdP sample and a detail of the Ti/TiN contact pads.

Design and Modeling of Accurate Test Structure for Hall Measurements

Personnel: Chiara Corvasce, Davide Barlini, Mauro Ciappa

Funding: BBW, EU-IST-2000-30033 DEMAND

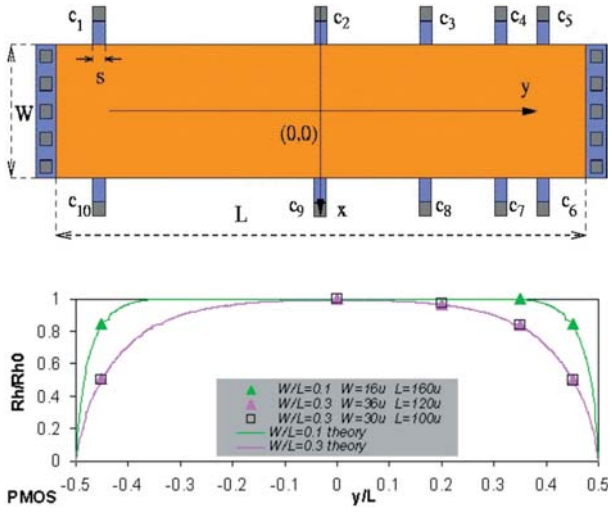
Partners: Uni Bologna, Infineon

The extraction of physical parameters as carrier conductivity and mobility is typically carried out using measuring schemes based on the Hall effect. The constraints set by the elementary Hall theory onto the samples (very small aspect ratio and extremely thin Hall probes at the sample midpoint) are not necessarily met by the structures available for this type of measurements. This introduces systematic errors in the extracted parameters.

An analytical model of the Hall problem on devices like resistors and MOSFETs has been developed at University of Bologna that led to the determination of the Hall voltage as a function of the position along the y axis in the devices under test with no constraints on the W/L ratio or probe position.

In order to validate the model, a new set of devices were designed with multiple Hall sensing contacts along the y direction. A full set of measurements was carried out on n- and p-MOSFETs realized with different W/L. The experimental data and the predictions of the analytical model are in excellent agreement. The collected data prove the capability of the model to provide a correction factor to eliminate the systematic measurement errors due to the sample geometry.

The measurements performed according to the proper procedure has demonstrated that the surface mobility models presently used in simulators require a new calibration that involves a correction in the range of 40%.



Top view of the transistor with multiple Hall sensing contacts along the channel (top). Experimental validation (dots) of the analytical model (solid lines), which predicts the normalized decrease of the sensed Hall voltage as a fuction of the normalized sensing location y (bottom).

Imaging of Silicon Devices Scanning Spreading Resistance Microscopy

Personnel: Maria Stangoni, Mauro Ciappa

Funding: BBW, EU-RTN-00031 HERCULAS, EU-IST-2004-506844 SINANO

Partners: HERCULAS Consortium, SINANO Consortium

The measure of IC features like the channel length of a transistor is one of the main application of the Scanning Spreading Resistance Microscopy (SSRM). Already successfully characterized with Scanning Capacitance Microscopy (SCM), a MOS transistor has been measured with SSRM. With this technique it is possible to measure a two-dimensional resistance map of the cross-sectioned device and to relate it to the dopant concentration.

A dedicated test structure has been designed both to simplify the sample microsectioning process and the quantification of the acquired data. It consists in a lateral MOS transistor with a channel width of 640 μm and a channel length of about 1.5 μm. Source, drain, gate, and substrate are contacted by pads located at the bottom side of the chip.

Since the measurement has been carried out with all terminals shortcircuited, during the sample preparation all pads have been coated by a conductive silver paint, sputtered with gold, and finally contacted to the sample holder with a conductive epoxy glue.

The measurement has been performed with the use of diamond coated probes, especially produced for SSRM, which requires very stiff cantilevers due to the high pressures needed by the technique.

The resulted colormap is related to high resistance values where the color is dark and to lower resistance values where the color is light. Nevertheless, the interpretation of the image is not straightforward, since SSRM does not discriminate between different doping types.

Furthermore, the dependence of the local resistance upon different bias conditions, produces a contrast that is not related with the same proportion to the doping concentration. Moreover, the measured resistance values strongly depends on the applied tip pressure.

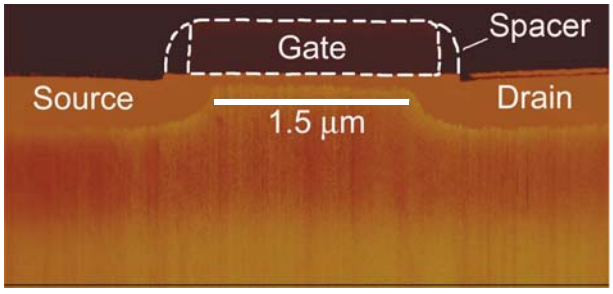


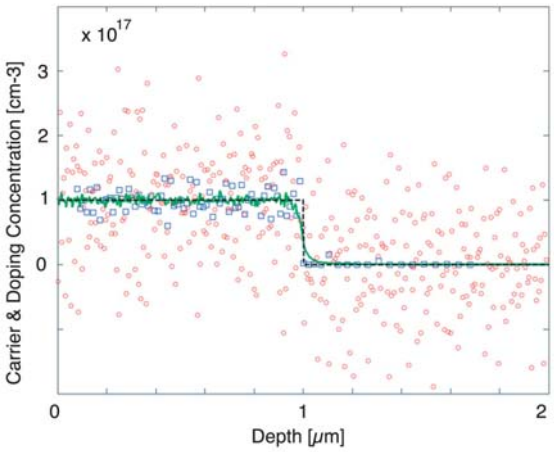
Image of the MOS transistor referring to a horizontal scanning size of 4.85 μm, acquired under a load defined by a deflection setpoint of 6 V and at a tip bias of 500 mV.

Solution of the Reverse Modeling Problem by Artificial Neural Networks

Personnel: Mauro Ciappa, Maria Stangoni

Funding: BBW, EU-RTN-00031 HERCULAS, EU-IST-2004-506844 SINANO

In the practical use of Scanning Spreading Resistance Microscopy (SCM) and Spreading Resistance Microscopy (SSRM), several problems arise when trying to establish an unique correlation between the mapped electrical property (capacitance or resistivity) and the doping concentration at a given sample location, since both techniques provide the local concentration of the carriers, rather than the impurity profile. If the doping density varies slowly over a scale comparable to the local Debye length, the carrier density is a reasonably good measure of the activated doping density. According to this principle, tools for the direct conversion of the measured data have been proposed in recent years by the ETH and the NIST. With the occurrence of abrupt profiles as it is the case for ultra-shallow junctions, this approximation is no longer accurate. A procedure based on Artificial Neural Networks (ANN) has been developed to convert the carrier profile, measured both by SCM and SSRM, to the real doping distribution (IMP). A two-layered feed forward network (11 inputs) has been used with a sigmoid transfer function in the hidden layer (70 hidden units) and with linear transfer functions in the output layer. The proposed ANN has been trained by a set of 2500 sequences computed by DESSIS-ISE. A data sampling strategy has been developed on the base of the local Debye length to take into account the carrier diffusion length in presence of steep doping gradients. ANNs have been proven to be an efficient solution to solve both the DMP and the IMP. ANNs provide superior performances than the common analytical methods, especially for the conversion of noisy data.



Solution of the IMP by the ANN (blue squares) and by an usual analytical technique (red circles) for a carrier profile (green line) with a signal-to-noise ratio of 26 dB, generated from a doping step (black dashed line).

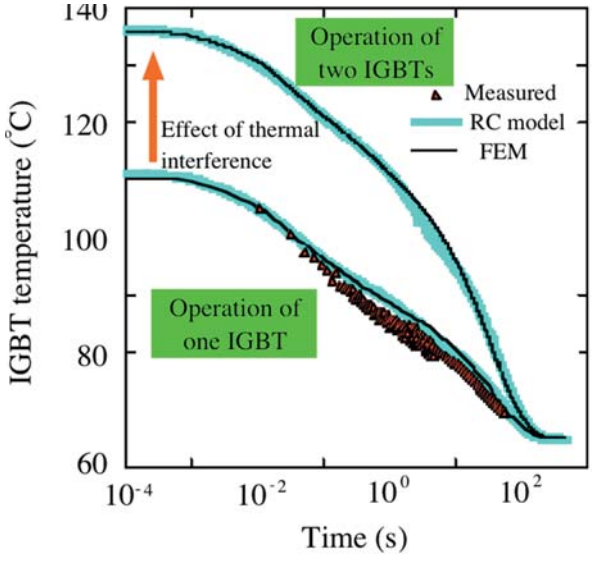
Thermal Modeling of Power IGBT Modules for Automotive Traction

Personnel: Mauro Ciappa;
Toyota: Takashi Kojima, Yasushi Yamada

Funding: Toyota

Partners: Toyota

Due to the high degree of integration and to the hostile operating environment encountered in automotive traction applications, new electro-thermal simulation tools are required to improve the accuracy of the prediction of the instantaneous temperature in IGBT power modules. On one side, conventional approaches based on circuit simulators have shown important limitations as the difficulty to implement temperature-dependent device parameters and the insufficient accuracy in predicting the transient behavior of complex automotive power modules by simple network models. On the other side, though transient thermal simulations based on the Finite Element Method (FEM) can provide accurate results, they find very limited applications in the automotive field due to the long computational time required to simulate realistic application profiles of vehicles. A novel method has been proposed to extract accurate electro-thermal compact models of IGBT power modules for automotive applications. This new technique combines the accuracy of the FEM approach with the fast computational performances of circuit simulators. Furthermore, a simple parameter definition method for power device models has been introduced, which enables the dynamic adaptation of the device characteristics. In particular, this method provides an excellent tool to investigate issues as the temperature non-homogeneity in parallel-connected devices caused either by mismatches in their electrical characteristics or by uneven heat dissipation.



Calculated vs. measured (dots) step response of the thermal system without (lower curve) and with thermal interference (upper curve). The power loss at the steady-state (before turn-off) is 93.7 W.

Assessing the Performance of 2D Dopant Profiling Techniques

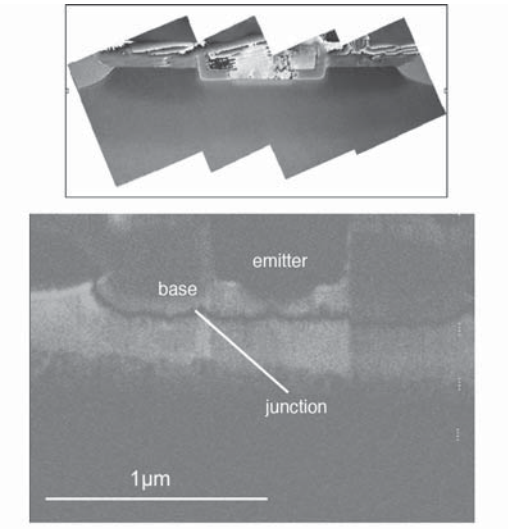
Personnel: Mauro Ciappa, Maria Stangoni

Funding: BBW, EU-RTN-00031 HERCULAS, EU-IST-2004-506844 SINANO

Partners: HERCULAS Consortium, SINANO Consortium

During the past several years different techniques have emerged for two-dimensional dopant and carrier profiling for Si and other advanced materials. However, until now no technique has been available which can fulfill all the requirements in terms of spatial resolution, reproducibility, and quantification as proposed by the ITRS Roadmap. Within the framework of a European project HERCULAS focused on the improvement of 2D-profiling tools, an extensive comparison was set up between nine European laboratories with different 2D-profiling methods SSRM, SCM, KPFM, electron holography, and SEM. Each of these techniques have demonstarted its own weak and strong points. By exchanging dedicated samples this cooperation intended to study and improve the performance level of the different profiling techniques and bring them closer to industrial requirements limits.

All the techniques succeeded in measuring the p- and n-type calibration samples. SCM required proper biasing of the tip to obtain a monotonic behavior. This is also an important issue for junction delineation. Both SCM and SSRM are sensitive to the whole dynamic range between 5 10^{14} and 2 10^{19} atoms/cm^3. KPFM in UHV and SEM have more problems related to the sample surface quality. Electron holography was not able to resolve doping levels lower than 10^{18} atoms/cm^3. SCM and SSRM behave similarly while imaging a bipolar structure. The accuracy of the quantitative delineation of the electrical junction in pn-junctions by SCM and SSRM has been demonstrated to be prone to the presence of surface states and fixed charges.



The same emitter-base junction of a bipolar transistor imaged by electron holography (top, IHP) and by Scanning Capacitance Microscopy (bottom, ETH).

Comparison of Boron Diffusion in SiGe and SiGeC by Scanning Capacitance Microscopy

Personnel: Hidehiko Yabuhara, Mauro Ciappa

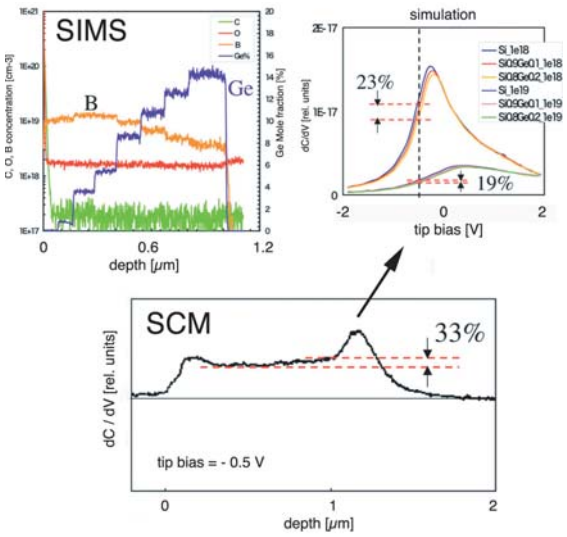
Funding: Toshiba, BBW, EU-IST-2004-506844 SINANO

Partners: Toshiba

SiGe and SiGeC are attractive materials for high-speed electric devices such as hetero-bipolar transistors. For higher performance of these devices, it is important to control the boron distribution in SiGe(C) layers. Secondary ion mass spectrometry (SIMS) is usually adopted for measurement of doping distribution. However it has a matrix effect in the case of SiGe and SiGeC, and some other methods have been expected.

Scanning capacitance microscopy (SCM) has been applied to estimate the diffusion of the boron in SiGe and SiGeC layers and also to delineate abrupt pn junction in SiGe. In applying SCM to SiGe(C), the SCM output signal intensity is expected to change with different Ge Mole fraction. This effect has been estimated by using device simulation and compared with the experimental data measured by SIMS. The simulation results reveal that the SCM signal intensity depends not only on the Ge Mole fraction, but also on the dc bias voltages in the SCM measurement.

Finally, based on the SCM measurement, B diffusion in SiGe and SiGeC has been compared and the controllability of B diffusion with SiGeC has been estimated.



SIMS profile of the SiGe test sample with the Ge Mole fraction modulated along the depth (top left), SCM profile of the test sample showing a signal dependence on the Ge Mole fraction modulation (bottom). Optimization of the SCM working point (tip bias) by device simulation for optimum contrast (top right).

Three Dimensional Effects in Flash Memory Cells

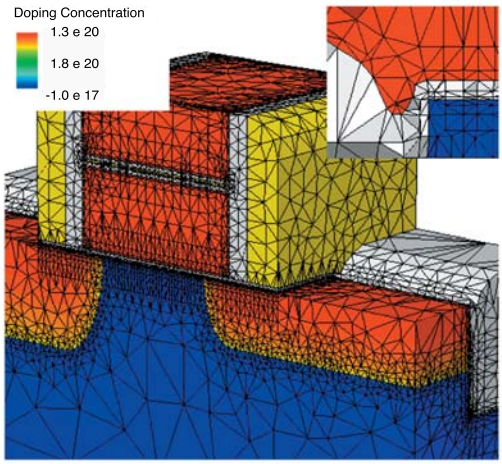
Personnel: Yves Saad, Mauro Ciappa;
Synopsys: Paul Pfäffli, Clement Tavernier

Funding: Synopsys (ISE AG)

Partners: Synopsys (ISE AG),
ST Microelectronics

The evolution of nonvolatile memories toward higher levels of integration is mainly based on decreasing the cell size, optimizing the geometry of the layer system, and introducing new materials. To meet these new technology requirements, more advanced Technology CAD (TCAD) simulations tools based on realistic and accurate models are needed, to take into account the relevant increase of three-dimensional (3D) effects. Since accurate results are needed in the design of flash memory to evaluate the program and erase speed, several methods and models have been proposed to extract the capacitance coupling ratios and to deduce precise electrical characteristics based either on simple dc measurement or 2D simulations.

In this project, we demonstrated the use of appropriate 3D TCAD tools for process emulation and device simulation applied to floating-gate structures taking into consideration of process-induced geometry effects. The floating gate to control gate capacitance of representative structures is extracted by full 3D simulation, with particular attention to effects related to the sidewall oxide, the spacer, and the bending radius of the polysilicon edges. The proposed methodology is assessed and compared with methods currently used in the industry. The impact of the overetch on the erase operation have been investigated in 3D by varying the depth of the overetch. All simulations are performed by an state-of-the-art device simulation tool, a 3D process emulator, and a mesh generator that generates boundary-conforming meshes, allowing for high resolution descriptions of the complex geometry.



Three-dimensional half-structure of a flash memory cell discretized with the mesh generator NOFFSET3D. The insert shows the penetration of the gate polysilicon into the trench isolation.

Identifying Operation Modes of Diode Strings for ESD Protection

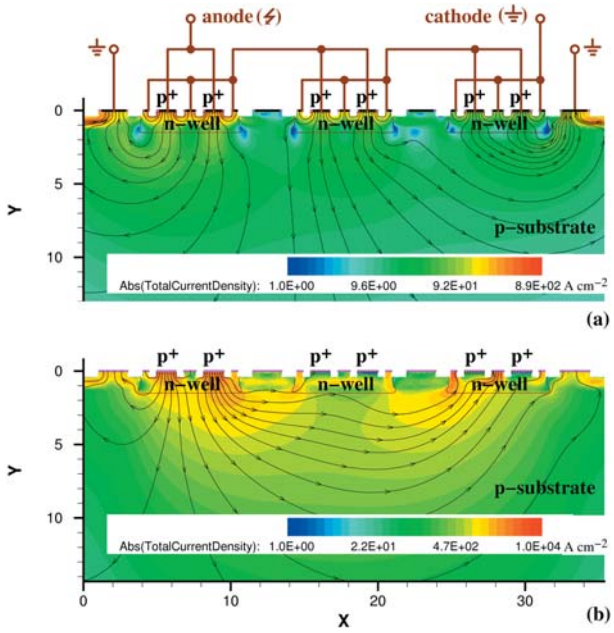
Personnel: Ulrich Glaser

Funding: ETHZ, Infineon

Partners: Infineon

In modern deep submicron technologies, the devices may reveal different operation modes due to the impact of inherent parasitic devices. TCAD device simulations enable the study of such devices including all relevant parasitic devices. The identification of the different operation modes as well as the discrimination between and the weighting of the pure device behaviour and parasitic device effects lead to a better understanding of the internal device physics and thereby to methods for device optimization.

The purpose of this work was such an investigation for a string of three p^+/n-well diodes under ESD conditions. The diodes are connected as depicted in the upper part of picture (a). Only the substrate contacts on the left and on the right of the diode string are grounded. The anode is stressed positively compared to the grounded cathode. In part (a), the diode string conducts current via the p^+/n-well diodes and the parasitic p^+/n-well/p-substrate transistors. In part (b), a parasitic SCR (thyristor) operation mode appears at higher currents. The main current flows now directly from the diode on the left side to the cathode on the right side via the p-substrate. Finally, the clamping voltage of the diode string was successfully reduced by analysing and optimising the impact of the parasitic devices.



Total current density showing two distinct operation modes in an example string of three p^+/n-well diodes. An extended description of the figures is given in the text.

Determining 'Charged Device Model' ESD Robustness of ICs with Circuit Simulation

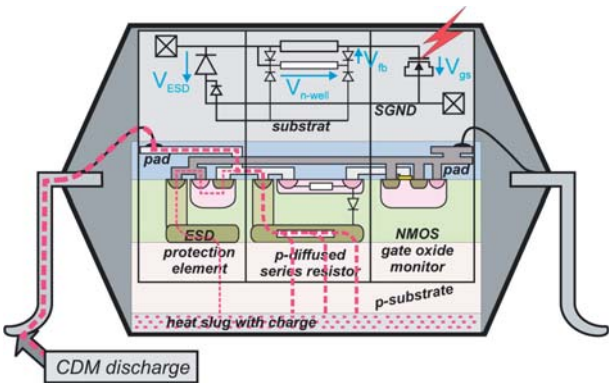
Personnel: Melanie Etherton
Bosch: Wolfgang Wilkening

Funding: Bosch, MEDEA+ T102 ASDESE

Partners: Bosch

Failures in Integrated Circuits (ICs) caused by Charged Device Model (CDM) Electrostatic Discharge (ESD) stress are an important reliability issue. Due to technology scaling and increased automated handling, a high quantity of today's field returns are due to damages caused by CDM ESD. Some research works deal with the ability to determine the behavior of ICs during CDM discharges with circuit simulation to discover and correct weak circuit elements and increase product reliability. However, accurate simulation of CDM events is challenging, since parasitic inductive and capacitive elements as well as parasitic devices and discharge paths play an important role.

In this project, the influence of parasitic elements on the behavior of ICs during a CDM discharge was studied. It was demonstrated that parasitic discharge paths have a significant influence on the circuit behavior. The observed failure mechanism of an ESD input protection in a 0.8 µm smart power technology was mainly attributed to CDM currents through substrate and parasitic devices. With consideration of these factors meaningful conclusions could be achieved for the failure mechanism and the CDM robustness of the input structure. The applicability of circuit simulation for determining CDM failure mechanisms and CDM failure levels, when an accurate simulation setup is used, was demonstrated.



CDM failure mechanism of the smart power input structure. A high amount of the charge that is stored in the heat slug of the package discharges through the substrate and the n-well of the p-diffused resistor into the discharge pin. The resulting high voltage across the n-well of the resistor causes a high voltage drop across the gate oxide monitor [$V_{gs} = V_{ESD} - V_{n\text{-}well} - V_{diode,forward\ bias}$], which exceeds the time dependent dielectric breakdown voltage and as a consequence, oxide rupture occurs. With a simulation setup including compact models for the CDM tester, the current dependent arc resistance, the RF package and bond wire parasitics and the input structure circuit elements with parasites, this failure mechanism could be demonstrated with circuit simulation.

Bio-Electromagnetics and Electromagnetic Compatibility

Coordinator:

Niels Kuster
(Adjunct Professor, Department of Information Technology and Electrical Engineering)

Automated Mesh Generation For Highly Complex CAD Models Used In Conformal FDTD

Personnel: Stefan Benkler,
IT'IS: Nicolas Chavannes, Niels Kuster,
SPEAG: Emilio Cherubini

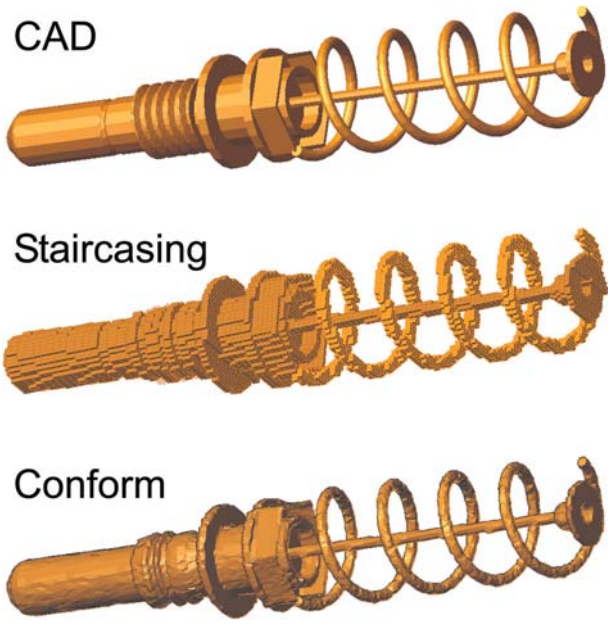
Funding: KTI 6757.2 NMS-NM TRINITY

Partners: IT'IS, SPEAG

The Finite-Difference Time-Domain (FDTD) method originally presented by Yee has become the most widely used technique in electromagnetic computations. However, the classical staircasing approach may lead to significant uncertainties for grid non-conformally aligned structures. An effective way to reduce staircasing errors is the incorporation of locally conformal meshes, e.g., sub-cells in which modifications in the original Yee scheme need only be applied to cells in the immediate vicinity of the structure's material interfaces.

The basis of all these sub-cell models is a detailed, robust and versatile discretization of the CAD simulation environment, which is addressed within this study. The surface triangle mesh of the CAD object is discretized with computer graphics methods (scan conversion algorithm). The result is a description of the environment to simulate in which each voxel knows its material and its possible cut-planes of the material transitions.

Implemented into the SEMCAD simulation environment, the developed techniques were applied and validated to different largely inhomogeneous, complex 3D configurations, e.g., CAD models of cars, mobile phones, each consisting of several hundred distinguished sub-parts. The techniques have proven to be suitable for the generation of locally conformal 3D FDTD grids for real-world geometries without any limitations to complexity.



Detailed wire of a commercial mobile phone antenna modeled in SEMCAD. The difference between staircasing and conform discretization is visualized.

Performance Analysis of Conformal FDTD Schemes

Personnel: Stefan Benkler,
IT'IS: Nicolas Chavannes, Niels Kuster

Funding: KTI 6757.2 NMS-NM TRINITY

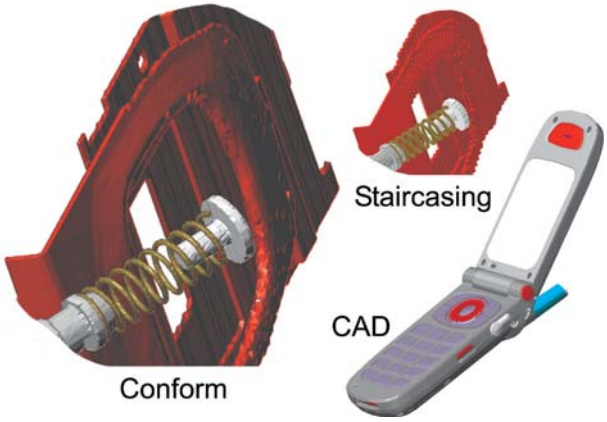
Partners: IT'IS

The Finite-Difference Time-Domain (FDTD, Yee 1966) is one of the most successfully used technique in electromagnetic (EM) computations. Whereas, a well known shortcoming is that the staircasing meshing can lead to inaccuracies in the geometrical discretization of complex models. This shortcoming can be overcome by using conformal meshing and a locally modified Yee update scheme. The modification is only applied to cells, which are near material interfaces.

However, key issues such as the robustness of the conformal mesher (see left column) and stability of the modified Yee scheme need to be addressed in order to allow application of the schemes within, e.g., commercial EM simulation environments and general R&D purposes.

The main advantage of such subcell models is that a coarser but conformal mesh produces the same accuracy than a fine but staircasing mesh. The saving in memory consumption (less cells) and simulation time (larger time step due to the stability criteria) is remarkable.

In the framework of this investigation, incorporating the conformal mesher to subsequently assess the performance of various schemes, different averaging functions (arithmetic, harmonic, others) and weights (line, area, volume) are compared to each other for dielectric material transitions. The SEMCAD simulation environment acted as a basis for implementation and application. For PEC surfaces contour path based subcell models were validated and compared to each other (stability, complexity, accuracy).



Flip phone: the secondary PCB (see detail images) is not aligned with the computational grid and therefore the staircasing errors are not neglectable (SEMCAD environment).

Simulation, Design and Optimization of Integrated Transmitters for Wireless Communications

Personnel: Stefan Benkler,
IT'IS: Nicolas Chavannes, Niels Kuster,
SPEAG: Peter Futter

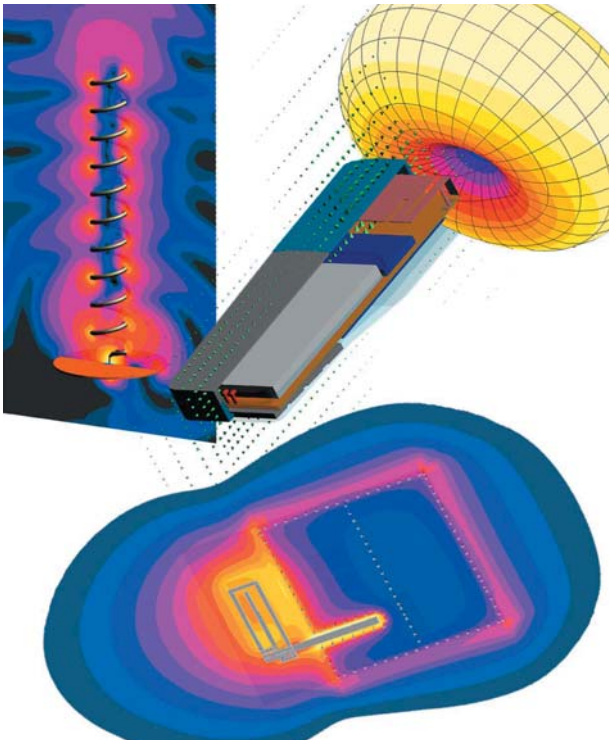
Funding: KTI 6757.2 NMS-NM TRINITY

Partners: IT'IS, SPEAG

Whereas just a few years ago the main focus of mobile communication was on pure transmission of audiophonic signals, today's devices incorporate a multifunctional application range covering, in addition to speech transmission, personal services such as internet access and connection capabilities with contiguous accessoires. This widened functionality is coupled with multi-band integration for single devices, e.g., combined quad band phones and PDAs featuring Bluetooth and WLAN protocols.

Within the framework of the project TRINITY the numerical simulation platform SEMCAD is enhanced with a variety of new solver engines and features which should finally enable to import and process complex transmitter CAD datasets without the need for substantial simplifications.

The range of developed features was subsequently applied for the analysis and optimization of different real-world transmitter structures, in particular to integrated antennas used in wireless communications, e.g., a folded monopole antenna of a only 4.5 x 25 x 6 mm extension. Furthermore, the simulation results were compared to data obtained from experimental evaluations whereas excellent agreement was obtained for all performance parameters examined.



Near- and far-field distributions of different transimitter types which were investigated (helix, patch, folded monopole) and processed in SEMCAD.

Development of a Fast 3-D OGL Rendering Engine for Modeling and Visualization of Scientific Data

Personnel: Stefan Benkler,
IT'IS: Nicolas Chavannes, Niels Kuster,
SPEAG: Emilio Cherubini, Hans-U. Gerber

Funding: KTI 6757.2 NMS-NM TRINITY

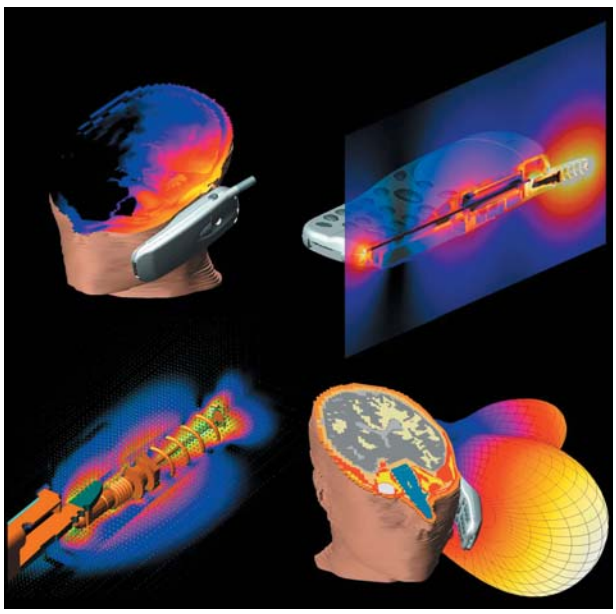
Partners: IT'IS, SPEAG

The project TRINITY aims at the modeling and electromagnetic (EM) simulation of highly complex setups resulting from direct 1:1 import and processing of CAD datasets. Regarding the handling of CAD data consisting of 1,000 or more distinguished sub-parts as well as large results computed on 64-bit systems, fast and robust visualization algorithms embedded within effective GUIs are a crucial parameter.

Therefore, a new OpenGL based rendering engine has been developed for the fast visualization of complex CAD models and the visualization of scientific 3D data. OpenGL is used as a low-level layer to access the graphics hardware. Since its introduction in 1992, OpenGL has become the industry's most widely used and supported 2D and 3D graphics application programming interface (API).

The incorporation of the latest features with respect to modern graphics devices allows fast processing and visualization of very detailed visual models including post-processed field distributions and CAD models. Furthermore, an optimized data-structure has been developed in order to minimize the geometric pre-processing of the visual data and to improve the speed of data transfer to the graphics hardware.

The range of new algorithms was finally implemented into the EM simulation platform SEMCAD.



3D OpenGL based visualization of CAD and result data within SEMCAD. The developed algorithms allow the fast processing of several 1,000 CAD parts including overlaid EM field data (SAR / EM plot, vectors, radiation pattern).

Derivation of UPML-FDTD Boundary Conditions for Intersecting Lossy Dielectric Media

Personnel: Chenghao Yuan
IT'IS: Nicolas Chavannes, Niels Kuster,
SPEAG: Harald Songoro

Funding: KTI 6757.2 NMS-NM TRINITY

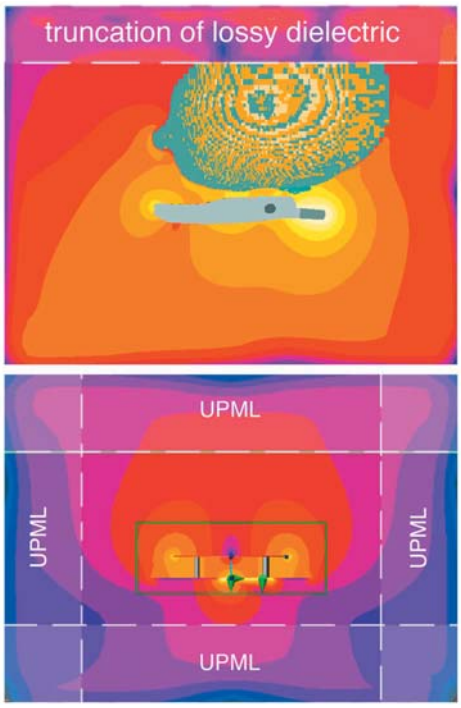
Partners: IT'IS, SPEAG

The Alternating Direction Implicit Finite-Difference Time-Domain method for Maxwell's equations (ADI-FDTD) is an approximation of the Crank-Nichoslon time integration scheme (CN) applied to a spatial discretization on the Yee grid. The ADI-FDTD factorization retains the unconditional stability and the global 2nd order accuracy of CN while leading to a lower computational cost and thus making it attractive.

Like in the common FDTD scheme, the computational domain must be truncated with highly efficient and flexible Absorbing Boundary Conditions (ABCs) in order to minimize both memory usage and run-time.

Within the framework of the project TRINITY, this motivation has lead to the derivation of Uni-axial Perfectly Matched Layer (UPML) ABC for ADI-FDTD including support for the truncation of lossy dielectric media which is encountered in a wide range of electromagnetic applications. All implementations have been performed within the simulation platform SEMCAD.

In addition, the calculation of the parameters of the UPML layers (conductivity of first layer, conductivity profile, number of layers) which are of great importance to realize the full potential of the ABC type, has been automated based on user-defined strength parameter for the ABC.



Application of UPML ABC within ADI-FDTD (SEMCAD): truncation of the computation domain by intersection of lossy dielectrics (head-phone, microstrip).

Development of Novel Source and Excitation Models for the ADI-FDTD Method

Personnel: Chenghao Yuan
IT'IS: Nicolas Chavannes, Niels Kuster,
SPEAG: Harald Songoro

Funding: KTI 6757.2 NMS-NM TRINITY

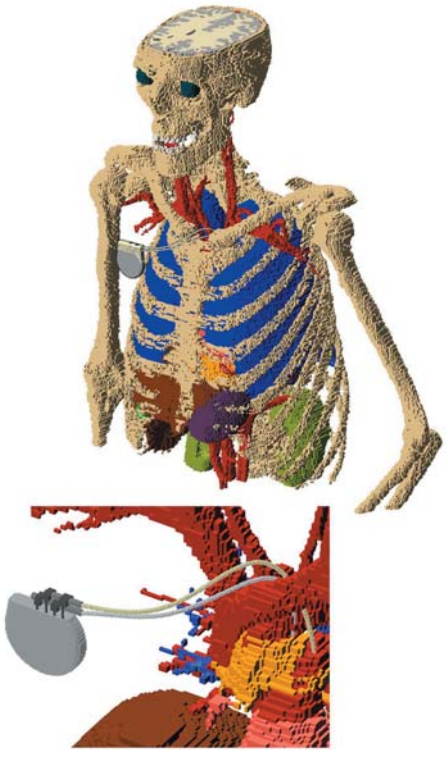
Partners: IT'IS, SPEAG

Within this investigation, an ADI-FDTD solver supporting UPML for conductive media has been integrated into a 3D CAD FDTD simulation platform (SEMCAD) enabling the simulation of complex setups for which ADI-FDTD can provide performance advantages over FDTD. This is the case for electrically over-discretized models, for instance due to the presence of very fine geometrical details or because of the need to operate at frequencies relatively low for the overall spatial discretization.

Real-world simulations in particular require the modeling of lumped elements (R, L, C components) together with voltage, current and plane wave excitations.

These models had to be included into the ADI-FDTD formulation with great care in order to maintain its unconditional stability and to fit the non physical nature of the ADI splitting into two substeps.

Subsequently, the performance of ADI-FDTD was assessed for industry driven applications targeting simulations various radiating devices with very fine geometrical features including pacemakers, hearing aids, mobile phones etc. - in interaction with anatomical numerical phantoms.



ADI-FDTD - typical application (SEMCAD): spatially over-discretized modeling of a pacemaker within a human body (resolutions < 0.1 mm at f = 400 MHz).

A Fast and Robust 2.5-D FDTD Based Method for the Solution of General Waveguide Structures

Personnel: Chenghao Yuan
IT'IS: Nicolas Chavannes, Niels Kuster

Funding: KTI 6757.2 NMS-NM TRINITY

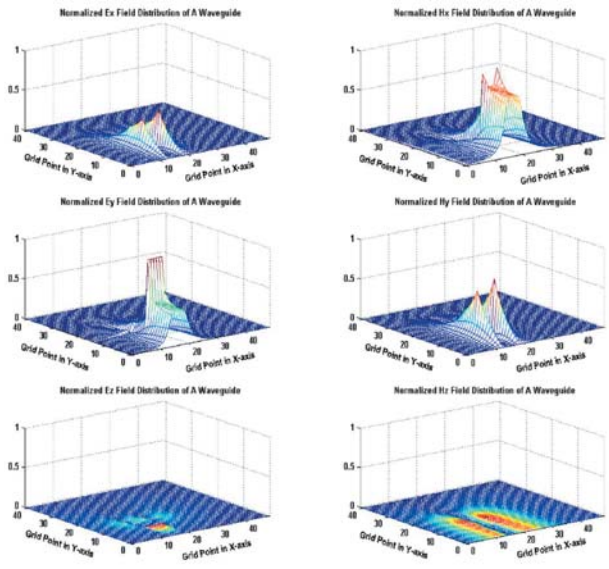
Partners: IT'IS

Numerical simulation applied to electromagnetics (EM) has become a popular technique to support RF engineers in the design process for a variety of devices. In particular the Finite-Difference Time-Domain (FDTD) technique has gained increasing interest due to the straight forward and computationally effective approach. Applied to wave-guiding structures like microwave circuits, the computation of the S-parameter frequency response provides an accurate and complete description of the system performance.

In the framework of this project, the development and implementation of a numerical Eigen-solver for computationally extracting Scattering-wave Parameters was targeted. The emphasis was put on a robust and fast solution for arbitrary shaped Micro/Millimeter-wave structures, embedded within the simulation enviroment SEMCAD.

The realized method is based on a 2.5D FDTD scheme which substitutes the phase constant for the spatial derivative in propagation direction. All six Yee field components are still involved (2.5D), providing a major benefit for full-wave analysis of, e.g., TE and TM modes. Furthermore, Uniaxial PML ABC have been derived.

Incorporating the proposed schemes, the method of Mode-Template S-parameter extraction provided excellent performance for solving a wide range of problems with respect to accuracy and speed, including closed and open structures, irregular shaped ports as well as inhomogeneous media.



Low-pass microstrip filter operating at 10 GHz: 2.5D UPML FDTD simulation of the mode template subsequently used for the full-wave 3D simulation (E, H, component wise visualization).

Active Optical Sensor for Field Measurement in Time and Frequency Domain

Personnel: Peter Müller;
IT'IS: Axel Kramer;
SPEAG: Fin Bomholt

Funding: KTI 7146.2 NMPP-NM TDS, IT'IS, SPEAG

Partners: IT'IS, SPEAG

This project covers the development of a prototype sensor for electromagnetic field measurements in complex environments. The sensor targets RF exposure assessment, EMI analysis, medical diagnostics and therapy. Its small size guarantees high spatial resolution to cover near-field problems. Minimal disturbance of the fields is realized by complete electrical isolation of the sensor head.

A small exclusively optically linked sensor was developed to measure magnetic fields in the frequency range between 100 MHz and 10 GHz. The system consists of a sensor head and a remote unit. The sensor head is optically powered by a laser illuminating a photovoltaic converter. A loop antenna is employed to detect the magnetic field. The detected signal modulates a chip laser (VCSEL), whose signal is transferred to the remote unit by an optical fiber.

The challenges of this project are size reduction, power consumption minimization and suppression of unwanted fields.

Two different generations of setups have been prepared and tested. The latest sensor head revision has an approx. 3.4 mm outer diameter, approx. 75 dB dynamic range and 0.09 mA/m minimum detectable H-field (at 2.45 GHz) with respect to 1 MHz bandwidth.

Sensor Head, loop diameter: 3.4 mm.

Multi-Sensor Scanning Setup for Measurement of Non-Uniform RF Fields

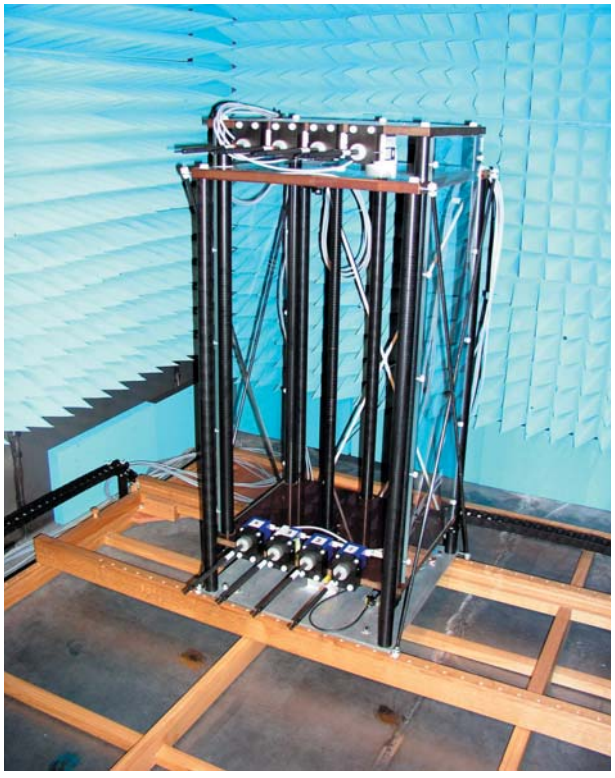
Personnel: Walter Oesch
IT'IS: Axel Kramer, Niels Kuster

Funding: FNM, TDC

Partners: IT'IS

This project focuses on the development of a setup for accurate and systematic measurement of non-uniform field distributions, e.g., appearing inside buildings due to base station radiation. Comparison of measurements gained with this setup with current exposure assessment methodologies will provide the scientific basis for the development of adapted and improved compliance test protocols.

Our measurement setup consists of a tower holding 8 miniature field probes; a linear array of 4 probes are placed on two platforms, respectively. The platforms are one upon the other and separated by one meter. A high precision motor drives the platforms in vertical direction with a positioning resolution of 1-3 mm. Lateral positioning is done by moving the tower on a wooden rail system. The whole measurement procedure and data acquisition is software-controlled. It allows 1-, 2- and 3-dimensional field mapping with data point spacing of 5 cm. First experimental evaluations of the system suggest that the tower motion and probe electronics change the field pattern in the room, implying field deviations of 20-30%. Future tasks involve the improvement of the mechanical construction of the tower including consideration of a different arrangement of the probes.



Multi-Sensor tower setup in semi-anechoic chamber.

Development of a Measurement Procedure for Compliance Testing at Higher Frequencies (5 - 6 GHz)

Personnel: Neviana Nikoloski
IT'IS: Niels Kuster, Andreas Christ
SPEAG: Katja Pokovic, Dominik Schmid

Funding: SARSYS BWP

Partners: SARSYS Consortium, MMF, SPEAG

New frequency bands have been opened up for wireless local networks. Since these devices may operate in the immediate vicinity of the human body, it is required that they be tested for compliance with safety standards for electromagnetic radiation. Current compliance testing protocols only support a frequency range of up to 3 GHz. Due to the strong field gradients at frequencies between 5 and 6 GHz, these protocols cannot be applied directly. The objective of this study was the development of new measurement procedures for the compliance testing of wireless devices with current safety limits for the frequency range between 5 and 6 GHz. This included the development of:

1) head and body tissue simulating liquids for worst-case SAR assessment;
2) miniature E-field probes with increased spatial resolution;
3) an efficient SAR scanning procedure using a cube with a graded z-axis.

The worst-case tissue composition was evaluated for frequencies between 5 and 6 GHz. Dielectric parameters were determined for head and body tissue simulating liquids and corresponding recipes were derived. The new high resolution probe has a tip diameter of 2.5 mm and distance from probe tip to dipole sensors of 1mm. It can be operated at the required distance of 1.5 mm from the phantom surface. The measurements on the different grids showed that the number of points can be limited by increasing the grid step in the z-direction without a negative impact on the accuracy.

The smallest isotropic dosimetric probe with diameter of 2.5 mm and sensor-to-tip distance of only 1.0 mm, which was developed within the study.

Assessment of ELF Magnetic Fields from Five Mobile Handsets

Personnel: Sven Ebert, Markus Tuor, IT'IS: Jürgen Schuderer, Niels Kuster

Funding: BAG

Partners: IT'IS

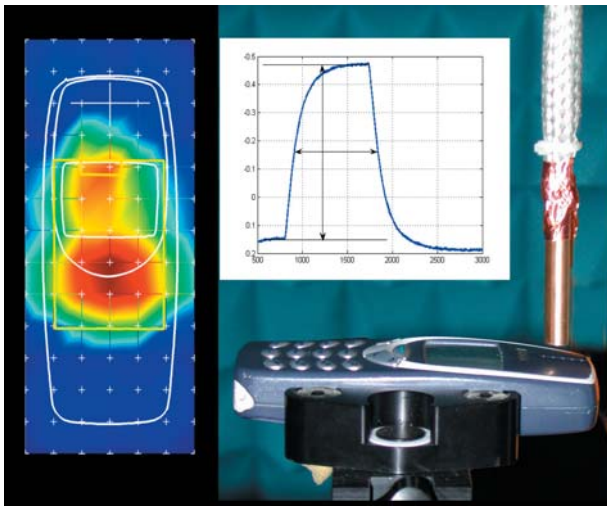
In addition to RF fields mobile phones also radiate extremly low frequency (ELF) electromagnetic fields. To examine the interaction between these ELF fields and biological tissue, knowledge of the spectral characteristics from different mobile phones is required.

In this study the ELF magnetic field components of five mobile phones were examined: Sony Ericssson T610, Siemens A50, Motorola TP, Sony Ericsson T68, Nokia 3310.

Surface scans of the front and back sides of the phones were conducted with a DASY4 near-field scanner equipped with a hallmeter probe (5 mm spatial resolution). Time domain measurements with a Narda ELT-400 probe (up to 400 kHz) were performed at the position of the maximum B-field.

The maximum ELF magnetic field strength at 5mm measurement distance was determined on the back side of the phones with up to 34µT and on the front side with up to 15µT; typical GSM frequency components were detected: 8 Hz and 217 Hz together with their higher harmonics. Each phone showed a characteristic pulse shape in the time domain.

The resulting data enable the definition of a worst-case exposure signal including ELF components, which could be used for risk assessment exposure setups.



The front side surface scan recorded with a hallmeter, magnetic field pulse shape measured with a Narda ELT-400 and the scanning setup for the mobile phone Nokia 3310.

Derivation of the Maximum Power Limit to Exclude Body-Worn Wireless Devices from Compliance Testing

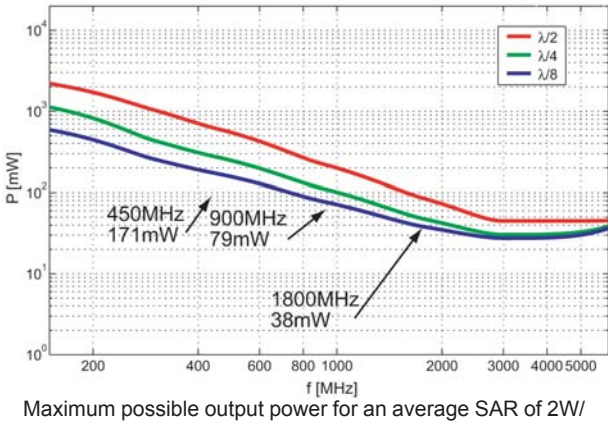
Personnel: Martin Loeser;
IT'IS: Andreas Christ, Niels Kuster

Funding: SARSYS-BWP

Partners: IT'IS, SPEAG

In most countries, governmental regulations require the testing of wireless devices with safety limits according to IEEE 1528, IEC 62209 Pt. 1, CENELEC EN 50361, etc. Current safety limits allow a maximum averaged SAR of 1.6 W/kg for an averaging mass or 1 g and 2.0 W/kg for an averaging mass of 10 g. Supposing that all the emitted power is absorbed in the body, a device could be considered as compliant if its maximum output power is less than 1.6 mW or 20 mW, respectively. However, not all of the power is absorbed in the human body and only a fraction of the absorbed power is in the cube of the spatial peak SAR. If the maximum output power can be reliably determined to be below the limits, the costly testing procedure can be saved for low-power devices.

The coupling mechanism between the near field of dipole antennas and biological tissue was studied for a wide frequency range (30 MHz - 5,800 MHz) and an approximation equation was derived which allows to determine the averaged SAR with an accuracy of ±3 dB. The approximation equation a convenient means to assess the ratio of radiated and absorbed power and is therefore applied to derive the output power limit at which a device can be excluded from compliance testing. Since changes in the antenna loading due to the presence of the body can affect the output power, two different amplifier models were considered: 1) constant feedpoint current and 2) constant feedpoint power. The comparison of the two amplifier models shows that the constant current source yields a more conservative estimation of the user exposure. For high frequencies (above 2 GHz), the absorption in the tissue reaches a maximum value for both amplifier models.



Maximum possible output power for an average SAR of 2W/kg in a 10g cube for dipole antennas of different lengths operated at a distance of 10mm from the body with a constant output power.

Development of a Flat Phantom for the Compliance Testing of Body-Worn Wireless Devices

Personnel: IT'IS: Andreas Christ, Anja Klingenböck, Niels Kuster

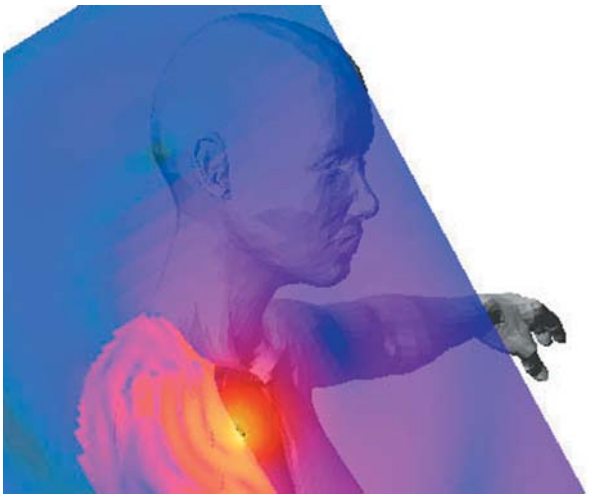
Funding: SARSYS-BWP

Partners: IT'IS, SPEAG

In the recent years, novel wireless devices such as WLAN transmitters, and body-mounted health support systems have further increased user exposure to electromagnetic radiation. Whereas the absorption mechanisms of the electromagnetic fields caused by cell phones have been intensively studied and standardized methods for compliance testing have been established, additional factors must be considered for body-mounted devices. These include:

- a large frequency range (30 MHz - 6 GHz)
- variation in positions and distances from the body
- other compositions of the body tissues
- different output powers and amplifier characteristics

This study aimed at the rigorous analysis of the energy absorption mechanisms considering these conditions and at the assessment of an appropriate phantom size required for a conservative SAR assessment. The tissue composition of the human body was studied with respect to worst case energy absorption. Because of the high range of frequencies and distances, both near- and far-field effects were considered. The results show that the presence of a tissue layer with low water content such as fat between two tissues with high water content (skin, muscle) has a significant impact on the energy absorption. Under far field exposure conditions, standing wave effects can cause an SAR increase in the skin, whereas reactive electric field components can penetrate the low permittivity fat tissue in the near field. Both effects can lead to higher SAR in comparison to homogeneous tissue modelling, and an additional safety factor between 2 and 3 may be necessary to assert a conservative SAR assessment.



Simulation of the field distribution from a body mounted miniature antenna.

Exposure from Indoor Wireless RF Devices

Personnel: Sven Kühn, IT'IS: Axel Kramer, Niels Kuster

Funding: BAG

Partners: IT'IS

Short-range wireless RF devices are being used pervasively in home and office environments, although their contribution to the electromagnetic field exposure of the human has not yet been systematically assessed.

The aim of this study is to provide classifications of RF exposures from wireless devices other than mobile phones used in home and office environments.

Five device classes (DECT, Bluetooth, WLAN, Wireless PC peripherals, Baby Surveillance Devices) were chosen for experimental exposure determination and measurement procedures for the specific transmission modes were designed. The experiment was designed for operating the devices under test at the mode with the highest output power. In the case of proprietary technologies the worst-case operational mode was determined experimentally due to lack of technical information.

The devices were analyzed by measurement of the Specific Absorption Rate using a DASY4 system (SPEAG, Switzerland). For devices used at a greater distance the E-field was also measured in the far field.

The results allow to compare the considered device classes against already well investigated sources of exposure (e.g. cell phones, base stations) as well as to compare with the recommended limits from guidelines for human exposure by radio frequency fields.

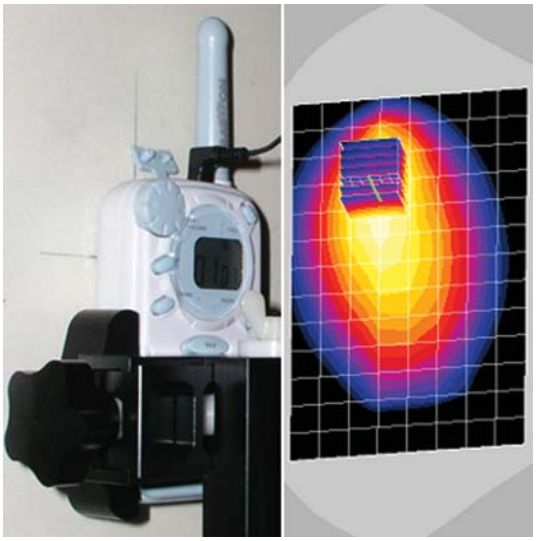


Figure displays a baby surveillance device applied to the SAR measurement phantom (left) and the measured SAR distribution for this device (right).

Relevant Parameters for the Comparison of Animal Studies

Personnel: Verónica Berdiñas Torres, Neviana Nikoloski
IT'IS: Jürg Fröhlich, Anja Klingenböck, Niels Kuster

Funding: PERFORM A Consortium

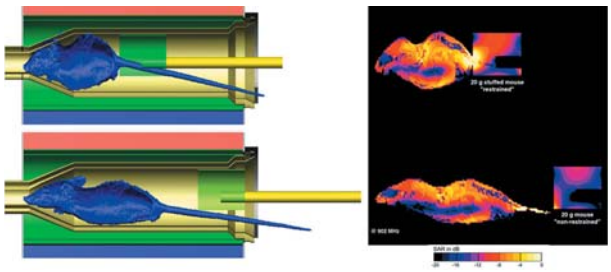
Partners: ARCS

Classical toxicologic and carcinogenic bioassays are evaluated based on the outcome of the histopathology. In order to enable inter-study comparison an accurate dosimetry for the various tissues investigated must be conducted. This should include the average exposure per organ as a function of age. In general, the exposure is rather non-uniform and dependent upon various parameters such as anatomy, posture, polarization of the incident fields, moisture/sweating, etc. This requires the assessment of the instant exposure variations per organ as well as variations of the average exposure during an exposure session and lifetime exposure. In addition to these parameters, the uncertainty of each of these values should also be estimated as well as the spatial peak SAR values.

In order to facilitate such assessments, several high-resolution anatomical models of rats and mice of differing ages, genders and strains were generated. For the PERFORM A setup various parameters and their interactions with respect to the animal models and exposure setup have been considered to assess the SAR variations and uncertainties for whole-body and single organs:

- animal weight: 7 models (3 original, 4 scaled)
- posture: restrained animal versus non-restrained
- position: animal displacement in the restrainer tube
- sector position: 4 different positions in the wheel
- stopper contact: from full contact to no contact
- anatomy: 3 models scaled to the same weight (different strain and gender)
- dielectric parameters: variations of ±10% in ε and σ
- spatial and anatomical resolutions
- sweating

Simulations were performed with the FDTD simulation platform SEMCAD. The results were validated by measurements using DASY4 and EASY4 and appropriate phantoms.



Left: Stuffed and original mouse anatomical models in the restrainer tube of the exposure system. Right: Corresponding SAR distributions at 902 MHz.

Reevaluation of a 2.45 GHz Circularly Polarized WG as *In Vivo* Exposure System

Personnel: Verónica Berdiñas Torres
IT'IS: Jürg Fröhlich, Niels Kuster

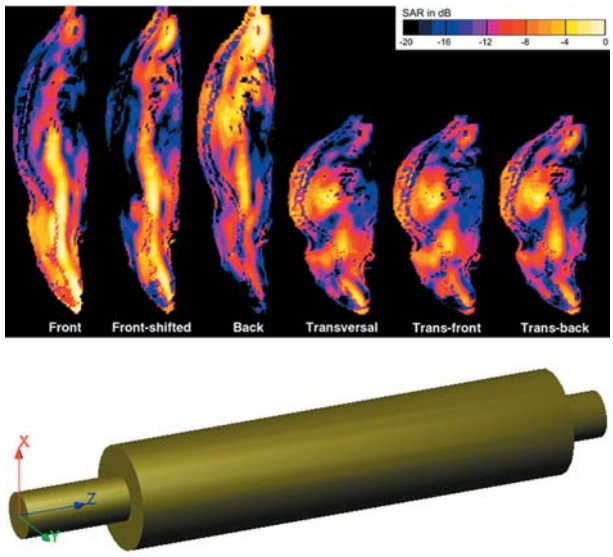
Funding: PERFORM B Consortium

Partners: ULP Strasbourg

A circularly polarized 2.45 GHz waveguide system for chronic exposure of small animals to microwaves was developed and utilized for the exposure of rats prior to a radial-arm maze task. The system has been reevaluated within the European Project PERFORM B.

Although this waveguide is not a mono-mode cavity, it has relatively small dependence of the whole-body absorption on the size, orientation and posture of the animals. The aim of this reevaluation study is to improve and complete the dosimetry work published until now. In the past, only three major orientations of the animals in the waveguide had been considered. Displacements of the animals to the left, right, front and back sides of the cage with respect to the center have now been taken into account, providing 12 different locations. Within this study the influence of these displacements on whole-body and brain averaged SAR as well as the corresponding standard deviations were assessed.

A detailed numerical model of the waveguide including high-resolution anatomical models of two male rats was used for the assessment of the variability in whole-body and brain SAR. All simulations were performed using the FDTD-based simulation platform SEMCAD.



SAR distribution of a male rat exposed in a Circularly Polarized Waveguide (CWG) in different locations, and external view of the CWG.

Risk Assessment: Thermal Response and Threshold Measurements in Mice Exposed to 905MHz

Personnel: Sven Ebert; IT'IS: Niels Kuster; Fraunhofer ITEM: Clemens Dasenbrock, Thomas Tillmann

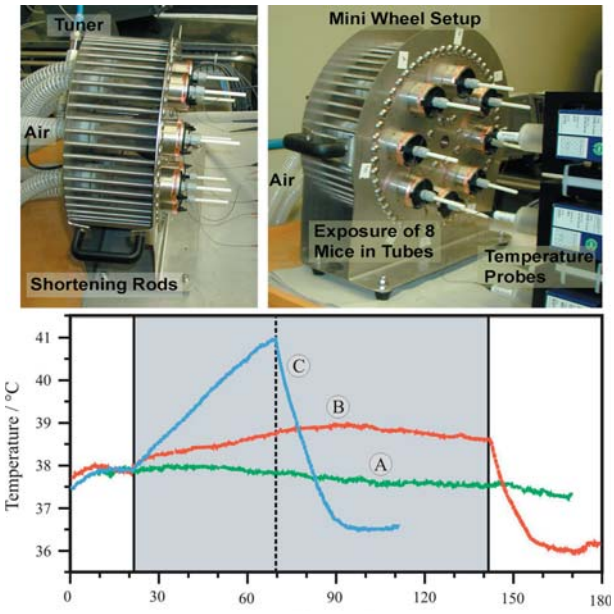
Funding: PERFORM A Consortium

Partners: Fraunhofer ITEM

The objective of this study was the determination of the thermal regulatory and the thermal breakdown thresholds for restrained B6C3F1 and NMRI mice exposed to radio-frequency electromagnetic fields at 905 MHz.

Different levels of the whole-body averaged specific absorption rate (SAR = 0, 2, 5, 7.2, 10, 12.6 and 20W/Kg) have been applied to the mice, and their body temperature was rectally measured prior, during and after the 2h exposure session in a parallel plate waveguide setup. For B6C3F1 mice, the thermal response was examined for three different weight groups (20 g, 24 g, 29 g), both genders and for pregnant mice. Additionally, NMRI mice with a weight of 36 g were investigated for an interstrain comparison.

The thermal regulatory threshold of tube-restrained mice was found at SAR levels between 2 W/kg and 5 W/Kg, whereas the breakdown of regulation was determined to be 10.1±4.0 W/kg for B6C3F1 mice and 7.7±1.6 W/kg for NMRI mice. Based on a simplified power balance equation, the thresholds show a clear dependence upon the metabolic rate and weight. NMRI mice were more sensitive to thermal stress and respond at lower SAR values with regulation and breakdown. The presented data suggest that the thermal breakdown for restrained mice may occur at SAR levels of 6 W/kg (K=2) under standards environmental laboratory conditions.



A Mini Wheel Setup was used for the experiments. Three characteristic thermal responses were observed: (A) below the thermal regulatory threshold, (B) in the thermal regulatory region and (C) above a thermal breakdown threshold.

Risk Assessment: Flexible and Mobile Setup for a Large Human Provocative GSM Exposure Study

Personnel: Sven Ebert, IT'IS: Jürgen Schuderer, Niels Kuster

Funding: MMF

Partners: IPM

A large-scale human provocation study in the context of the health risk assessment of low-level exposure to the RF of mobile phones is currently being conducted at IPM, Stockholm. Examined are effects of the 900 MHz GSM signal on subjective symptoms, physiological reactions, alertness, performance and sleep. IT'IS has developed the exposure setup for this study.

The setup enables the exposure of the left head hemisphere and is designed to maximize the exposure of brain tissue as may occur during the actual usage of GSM phones. The system is based on a low-weight, stacked micropatch antenna fixed on a headset and allows the subject to move/rotate within a limited area without changing the exposure distribution; this allows flexible and comfortable exposure situations and also simultaneous recording of an EEG.

A fully computer-controlled signal unit allows the application of GSM modulated RF exposures for two different subjects. The RF exposure is monitored, controlled and recorded in an encoded file at all times and is in compliance to double-blind exposure protocols. The exposure signal was chosen with respect to exposure strength (SAR), GSM modulation (DTX, power control) and time course of exposure and consists of a GSM signal at an average SAR of 1.4 W/kg simulating a conversation, i.e., including periods of DTX (active during talking) and Non-DTX (active during listening).

Flexible, comfortable and well-defined exposure system for human provocative studies at 900MHz with automatic exposure control.

Risk Assessment: Comparison Study of Wheel-like Mouse Exposure Systems

Personnel: Sven Ebert, Veronica Berdinas Torres, IT'IS: Jürg Fröhlich, Niels Kuster

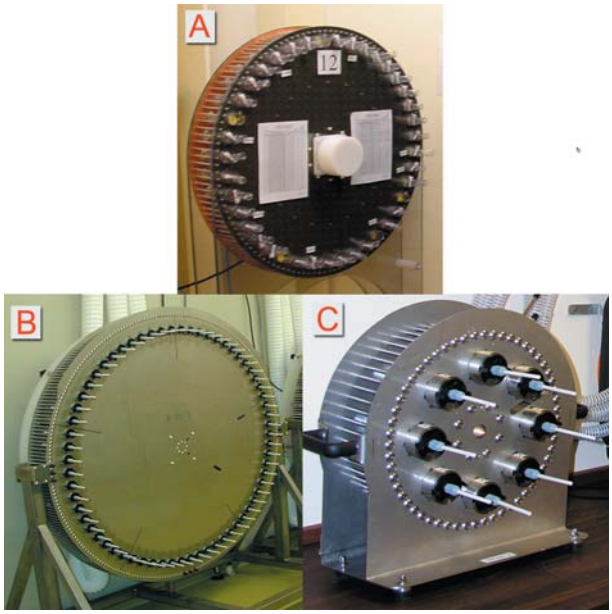
Funding: PERFORM A Consortium

Partners: IT'IS

Wheel-like exposure systems for mice at 900 MHz are widely used for *in vivo* risk assessment studies at mobile communication frequencies. This study examines three different mouse exposure setups operating at 900 MHz which are used in international studies examining potential effects due to RF exposure from mobile communication frequency signals.

The wheel-like exposure setups are designed as resonant waveguide structures of two parallel, circular-shaped metallic plates shorted with metallic bars along the outer edge and with an isotropic antenna at the center. The mice are circularly positioned in restrainer tubes at a fixed distance from the antenna. The animal body axis is orientated parallel to the E-field.

The study compares three setups: (A) the Motorola M-40 wheel developed in 1999 enables the exposure of up to 40 mice; (B) the PERFORM A M-65 wheel developed by IT'IS in 2000 enables the exposure of up to 65 mice and (C) the Mini Wheel M-8 developed by IT'IS in 2003 enables the exposure of up to 8 mice. The exposure setups were compared with respect to the following performance parameters: uniformity, temperature rise, SAR efficiency, occurance of higher modes, loading efficiency and provision of exposure and environmental control.



(A) Motorola M-40, (B) PERFORM A M-65, (C) Mini M-8 Wheel exposure setups examined in the comparison study.

Development of a Comprehensive Hyperthermia Treatment Planning Tool

Personnel: Esra Neufeld
IT'IS: Nicolas Chavannes, Niels Kuster,
Aristotle Uni, Thessaloniki: Theo Samaras

Funding: IT'IS

Partners: IT'IS, SPEAG, ERASMUS MC Rotterdam

Hyperthermia is a treatment modality for cancer that can strongly increases survival rates. It consists of heating the tumor to a temperature that should ideally lie above 43 °C. This is commonly achieved by exposing the patient to electromagnetic (EM) radiation. Often an antenna array is used to achieve the desired deposition pattern.

Unfortunately hyperthermia is not as widely applied as it deserves to be. This could be changed by improving the treatment quality and efficiency and providing better visualization. For this a patient based planning tool is required that will have to perform the following main tasks:

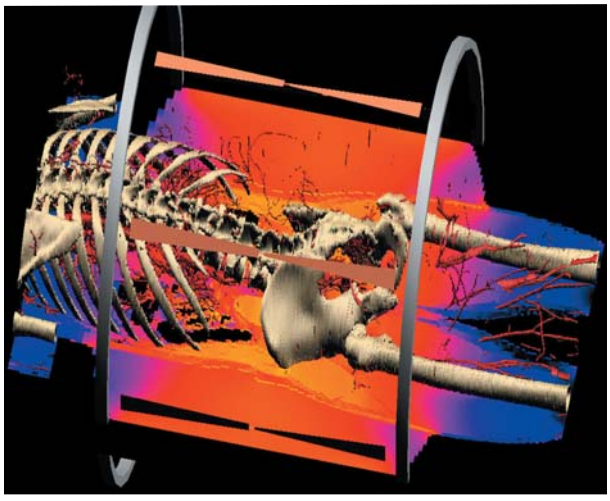
- Transform medical imaging data into a model of the patient on which simulations can be carried out.
- Simulate the EM field distributions generated by the different antennas.
- Predict the resulting temperature increase in the patient taking into account the blood-flow and specific heat generation rates of the various tissues.
- Determine the 'optimal' antenna settings.

Detailed applicator models have been constructed and calculations carried out using the *SEMCAD* software. Problematic areas could be identified and are being addressed. The influence of some parameters (e.g., temperature of water bolus) has been studied.

The main effort has gone into creating a flexible image segmentation toolbox.

Important future work will include the development of a model for temperature flow, clarification of the necessary model detailedness and validation of the treatment planning tool.

The software will also be helpful for the development of new applicators, as much is left to improve there as well.



Simulation of the specific absorption rate (*SAR*) distribution induced by a *Sigma60*-applicator (*BSD Med. Corp.*)

A Toolbox for the Segmentation of Medical Image Data

Personnel: Esra Neufeld
IT'IS: Nicolas Chavannes, Niels Kuster,
Aristotle Uni, Thessaloniki: Theo Samaras

Funding: IT'IS

Partners: IT'IS, SPEAG

When individualized simulations involving human beings have to be carried out, the first step consists in generating a specific model based on image data. An example would be medical treatment planning, in which medical images (*CT/MRI*) are used. In a process called *segmentation* the image is decomposed into regions that can be considered as homogeneous.

Currently, a *hyperthermia* treatment planning tool is being developed. In this context a toolbox has been constructed that permits flexible intercombination of various segmentation techniques as well as pre- and post-processing steps. The software aims at unifying the advantages offered by region and contour based segmentation techniques. Its goal is to provide a package that permits robust segmentation of whatever input data is available, permitting the necessary level of user interaction while enabling as much automation as reasonably possible.

Methods as diverse as *region-growing*, *level-sets*, *fuzzy connectedness*, *k-means classification*, *watershed transformation* and *intelligent scissors*, to name only a selection, have been implemented. Various filters can be used to improve the image quality or to highlight specific image features (e.g. edges). Routines to perform contour extraction, line simplification, connected component analysis, distance transformation, interpolation between slices, mathematical and morphological operations are available. Many operations can easily be extended to 3D as well. An interface to the *SEMCAD* software exists.

The next step will be to add a front-end to make the toolkit more useable.

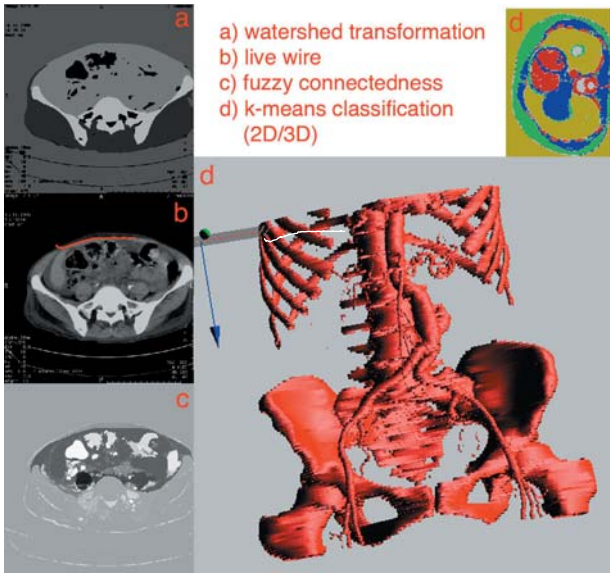


Illustration of some segmentation techniques.

Education Program

Student Projects

Coordinator:

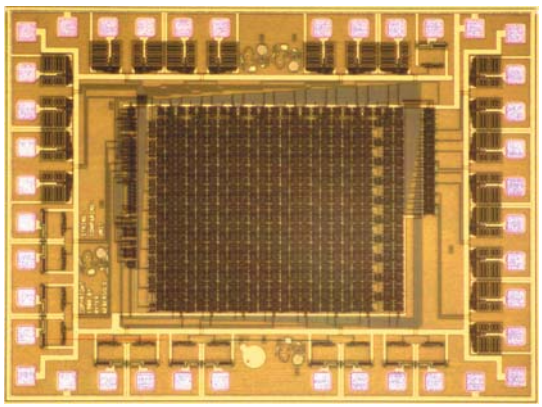
Norbert Felber

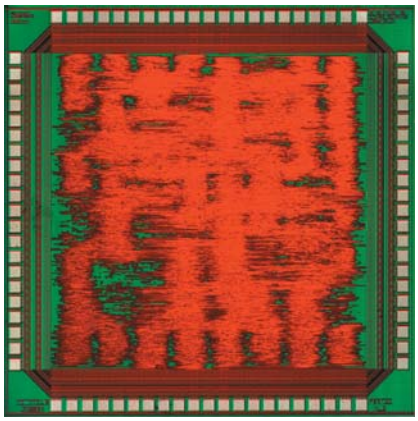
Introduction and History

Teaching microelectronics is one of the core activities of the Integrated Systems Laboratory. Shortly after the laboratory was founded in 1986, it started to offer projects in IC design to students. Probably as the first European university ETH financed the fabrication of student chips. This gave students the opportunity to carry out a VLSI design project from the specification to the test of their own silicon chips. Still today, the majority of student term projects at IIS are in practical chip design, and many diploma projects include the realization of integrated circuits or the development of components as contribution to research ASICs. A lot has changed during these almost 20 years. The largest student chip designed in a semester thesis in 1987/88 had 7,000 transistors, in 2003/04 this number was around 500'000. In 1988 the active region of one transistor was 3 μm long, in 2003 0.25 μm. The chip sizes however stayed comparable: 2.4 x 3.2 mm^2 with 32 pins and 2.5 x 2.5 mm^2 with 84 pins for a student term project chip. The figure below shows the most complex chips of the first VLSI curriculum 1987/88 and of the one reported in this research review (2003/04) in the same scale.

Left: Photograph of student chip of the first run with approx. 7000 transistors in CMOS 3 μm technology. It implements a string comparator.

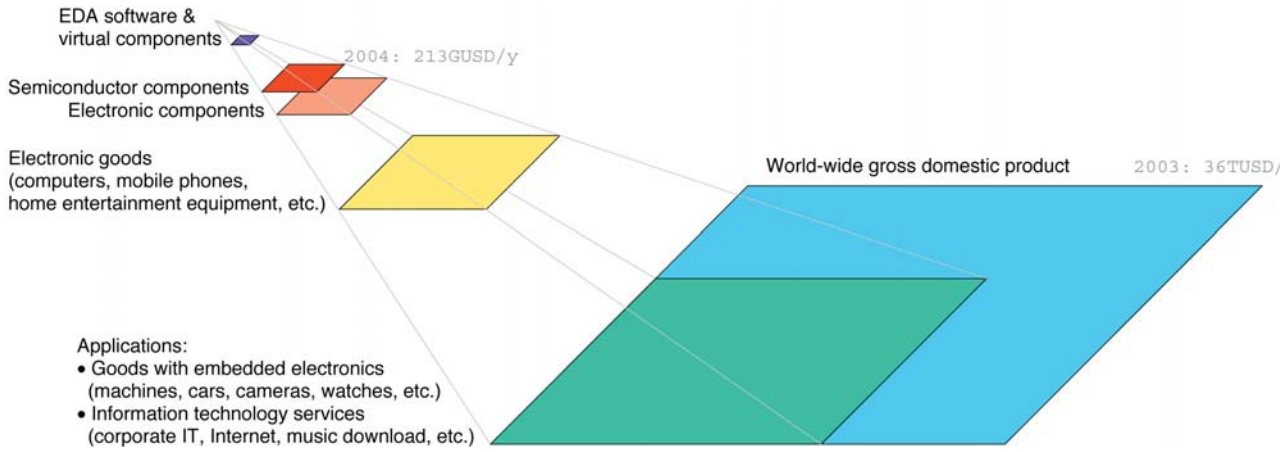
Right: Photograph of a recent student chip in 0.25 μm CMOS technology implementing the AES Rijndael cryptography algorithm. The chip contains 480,000 transistors





Economics of Microelectronics Education in Switzerland

Since the first VLSI course offered by IIS, more than 450 engineering students have had the chance of designing real silicon. This was only possible due to the generous funding of the chip fabrication by the Board of the ETH Zürich. During times of a prospering market, our students had all the chances of finding jobs in and outside Switzerland. More important, also during the periodic low-phases of the electronics industry, hardly any student specialized in VLSI had problems to find an adequate job in less than a few months. Most of our former students are now working in the microelectronics research and development centers of Swiss industry. Others found the way to well-known international companies all over the world.



Impact of the EDA and microelectronics activities on the market of electronic products. The area of the colored squares is proportional to the estimated revenues. It demonstrates the multiplication effect. For the semiconductor components and the gross domestic product, world-wide figures are indicated.

Although basic microelectronics industry is rare in Switzerland, many other companies need chip knowledge for the development of their products. The figure above shows the world-wide economic leverage of microelectronics (red square) on "downstream" industries and services, starting from the Electronic Design Automation (EDA) market. For Switzerland a comparable scenario will hold (with lower figures). Our students become specialists mainly in the red square.

Education in Microelectronics

During the first four semesters, students are motivated towards microelectronics by several PPS (Practicals, Projects, Seminars) (http://www.iis.ee.ethz.ch/stud_area/pps.en.html). In semester 5 and 6 the practical trainings (Fachpraktika, http://www.iis. ee.ethz.ch/stud_area/fachpraktika.en.html) offered by IIS aim at the same goal.

The three VLSI lectures from the 6th to the 8th semester illustrated in the figure on page 116 build the main block in microelectronics education by the Integrated Systems Laboratory.

VLSI I: Architectures of Highly Integrated Circuits teaches the development of an electronic system from specification to implementation. Architecture design and the definition of the functionality in Hardware Description Language are treated in depth. Verification by simulation is the next topic. The course is completed by implementing the system in a programmable chip (FPGA). Since bachelor students will not follow the higher courses, VLSI I is self contained in the sense that it provides the knowledge required in a typical small Swiss company not specialized in custom IC design. The course is followed by 60 to 70 students each year.

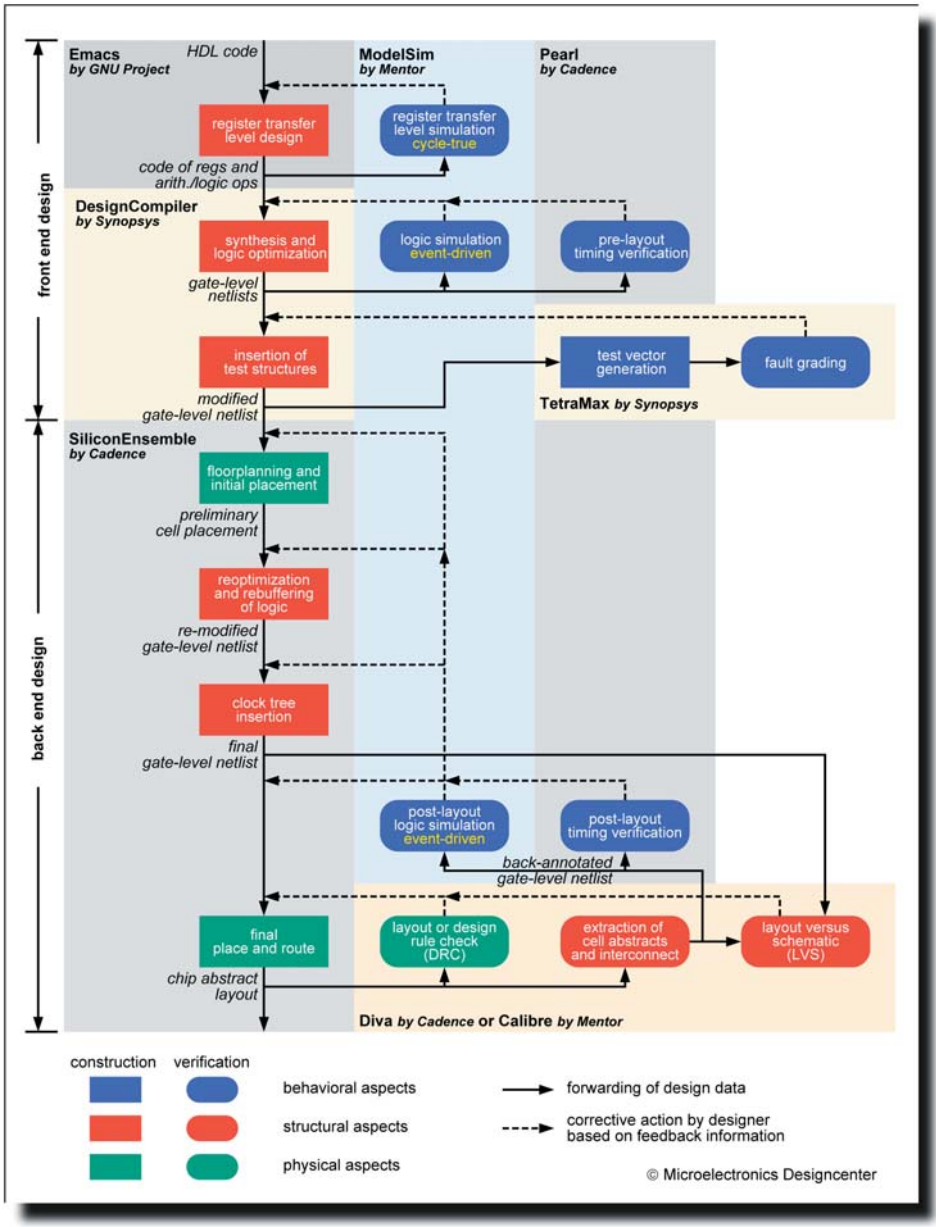
VLSI II: Design of Highly Integrated Circuits focuses on all design issues required for a sound development of first-time-right Application-Specific Integrated Circuits (ASIC). In parallel, as a semester project, around 12 groups of one to four students realize their own ASIC. Typically, 40 students attend the course and the exercises, 24 of which do also the design project.

VLSI III: Fabrication and Verification of Highly Integrated Circuits provides more in-depth knowledge on VLSI fabrication technologies and focuses on requirements for full testability of chips. During the exercises, the chips designed in parallel to VLSI II and fabricated during the semester break are tested by their designers. So, the full development cycle has been completed. Around 30 students follow VLSI III. For the designers of the fabricated ASICs the attendance is mandatory.

Students who want to further deepen their experience in microelectronics often chose a diploma or master thesis in the framework of a research project of IIS as culmination of their education. Some then stay in these research fields for performing a PhD thesis.

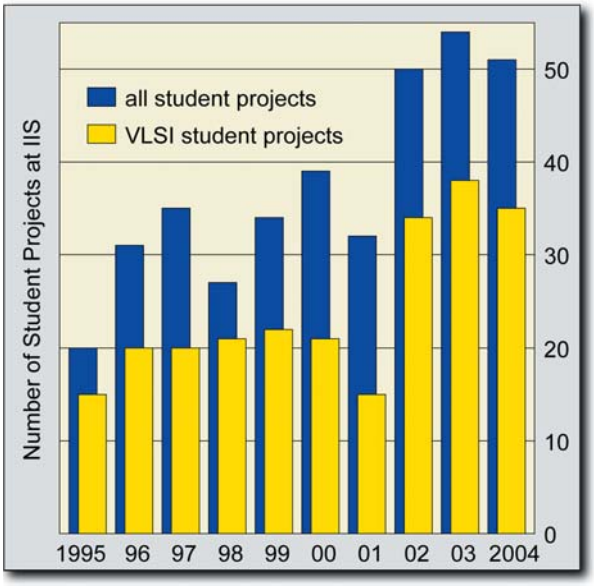
ASIC Design Projects

Students who have decided to realize an integrated circuit will learn a professional design flow using industrial CAD tools. The figure to the right shows a simplified view of all tools involved and of the task they are applied for during the work. The tools are the same as used in research and by our main industry partners; providers and products are indicated. The diversity of this design environment demonstrates the considerable effort our students have to provide just to master the tools. Besides their "handcraft" they want to learn IC design, and to realize an often challenging and complex project. Despite the hard work with many traps and complications, almost all chips finally work as intended.



Overview over the tool framework for IC design supported by the Microelectronics Design Center of the Department of Information Technology and Electrical Engineering. In the exercises to the VLSI lectures, the students practice to use these tools which they then intensely apply during the design projects.

During the 14 weeks of a semester project, the design students put 'official' 50% of their work load into the realization of the chip, mostly even considerably more. First-time-right digital ICs of industrial complexity level often result. This is only possible due to the sound VLSI education and an excellent support for design and test offered by the PhD students of our Laboratory and the Microelectronics Design Center of the Department of Information Technology and Electrical Engineering (http://dz.ee.ethz.ch).



Further Student Projects at IIS

Besides in digital ASIC design students are offered projects in the fields of all other research groups of IIS and IT'IS. This regards analog and mixed-signal IC design, TCAD tool development and applications, optoelectronics device development and simulation, physical characterization of semiconductor devices, as well as tool, measurement and experiment contributions in bio-electromagnetics. The graphics to the left gives an overview over the number of student projects at IIS (blue bars) during the last ten years with emphasis to the VLSI student projects (yellow bars).

Organization of this Chapter

On the following pages the VLSI projects are reported first. When there are successor projects with hardware development for student Chips, they are placed directly beside the ASIC report. Analog and mixed-signal projects, as well as further hardware system designs are the next group of reports. Optoelectronics and physical characterization projects conclude this chapter.

A special case are some student projects which are direct and important contributions to research projects presented in the preceeding chapters. These projects are printed next to the corresponding research reports. This concerns the contributions on pp 38 (left), 39 (left) and 42 (right).

As second-last remark, it is worth to mention the student papers of some of the projects that have been accepted in international conferences and presented by the students as their first contribution to the research community. The bibliographies can be found on pp 135ff.

Last but not least it stays to mention that the project *Spere Decoder ASIC for MIMO Communications* on page 38 has been awarded with the *Prix du Jeune Entrepreneur 2004* of the Section Suisse des Conseillers du Commerce Extérieur de la France.

Complex Matrix QR Decomposition for Inversion

Personnel: Thomas Helbling, Livia Seemann; David Perels, Andreas Burg (assistants)

Thesis: Semester Project

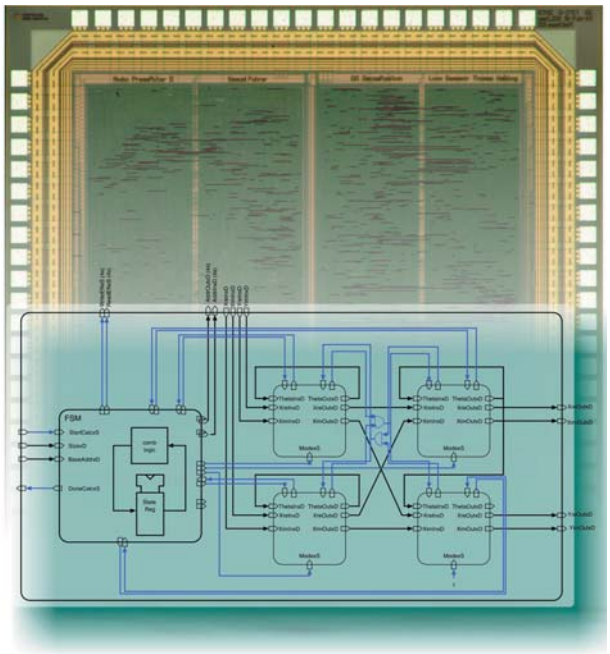
For modern wireless communication systems the signal processing algorithms become more and more demanding. Algorithms related to Multiple-Input Multiple-Output (MIMO) systems employ the theory of linear algebra extensively.

A prominent and complex operation is the matrix inversion of a complex-valued matrix. Several approaches to realize this operation exist. A salient example is to first decompose the matrix into a orthonormal Q and triangular R part. Through back-substitution the inverse can be found easily.

In this project, the QR decomposition algorithm is implemented. To execute the oprations needed on the matrix, the processing element is implemented as a complex CORDIC (COrdinate Rotation DIgital Computer).

The QR processor uses iterative CORDICs since the processing elements need to run both in vectoring as well as in rotation mode.

The final QR processor calculates the R matrix of a 4x4 complex-valued matrix in 11·59 cycles. The chip was manufactured in 5-metal-layer CMOS technology at UMC. 1.2 mm^2 is the size of the core area. The tested chip runs at 250 MHz.



The processor was manufacutred together with another project. The macro cell of this project is located on the right. In the overlay, the top level design is presented. Note the four CORDIC blocks needed for a complex rotation.

Power and Performance Optimization of a Complex-Number ALU

Personnel: Conradin Merk, Christoph Studer; Frank K.Gürkaynak, Eric Roth (assistants)

Thesis: Semester Project

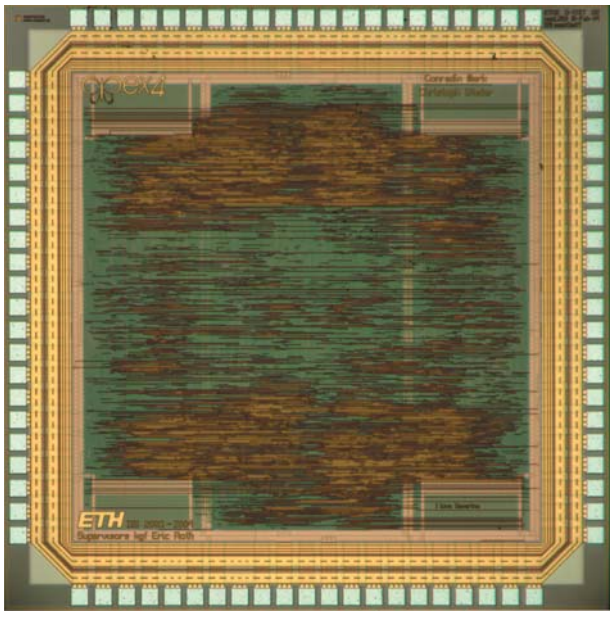
Architectures designed for high throughput are generally considered to be power hungry. A successful design tries to achieve the best possible compromise between power consumption, silicon area and operation speed.

In this project, a recently designed high-performance complex-number ALU has been re-designed and implemented. The initial ALU was not designed under power consumption considerations and therefore delivered a good comparative platform throughout the design process.

The ALU is designed to be used in a DSP capable of performing high-speed FFT operations. An architecture using four parallel execution units was considered to be the most optimal for an ALU tailored for FFT operations. Each execution unit houses a 16 bit complex multiplier, a configurable 32 bit ALU and a 32 bit adder.

Optimizations in the datapath structure have reduced the critical path by nearly 50 %. Significant power savings were obtained by using extensive clock gating and by setting the inputs of inactive modules to constant values.

The implemented design has a complexity of 120 kGate equivalents and is able to run at a clock frequency of 125 MHz. With these parameters the new design is nearly twice as fast and consumes only 28% of the energy of the initial design while computing a 1024 point complex FFT.



The chip photograph of the complex-number ALU design named CPEX-4.

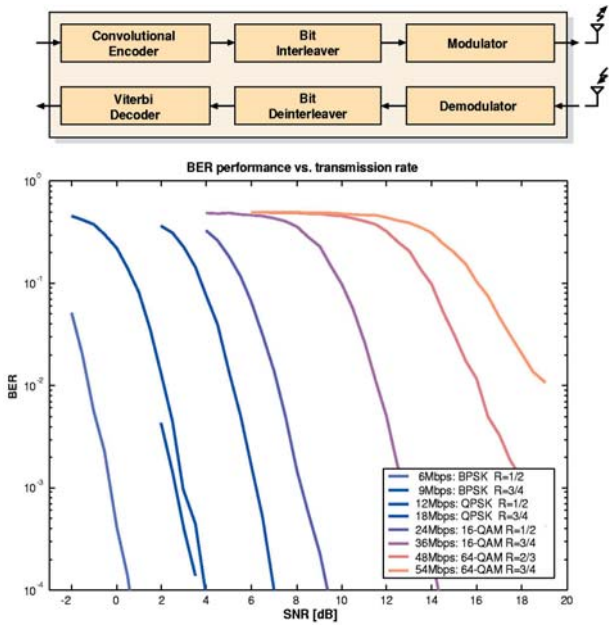
Metric Computation Unit for Bit-Interleaved Coded Modulation

Personnel: Marco Chicherio;
Moritz Borgmann (IKT), Daniel Baum (IKT),
Simon Häne (assistants)

Thesis: Master Thesis

In order to improve the bit-error rate (BER) over fading wireless channels, error correcting codes are usually employed. Bit-Interleaved Coded Modulation (BICM) has recently emerged as a more scalable alternative to classical Trellis Coded Modulation (TCM). A BICM transmitter is a serial concatenation of a convolutional encoder, a random bit interleaver and a memoryless modulator. With this approach, any convolutional code can be used, independently of the PSK or QAM constellations used in the modulator. At the receiver, the bits are de-mapped (hard or soft), de-interleaved, and fed to the Viterbi decoder. Only the mapping and de-mapping needs to be changed for varying transmission rates, thus simplifying the system design. Computing soft information for each bit from the received PSK or QAM symbols is the most involved task and can usually only be approximated for reasons of computational complexity. The receiver building block that computes these soft metrics is named metric computation unit (MCU).

In this project a bit-true model for a 802.11a wireless LAN standard compliant BICM transceiver was implemented in C++, devoting particular attention to the design of hardware-efficient approximations for the soft metric computation. The results of BER simulations of the overall system were used to tune the main design parameters of the Viterbi decoder ASIC reported on the right half of this page.



Block diagram of a BICM transceiver and BER plot for the different data transmission rates defined in the 802.11a wireless LAN standard using the proposed MCU.

Viterbi Decoder for Wireless LAN

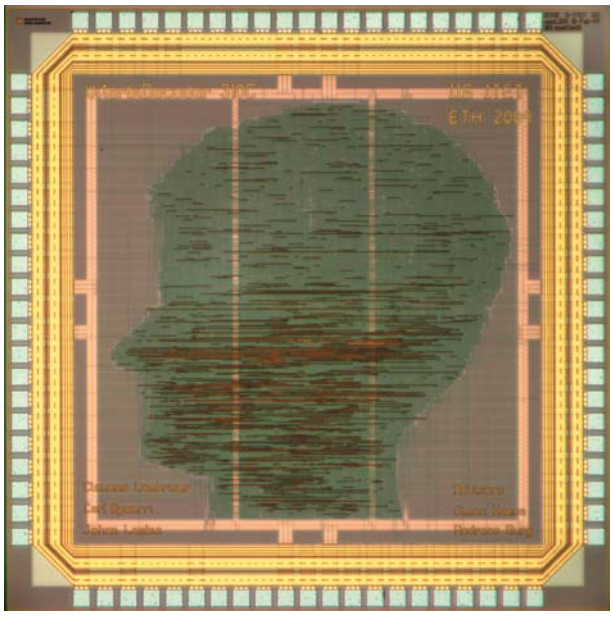
Personnel: Clemens Lombriser, Carl Spörri,
Johan Lambie;
Simon Häne, Andreas Burg (assistants)

Thesis: Semester Project

Wireless digital communications require reliable data transfers even if the available channel is fading. Viterbi decoders are widely used at the receiver in order to perform maximum-likelihood sequence detection in sub-exponential time. An error-correcting code is applied at the transmitter, whereas the Viterbi decoder is used to reconstruct the original data stream at the receiver. The problem can be shown to be equivalent to finding the shortest path through a weighted and directed graph.

This particular IC was designed to be compliant with the error-correcting code defined in the 802.11a wireless LAN standard which is a 64-state, rate-1/2 convolutional code. At each time step, the decoder computes a new path metric for each of the 64 states, based on the previously computed path metrics. This computation is recursive and represents the performance bottleneck of hardware Viterbi decoders. In this realization all 64 path metrics are updated concurrently by 64 parallel so-called Add-Compare-Select (ACS) units. A unit termed survivor path memory produces the output bits by tracing the decisions made in the ACS units using the register exchange algorithm.

The ASIC was fabricated on a 0.25 µm five-metal-layer CMOS process from UMC. The maximum operating frequency of the tested chips is 225 MHz which allows to decode a 225 Mbps data stream.



Chip micrograph of the Viterbi decoder ASIC containing the MCU of the project reported in the left side column.

SOLARIS - High-Order, Low-Latency Convolution Processor ASIC

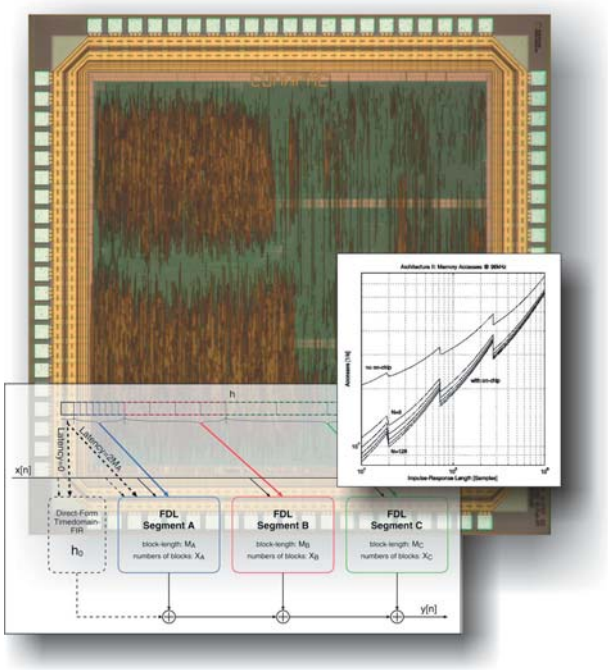
Personnel: Rolf Anderegg, Ulrich Franke; Norbert Felber, Peter Lüthi (assistants)

Thesis: Master Thesis

Partners: Weiss Digital Audio

The demand for convolving digital audio streams with a given one-dimensional function grows rapidly in today's digital audio systems. Typical applications are generation of hall effects, room modelling for movies, or architectural acoustics. These applications require convolutions with impulse responses of very long duration (up to many seconds) and are therefore extremely costly in their computational requirements because of linear dependency on impulse response length. The approach to execute the convolution in the frequency domain by employing the Fast Fourier Transformation (FFT) greatly relieves the computational burden mainly imposed by multiply-add operations. However, the advantage of the FFT approach comes at the expense of an input to output delay of the impulse response length. The FFT-based fast-convolution algorithm reduces latency by combining time and frequency methods. By using parallel processing of blocks in a highly regular manner, it is predestinated for a dedicated implementation in an integrated circuit as an interesting alternative to a general-purpose digital signal processor (DSP).

The integration in UMC 0.25 µm CMOS technology requires 3.56 mm^2 core area. The maximal clock frequency is 100 MHz. The impulse length per channel is 5.29 s at 48 kS/s with a I/O latency of 10.7 ms. The THD+N of 142.7 dB guarantees high audio quality.



SOLARIS - High-Order, Low-Latency Convolution Processor ASIC, able to generate hall effects of up to 5.29 seconds at 48 kHz sampling rate.

Asynchronous Digital-Audio Sample Rate Converter

Personnel: David Grünert, Roman Kappeler; Norbert Felber, Stephan Oetiker (assistants)

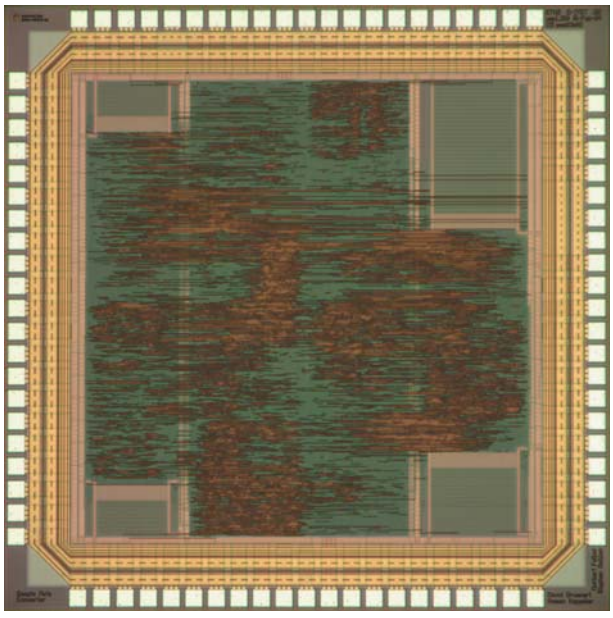
Thesis: Semester Project

The chip developped in this project is an asynchronous sample rate converter targetting professional audio applications. Input and output sampling frequencies in the range of 1 to 192 kHz are supported with a resolution of up to 24 bits. The standard I2S audio input port accepts samples of a fully asynchronous data stream from any audio source, and the I2S output port delivers the interpolated samples at the precise rate requested by the sink.

After a conventional four-fold up-sampling of the input data a B-Spline interpolation of order 8 is used to calculate the new samples at double output sample rate which is finally decimated to the requested output format. Two all-digital phase-locked loops (PLLs) de-jitter the source and sink data clocks and calculate the precise points in time for the B-Spline interpolation.

The excellent total harmonic distortion and noise (THD+N) figures of at least 142 dB could be achieved by high-precision arithmetic datapaths and the PLLs providing a time resolution of 5 picoseconds.

The ASIC has been fabricated in a 0.25 µm five-metal-layer CMOS process. The chip contains 4 RAMs (a total of 1.7 kBytes) and occupies the whole die size of 2.5 mm x 2.5 mm offered to the students for their VLSI design semester projects. The system clock frequency ranges from 26.5 to 33 MHz, independent of sampling rates.



Chip photomicrograph of the sample rate converter ASIC which is able to interpolate incomming digital audio samples to any requested output rate.

3D Audio Correlator ASIC

Personnel: Thomas Frech, Jean-Daniel Merkli; Flavio Carbognani, Norbert Felber (assistants)

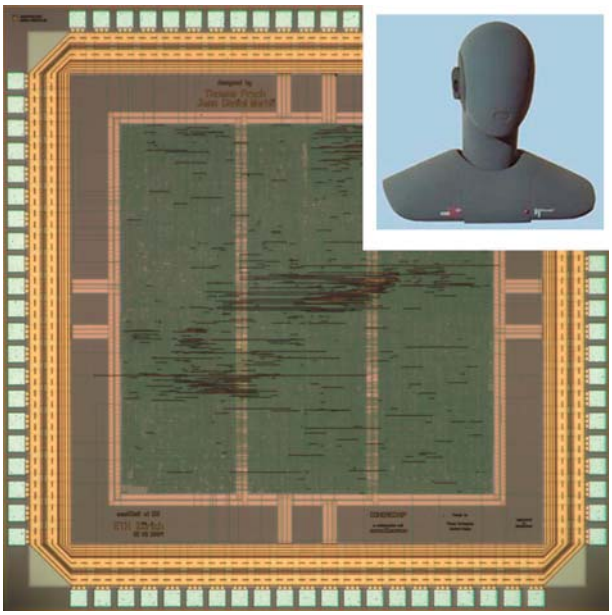
Thesis: Semester Project

Partners: Renato Pellegrini, Mathias Rosenthal; sonic emotions AG

Different applications, such as radio dramas, games for PCs and others, take advantage from knowing in real time the direction, from which a recorded voice or sound is coming from. In the first phase, the sound is recorded by means of both a near-distance microphone and an artificial head (see inlet in the picture). In the second phase, the so called *rendering*, the near-microphone recording is combined with the spatial information coming from the artificial head, to reproduce a high quality sound, together with the impression of the movement in a virtual environment.

The 3D audio correlator ASIC called CohereChip (main image in the picture) is used to extract the spatial information out of the stereo recording of the artificial head in real time. To achieve such a result, it performs 72 correlations with as many *Head Related Transfer Functions* (HRTF). These are nothing else than predetermined impulse responses with an angle displacement of 5º in the given environment. The 3D audio correlator chip outputs the direction of origin of the sound, by calculating the maximum among the different correlation values. Some relevant features of the chip are:

- High-quality audio data (sampling frequency of 48 kHz);
- USB transfer facilities;
- Package-structured data.



Main figure: Die photo of the 3D audio correlator ASIC. Inlet: artificial head for realistic stereo recording.

3D Audio Correlator System

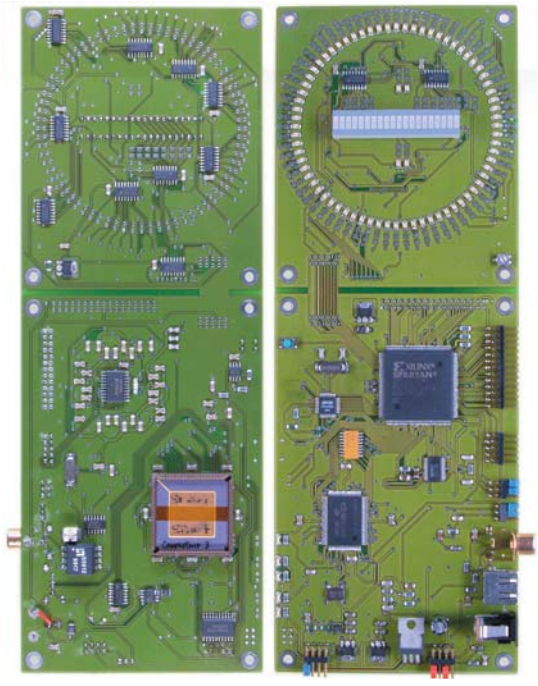
Personnel: Jean-Daniel Merkli, Christoph Reller; Flavio Carbognani, Norbert Felber (assistants)

Thesis: Semester Project

Partners: Renato Pellegrini, Matthias Rosenthal; sonic emotions AG

Based on the CohereChip, described on the left side of this page, an audio correlator system has been developed in this project. The hardware consists of a printed circuit board (PCB) which, besides the CohereChip, contains all required supply circuitry and a USB interface. According to the partner sonic emotions the originally specified audio packet size was too small for real-time operation with a PC. The system has therefore been enhanced by adding an FPGA to provide additional buffering. Due to this FPGA further functionality could be implemented: a digital audio interface (SP/DIF) and an angular/power display. Due to these enhancements, after loading the head-related transfer functions from a PC, the hardware offers a real-time display of direction and strength of the strongest component in an SP/DIF audio input stream.

In addition to the hardware, a Linux-based software library of important tools and interfaces for the interaction of a PC with the Cohere system functions has been developed in this project. It is written in C++ using the KDevelop integrated environment. Besides the message handler for communication with the PC, an easy-to-use command-line tool for testing and debugging the functionality of the hardware has been added.



PCB of the 3D audio correlator system. The front side (right) shows the angular display with the power level indicator in its center, the FPGA and a RAM buffer. The CohereChip is visible on the back side of the PCB (left).

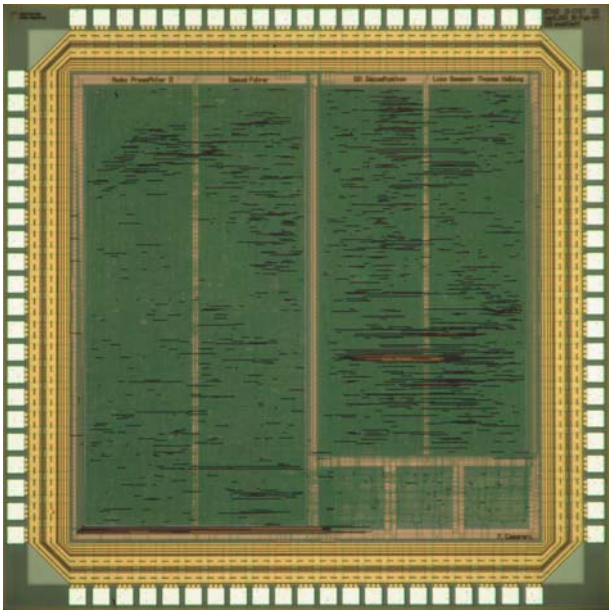
ASIC Design: Multi-Channel Digital Audio Preamplifier Simulation

Personnel: Samuel Fuhrer;
Norbert Felber, Marc Wegmüller (assistants)

Thesis: Semester Project

Digital audio equipment is rapidly conquering the consumer market. With the advance of the DVD player and home cinema systems supporting multi-channel audio, digital signal flow and signal processing have gained importance. Devices that still produce analog outputs, like CD players, will be superseded by cheaper all-digital systems in the near future. The goal of this semester thesis was to design a digital integrated circuit, that implements important features of a digital preamplifier as found in home audio systems on a single chip.

The functionality of a digital preamplifier ranges from a simple stereo volume control to a multi-channel audio system with many features. From the beginning, it was the goal to create a chip that can handle 5.1 surround sound. The look and feel of the complete system should be the one of a classical analog amplifier with many analog items. The desire for multi-channel sound lead to the decision to implement a matrix decoder that can derive surround, center, and bass channels from a two channel stereo input signal. The chip is as well able to process true six-channel audio through a surround input. Additional features include a bass and treble filter and a programmable delay of the surround channels. To imitate the user interface of old-fashioned amplifiers, knob encoders are supported as control inputs. Multiple audio source inputs enable the chip to act as a central unit that can handle a great range of audio devices like CD player, tuner, minidisc and DVD player.



Chip photograph of Multi-Channel Digital Audio Preamplifier.

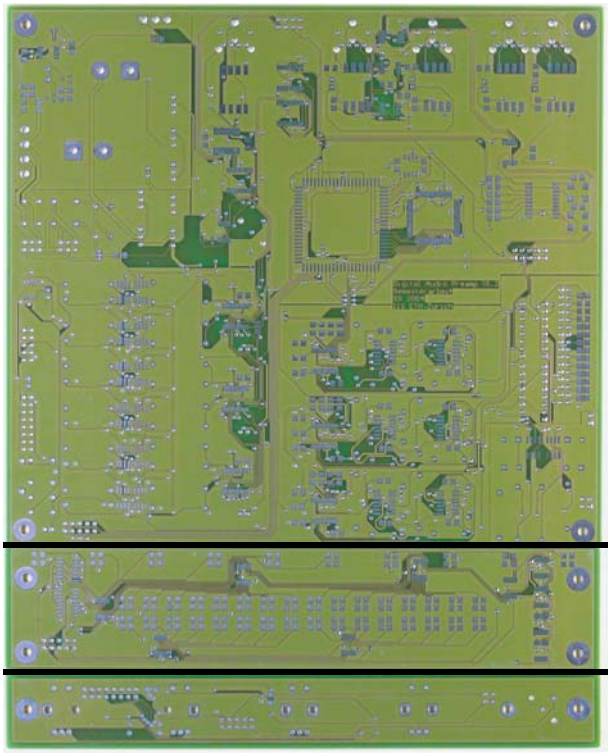
System Design: Multi-Channel Digital Audio Preamplifier

Personnel: Philippe Hefti, Tobias Tomaschett;
Felix Bürgin, Norbert Felber (assistants)

Thesis: Semester Project

The aim of this project was to implement a complete digital audio preamplifier based on the student chip described in the column to the left. The system contains numerous analog and digital (optical/coax) inputs. Three outputs are provided: analog line, headphone, and digital, the latter with selectable word width and sampling frequency. Additionally, the system features the emulation of surround channels with adjustable delay. Many sound parameters, such as volume of all channels, balance and trebble can be adjusted by the user. LED bars display the level of the parameter currently being changed. Ten LEDs show the selected actual input and its type (analog or digital). Active digital de-emphasis and clipping of the audio signal are indicated as well. In case of a power down all settings are saved into an EEPROM, which will be restored when the system is switched on again.

A printed circuit board (PCB) has been designed which connects the central ASIC to all other components and circuits for the analog and digital signal conditioning and the user interface. To simplify the mechanical construction, the PCB has been split up into three smaller subboards which are currently being soldered and tested.



Photograph of the designed printed circuit boards. The upper part is the main board. The middle one will carry the LEDs. The small board at the bottom will be populated with the knob encoders.

ASIC Design: Digital Audio Stereo Preamplifier

Personnel: David Stadelmann, Thomas Zurbrügg; Felix Bürgin, Norbert Felber (assistants)

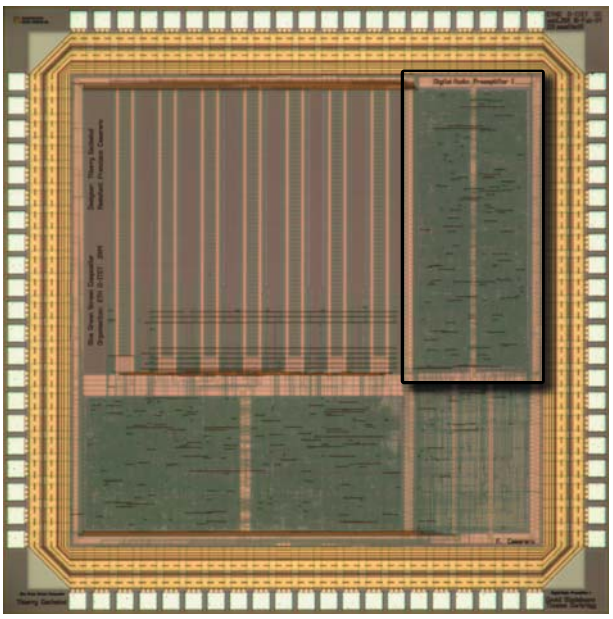
Thesis: Semester Project

The aim of this semester project was the design of a digital audio preamplifier chip. The main task of such a preamplifier is to give the user the choice among different digital and analog audio sources at its input. Usually preamplifiers do not contain complex digital signal processing. This design contains only a de-emphasis filter, volume and balance adjustment. For further demands, the chip features an additional interface to perform more sophisticated digital signal processing externally. Stereo data are input and output via common *I2S* interfaces with 24 bit resolution and 96 kHz sampling frequency.

The user interface provides knobs for the input selection, volume and balance adjustment. The input selection knob allows to choose from a set of four analog and four digital inputs. The external filter loop can be disabled or enabled by a switch. For digital recording, a selected digital input source can be fed out directly. LED bars are supported to display the input and output levels as well as the positions of the volume and balance knobs.

The ASIC provides all the needed control signals for the externally required chips. Those include AD, DA and sample rate converters as well as digital audio interfaces (*AES/EBU* and *SP/DIF*, respectively).

The chip has been fabricated in UMC's 0.25 µm CMOS technology. The design runs at 24.576 MHz.



Die photo of the designed audio preamplifier. The design shares one die with another student project. The preamplifier is marked with a black frame in the top right corner of the die.

Digital Noise Generator for Audio Applications

Personnel: Christof Küng, Blaise Lovisa; Peter Lüthi, Norbert Felber (assistants)

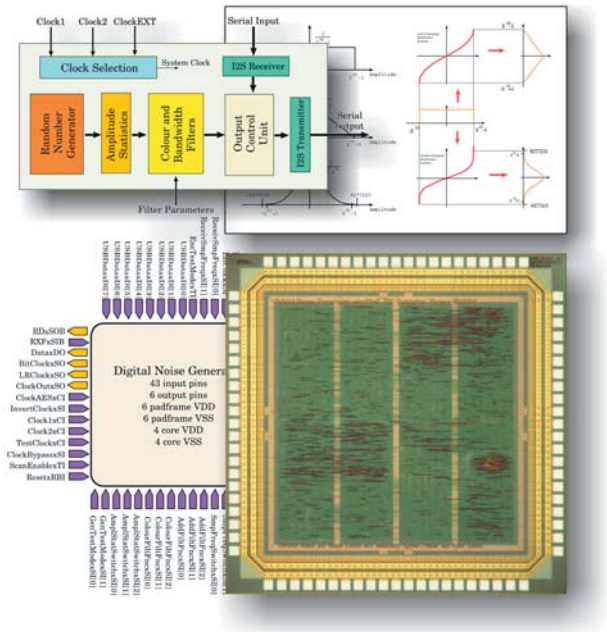
Thesis: Semester Project

For profound testing and characterization of audio devices or room acoustics, noise signals with dedicated properties are required. This ASIC design is a digital noise generator, intended either for audio testing of telecommunication equipment, head sets, and amplifiers, or transmission pathes such as auditorium equalization.

The random number generator is based on so-called Gold sequences, which form a class of sequences that have good periodic cross-correlation properties. For this implementation, the Gold sequence has a period of 2^{25}-1 samples, what corresponds to 85 s at 192 kHz. The random number generator produces 24 bit output samples, which are then delivered to the amplitude statistics block, applying either gaussian, triangular or uniform distribution.

The noise generator can be used in two basic operation modes: as a stand-alone noise generator, issuing noise samples with the selected sample rate (32, 44.1, 48, 88.2, 96, 176.4 or 192 kHz) or in slave mode, where the chip generates a noise sample for every received sample of an input signal. In slave mode, the chip may output either the input signal added with noise, or only the noise signal.

The system has been integrated using a core size of 1.76 mm² in UMC 0.25 µm 5M1P 3.3 V CMOS technology, running at a maximal clock frequency of 45.5 MHz.



Digital Noise Generator ASIC supporting audio sample rates up to 192 kHz.

Blue/Green Compositing ASIC

Personnel: Thierry Gschwind;
Francisco Camarero (assistant)

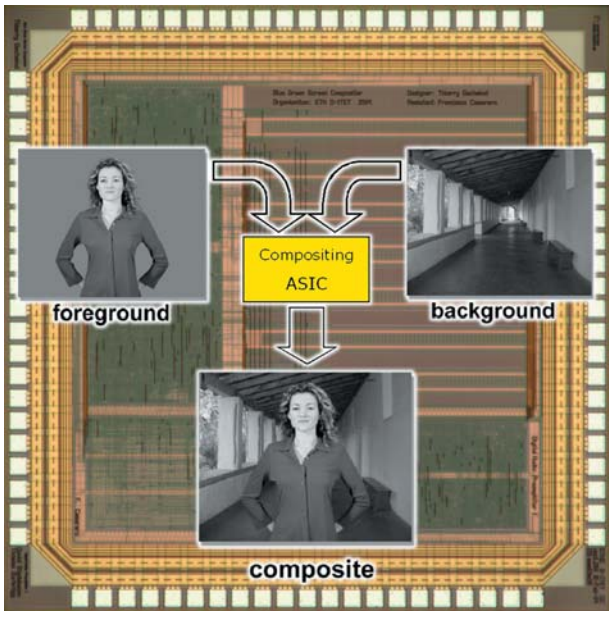
Thesis: Semester Project

The first compositing in History was made in 1857. The photographer Oscar G. Rejlander took 32 different pictures and composited them together. In the beginning of motion pictures compositing was done by two different methods: either filming in front of a screen were another movie was projected, or by partially exposing the film negative to light, and later exposing the other part. The principal reason for using composites is to save costs, or because it would be impossible to film a scene as such, e.g. space ship movies.

This project implemented a real-time compositing ASIC that takes two ITU-R BT.656 video streams (background and foreground), extracts the foreground object from the constant (green or blue) background in the foreground video stream using a color difference method, and composites it over the background video stream to output a new ITU-R BT.656 compatible video stream (composite).

Internal color space conversions from YCrCb to RGB and back, and several other operations (matte refine, despill, color match, subsampling, etc.) are implemented and user configurable in order to enhance the quality of the composite depending on the situation.

The design has been successfully integrated in a 0.25 µm standard CMOS technology on a multi-project die that contained one additional student project and the corresponding de-/multiplexing logic for the I/O pads.



Two ITU-R BT.656 video streams are composited in real time (composited with the chip photograph).

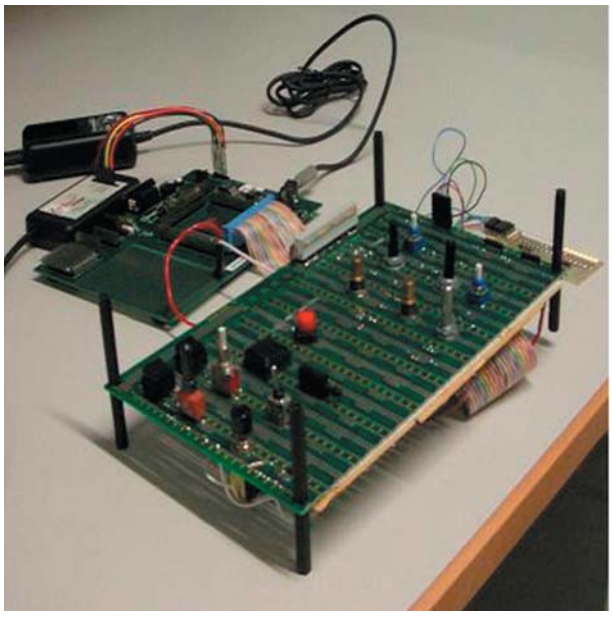
Audio Level-Control System

Personnel: Vedran Galijas;
Marc Wegmüller, Norbert Felber (assistants)

Thesis: Semester Project

An audio mixer is an electronic device that handles a lot of different types of control units and displays. Numerous control switches enable amplifier configurations for several channels and give feedback by visual display of actual control settings. Multiple modes allow area optimized usage of many types of pushbuttons, knobs, diodes and LED bars. Reconfiguration and flexible allocation of dedicated mixer devices are main features of a future-proof electronic control system.

The implementation of this audio level-control system is realized as an FPGA prototype with many different I/O connections on a separate interface board. The architecture is channel-ordered and adaptable to different types of push-buttons, encoders (rotating knob) and LED-bars. Special features are direct or coded controls, accelerated knob reaction, linear-logarithmic conversion, physiological brightness display and dual-channel encoding with LED bars. Configuration is realized by a serial processor interface writing status register, selecting dedicated standard blocks and connecting input and output ports through a switching matrix.



Audio level-control system implemented on a Spartan2 demo board interfacing multiple push-buttons, encoders and LED-bars.

CMOS Current Steering DAC

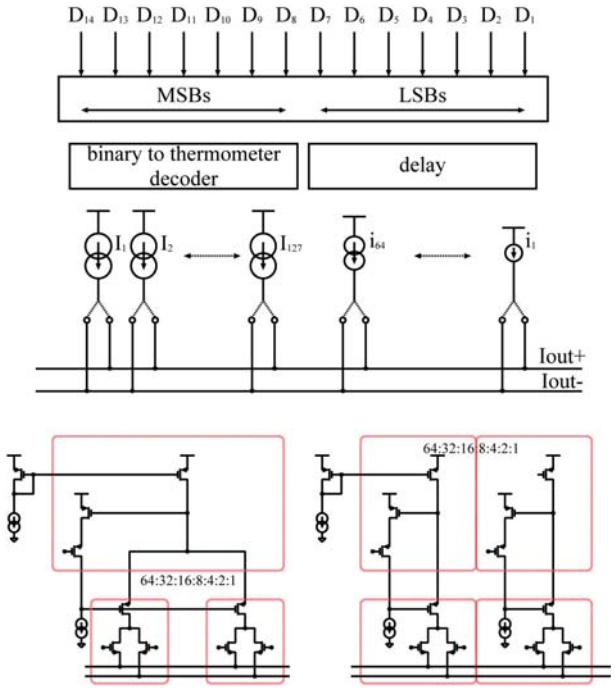
Personnel: Chen Wang, Xiao Zhen;
Pier Andrea Francese (assistant)

Thesis: Semester Project

High-speed Digital-to-Analog Converters (DACs) are fundamental blocks in various mixed-signal applications. The economical benefit of implementing those systems in deep-submicron CMOS technology drives the demand for CMOS DACs. The current steering architecture is commonly chosen because it does not require any process option and is capable of operating at very low power supply. Scope of the work was the analysis and design of a 14 bit current steering DAC in 0.13 μm CMOS technology.

A very important performance metric is the spurious-free-dynamic-range (SFDR) that exceeds 80 dB in the best published works. In order to aim at such high SFDR levels, the output impedance of the unit current cells making up the DAC current array has to be very high. Therefore regulated cascoded current sources are adopted in this project.

The systematic and random mismatches between all the current sources affect the DAC linearity. A full mismatch analysis within each regulated current source is carried out to determine the dimensions of the transistors. The mismatch analysis covers also the two different implementations for the LSB current array that are depicted below.



The current array is segmented into 127 identical current sources, controlled by the thermometer decoded 7 MSBs of the 14 bit input word. The remaining 7 LSBs control seven binary scaled current sources.

Programmable Base-Band Filter for a Multi-Standard Wireless Receiver

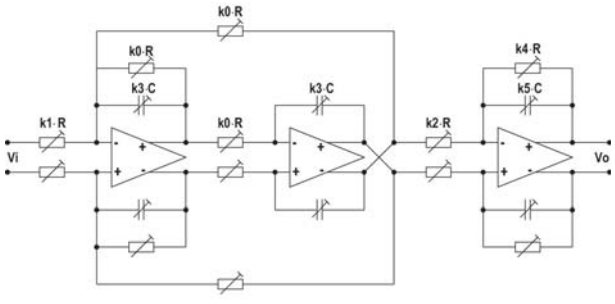
Personnel: Oliver Isler, Vaibhav Maheshwari,
Silvan Wehrli;
Thomas Burger (assistant)

Thesis: Semester Project

In the last couple of years the direct-conversion receiver architecture has become more popular because it allows a higher integration density to be realized. This is particularely interesting with modern CMOS technologies that are capable of handling the RF signals as well. For such an architecture the essential channel filtering and signal amplification has to be realized at base-band which makes this task more demanding as with a conventional multi-conversion architecture where filter and gain stages are distributed over IF and base-band to relax the requirements. The main advantages of a single filter at base-band is flexibility and ease of integration. With this concept the realization of a configurable filter serving different standards becomes possible.

In two consecutive semester thesis projects the students investigated the circuit implementation of the same prototype 3rd order Butterworth low pass filter (figure). The filter topology is chosen to facilitate variable gain-settings and corner frequencies by connecting resistors and capacitors in parallel or in series to change the k-coefficients accordingly.

The investigated circuit techniques included 1) active RC (figure), 2) OTA-RC (high instead of low output impedance amplifiers), and 3) gm-C (poles are realized by a transconductance gm and a capacitor C in open loop). It was found that the active RC implementation is best suited to meet the stringent linearity and noise requirements of the filter. The OTA-RC and gm-RC implementations can lead to significantly lower power consumption for large signal bandwidth (>5 MHz), but they did not meet the high linearity requirements.



$$\frac{V_o(s)}{V_i(s)} = \frac{k_0 k_4}{k_1 k_2} \cdot \frac{1}{(1+sk_4k_5RC)(1+sk_0k_3RC+(sk_0k_3RC)^2)}$$

Prototype 3rd order Butterworth low pass filter, shown as active RC implementation. As filter topology a bi-quad (Tow-Thomas) and a single stage are cascaded. Variable gain and corner frequency is obtained by the k-coefficients.

A Clock Generator with Wide Tuning Range in 0.13 μm CMOS

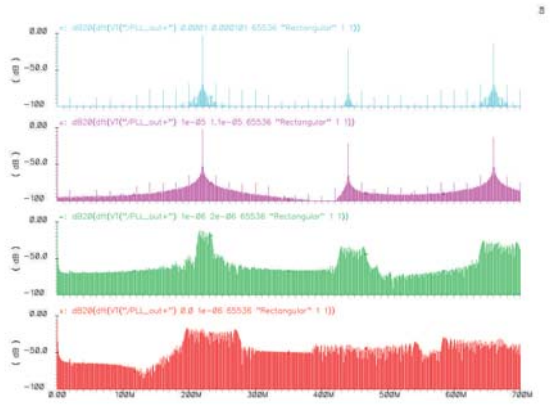
Personnel: Sven Mumenthaler;
Thomas Burger (assistant)

Thesis: Semester Project

In the last years it has become clear that a broad set of wireless standards will coexist in the foreseable future. Even if one looks at a particular application such as e.g. cellular, the second generation standards such as GSM will coexist for a long time with the upcoming third generation standards such as WCDMA or cdma2000.

Therefore the manufacturers are looking for terminal solutions that are capable of multi-standard operation while using the same basic hardware. Direct conversion receivers are particularily well suited for the implementation of such multi-standard terminals. Because there is no channelization at IF, all analog and digital signal processing for conditioning of the received radio signal can be done at base-band where the flexibility to satisfy different requirements in terms of dynamic range or signal bandwidth is highest.

This semester thesis seeked to make a contribution for the base-band receive part of a multi-standard terminal based on direct-conversion architecture. It provides a very flexible clock source for the analog-to-digital converter (ADC) and the digital front-end that follows it. Based on a fixed external frequency derived from a crystal oscillator, it supports clock generation at rational number ratios by a reference clock divider and an integer-N PLL. A ring oscillator with a wide tuning range is used as VCO. With this choice output frequencies from 10 MHz up to 300 MHz can be obtained which are suited to drive an over-sampled ADC.



Short-time spectrum (1μs) of the single-ended clock generator output after 1μs (bottom), 2 μs, 10μs and 100μs (top) from a 220 MHz clock.

USB Audio System

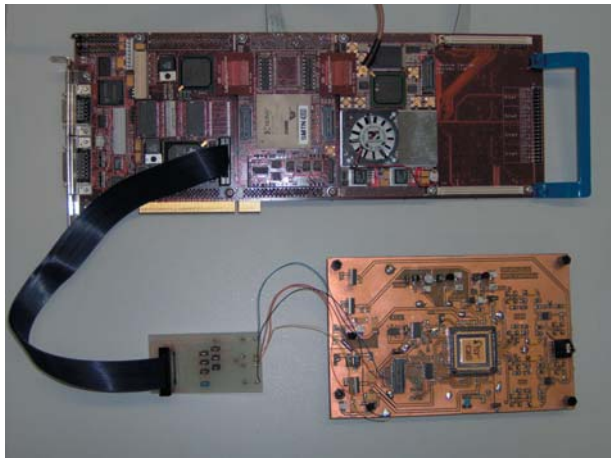
Personnel: Tareq Hossain, Reto Stalder;
Andreas Burg, Chiara Martelli (assistants)

Thesis: Semester Project

Modern PCs are more and more incorporated into consumer electronics systems in order to support audio and video applications. PC users employ any types of sources and sinks despite any standard or interface. A a global synchronization of sources and sinks is clearly not feasible, this project solves the problem for the case of an USB audio sink by implementing an adaptive sample rate converter: The data are sent via USB interface at a certain rate, re-sampled with to the local master clock, and converted into analog.

The system is divided into two main parts: A DSP belonging to a stand-alone subsystem handles the communication via USB and the estimation of the audio data rate, and an ASIC re-samples the incoming data and then converts them into an analog signal. The analog output of the ASIC is sent to the user's audio device through an off-chip active analog low-pass filter.

The ASIC has been integrated during a previous student project in 0.18 μm CMOS technology. The DSP has been programmed in C to emulate the USB data transfer protocol and execute the frequency estimation algorithm. The DSP reads audio data from the PC through the PCI bus, estimates its rate, serializes and sends it to the ASIC, together with the frequency estimates. A custom PCB has been implemented to carry the ASIC, in accordance to the DSP system interface. The ASIC reads the serialized data signal and re-samples it according to the local master clock of 6 MHz. After on-chip D/A conversion and on-board low pass filtering, the audio-signal is sent to a logic analyzer to measure the system performance. The adaptability of the ASIC has been proven in the whole range of input sampling frequencies from 5 kHz to 55 kHz; due to an error in the on-board low-pass filter, the SFDR of the DAC couldn't be measured.



DSP board connected to custom ASIC board.

AGC for a MIMO Testbed

Personnel: Kun Fang;
David Perels, Daniel Baum (IKT-ETHZ) (assistants)

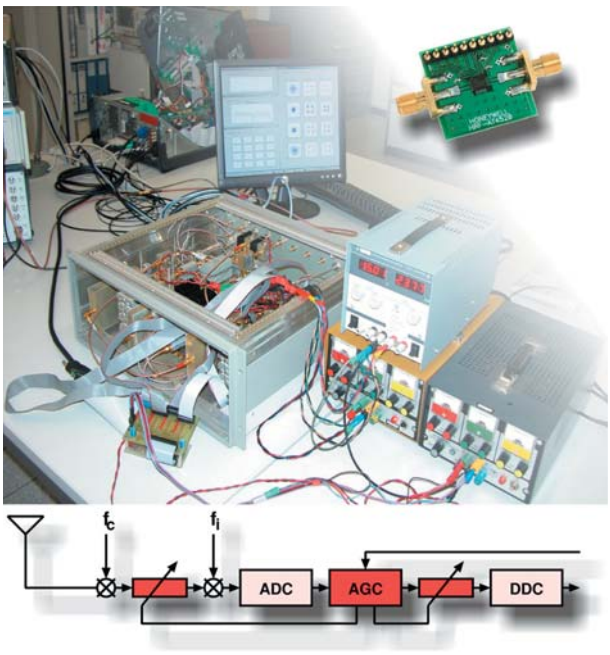
Thesis: Semester Project

This work is part of the MIMO-OFDM (Multiple-Input Multiple-Output) testbed project.

The Automatic Gain Control (AGC) is an important part of the frontend of a receiver. Its task is to achieve an optimal signal power level at both the AD converter and the input of the Digital Down Converter (DDC) in order to use the full digital dynamic range of the subsequent blocks. The control loop should settle as fast as possible since any change of settings in the AGC distracts subsequent tasks such as synchronization and frequency offset estimation.

In the analog frontend a digitally controllable attenuator has been integrated. It enables to adjust the input signal to the optimal power level for the analog domain. In the digital domain, the signal may be additionally amplified if the analog variable attenuator is set to maximal gain due to a too weak input level.

The algorithms have been simulated in MATLAB™ and different effects of components comprising the AGC have been investigated. A solution for the control of the variable attenuator by the host PC was investigated and has been realized. The optimized algorithm has finally been implemented in VHDL, integrated into the frontend and characterized.



The bottom image gives an overview with the red blocks representing the different parts of the AGC. At the top right the variable attenuator is shown which has been integrated into the testbed which is visible in the background.

Wireless Ethernet Bridge

Personnel: Frederic Poncioni;
Andreas Burg, Simon Häne (assistants)

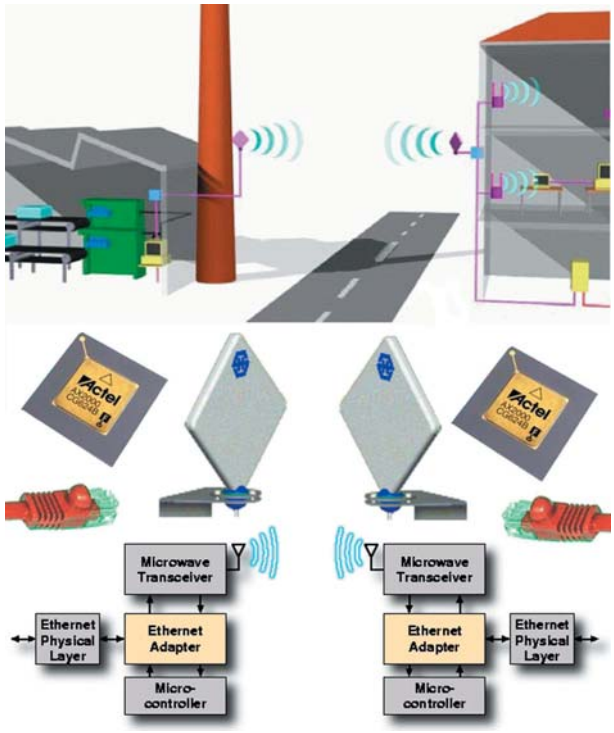
Thesis: Semester Project

Partners: Huber+Suhner

The Huber+Suhner microwave communication system replaces cables of an Ethernet network by a fully transparent wireless connection. A typical application scenario is the interconnection of buildings across public roads or places, where no wires can be installed.

The goal of this project was the development of the logic that connects the wireless system to the Ethernet network. The design is based on an Open-Core IP-module that provides a standard interface to an Ethernet physical layer ASIC. This module has been adapted and extended to fulfill the requirements of the Huber+Suhner wireless system. Besides the data connection, the system also provides an interface to a microcontroller for monitoring and configuration.

The VHDL code has been optimized for an implementation on a low-cost ACTEL FPGA.



Application scenario for the Huber+Suhner wireless Ethernet bridge (top) and its key components (middle) together with a block diagram of the system (bottom).

Versatile Digital Audio Processing Board

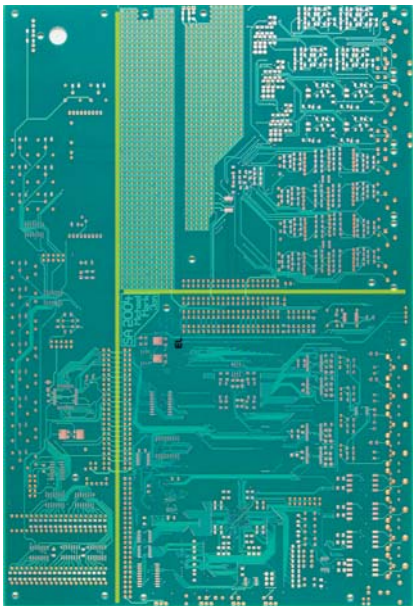
Personnel: Mark Blum, Jon Rohrer, Michael Deman; Norbert Felber, Peter Lüthi (assistants)

Thesis: Semester Project

The PPS (Project, Practical, Seminar; for first to fourth semester students) with the topic Digital Audio was based so far on a printed circuit board (PCB) containing a digital signal processor (DSP) ADSP21065L, a stereo codec, and some user interface facilities. During the four years of PPS a lot of individual add-ons have been realized in order to augment the functionality.

The goal of this semester project was to design a new PCB which supports a larger scope of possible projects with one versatile board. The students have developed a PCB in such a way that it can be cut into three units if required, one with all digital audio components, one with the analog audio ports, and a third with the user interface.

The digital section contains 8 digital audio input channels with SP/DIF receivers (DIR1703) and sample rate converters (SRC4193), a DSP with 3 times more processing power than the predecessor (ADSP21161), and 8 digital outputs (DIT4192). To connect all chips and provide flexibility, an FPGA is included. Furthermore, an USB interface allows connecting a PC for control and data exchange. The analog section contains an 8+2-channel codec (AD1835A), 3 stereo A/D converters (PCM1804), and all analog anti-aliasing and reconstruction filters. The user interface hosts a microprocessor (PIC16F77), an LCD display, an encoder knob, push buttons and an IR remote control receiver.



Four-layer printed circuit board developed in this semester project. Right top is the analog and right bottom the digital section. The left part is the user interface board. If required, the sections can be separated and connected by cables.

Coprocessor Evaluation Environment for PowerPC

Personnel: Daniel Engeler; Silvio Dragone (assistant)

Thesis: Master Thesis

Partners: IBM Research

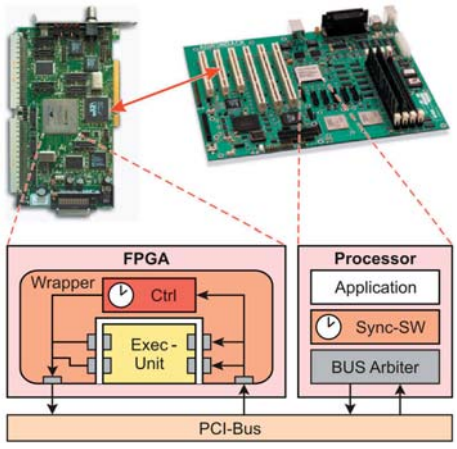
The performance of a new System-on-Chip (SoC) design has to be quantified as early as possible to ensure the anticipated performance. In this Master Thesis, a coprocessor evaluation environment for PowerPCs has been developed. The emulator is targeted to benchmark and validate coprocessors under development.

Two types of coprocessors are supported: tightly and loosely coupled ones. Tightly coupled coprocessors are datapath extensions for the processor itself. Loosely coupled coprocessors in contrast are stand-alone units connected to the processor over a on-chip interconnect system, e.g. a parallel bus.

As shown in the block diagram below, the benchmark application runs on the actual processor, and the coprocessor is loaded into an FPGA on a separate board with PCI interface. The application can access the coprocessor via the so-called middleware (Sync-SW). It sends the requested instruction over the PCI bus to the wrapper. The coprocessor consists of the execution unit and the wrapper. After processing, the wrapper returns the result of the instruction and the measured time information to the middleware. The middleware passes the result to the application.

To accurately benchmark an emulated coprocessor, the emulation overhead must be hidden from the performance measurement by modifying the benchmark timer. Furthermore, the middleware must not influence in any way the data flow of the application such, as overwriting the content of the data cache.

The functionality of the platform has been proved by successfully emulating a floating-point unit for the PowerPC with the freely available benchmark MiBench.



The picture shows the hardware of the prototyping platform (processor and FPGA board) with a diagram of the emulator functionality.

Simulation of 1.3 Micrometer VCSEL with Tunnel Junction

Personnel: Beat Hangartner;
Matthias Streiff, Stefan Odermatt (assistants);
UCSB: Joachim Piprek

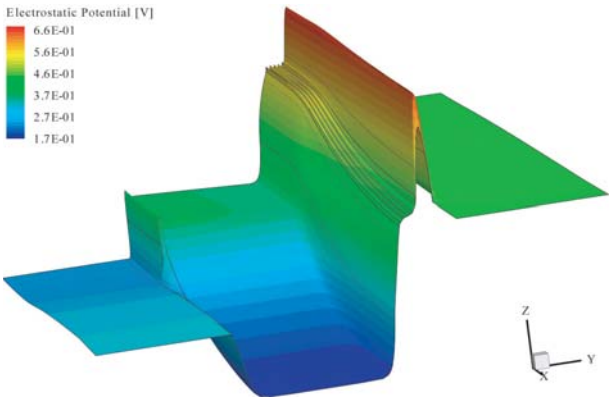
Thesis: Master Thesis

Partners: UCSB

Long-wavelength VCSEL are of great interest in next-generation metropolitan network access infrastructure due to low cost, high bandwidth and ease of use. In this work, for the first time, a long-wavelength high performance vertical-cavity surface-emitting laser (VCSEL) device was investigated using the DESSIS electro-opto-thermal device simulator.

The device has an optical resonator formed by two distributed Bragg reflectors (DBR). These are grown in the AlGaAs/GaAs material system, and are wafer bonded to the InAlGaAs active region. The latter contains five strained quantum wells. Moreover, a laterally structured buried tunnel junction is used for current and optical mode confinement. Intra-cavity contacts are employed as electrodes.

A stand-alone tunnel junction was simulated with different tunneling models. It was shown that non-local tunneling models are able to match the device characteristics for forward and reverse bias operation quantitatively. Local tunneling models, in contrast, are only valid for forward biasing. The optical properties of the VCSEL cavity were investigated in detail. The wavelength and losses of the cavity are in good agreement with measurements. Finally, good agreement was also obtained between measurement and simulation results in fully coupled electro-opto-thermal simulations.



Profile of electro-static potential in cross-section of long-wavelength VCSEL device with tunnel junction and intra-cavity contacts.

Nonequilibrium Model for Semiconductor Laser Simulation

Personnel: Manuel Aschwanden;
Stefan Odermatt, Mathieu Luisier (assistants)

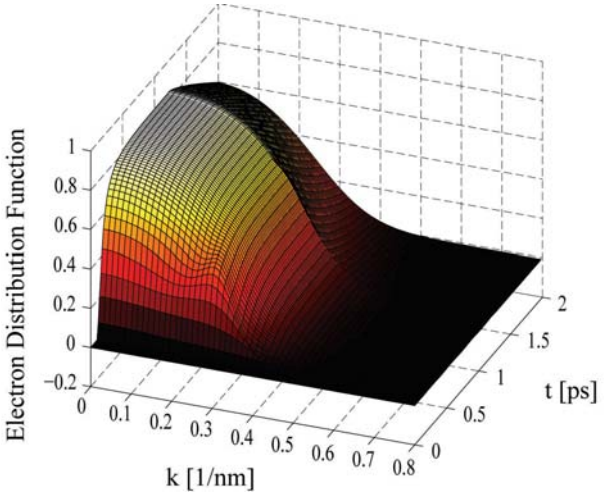
Thesis: Semester Project

In this project, a model for nonequilibrium effects in quantum-well semiconductor lasers has been investigated. In order to achieve this, microscopic equations for the polarization and the distribution function are self-consistently solved in the framework of the so-called semiconductor Maxwell-Bloch equations.

The aim of this computer-based study is to understand effects like spectral hole burning and the influence of the nonequilibrium carrier distributions to the laser modulation response: At high laser intensities and for events on a pico-second time scale, the carrier dynamics can not equilibrate the distribution functions towards the Fermi distribution and the conventional semi-classical adiabatic theory breaks down.

The model implemented in this project was also used to simulate the nonequilibrium effects of optical pumping in the active region on the distribution functions: It has been shown that in this case, the spectral holes in the distribution function have major influence on the device characteristics.

It is shown below, that spectral holes build up in the momentum space (k-space) where carriers recombine and photons are emitted.



Time evolution of the electron distribution function in the quantum well. A spectral hole in the distribution function occurs where carriers recombine (at around k=0.15nm).

Simulation of Semiconductor Quantum-Well Lasers using Gain Tables

Personnel: Beat Hangartner;
Stefan Odermatt, Valerio Laino (assistants)

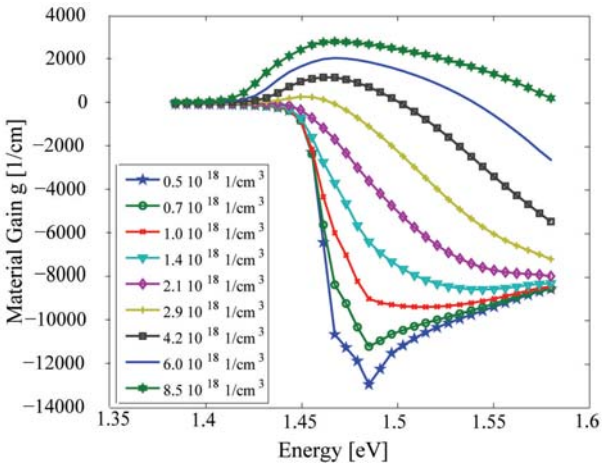
Thesis: Semester Project

Partners: ISE AG

Semiconductor lasers are important light sources for fiber-optic communications and are key components of sensing applications. Comprehensive device simulators are becoming essential tools to explore the parameter space for optimizing these components. These simulators require multidimensional, physics-based models such that the simulation input can be restricted to geometry and microscopic material parameters.

Microscopic material gain is one of the key parameters required to describe the characteristics of the laser correctly. Therefore, the most accurate models available have to be used to describe the material gain. Since it is extremely time-consuming to calculate gain at runtime, in this work, the material gain is calculated in a preprocessing step.After its calculation for different wavelengths, carrier densities and temperatures, the results are stored in a so-called “gain table”. During the laser simulation, the actual material gain is calculated from the gain table through interpolation.

This allows to speed up the simulation time and to use accurate microscopic gain models at the same time. Usually, the band structure is calculated with a 8-band kp method and the material gain is calculated in the framework of the semiconductor Bloch equations. Many-body effects are taken into account by the Second Born approximation.



Excerpt of a gain table for a GaAs-AlGaAs laser. The band structure is calculated with a 8-band kp method and the material gain is calculated in the framework of the semiconductor Bloch equations.

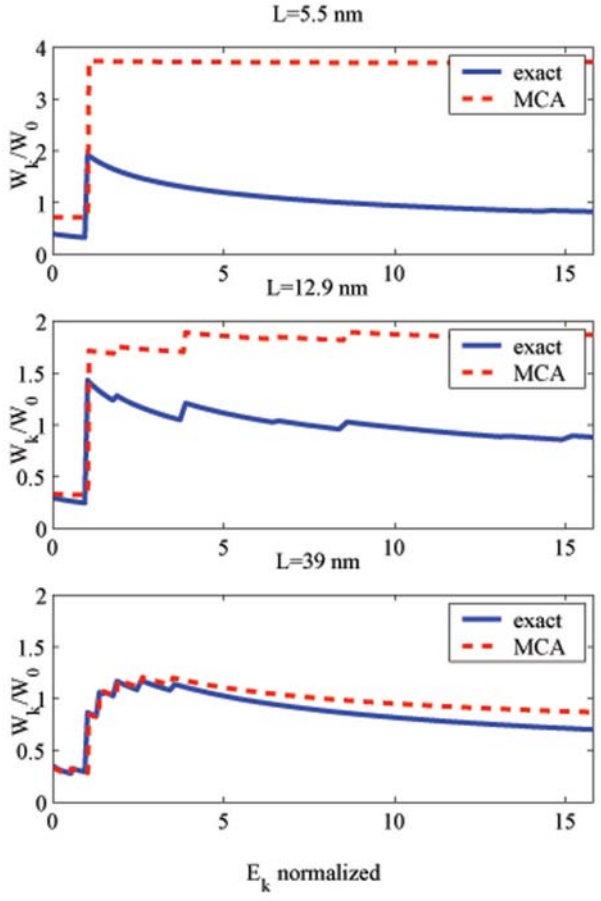
Simulation of Scattering Processes in Quantum-Well Lasers

Personnel: Zoltan Schlegel;
Stefan Odermatt, Mathieu Luisier (assistants)

Thesis: Semester Project

Scattering processes are very important in quantum well (QW) semiconductor lasers because they determine the replacement rate of carriers lost during the creation of a photon. Among these processes, electron-optical-phonon and electron-electron scattering are significant but, while the latter process occurs at high carrier densities, electron-optical-phonon interactions are always present and dominate at low carrier densities.

Therefore, in this semester work, the electron-optical-phonon capture rate between different QW energy subbands was calculated using Fermi’s Golden Rule. Two different models were studied: the so-called momentum conservation approximation (MCA) and the exact calculation taking rigorously into account the interactions between the different QW wave functions. It was noticed that, when the QW width increases, the two models give more and more the same results for the electron-phonon scattering rate.



Comparison between the MCA (momentum conservation approximation) and the exact calculation for the electron-phonon dephazing rate.

Simulation of Scanning Spreading Resistance Measurements

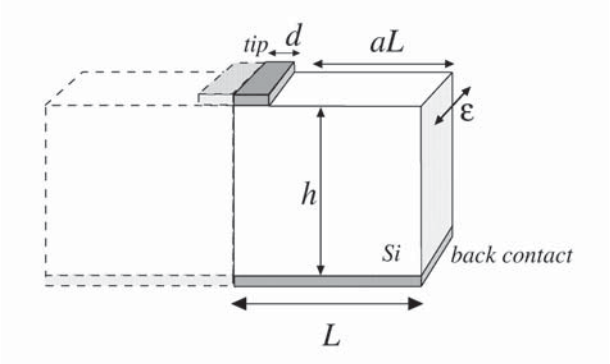
Personnel: Mauro Chiappini;
Maria Stangoni, Mauro Ciappa (assistants)

Thesis: Master Thesis

Partners: Uni Perugia

The aim of this work is to assess the efficiency of the models used to simulate the Scanning Spreading Resistance Microscopy (SSRM) measurement process. 2D simulations have been performed in order to set up a preliminary structure. The optimization of the accuracy of the simulation model is achieved by comparison of the obtained data with the results of analytical equations. This allows to investigate the impact of the model size, model boundaries, and of the grid density on the accuracy of the results, keeping under control the computational time. The sample has been modeled as a rectangle of silicon, the backside and the tip contacts are considered as two ohmic electrical boundary conditions. The mesh grid has been built with the classical box method, a coarse mesh is defined for the whole rectangle, while a refinement is added in a square region below the tip contact.

During the simulation a voltage ramp has been applied to the tip of the microscope, while the backside has been kept to ground. As a result, a current flows into the silicon, spreading from the tip contact. The IV characteristic for this simple model is linear, and the overall resistance is calculated from its slope. In the case of homogeneous doping concentration, the simulation time is reduced by simulating just one half of the model, making use of the symmetry of the structure. The simulator delivered a resistance related to a default thickness of the model of 1 μm. The analytical expression used to validate the simulation and to convert the simulated resistance into the resistivity is derived from the Hall's formula. A geometry depencence has been defined in 2D, therefore a 3D simulation is required for a quantitative simulation of SSRM. The same procedure has been successfully applied, with some precautions, also to non-homogeneous doping distributions and to pn-junctions.



Sketch of the geometrical structure used for the 2D simulation of SSRM. The tip contact has a blade shape along the default length ε =1 μm. In case of homogeneous doping concentration only half the structure is simulated (dashed line).

3D Simulation of Scanning Probe Techniques for Dopant Profiling

Personnel: Camilla Coletti;
Maria Stangoni, Mauro Ciappa (assistants)

Thesis: Master Thesis

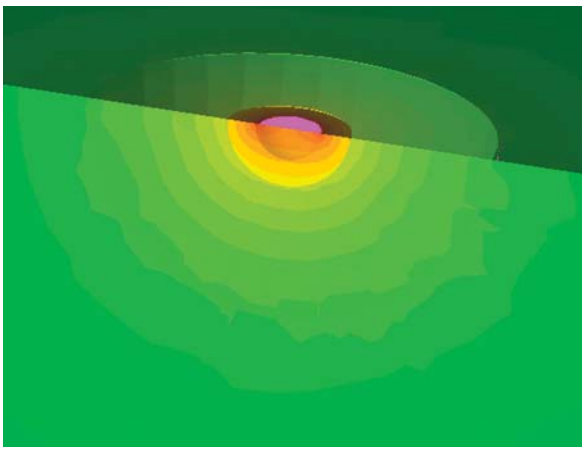
Partners: Uni Perugia

Significant aspects of Scanning Probe Techniques like Scanning Capacitance Microscopy (SCM) and Scanning Spreading Resistance Microscopy (SSRM) are still under investigation. The complexity of the physical system created by the measurement itself requires a thorough study for the interpretation of the output data.

With the aid of device simulation it has become possible to highlight some aspect of the physics involved. In order to set up a grid structure with proper boundary conditions, both techniques have been considered separately. Besides, the possibility to execute full 3D simulation within a reasonable cpu time yields to quantitative results that can be easily validated, especially for SSRM. The simulation model used to perform SSRM simulations is a block of silicon, whose dimensions are 2 mm x 2 mm x 1 mm. The backside contact is as large as the bottom surface, while the sensing tip is modeled as a circular contact positioned in the center of the top surface. Both tip and backside contacts are modelled as ohmic boundary conditions. The tip contact radius is in the order of tens of nanometers reflecting the real tip dimensions.

A sequence of concentric shells of silicon are defined under the tip contact. Succesively, a boundary conforming mesh is created to follow the spreading of the current from the tip contact to the bulk. Theoretical studies report that the voltage decreases by more than 80% of the initial value within five tip radii, with a symmetrical distribution in the case of a homogeneous doping concentration.

The number of grid points created with the 3D simulation tool is acceptable such that a full 3D simulation requires about 20 minutes of cpu time on an Alpha Server 4x1250 MHz.



Section of the grid used for the 3D simulation of SSRM. A sequence of concentric hemispheres is generated under the tip contact (pink semicircle) up to a distance of about five times the tip radius.

Development of a Transmission Line Pulser

Personnel: Simone Sponton;
Chiara Corvasce, Davide Barlini (assistants)

Thesis: Master Thesis

Partners: Uni Padova, Infineon

The main scope of this diploma thesis was to investigate the selfheating behavior of different devices when submitted to Transmission Line Pulses (TLP) at different environment temperatures. The first nanoseconds of the pulse are of special interest.

The measurements enabled to extract calibration curves relating the voltage drop across the device with the average temperature within the device. TLP has been used to characterize buried silicon resistors, vertical p-n diodes, and ESD protections for smart-power technologies.

Since the relevant information has to be extracted from the first 10-20 ns of the pulse, the first critical point of the work has been to design and realize a dedicated TLP-system where the parasitic effects due to inductive loads, parasitic impedances, cables losses, and reflections have been minimized.

The TLP system has been operated up to environment temperatures of 800 K, in conjunction with a dedicated thermal chamber using connections with very low parasitic inductance.

Finally, several dedicated software tools have been realized to postprocess the acquired experimental data.

Labview-controlled Transmission Line Pulser developed in the thesis.

Quantification of Scanning Spreading Resistance and Scanning Capacitance Microscopy Data by Neural Networks

Personnel: Elisa Ricci;
Mauro Ciappa, Maria Stangoni (assistants)

Thesis: Master Thesis

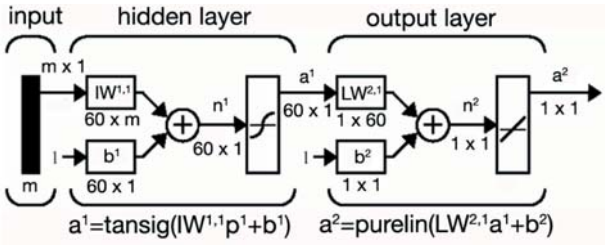
Partners: Uni Perugia

Scanning Spreading Resistance Microscopy (SSRM) and Scanning Capacitance Microscopy (SCM) had a large development in the last years, demonstrating good capability for two-dimensional dopant profiling of semiconductor devices. The quantification of the measurement data for both techniques requires to establish a unique correlation between the mapped electrical parameter (local carrier density) and the dopant concentration.

In the past, procedures making use of analytical formulas and complex self-consistent schemes have been proposed to solve the inverse problem, however with a limited success.The scope of the present diploma thesis has been to explore the feasibility of the use of artificial neural networks in combination with a device simulator to solve the inverse problem.

The first part of the work deals with the direct problem involving the solution of the drift, diffusion, recombination, generation, and of the Poisson's equations by a device simulator. The second section introduces the concept of neural networks. Multilayered networks and the method of the back propagation are extensively presented. A first network created to solve the one-dimensional direct problem (generating carriers profiles for arbitrary dopings) is developed to set the bases for the solution of the inverse problem. This network is implemented using the neural network toolbox of MATLAB, whereas the training set and test data are generated with DESSIS.

The last section deals with possible solutions of the inverse problem. The accuracy of the network in reconstructing one-dimensional doping profiles in case of arbitrary carriers concentrations has been assessed using experimental and simulated data.



The structure of the optimum artificial neural network developed to solve the inverse problem. It includes 70 hidden units and it has been optimally trained by the BFGS algorithm.

PhD Theses – Abstracts

Simulation Approaches for Nano-Scale Semiconductor Devices

Frederik Heinz

Topic of this dissertation are the development and implementation of a three-dimensional simulation environment for semiconductor nanoelectronics devices, that are dominated by quantum effects, and the modelling of the properties of various candidate structures for future ultra-large scale integrated circuits. In this context, Coulomb blockade in the presence of strong quantum confinement, quantum-ballistic transport and the effect of atomistic doping in aggressively scaled semiconductor devices have been studied. The simulation framework presented in this work extends the SIMNAD quantum mechanics simulator developed at the Integrated Systems Laboratory in a previous project and couples it to the standard device simulator DESSIS.

Basis of the simulation model is an effective mass formulation of density functional theory in local density approximation. In its generalisation to finite temperatures it may be used for the computation of the quantum mechanically correct charge distribution inside the device. Additionally, in conjunction with Bardeen's transfer Hamiltonian method, it may be used to compute tunnelling currents between classically insulated regions (channels, quantum dot) of the device. Doing so requires knowledge of the statistical mechanics of the quantum dot. To make the necessary phase space averages tractable, a Monte-Carlo approach is used.

On the classically conducting regions of the device the drift-diffusion model may be used for current computation. Coupling the device simulator DESSIS with the SIMNAD quantum mechanics simulator results in a simulation tool capable of modelling devices that feature both classical dissipative currents and 3D quantum effects.

Prof. Dr. W. Fichtner, ETH Zürich, examiner
Prof. Dr. G. Iannaccone, co-examiner

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Opto-Electro-Thermal VCSEL Device Simulation

Matthias Streiff

A physics-based software for the self-consistent electro-thermo-optical simulation of vertical-cavity surface-emitting laser (VCSEL) devices is presented. The simulator model is based on semiclassical microscopic laser theory. The model self-consistently describes spatially resolved quantities, namely, electrical potential, electron and hole densities, local temperature, and mean optical intensity. The input parameters to the model equations are the topology and the local physical material parameters. Static, small signal modulation, and transient device characteristics can be computed. The model is suitable for the analysis of a wide range of VCSEL types with realistic device structures.

The semiclassical laser model employs the slowly varying amplitude approximation: the optical field is decomposed into a given number of modes at discrete frequencies, and the temporal evolution of the mean electromagnetic energy in each mode is described by a separate photon rate equation. The optical modes are determined by solving Maxwell's vectorial wave equation, subject to an open boundary, taking into account diffraction of electromagnetic waves. Perfectly matched layer absorbing boundaries are used to model the open microcavity. Bulk electro-thermal carrier transport is modeled by a thermodynamic model that accounts for self-heating. At abrupt heterointerfaces a thermionic emission model is used. Electro-thermal transport in the distributed Bragg resonators is rendered by transport through a homogeneous region with an effective conductivity for heat, electrons and holes, and an effective heat capacity. Quantum wells are treated as scattering centres where ballistic transport applies for electrons and holes.

The VCSEL simulator is based on the DESSIS device simulator. The LUMI mode solver library was developed as an extension in order to handle the optical problem. The Finite Element Method is employed to formulate the physical equations: Box Method for the electro-thermal problem, and combined edge / node finite elements of different polynomial order for the optical problem. Expansions are in cylindrical coordinates assuming rotational symmetry of the device structure. The non-linear electro-thermal matrix equations augmented with a photon rate equation per optical mode are solved by Newton's Method. Solutions to the inhomogeneous form of Maxwell's wave equation are computed using a direct linear solver. The eigenpairs of the homogeneous form are obtained by the Jacobi-Davidson QZ algorithm with a suitable preconditioner. The electro-thermal together with the photon rate equations are coupled to Maxwell's wave equation employing a Gummel type iteration scheme.

The efficient computation of the optical modes based on a continuation scheme allows, for the first time, that Maxwell's vectorial wave equation — for VCSELs with realistic structures and optical sizes — subject to an open boundary, can be solved self-consistently with the electro-thermal device equations.

Simulation results are compared to measurements and show excellent agreement. In order to demonstrate the practical use of the simulator as a computer aided design tool a tutorial is given.

Prof. Dr. W. Fichtner, ETH Zürich, examiner
Prof. Dr. W. Bächtold, co-examiner

Diss. ETH-Nr. 15464
ISBN 3-89649-915-7

The Design of Direct-Conversion CMOS Radio Transmitters

Gabriel Brenna

The advent of the third generation mobile radio system UMTS has been a vehicle for extensive research in the area of high-performance transceivers. The demand for low-cost solutions has driven the focus towards eliminating expensive external components by the use of highly integrated architectures.

The stringent specifications of the WCDMA system poses significant challenges to the design of direct-upconversion CMOS transmitters, which forms the subject of this dissertation. Design techniques are explored that allow operation at low supply voltages, while still maintaining a sufficient signal-to-noise ratio at the output to provide the phone makers with the option to remove costly external filters and reduce the overall cost. A major challenge is to devise circuit and calibration techniques that sufficiently suppress carrier leakage over the complete gain control range.

This dissertation presents a highly-integrated, direct-upconversion transmitter IC implemented in 0.13μm CMOS technology and operating at a supply voltage of 1.5V. With carrier leakage suppressed by an automatic calibration loop including an on-chip RF power detector, the transmitter meets all specifications for type approval. It achieves good linearity, high unwanted sideband suppression and guarantees excellent linear-in-dB gain accuracy over its complete gain control range of 101dB. With 68mW, the power consumption is far lower than most published transmitters for this application in any technology.

This work demonstrates that direct-upconversion and CMOS technology are viable and cost-effective alternatives to superheterodyne and BiCMOS, not only for low-performance standards but also for very demanding applications such as WCDMA.

Prof. Dr. Q. Huang, ETH Zürich, examiner
Prof. Dr. M. Declercq, EPF Lausanne, co-examiner

Diss. ETH-Nr. 15495
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Direct-Conversion Receiver Design for Wideband Cellular Communications

Jürgen Rogin

This work describes the planning, design and implementation of a direct-conversion mobile radio receiver for the upcoming UMTS cellular telecommunication standard. Key aspects are passing type approval, a high integration level, and lowest possible power consumption.

Minimization of power consumption requires efforts on all levels of the design. The first step is to find precise system specifications from type approval requirements, because an overdesigned specification set directly leads to excessive power consumption. Once receiver requirements are known, a suitable architecture is chosen, and block level requirements are derived. WCDMA receiver interference level is dominated by TX leakage, and the use of an extra RX filter relaxes demodulator linearity requirements for lower power consumption despite the need for a second LNA.

Direct conversion promises the highest integration level, but poses several well known challenges for the RF mixer and the baseband filter and programmable gain amplifier. The most fundamental problem is that of baseband offsets, which may be orders of magnitude larger than the wanted signal at the baseband input. Consequently, the second main part of this work focuses on the design of the baseband strip and on offset compensation, together with the problems arising from the combination of continuous operation and programmable gain.

The circuit-level design phase is the last step determining power consumption. Measured performance of the prototype receiver realized in 0.13μm CMOS meets specifications for type approval,and power consumption is a very low 45mW.

Prof. Dr. Q. Huang, ETH Zürich, examiner
Prof. Dr. Kari A. I. Halonen, co-examiner

Diss. ETH-Nr. 15506
ISBN 3-89649-928-9

Coulomb Correlation Effects in Silicon Devices

Frank Geelhaar

Topic of this doctoral thesis are the correlation effects between the charge carriers in semiconductors which originate from the long-range Coulomb interaction. In particular, their relevance to the operation of silicon devices is considered.

In the first part, the formation of bound states and the plasma-induced band gap narrowing are investigated. A many-body Green's function formalism is employed in which the random phase approximation (RPA) for the self-energies is complemented by statically screened, higher-order ladder terms. Alternative concepts of an effective compound particle, the quasiexciton, are introduced and discussed. A numerical analysis indicates that bound states are insignificant at room temperature, contrary to claims that can be found in the literature. Results are presented for the density-dependent, rigid valence and conduction band shifts which suggest that the band gap narrowing is well described by the RPA alone.

The second part deals with the ohmic transport properties of the electrons and holes, as derived from the linearised Boltzmann equation. First, the relaxation time approximation (RTA) for phonon and ionised impurity scattering is treated. Then, a generalisation of Kohler's variational principle is formulated which accounts for intra- as well as interband carrier-carrier scattering processes. The Chapman-Enskog method is employed to compute the low-field mobilities, both in the T-matrix approximation (partial wave method) and the Born approximation. Concerning the room temperature mobility of majority carriers in bulk silicon, it is demonstrated that the previously observed discrepancies between the RTA and experiment cannot be resolved by including carrier-carrier interactions. Regarding the mobility of minority carriers, numerical simulations are performed which elucidate the importance of electron-

hole scattering in bipolar devices. The computed curves are in very good agreement with measured data.

Finally, the numerical solution of the radial Schroedinger equation is addressed, and a computationally efficient method for the evaluation of the higher-order transport cross sections is devised.

Prof. Dr. W. FIchtner, ETH Zürich, examiner
Prof. Dr. Redmer, University of Rostock, Germany, co-examiner

Diss. ETH-Nr. 15530
ISBN 3-89649-941-6

Adaptive Stream Processor for Networked Multimedia Consumer Electronic Devices

Thomas Bösch

Todays multimedia Consumer Electronic (CE) devices are networked in order to exchange audio/video data with other devices. The multimedia content is transmitted over computer networks as continuous stream of data items, such as pixels, frames, or samples.

Multimedia CE devices include highly integrated Systems-on-Chip (SoC) which provide the system core functionality. These SoCs contain data processing circuits to apply algorithms to the content, such as compression/decompression, encryption/decryption, signal processing, and packet handling. For these circuits, low cost, high processing performance, flexibility, and short time-to-market are of great importance.

In this thesis, the requirements of multimedia stream processing circuits are investigated and an Adaptive Stream Processor (ASP) optimized for SoCs in networked multimedia CE equipment is presented.

The ASP consists of a General-Purpose Processor (GPP) coupled with one or multiple Adaptive Stream Processing Engines (ASPE). The ASPE is tightly-coupled to the GPP as an instruction set extension which accelerates the GPP's task execution. In addition, ASPE and GPP are loosely-coupled and autonomous task execution controlled by program-sequencers is performed.

The ASPE architecture provides scalable flexibility and application adaptation through system customization at design-time. By selecting various program sequencers, storage and functional modules, which are integrated in a stream processor framework, the ASPE is optimized for a specific application range. Various general-purpose, dedicated, and reconfigurable functional modules and program sequencers can be selected to adjust the desired size, run-time performance, and application flexibility.

The implemented modules and sequencers are configured at run-time to form clusters which execute multiple tasks in parallel. Data streams can be processed in a pipeline fashion by a chain of clusters. The cluster shape may be changed on demand according to the application requirements. Program sequencers can be combined to groups to scale the level of parallel operation execution in a cluster.

Prof. Dr. W. Fichtner, ETH Zürich, examiner
Prof. Dr. L. Thiele, ETH Zürich, co-examiner

Diss. ETH-Nr. 15582
not yet available

Folding and Interpolating A/D Converters for Communications Applications

Jürgen Hertle

In this thesis problems related to the design of A/D converters for communications applications are examined. The focus is on systems which require high data rates at medium accuracy. Since these converters are extensively used in consumer products, low cost is of major importance, and hence they must be integrated in a mainstream digital CMOS technology.

A discussion of the pros and cons of the newly available sub-micron CMOS technologies and their impact on the design of high speed, medium resolution A/D converters reveals that the main challenge is to achieve high accuracy rather than high speed.

In order to optimize the existing architectures in terms of accuracy a detailed understanding of the quantization process, which is the fundamental operation of all A/D converters, is needed. A comprehensive discussion on that issue is conducted.

Equivalently important is the selection of an appropriate A/D converter architecture for the target application. Based on the foreseeable limitations of future technology generations with ever decreasing feature sizes, it is shown that the folding and interpolating architecture is a promising candidate for future A/D converters. Their key advantage is that they neither use high gain blocks nor any switches are needed in the signal path (except in the sample-and-hold circuit).

Next, a detailed discussion of the building blocks of folding and interpolating A/D converters is presented. It includes a principal description of the architecture, speed related issues, noise considerations, and also the accuracy limiting effects are identified and their impact on the overall converter accuracy will be given.

The first described design is an 8 Bit, 50 MS/s folding and interpolating A/D converter implemented in a 0.25 μm CMOS technology with a maximum supply voltage of 2.5 V. To minimize the power consumption an optimized architecture with four parallel folding signals, a folding factor of eight, and eight times interpolation is used. The measured SNDR is 42 dB and the SFDR is 50 dB up to the Nyquist frequency. The power consumption is only 50 mW and the chip area is 2.4 mm^2.

The second design addresses the limited accuracy of the folding and interpolating architecture. A calibration scheme tailored to this type of converter is developed and the related problems are discussed. The 10 Bit, 125 MS/s converter was implemented in a 0.18 μm CMOS technology with a maximum supply voltage of 1.8 V. Due to some minor design and layout problems the accuracy of the converter is limited to 50.8 dB. The power consumption is 126 mW (without I/O drivers) and the chip area is 4.1 mm^2.

Prof. Dr. Q. Huang, ETH Zürich, examiner
Prof. Dr. H.-A. Löliger, ISI, co-examiner

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ISBN 3-89649-950-5

All-Digital Standard-Cell Based Audio Clock Synthesis

Eric Roth

Consumer electronic (CE) devices connected by computer networks become more and more popular. Data transportation between CE devices must exhibit real-time behaviour to prevent interruptions of the data stream. This requires a synchronization of the data rates at the sending and the receiving streaming device, which is achieved with the transmission of timing information over the network. A phase-locked loop (PLL) in the receiver filters the jitter on the timing information and generates an accurate audio sample clock.

In order to save cost and to allow a high portability to different CMOS technologies, the PLL is proposed to compose of standard-cells only and integrated into the System-On-Chip (SoC) of the CE device. The key component of the all-digital PLL is the digitally-controlled oscillator (DCO), which generates the audio clock.

In this work, two alternative DCO circuits are proposed. The first is based on the phase shift principle, where the position of the output clock edges are pre-calculated, and a delay line shifts the edges of a fixed input clock to the predetermined position. An all-digital delay-locked loop (DLL) is used for the calibration of the delay line.

The second DCO architecture is based on a ring oscillator. The limited frequency resolution of conventional digital ring oscillators is extended by a method that switches rapidly between two adjacent frequency steps. A frequency calibration mechanism tunes the DCO to the target operation range.

Both DCO architectures are implemented on silicon for proof of concepts. The measurement results demonstrate that high-quality audio clock recovery is achieved with the phase shift DCO. The ring oscillator based DCO offers a significantly lower circuit complexity, but due to the high clock jitter, it is only applicable to lowest-cost, and less quality demanding devices.

As an important goal of the thesis, the porting of the DCO architecture to different CMOS technologies could be realized within two person-days.

Prof. Dr. W. Fichtner, ETH Zürich, examiner
Dr. Steven Harris, co-examiner

Diss. ETH-Nr. 15667

Industrial-Strength Simulation of Quantum-Well Semiconductor Lasers

Michael Pfeiffer

Physics-based simulation of optoelectronic semiconductor devices is becoming increasingly popular with device manufacturers due to its potential to speed up product cycles and to reduce costs in the device design process. The inclusion of simulation tools into the design process, however, is difficult. There are few tools available that are comprehensive, reliable and fast at the same time, and allow for a systematic scanning of parameter spaces in order to find optimal device structures.

This doctoral thesis deals with the development and implementation of advanced physical models and numerical methods for the simulation of quantum-well semiconductor lasers. Furthermore, it proposes a circuit-like simulation approach to the modeling of complex and integrated optoelectronic devices. The goal of the thesis is to provide a comprehensive simulator that is suitable for the application in an industrial environment. The work presented here is based on the commercial multi-dimensional semiconductor laser simulator DESSIS-Laser that is embedded into the ISE TCAD suite. This enables the use of advanced meshing, visualization and parameter optimization tools.

DESSIS-Laser has been developed at the Integrated Systems Laboratory (IIS) of the Swiss Federal Institute of Technology Zürich (ETH) and is distributed by Integrated Systems Engineering AG (ISE) which is a spin-off of IIS. DESSIS-Laser originally covered the isothermal multi-dimensional simulation of Fabry-Perot edge-emitting lasers. Over the past few years it has been extended to other types of edge-emitters as well as to Vertical-Cavity Surface-Emitting Lasers (VCSELs). It is based on the Poisson equation and a drift-diffusion model for modeling charge carrier transport, including thermionic emission at the hetero-interfaces. Carrier capture into the quantum-wells is modeled by a capture rate description. For the interaction between carriers and the light field, a rate equation approach is applied, while the optical eigenmodes are calculated in the frequency domain using the finite-element method. The electro-opto-thermal system of equations is solved by applying a Newton-Raphson scheme.

In the work presented here, the simulator DESSIS-Laser has been extended to cover the modeling of self-heating effects in semiconductor lasers. The underlying physical model is based on a thermodynamic description of heat generation and transport.

Furthermore, in order to enable the use of advanced gain models, a new interface has been implemented for user defined gain models. For the selfconsistent inclusion of k.p bandstructure calculation and the calculation of many-body interactions, an interface to the bandstructure and gain calculation library, GEBAS, has been introduced.

Some complex structures require a special treatment of the optical eigenmode problem on a special grid. A dual-grid scheme for the self-consistent inclusion of such calculations into DESSIS simulations has been realized. In order to couple the the electro-opto-thermal system of equations, the optical eigenmode search, the calculation of the lasing wavelength, and the bandstructure calculation in a robust manner, a Gummel-type procedure has been introduced that ensures the self-consistency of the overall solution.

Going beyond the simulation of semiconductor lasers, a circuit-like approach based on photonic circuit equations is proposed for the simulation of complex and integrated optoelectronic devices.

The capabilities of the models and features implemented in this work are illustrated by a number of example simulations, including the simulation of a high-power pump laser, the investigation of mode competition in a leakywaveguide laser, and the simulation of a VCSEL.

Prof. Dr. W. Fichtner, ETH Zürich, examiner
Dr. B. Schmidt, Bookham, co-examiner

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Deactivation and Activation of Donors in Silicon

Christoph Müller

Topic of this dissertation is the examination of processes which are responsible for the deactivation of donors in heavily doped silicon. In CMOS technology of the near future, source, drain, and channel regions of transistors need to feature doping concentrations in excess of the respective solid solubility limits. At the same time, every donor atom should release one of its electrons to the bulk, thereby contributing to a raise in electrical conductivity in the corresponding region.

Due to sophisticated process technologies, it is possible nowadays to manufacture such supersaturated samples. However, subsequent heating will push the system towards the thermodynamic equilibrium, donors start to rearrange, and ultimately precipitation of the donors sets in. Interestingly enough, a substantial electrical deactivation of donors already happens prior to the actual precipitation. There can be observed a certain amount of inactive donors even in highly doped samples prepared by low temperature molecular beam epitaxy, where no noticeable dopant diffusion takes place.

In this work, extensive computer simulations have been carried out in order to shed light upon the atomic scale mechanisms involved in the entire deactivation process. Calculations were performed using the *ab initio* density functional theory code *vasp* (*Vienna Ab initio Simulation Package*) from the University of Vienna. For the visualization and post-procesing of the output data *matlab* software was developed. The conclusions of the theoretical studies in conjunction with published experimental data can be summarized as *the three step model of donor deactivation*.This model is developed and elucidated in this work. The last part of the thesis discusses solutions to the topic. Possible co-dopants are presented and evaluated for their effectiveness at forestalling the deactivation process.

Prof. Dr. W. Fichtner, ETH Zürich, examiner
Prof. Dr. N. Cowern, University of Surrey, UK, co-examiner

Diss. ETH-Nr. 15786
ISBN 3-89649-977-7

Parallel iterative solvers in computational electronics

Stefan Röllin

This work investigates parallel iterative solvers for large sparse linear systems of equations arising in computational electronics. The sparse linear systems in this field are unsymmetric, highly ill-conditioned and pose large demands on the linear solver.

For the iterative solution of sparse linear systems many ingredients arerequired. Thus, a state-of-the-art iterative solver consists of various parts, such as algorithms to compute permutations, preconditioners and, of course, methods that iteratively compute an approximation of the solution. For each category of algorithms, there are several possible choices. In thefirst part of this work the most important ingredients are presented. The optimal set of these algorithms is then evaluated for semiconductor device simulations through an extensive number of numerical experiments. It is shown that algorithms to place large entries on the diagonal using unsymmetric permutations and scalings play an important role and greatly enhance the reliability of iterative solvers in this field. Incomplete LU-factorisations are the preconditioners that show the best performance for semiconductor device simulations. Furthermore, some simple but important techniques are discussed to improve the efficiency of iterative solvers in this field.

The second part of this work is concerned with the parallelisation of the best algorithms and methods evaluated in the first part. The target architectures for the parallelisation are shared memory multiprocessors. The aim is to reach a good speedup for the whole linear solver when using a modest number of processors. In order to achieve this goal it is necessary that as much as possible of the iterative solver runs in parallel. Therefore not only the parallelisation of the preconditioner is realised, but also of the permutations and in particular of the unsymmetric permutations and scalings. Unfortunately, the mentioned parts are not straightforward to parallelise. In this work, techniques for the parallelisation of incomplete LU-factorisations are analysed, which are based on the information of the elimination tree of the matrix. Similar strategies are used for the other parts. Our numerical results show that a good overall speedup can be reached on a modest number of processors.

Prof. Dr. W. Fichtner, ETH Zürich, examiner
Prof. Dr. M. H. Gutknecht, ETH Zürich, co-examiner

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Master Theses – Overview

Summer Semester 2004

Beat Hangartner	Simulation of 1.3μm Vertical Cavity Surface Emitting Laser with Tunnel Junction
Camilla Coletti	Quantification of Scanning Spreading Resistance Microscopy Measurement by Device Simulation
Reinhard Bischoff Jonas Biveroni	Generic Hardware Prototyping Platform

Winter Semester 2004/2005

Vaibhav Maheshwari	Design of Building Blocks for a UWB Transceiver
Sven Mumenthaler	Switchable and Tunable Active-RC Filters for Mixed-Mode VLSI Communication Systems
Manuel Aschwanden	The Quantum Information of the Greenberger-Horne-Zeilinger Experiment viewed from the Framework of Claude Shannon's Information Theory
Clemens Lombrisier	Process Synchronization Methods for Prototyping Platforms
Stefan Achleitner	A Strong-Authentication Module Resistant Against Side-Channel Attacks
Samuel Fuhrer	Sigma-Delta Modulator for a Class-D Audio Amplifier
Alain Brenzikofer	High-Efficiency High-End Audio Power Amplifier

Student Projects – Overview

Summer Semester 2004

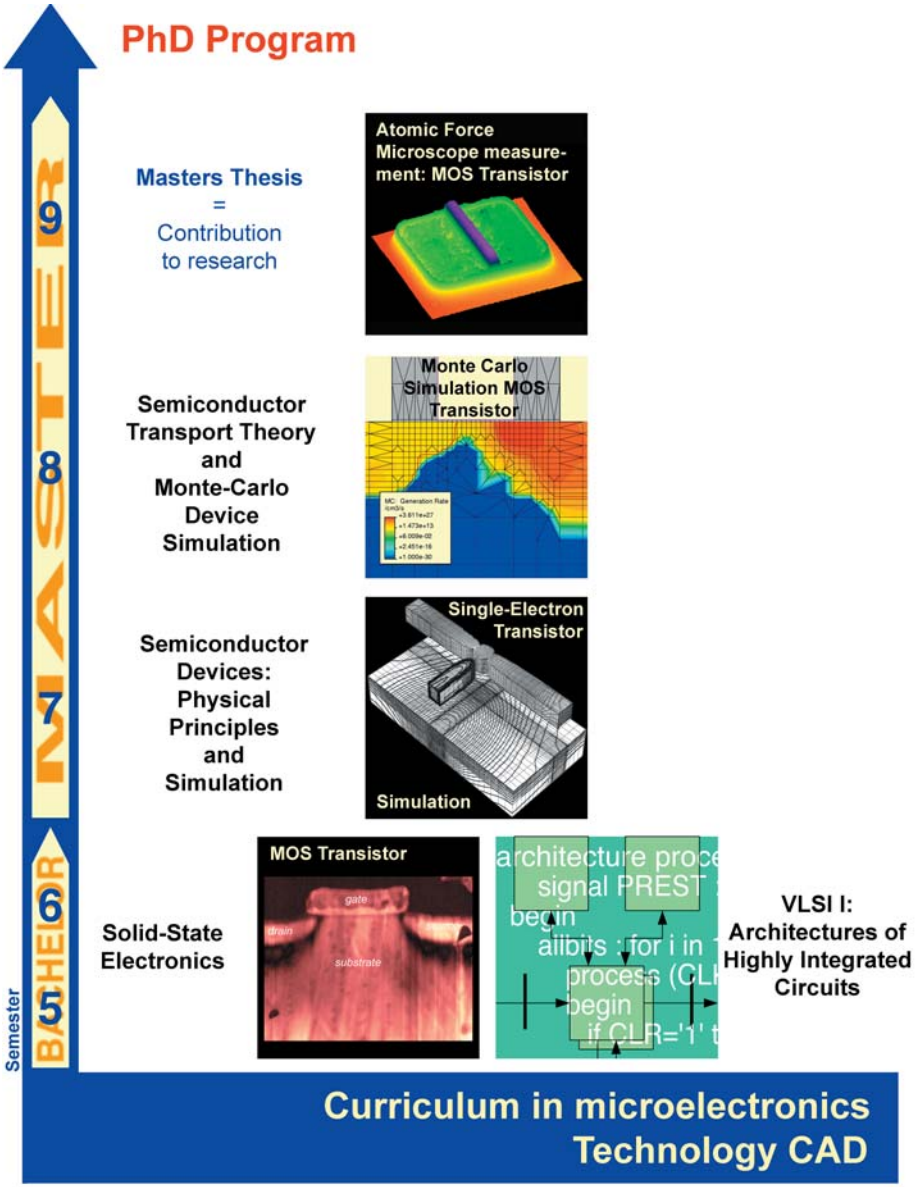
Sven Mumenthaler	Wide Tuning Range Clock Oscillator in 0.13µm CMOS
Vaibhav Maheshwari Silvan Wehrli	Programmable Base-Band Filter for Multi-Standard Wireless Receiver
Kun Fang	AGC for a MIMO-OFDM Testbed
Frédéric Poncioni	Ethernet Bridge for Radio Communication System
Vedran Galijas	Audio Level-Control Chip
Philippe Hefti Tobias Tomaschett	Multichannel Digital Audio Preamplifier System Design
Mark Blum Jon Rohrer Michael Deman	Digital Audio Board for PPS
Christoph Reller Jean Daniel Merkli	Audio Correlator System

Winter Semester 2004/2005

Thomas Nanzer	Simulation and Measuremnet of the Amplified Spontaneous Emission Spectrum of VCSELs
Beat Kessler	A Complex Sigma-Delta Modulator for GSM/EDGE Application
Raphael Berner	LNAs for Multistandard Wireless Receiver
Wang Chen	14-bit Current Steering DAC
Wolfgang Haid Stefan Ludwig	High-Performance NDIS Miniport Driver for a MIMO Communication System
Bürli Adrian Karin Weinmann	ARC - Activity Recognition Chip
Thomas Koch Sven Kuonen Julian Heeb	VLSI Implementation of the Finger Mouse Algorithm
Cyril Flaig Simon Heinzle	EWA Splat Rasterizer
Flurin Bühler Michael Casty	ASIC for Railway Signal Light Monitoring
Adrian Ziswiler	Signal Processing ASIC for Energy Meters
Luca Henzen Hovia Magdassian	Low-Power Adaptive Directional Microphone for Hearing Aids in Isomorphic Architecture
Herbert Koch Christoph Pedretti	Low-Power Adaptive Directional Microphone for Hearing Aids in Time-Sharing Architectur
Hektor Meier Rafael Santschi	Low-Power Speech Enhancement through Spectral Sharpening in Isomorphic Architecture
Martin Hediger Robert Meyer-Piening	Low-Power Speech Enhancement through Spectral Sharpening in Time-Sharing Architecture
Peter Haldi Stefan Zwicki	A Strong-Authentication Module Resistant Against Side-Channel-Attacks
Pascal Elsener Nadim el Guindi	Network on Chip: PANACEA a NOSTRUM Integration
Denis Müller Stefan Schmid Marc André	SoC Development and Testing Environment

Markus Billeter Mathias Meyer	Modulator for MIMO SoC
Yves Kunz Christoph Röthlisberger	Digital MIMO OFDM Frontend for MIMO SoC
Christoph Rüegg Andy Staudacher	MMSE-OSIC Detector: Linear and Successive Interference Cancellation Detector for a MIMO-OFDM System
Reto Jenny Carsten Meder	Concurrent Error Detection
Daniel Aggeler Daniel Widmer Daniel Dalquen	JPEG2000 Encoder VLSI Implementation

Education at IIS – Overview


PhD Program
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Atomic Force Microscope measure-ment: MOS Transistor
Semiconductor Transport Theory and Monte-Carlo Device Simulation
Monte Carlo Simulation MOS Transistor
Semiconductor Devices: Physical Principles and Simulation
Single-Electron Transistor
Simulation
Solid-State Electronics
MOS Transistor
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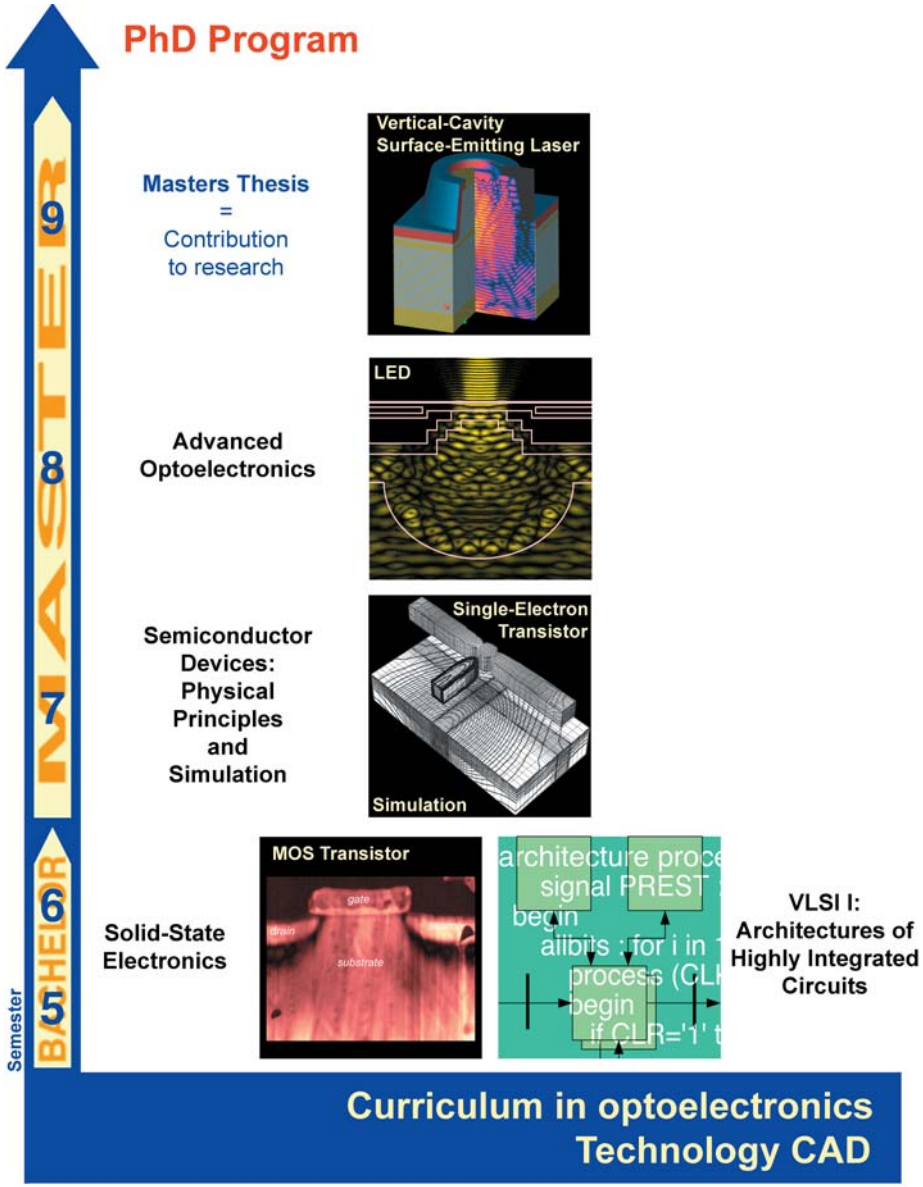
substrate
VLSI I: Architectures of Highly Integrated Circuits
Curriculum in microelectronics
Technology CAD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Advanced Optoelectronics
LED
Semiconductor Devices: Physical Principles and Simulation
Single-Electron Transistor
Simulation
Solid-State Electronics
MOS Transistor
gate
drain
substrate
VLSI I: Architectures of Highly Integrated Circuits
Curriculum in optoelectronics
Technology CAD

Lectures

Halbleiterbauelemente **4th Sem.**
Semiconductor Devices **EE**

W. Fichtner

This lecture gives an introduction to the basics of modern semiconductor devices for micro-, opto-, and power-electronics. It bases on semiconductor physics and covers band structures, band models, dispersion relations, statistics, transport equations, macroscopic models, and the characteristics of silicon and other semiconductors. An overview on device families is presented.

The part on technologies covers the properties of materials, and introduces the steps of modern process technologies as well as packaging. To understand the basic principles of devices, ohmic and rectifying contacts, physical and electrical characteristics of pn junctions, and types of diodes are explained. The lecture continues with the bipolar transistor's function, working regions, characteristic diagrams, and its simulation. MOS devices are treated based on band diagrams, and the MOSFET behavior is deduced. Power devices, their working regions and static and dynamic behavior are followed by examples of optoelectronic devices as photo conductor, photodiode, LED, and fiber. Semiconductor measurement and characterization methods conclude the course.

Kommunikationselektronik **5th Sem.**
Communications Electronics **EE**

Q. Huang

This course provides basic design and circuit techniques for communications electronics. As a starting point, bipolar and MOS transistors are reviewed. The discussion of circuit design begins with basic amplifier topologies, impedance matching concepts, and a bit of two-port theory. Important non-ideal aspects such as non-linearity and noise are discussed. This sets the ground for more involved topics. Important building blocks of communications equipment, such as mixers and oscillators, are examined in detail. The discussions include the basic topologies, mathematical descriptions, and a thorough analysis of non-ideal behavior, from which finally guidelines for the design can be derived.

The exercises form an integral part of this course. The definitions and concepts presented in the lecture will be reinforced by small design examples, therefore providing a link between the theoretical description and real-world problems.

VLSI I: Von Architektur zu hochintegrierter Schaltung und FPGA **6th Sem.**
VLSI I: From Architectures to Very Large Scale Integrated Circuits and FPGAs **EE/CS/Phys/CSE**

N. Felber, W. Fichtner, H. Kaeslin

As becomes clear from the subsequent list of topics, the first course in this series of three is mainly concerned with system-level issues of VLSI. Terminology, overview on design methodologies and fabrication avenues, levels of abstraction used for circuit description and simulation, VLSI design flow, dedicated VLSI architectures, how to obtain an architecture for a given processing algorithm, architectural transformations for meeting throughput, area, and power requirements. Hardware Description Languages (HDL) and their underlying concepts, VHDL for simulation and synthesis, the IEEE-1164 logic system, Register Transfer Level (RTL) synthesis. Timing models, Anceau diagrams, functional verification of digital circuits and systems, building blocks of digital VLSI circuits, case studies of actual circuits, comparison with microprocessors and DSPs.

During the exercises students learn how to model digital ICs with VHDL. They write testbenches for simulation purposes and synthesize gate-level netlists for ASICs and FPGAs.

VLSI II: Entwurf von hochintegrierten Schaltungen **7th Sem.**
VLSI II: Design of Very Large Scale Integrated Circuits **EE/CS/Phys/CSE**

N. Felber, W. Fichtner, H. Kaeslin

The second course begins with a thorough discussion of various technical aspects at the circuit and layout level. It then moves on to economic issues of VLSI. Topics include: limitations of functional design verification, techniques for improving controllability and observability, design for test, block isolation, scan-path techniques, partial scan and its caveats. Evaluation of various synchronous clocking disciplines, skew margins, clock distribution techniques. Asynchronous inputs, data inconsistency and metastability problems, synchronization. Cell libraries, Process-Temperature-Voltage (PTV) variations, transistor models, characteristics of CMOS inverters, complex gates. Power estimation and low-power design. Layout parasitics, transport delay, switching currents, ground bounce, controlling noise problems, power distribution, floorplanning, chip assembly. Layout design at the mask level, symbolic layout. Timing verification, physical design verification. Cost structures of microelectronics design and fabrication, avenues to low-volume fabrication, management of VLSI projects.

Exercises are concerned with physical design and sound engineering practices for avoiding timing, testability, and layout parasitics problems. Industrial CAD tools are being used for place and route, clock tree generation, chip assembly, and physical design verification. Students that elect to carry through a term project at the laboratory are offered the opportunity to complete a full IC design cycle on a circuit of their own which gets actually fabricated.

VLSI III: Fabrikation und Verifikation hochintegrierter Schaltungen — 8th Sem.
VLSI III: Test and Fabrication of Very Large Scale Integrated Circuits — EE/CS/Phys/CSE

N. Felber, W. Fichtner, Kaeslin

Whereas the preceding courses deal with design aspects of VLSI circuits, this one addresses manufacturing, testing, physical analysis, and packaging issues, such as: Effects of fabrication defects, abstraction from physical to transistor- and gate-level fault models, fault grading of large ASICs. Generation of efficient test vector sets, enhancement of testability by built-in self-test techniques. Modern IC testers: Architectures and application. Deep-submicron CMOS fabrication processes with multi metal levels and the physical analysis of their devices. Packaging problems and solutions. Technology outlook.

Exercises teach students how to use CAE/CAD software and automatic test equipment for verifying ASICs after fabrication. Students that submitted a design for manufacturing at the end of the 7th semester do so on their own circuits. Physical analysis methods with professional equipment (AFM, DLTS) complement this training.

Analog Integrated Circuits — 6th Sem. EE

Q. Huang

This course provides a foundation in analog integrated circuit design: After a review of bipolar and MOS devices and their small-signal equivalent circuit models, building blocks in analog circuits such as current sources, active load, current mirrors, supply independent biasing are presented. Other topics are differential amplifiers, cascode amplifiers, high gain structures, and output stages, and comparators, gain bandwidth product and stability of op-amps. Second-order effects in analog circuits such as mismatch, noise, and offset are investigated. More complex circuits such as A/D and D/A converters, analog multipliers and oscillators are analyzed. An introduction to switched-capacitor circuits from an IC designer's point of view is given.

The exercise sessions aim to reinforce the lecture material by well-guided step-by-step design tasks. Cadence design tools are used to facilitate the tasks. There is also an experimental session on op-amp measurements.

Advanced Optoelectronics — 5th/7th Sem. EE

B. Witzigmann

This lecture consists of two main parts. First, it briefly reviews the fundamentals of semiconductor optoelectronic devices. They include the electronic properties of semiconductors, electromagnetics theory and waveguides, and the interaction of light and matter. A chapter on fibers is included as well.

Second, the design principles and the functionality of the most important semiconductor optoelectronic devices are explained. These include e.g. lasers, modulators and photodiodes. The student will be able to connect the design criteria and the typical specifications to the fundamentals that are treated in the first part. See also page 120.

Halbleiter-Bauelemente: Physikalische Grundlagen und Simulation — 7th Sem.
Semiconductor Devices: Physical Principles and Simulation — EE/Phys

A. Schenk

This course aims at understanding the principles behind the physics of modern electronic silicon semiconductor devices and the foundations of physical modeling of transport and its numerical simulation. During the course basic knowledge on quantum mechanics, semiconductor physics, and device physics is also provided. The main topics are: Transport models for semiconductor devices (quantum transport, Boltzmann equation, drift-diffusion model, hydrodynamic model), physical characterization of silicon (intrinsic properties, band gap narrowing, scattering processes), mobility of cold and hot carriers, recombination (SRH statistics, lifetimes for tunnel-assisted transitions), interband tunneling (Zener diode), impact ionization, metal-semiconductor contact, MIS structure, and heterojunctions.

The exercises focus on the theory and the basic understanding of special devices, such as pn-diodes, bipolar transistors, MOSFETs, and thyristors. Numerical simulations of these devices with an advanced simulation package are compared with corresponding measurements, which are also part of the exercises.

Halbleitertransporttheorie und Monte-Carlo Bauelementsimulation — 8th Sem.
Semiconductor Transport Theory and Monte-Carlo Device Simulation — EE/CSE

F. Bufler, A. Schenk

The aim of the course is, on the one hand, to establish the link between microscopic physics and its concrete application in device simulation and, on the other hand, to introduce the numerical techniques involved. The scope encompasses therefore the basics of quantum mechanics, transport theory, and the Monte-Carlo method for the solution of the Boltzmann transport equation. The topics include second quantization, crystal symmetries, band structure calculation, phonons, Boltzmann equation, probability calculus, Monte-Carlo techniques, and device simulation.

The exercises comprise problems to illustrate the contents of the lecture, simple Monte-Carlo related programming tasks as well as the application of various professional tools for device simulation.

Elektrotechnik I **3rd Sem.**
Electrical Engineering I **MPE**

Q. Huang

This course provides the basic foundation in the specific field of electrical engineering. Starting from the basic concepts of voltage and currents, it covers the basic analyses of DC and AC networks. This includes series and parallel circuits, resistive circuits, circuits including capacitors and inductors, as well as the Kirchhoff's laws governing such circuits, and other network theorems. Transient response of RC-circuits, analysis of resonant circuits, concept of filtering, and simple filter circuits are all among the subjects covered in this course.

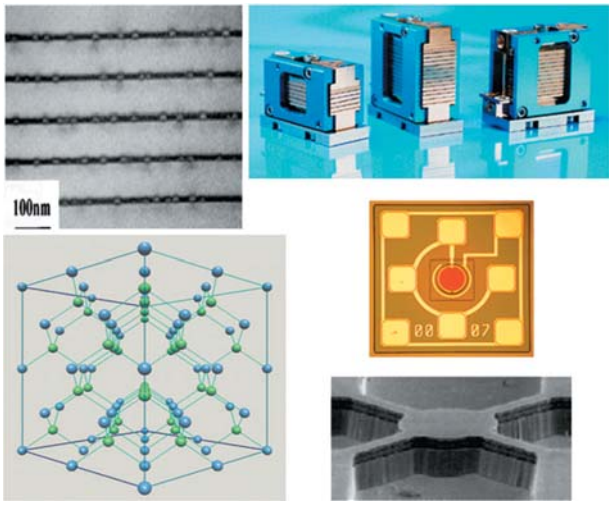
The understanding of the basic concepts of electrical engineering, particularly of circuit theory, shall be advanced. At the end of the course, the successful student knows the basic elements of electric circuits and the basic laws and theorems for determining voltages and currents in circuits with such elements. He/she is also familiar with basic circuit calculations.

New Lecture *Advanced Optoelectronics*

The new lecture *Advanced Optoelectronics* by Prof. Bernd Witzigmann consists of two main parts. First, it briefly reviews the fundamentals of semiconductor optoelectronics with an emphasis on the physics used to describe the most relevant phenomena and the materials that are used. In particular, fundamentals of the semiconductor, electromagnetics, and the interaction of light and matter are treated in detail. A chapter on fibers is included as well.

Second, the design principles and the functionality of the most important semiconductor optoelectronic devices are explained. These include e.g. lasers, modulators and photodiodes. The student will learn what the most critical design criteria and specifications for these devices are and how to optimize them with the knowledge gained from the first part of the lecture.

Besides reviewing the topics of the lecture, the exercise sessions include a Technology Computer Aided Design case, where a sophisticated industrial design software is used in order to analyze an optoelectronic device. The student has the opportunity to become familiarized with this software package.



Left: Photograph of a quantum confined semiconductor structure, and GaAs crystal lattice model. Right: High power laser, photodiode and tunable filter.

Abbreviations:

CS	Computer Science
CSE	Computational Science and Engineering
EE	Electrical Engineering
MPE	Mechanical and Process Engineering
Phys	Physics

Workshops and Courses

15th European Symposium Reliability of Electron Devices, Failure Physics and Analysis (ESREF) 2004

Organized by:	Integrated Systems Laboratory Conference Chair: Wolfgang Fichtner Technical Program Chair: Mauro Ciappa Local Arrangement Chair: Dölf Aemmer Exhibition Officer: Bruno Fischer
Location:	Swiss Federal Institute of Technology (ETH), Zürich
Technical co-sponsorship:	IEEE Electron Devices Society, IEEE Reliability Society
Presentations:	100 presentations (1 keynote speech, 7 invited talks, 52 talks, 40 poster)
Tutorials:	5 tutorials organized by companies and universities
Exhibition:	16 companies
Dates:	5 days from October 4 to 8, 2004
Participants:	234 participants from European and worldwide microelectronics industry (148 participants) and academia (86 participants)
Web:	www.iis.ee.ethz.ch/esref/index.html
Publication:	M. Ciappa, W. Fichtner Proceedings of the 15th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2004) Published by - Elsevier Ltd., Amsterdam, The Netherlands, 2004 and - Microelectronics Reliability, Special Issue ESREF 2004, vol. 44, pp. 1681-1686, Oct 2004

Physical Design and Verification for Student Projects in VLSI

Organized by:	Microelectronics Design Center
Trainers:	C. Balmer, M. Brändli, F. Camarero
Dates:	6 afternoons in winter term 2004/05
Participants:	39

Schematic Entry and Physical Layout for PCBs

Organized by:	Microelectronics Design Center
Trainers:	R. Köppel
Dates:	4 days from April 8 to April 29, 2004
Participants:	6

Schematic Entry and Physical Layout for PCBs

Organized by:	Microelectronics Design Center
Trainers:	R. Köppel
Dates:	4 days from November 11 to December 2, 2004
Participants:	9

Schematic Entry and Physical Layout for PCBs

Organized by:	Microelectronics Design Center
Trainers:	R. Köppel
Dates:	December 6, 2004
Participants:	2

IC Design Projects – Overview

2004:	Project:	Status:
Low-Power Adaptive Directional Microphone for Hearing Aids in Isomorphic Architecture	student project	/
Low-Power Adaptive Directional Microphone for Hearing Aids in Time-Sharing Architecture	student project	/
Low-Power Speech Enhancement through Spectral Sharpening in Isomorphic Architecture	student project	/
Low-Power Speech Enhancement through Spectral Sharpening in Time-Sharing Architecture	student project	/
MIMO-OFDM Transceiver	research project	/
Modulator for MIMO SoC	student project	/
Digital MIMO-OFDM Frontend for MIMO SoC	student project	/
MMSE-OSIC Detector: Linear and Successive Interference Cancellation Detector for a MIMO-OFDM System	student project	/
Reference Design of Strong-Authentication Module	student project	/
Strong-Authentication Module Resistant Against Side-Channel-Attacks	master thesis	/
GALS Version of Strong-Authentication Module Resistant Against Side-Channel-Attacks	research project	/
EWA Splat Rasterizer	student project	/
JPEG2000 Encoder VLSI Implementation	student project	/
ARC - Activity Recognition Chip	student project	/
VLSI Implementation of the Finger Mouse Algorithm	student project	/
Railway Signal Light Monitoring ASIC	student project	/
Digital Signal Processing Module for Energy Meters	student project	c
Network on Chip: PANACEA a NOSTRUM Integration	student project	/
Concurrent Error Detection	student project	/
Design of a Sigma-Delta Modulator for a Class-D Audio Amplifier	master thesis	c
Demodulator for Wireless Transceiver	research project	/
Integer-N PLL Based Synthesizer for Wireless Transceiver	research project	/

2003:	Project:	Status:
VLSI Implementation of a Sphere Decoder Core for MIMO Detection	student project	+
Viterbi Decoder for Wireless Lan	student project	+
Complex Matrix QR Decomposition for Inversion	student project	+
Power- and Performance-Optimized Complex-Number-Arithmentic ALU	student project	+
VLIW Complex DSP Specification and Architecture	student project	c
Video Blue/Green Compositing Chip	student project	+
CohereChip: Coprocessor ASIC for Virtual 3D Audio	student project	+
192 kHz Asynchronous Sample Rate Converter	student project	+
Stereo Digital Audio Preamplifier	student project	+
Multichannel Digital Audio Preamplifier	student project	+
Digital Noise Generator for Audio Measurements	student project	+
18 bit 48 kHz Sigma-Delta Modulator for Audio	student project	t
Oversampled Pipeline ADC with Mismatch Shaping	student project	~
14 bit Current-Steering DA Converter	student project	c
Programmable Base-Band Filter I for Multistandard Wireless Receiver	student project	c
Programmable Base-Band Filter II for a Multi-Standard Wireless Receiver	student project	c
RF Power Detector	student project	c
SOLARIS: High-Order, Low-Latency Convolution Processor ASIC	diploma project	+
DPA-Resistant Crypto Chip Design	diploma project	+
Adaptive Sampling Rate and Digital to Analog Converter	diploma project	+
Linear RF Amplifier with Large Gain Control Range	research project	+
25 Ms/s 14 bit 200 mW Sigma-Delta Modulator	research project	+
Resonant Clock Audio FIR Filter	research project	+
Clocking Schemes for Audio FIR Filter	research project	+
Sigma-Delta DAC with Semidigital Reconstruction Filtering	research project	+
200 Ms/s 14 bit DAC with Background Calibration	research project	+
Oversampled Sigma-Delta ADC for multistandard wireless	research project	~

Status Marks:

+	successfully tested design	/	chip in fabrication
~	functioning, but with minor bugs	•	design project in progress
–	severe design errors	t	chip under test
n	not submitted to integration (not implemented)	T	design for test structures
c	contribution to research or industrial chip	p	process errors

Research Projects – Overview

IC and System Design and Test

Subject: **Real-Time MIMO OFDM Systems for High Speed Broadband Wireless Access**
Partners: Communication Technology Laboratory, ETH Zürich, Zürich (Switzerland)
Period: July 02 – June 05
Funding, Number: ETH Zürich, Zürich (Switzerland), TH-6 02-2

Subject: **Lehre und Forschung in Mikroelektronik (Education and Research in Microelectronics)**
Period: April 99 – April 04
Funding, Number: ETH Zürich, Zürich (Switzerland), TH LF 99-01

Subject: **Netzwerkprozessor für LAN/WAN Bridging im Umfeld professioneller Multimedia Content Produktionen 2 (Network Processor for LAN/WAN Bridging in the Environment of Professional Multimedia Content Productions 2)**
Partners: BridgeCo AG, Dübendorf (Switzerland)
Computer Engineering and Networks Laboratory, ETH Zürich, Zürich (Switzerland)
Period: May 02 – April 04
Funding, Number: KTI*, 5845.1 NMS
BridgeCo AG, Dübendorf (Switzerland)

Subject: **Micropower Circuits for Digital Hearing Aids**
Partners: Bernafon AG, Bern (Switzerland)
Period: November 03 – October 05
Funding, Number: KTI*, 6695.2 NMS
Bernafon AG, Bern (Switzerland)

Subject: **GALS 2 Towards Practical GALS Circuits**
Partners: Infineon Technologies AG, München (Germany)
Period: April 01 – April 04
Funding, Number: Infineon Technologies AG, München (Germany), 401

Subject: **MIMO-OFDM Algorithm Implementatiuon for Future Mobile Communications (MAGIC)**
Partners: IKT-ETHZ, Zürich (Switzerland)
Siemens AG, München, (Germany)
Period: February 04 – September 04
Funding, Number: Siemens AG, München, (Germany), 0005/4400863409

Analog and Mixed-Signal Design

Subject: **OTRACOM – Optimization of Highly Linear Low-Power Transmitters for Third-Generation Mobile Communications**
Partners: Philips Zürich AG Semiconductors, Zürich (Switzerland)
Period: March 02 – August 04
Funding, Number: KTI*, 5731.1 NMS
Philips Zürich AG Semiconductors, Zürich (Switzerland)

Subject: **CMOS (SOI) for Low Power RF Wireless**
Partners: ACP AG, Zürich (Switzerland)
Period: January 03 – December 05
Funding, Number: KTI*, 6148.1 NMS

Subject: **CITE – Critical Circuit Technologies for Flexible Mobile Receivers**
Partners: Philips Zürich AG Semiconductors, Zürich (Switzerland)
Period: July 03 – June 05
Funding, Number: KTI*, 6171.2 NMS

Subject: **OREMO – Optimized Receivers for Mobile Communications**
Partners: ACP AG, Zürich (Switzerland)
Period: November 03 – April 06
Funding, Number: KTI*, 6767.1 NMS
ACP AG, Zürich (Switzerland)

Technology CAD

Subject:	**UPPER+ – User Group for Process Simulation European Research+ Device Simulation (European IST Project)**
Partners:	Fraunhofer-Institut für Integrierte Schaltungen, Erlangen (Germany) austriamicrosystems AG, Unterpremstätten (Austria) Infineon Technologies AG, München (Germany) Philips Research Leuven, Leuven (Belgium) STMicroelectronics SA, Crolles (France) STMicroelectronics Srl, Agrate Brianza (Italy) ISE Integrated Systems Engineering AG, Zürich (Switzerland) SIGMA-C, München (Germany) Institut für Mikroelektronik, Technische Universität Wien, Wien (Austria)
Period:	July 02 – June 04
Funding, Number:	BBW*, European Union, IST 2001-37903
Subject:	**Large Scale Eigenvalue Problems in Opto-Electronic Semiconductor Lasers and Accelerator Cavities**
Partners:	Institute for Scientific Computing, ETH Zürich, Zürich (Switzerland) Department of Computer Science, University Basel, Basel (Switzerland) Paul Scherrer Institute, Villigen (Switzerland)
Period:	January 2003 – December 2004
Funding, Number:	“Strategic Excellence Projects” (SEP): Computational Science and Engineering (CSE) ETH Zürich, TH-1 02-4
Subject:	**Large and Small Signal Analysis Methods for Physical Semiconductor Devices – Harmonic Balance and Optical AC Analysis (LASSIS)**
Partners:	Synopsys Switzerland LLC (ISE Integrated Systems Engineering AG), Zürich (Switzerland)
Period:	June 03 – Mai 06
Funding, Number:	KTI*, 6378.1 NMS Synopsys Switzerland LLC (ISE Integrated Systems Engineering AG), Zürich (Switzerland)
Subject:	**Parametric Design and Analysis for Semiconductor Technology Computer Aided Design (PARA – TCAD)**
Partners:	Synopsys Switzerland LLC (ISE Integrated Systems Engineering AG), Zürich (Switzerland)
Period:	November 03 – October 05
Funding, Number:	KTI*, 6650.2 NMS Synopsys Switzerland LLC (ISE Integrated Systems Engineering AG), Zürich (Switzerland)
Subject:	**Improvement of Semiconductor Process Simulator by Atomistic Simulation Techniques (MOLDYN)**
Partners:	ISE Integrated Systems Engineering AG, Zürich (Switzerland)
Period:	January 02 – December 04
Funding, Number:	TOP NANO 21, 5779.1 TNS ISE Integrated Systems Engineering AG, Zürich (Switzerland)
Subject:	**Raise of Active n-Dopant Concentration in Silicon by Codoping (CODOPING)**
Period:	October 04– September 06
Funding, Number:	SNF*, 200021-105414
Subject:	**Analysis and Simulation of SOI MOSFET Semiconductor Technology**
Partners:	Fujitsu Laboratories Ltd., Tokyo (Japan)
Period:	Oktober 02 – March 05
Funding, Number:	Fujitsu Laboratories Europe, Hayes (UK), -
Subject:	**Bauelementesimulation von ESD Schutzelementen (Device Simulation of ESD Protection Elements)**
Partners:	Infineon Technologies AG, München (Germany)
Period:	October 03 – September 04
Funding, Number:	Infineon Technologies AG, München (Germany), -
Subject:	**Model Development for Advanced CMOS and Bipolar Technologies**
Partners:	ISE Integrated Systems Engineering AG, Zürich (Switzerland)
Period:	January 04 – December 04
Funding, Number:	ISE Integrated Systems Engineering AG, Zürich (Switzerland), -

Computational Optoelectronics

Subject: **Simulation and Design of High Performance Semiconductor Optical Amplifiers and Superluminescent Light Emitting Diodes (SOA – SLED)**

Partners: Exalos AG, Zürich (Switzerland)
Synopsys Switzerland LLC (ISE Integrated Systems Engineering AG), Zürich (Switzerland)
Period: November 03 – October 06
Funding, Number: KTI*, 6429.1 NMS
Synopsys Switzerland LLC (ISE Integrated Systems Engineering AG), Zürich (Switzerland)

Subject: **High Speed and Quantum-Well Photodetectors**

Partners: Albis Optoelectronics AG, Zürich (Switzerland)
Synopsys Switzerland LLC (ISE Integrated Systems Engineering AG), Zürich (Switzerland)
Period: June 02 – Mai 05
Funding, Number: TOP NANO 21, 5782.1 TNS
Synopsys Switzerland LLC (ISE Integrated Systems Engineering AG), Zürich (Switzerland)

Subject: **Modeling of General Multi-Quantum-Well Structures Including Self-Consistent Coupling to a Laser Simulator (MQW)**

Partners: Bookham (Schweiz) AG, Zürich (Switzerland)
Synopsys Switzerland LLC (ISE Integrated Systems Engineering AG), Zürich (Switzerland)
Period: January 02 – March 05
Funding, Number: TOP NANO 21, 5785.1 TNS
Synopsys Switzerland LLC (ISE Integrated Systems Engineering AG), Zürich (Switzerland)

Subject: **TCAD Based Optimization of Vertical-Cavity Surface-Emittting Lasers (VCSEL-TCAD)**

Partners: Laboratory of Physics of Nanostructures, EPF Lausanne, Lausanne (Switzerland)
Avalon Photonics Ltd., Zürich (Switzerland)
Beam Express S.A., Lausanne (Switzerland)
Synopsys Switzerland LLC (ISE Integrated Systems Engineering AG), Zürich (Switzerland)
Period: Juni 04 – Mai 06
Funding, Number: KTI*, 6941.2 NMS-NM
Avalon Photonics Ltd., Zürich (Switzerland)
Synopsys Switzerland LLC (ISE Integrated Systems Engineering AG), Zürich (Switzerland)
Beam Express S.A., Lausanne (Switzerland)

Physical Characterization and Technology Development

Subject: **HERCULAS – High Resolution Electrical Characterization of ULSI and Advanced Semiconductor Devices (European IHP–RTN Project)**

Partners: Interuniversity Microelectronics Centre (IMEC), Leuven (Belgium)
Hahn-Meitner-Institut Berlin GmbH, Berlin (Germany)
STMicroelectronics SA, Crolles (France)
Philips Electronics Nederland B.V., Eindhoven (The Netherlands)
Universität Hamburg, Hamburg (Germany)
Infineon Technologies AG, München (Germany)
Consiglio Nationale di Metodolgie e Tecnologie per la Microelettronica (CNR-IMETEM), Catania (Italy)
Kungl Tekniska Högskolan, Kista (Sweden)
Institute for Semiconductor Physics, Frankfurt (Germany)
Tel-Aviv University, Tel-Aviv (Israel)
Period: Oktober 00 – March 04
Funding, Number: BBW*, European Union, RTN 1-1999-004

Subject: **DEMAND – Integrated Design Methodology for Enhanced Device Robustness (European IST Project)**

Partners: Infineon Technologies AG, München (Germany)
Technical University of Vienna, Wien (Austria)
Uni Bologna, Universita degli Studi di Bologna, Dipartimento di Elettronica Informatica e Sistemistica, Bologna (Italy)
ISE Integrated Systems Engineering AG, Zürich (Switzerland)
Period: September 01 – August 04
Funding, Number: BBW*, European Union, IST-2000-37903

Subject:	**SINANO – Silicon-Based Nanodevices (European IST Project)**
Partners:	SINANO Consortium
Period:	January 04 - December 06
Funding, Number:	BBW*, European Union, IST-2002-506844

Bio Electromagnetics and Electromagnetic Compatibility

Subject:	**TD Sensor**
Partners:	Foundation for Research on Information Technologies in Society (IT'IS), Zürich (Switzerland) Schmid & Partner Engineering AG, Zürich (Switzerland)
Period:	November 02 – December 03
Funding, Number:	KTI*, 6091.1 KTS Schmid & Partner Engineering AG, Zürich (Switzerland)
Subject:	**ULTRACOM: Channel Model of the Human Body for Medical Monitoring Systems**
Partners:	Miromico AG, Zürich (Switzerland) Foundation for Research on Information Technologies in Society (IT'IS), Zürich (Switzerland) University Hospital, University Bern, Bern (Switzerland)
Period:	October 03 – March 05 KTI*, 6454.3 NMS Miromico AG, Zürich (Switzerland)
Subject:	**Optical Link FR-Field Sensor for Time and Frequency Domain Measurements (TDS)**
Partners:	Foundation for Research on Information Technologies in Society (IT'IS), Zürich (Switzerland) Schmid & Partner Engineering AG, Zürich (Switzerland)
Period:	September 04 – August 06
Funding, Number:	KTI*, 7146.2 NMPP-NM Schmid & Partner Engineering AG, Zürich (Switzerland)
Subject:	**Definieren der Messmethodik und Verkleinern der Messunsicherheit bei Immissionsmessungen in Wohn- und Geschäftshäusern (Definition of Measurement Methodology and Reduction of Measurement Uncertainty of Electromagnetic Field Measurements in Living and Business Rooms)**
Partners:	Foundation for Research on Information Technologies in Society (IT'IS), Zürich (Switzerland)
Period:	August 00 – March 04
Funding, Number:	FNM, Zürich (Switzerland), 1-00-4
Subject:	**Forschungskooperation IT'IS – ETH Zürich (Research Cooperation IT'IS – ETH Zürich)**
Partners:	Foundation for Research on Information Technologies in Society (IT'IS), Zürich (Switzerland)
Period:	since January 00
Funding, Number:	IT'IS, Zürich (Switzerland), -

Abbreviations

BBT	Federal Office for Professional Education and Technology (a Swiss Government Agency)
BBW	Federal Office for Education and Science (a Swiss Government Agency)
KTI	Commission for Technology and Innovation (a Swiss Government Agency)
SNF	Swiss National Science Foundation
TOP NANO 21	Technology Oriented Program for Nano Sciences (Research and Technical Development Cooperations between Swiss Universities, Institutes, and Swiss Enterprises, funded by the Swiss Government)

Microelectronics Design Center (DZ)

Personnel

Dr. H. Kaeslin (head, VLSI CAE), C. Balmer (VLSI technology), M. Brändli (software operation, VLSI CAE/CAD), F. Camarero (VLSI CAE/CAD),R. Köppel (PCB CAD).

Better arrangements for EDA software

2004 has brought major improvements in the way EDA software is obtained. From October 2003, Mentor Graphics has begun to offer a Higher Education Program (HEP) to technical universities. This laudable initiative has been warmly welcomed by ETHZ because

- the software is being licensed in a few well-defined and comprehensive packages,
- the flat rates offer excellent value for money and afford classroom usage on a broad scale,
- the HEP is a consistent world-wide effort, and
- the program fosters direct contacts between Mentor Graphics and leading universities.

DZ has immediately embraced the HEP and has subsequently reorganized its procurement channels for Mentor Graphics EDA software. As for Cadence, current pricing precludes direct licensing of EDA software for classroom usage which is why DZ continues to procure the vast majority of its licenses through the Europractice program. Only a very small fraction of licenses is obtained directly from the vendor in order to fill gaps unacceptable in the context of industry-oriented research projects. During 2004, DZ has successfully renegotiated the conditions for such licenses to stay abreast of cost cutting measures at our university.

Unified platform for PCB design

During recent years, printed circuit boards (PCB) at D-ITET have been designed with the aid of CAD tools by Cadence, Protel and, to a lesser extent, also Eagle. As DZ felt this situation was unfortunate and inefficient, we have decided to evaluate the possibility of doing with one tool suite. To begin with, we have conducted a survey of needs with the aid of a questionnaire prepared by the “Fachverband Elektronik Design” and distributed to all D-ITET labs. DZ then has invited all labs to help in evaluating the current tools against the requirements so collected. Six experts from four entities have volunteered to actively participate in this effort. Using a representative benchmark circuit, the expert group has also worked through a design cycle with each of the three tool suites under consideration. As typical applications are very diverse and range from simple component carriers to demanding high-frequency boards, the evaluation essentially ended in a draw between the two more comprehensive tool suites. Arriving at a consensus turned out to be very difficult, but a majority has voted for what they felt to be a reasonable compromise between ease of use and number of features. It is hoped that this choice will find broad acceptance with D-ITET staff and students, and that synergies in user support, component libraries, expertise, guides, training, etc. will indeed materialize. Already, DZ has offered a first training course for beginners in November 2004.

Supported fabrication processes

As any list of fabrication processes and libraries would be outdated by the time it gets printed, we kindly ask prospective users to refer to our documentation on the Intranet available at www.dz.ee.ethz.ch/support/ic/technologies.

Design Activities

A statistical overview of all IC and PCB design activities conducted in 2004 with the EDA installations operated by DZ is given in the tables below along with the laboratory involved and other technical information.

IC Design		Teaching	Research					Total
Process family	Foundry		IIS	ISI	IfH	IfE	IQE	
250 nm CMOS	UMC	10	2	-	-	-	-	12
180 nm BiCMOS	IBM	-	-	1	1	1	-	3
250 nm BiCMOS	IBM	-	-	1	3	1	-	5
120 nm CMOS	IBM	-	-	-	-	1	-	1
130 nm CMOS	STM	-	19	-	-	-	-	19
180 nm CMOS	STM	-	2	-	-	-	-	2
120 nm CMOS	Philips	-	1	-	-	-	-	1
InGaAsP	IfE	-	-	-	-	1	-	1
HBT	IfE	-	-	-	-	2	-	2
150 nm AlGaAs/InGaAs HEMT	FhG	-	-	-	1	-	-	1
Total		10	24	2	5	6	-	47

Board design	IIS	IfE	ISI	IQE	TIK	IfA	EEK	INI	Total
with individual support	2	1	-	-	1	-	-	-	4
freelance projects	4	-	-	7	-	-	-	-	11
Total	6	1	-	7	1	-	-	-	15

Joint Research Cooperation with the IT'IS Foundation

Profile

The IT'IS Foundation was established on November 15th, 1999 through the initiative and support of the Swiss Federal Institute of Technology in Zurich (ETHZ), the global wireless communications industry, and several governmental agencies. IT'IS stands for Information Technologies in Society.

The aim of IT'IS is to create a flexible and dynamic research institution capable of addressing the research needs of society in the explosively expanding field of information technologies. Some of the areas encompassed are:

- evaluation of the safety and risks related to current and emerging information technologies
- exploration of information technologies for medical, diagnostic, and life support systems
- improvement of the accessibility of information technologies for all members of society including disabled persons.

IT'IS is committed to the advancement of science for the benefit of society at large and to maintaining strict independence from any particular interest groups. These principles are reflected in the Foundation's charter as well as the balance of the composition of its board, with distinguished personalities from science, the public sector, and the global wireless communications industry. IT'IS is a non-profit tax-exempt research organization.

Infrastructure and Cooperation

During the start-up phase of the Foundation, not only the main office but also the research units and laboratories were located at ETH Zurich. In April 2000, IT'IS opened jointly with Schmid & Partner Engineering AG one of the world's finest near-field laboratories in downtown Zurich. In 2003, the IT'IS facilities at Zeughausstrasse 43 were more than doubled, including two new laboratories (a large semi-anechonic chamber for general near-field and dosimetric measurements and a reverberation chamber for EMI and other tests) to address new chellanges in the area of health support systems.

The closest and most important cooperative ties of IT'IS are with the Integrated Systems Laboratory and other laboratories of ETH Zurich. In addition, the IT'IS team has substantial experience in multidisciplinary cooperation through a multitude of projects, resulting in an international network of over 50 academic and industry research partners in Europe, the USA, and Asia.

Current Research Focus

The current research focus of IT'IS lies in the three areas 1) sensing and computational techniques for electromagnetic analysis, 2) health risk assessment, and 3) health support systems. In addition, IT'IS offers various services to governments and industy, including antenna engineering, device optimization for operation in EMF hostile environments, testing of compliance, and safety white papers.

The first area, Sensing and Computational Techniques, consists of several projects, ranging from new sensor technolgies and new measurement procedures for testing the compliance of wireless devices and base stations with safety limits to extensions and improvements of FDTD for near-field applications and optics.

The currently most important research area is Health Risk Assessment. This mainly involves the development, provision, and maintenance of exposure setups as well as the provision of detailed dosimetry for more than thirty experiments conducted in cooperation with biological and medical research groups in Switzerland, Europe, USA, China, and Japan. These include *in vitro*, *in vivo*, and human provocation studies at different mobile communications bands as well as some ELF experiments. In addition, IT'IS is conducting basic and review studies for different agencies.

The Health Support System group, formed in 2003, is developing rapidly. Of particular mention are in-house projects supporting the development of hyperthermia planning tools for the treatment of cancerous tumors, controllable nerve stimulation for neuroprothysis, optimized signal transmission over the body, and antenna designs for on-body and implanted antennas.

In addition to providing research results for governmental agencies through participation in standardization bodies and providing consultation to governments, IT'IS also provides courses to members of the public, industry, and universities.

Current research projects are being supported by public funds such as those of NIEHS, the Quality of Life Programme of the European Union, EUREKA, KTI, VERUM Foundation, health agencies such as BAG and BfS, as well as other governmental institutions. Funding from industry comes from major mobile communications manufacturers and service providers as well as from smaller companies.

IT'IS FOUNDATION

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Technical Report 2004/4

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“Microscopic Gain Calculation and Comparison with Measurement for Different Temperatures and Multi-Quantum-Well Laser Structures”,
Technical Report 2004/5

F.M.Bufler,
“Exploring the Limit of Strain-Induced Performance Gain in p- and n-SSDOI-MOSFETs“,
Technical Report 2004/6

Technical Reports can be ordered form:

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Electronic and Physical Characterization Equipment

ECAD and TCAD Software

MODEL TECHNOLOGY INC. HDL Simulation Package
SYNOPSYS Simulation and Synthesis Tools
SYNOPSYS Test Compiler
PROTEL Printed Circuit Board CAE/CAD System
HEWLETT PACKARD IC-CAP Measurement Control and Parameter Extraction Tools
SYNOPSYS/ISE-TCAD Software for Process and Device Development
Mentor Graphics Eldo Circuit Simulator
Xilinx FGPA Tools
Avant! Hspice Circuit Simulator

Equipment for Electronic Test

Verification Systems & Logic Analyzers

HP83000, ASIC Verification System, 660MHz
Agilent 16760A, Logic Analyzer Module
HP16702A, Logic Analysis System, IEEE

Spectrum & Network Analyzers

Audio Precision System S1, Audio Analyzer
R&S FSIQ3, Signal Analyzer, 20Hz-3.5GHz
R&S FSP, Spectrum Analyzer, 9Hz-7GHz
R&S FSQ26, Signal Analyzer, 20Hz-26.5GHz
Agilent 8591E, RF Spectrum Analyzer, 9kHz-1.8GHz
HP89441A, Vector Signal Analyzer, DC-2650MHz
HP8720D, Network Analyzer, 50MHz-20GHz
HP8751A, Network Analyzer, 5Hz-500MHz, with HP87511A S-Parameter Set
HP8753E, Network Analyzer, 30kHz - 6GHz
R&S FSEB30, Spectrum Analyzer, 20Hz-7GHz
Tektronix TLS216, 16-Channel Logic Scope, 500MHz 2GS/s, IEEE

Scopes

Agilent 54855A, 4-Channel Digitizing Scope, 6GHz 20GS/s
Tektronix TDS6804B, 4-Channel Digitizing Scope, 8GHz 20GS/s
Tektronix TDS820, 2-Channel Sampling Scope, 6GHz, IEEE
Tektronix TDS794D, 4-Channel Digitizing Scope, 2GHz 8GS/s, IEEE
Tektronix TDS684A, 4-Channel Digitizing Scope, 1GHz 5GS/s, IEEE
Tektronix TDS784, 4-Channel Digitizing Scope, 1GHz 4GS/s, IEEE (2)

Function Generators, Signal Sources

Agilent E8267C, PSG Vector Signal Generator, 250kHz - 20GHz
R&S SML01, RF Signalgenerator, 1GHz (3)
R&S SML03, RF Signalgenerator, 3.3GHz (3)
R&S SMU200A, 2-Channel Vector Signal Generator, 100kHz-6GHz
Stanford Research DS360, Low-Noise and -Distortion Function Generator, 200kHz
R&S SMHU 58, Signal Generator, 100kHz-4.320GHz
R&S SMIQ6 RF Vector Signal Generator, 300kHz-6.4GHz
Marconi 2042, Low-Noise Signal Generator, 10kHz-5.4GHz
R&S AMIQ, 2 Channel Arbitrary Waveform Generator, 100MS/s (2)
HP 8000, 10 Channel Pattern Generator, 1GBit/s

Meters

HP8970B, Noise Figure Meter, 2GHz
HP5501B, Phase Noise Measurement System 1.6GHz
HP4284A, LCR Meter, 20Hz-1MHz, IEEE
R&S NRV D, RF Power Meter
UDT S380, 2-Channel Optometer, IEEE

Power Supplies

Heinzinger LNC3000-20, Power Supply, 3kV/20mA
FUG HCN 700-12500, Power Supply, 12,5kV/50mA, IEEE
Kikusui PAK20-18A, Power Supply, 20V/18A (2)
Kikusui PAK6-60A, Power Supply, 6V/60A

Active Probes, Amplifiers & Attenuators
Agilent 87405A, Preamplifier 22dB, 10MHz-3GHz
HP54701A, Active Probes, DC-2.5GHz, 100kOhm (2)
Tektronix P6015, High-Voltage Probe, 20kV
Tektronix AM503, A6302 Current Probe, TM502A Power Rack
Tektronix AM503A, A6303 Current Probe, TM502A Power Rack
Tektronix CT1, 5mV/mA Current Transformer (2)
Tektronix CT2, 1mV/mA Current Transformer (2)
Chase CPA 9231 Preamplifier, 9kHz-1GHz
MITEQ AMF-20-001080-20-10P RF Amplifier, 100MHz-8GHz
Stanford Research SR560, Low-Noise Preamplifier
Stanford Research SR570, Low-Noise Current Preamplifier
Rhode & Schwarz, RF Step Attenuator RSH, DC-5.2GHz

Physical Characterization
Balzers SCD 40, Sputter System
Cambridge Stereoscan 360, Electron Microscope
Cohausz FT1020 DLTS
Ebic Amplifier
Electron Microscope
Froilabo A, Thermo System
Hamamatsu, Emission Microscope System
Mazali A510Q1, Thermo Test Module
Nanoscope Dimension 3100, Atomic Force Microscope System
RH2010, Hall Effect Measurement System
Schlieter 125l, Thermo Chamber
Weiss 305 SB/10Ju40DU, Environmental Testing Chamber
Hughes TVS200, Thermal Video System
ESD Transmission Line tester IIS
MiniZap ESD-Simulator and HBM-Network

Parameter Analyzers
Agilent 4156C, Precision Semiconductor Parameter Analyzer (2)
HP4142B, Modular DC Source/Monitor
Tektronix Curve Tracer 370
HP4085/4084, Switching Matrix/Control

Probers and Utilities
Suss PA150, Semi Automatic Prober
Suss PSM6, Submicron Prober
Temptronic Thermo Chuck, 0 to 200C
Temptronic TPO4000, Thermo Stream, -60 to 140C
Temptronic TPO700A, Thermo Chuck System
Alessi LG2, Green Laser Cutting System

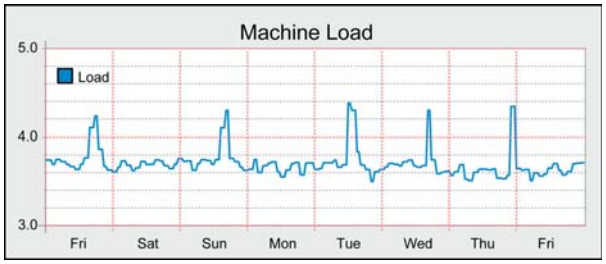
Optical Microscopes
Nikon Optiphot 66, Stereo Microscope
Zeiss Axiophot, Microscope
Zeiss Stemi SV8, Stereo Microscope

Optical Characterization Lab
HP71400C, Lightwave Component Analyzer 750nm - 870nm, 1200nm - 1600nm
Agilent AG 86030A, 50GHz Lightwave Component Analyzer
ANDO AQ 6317B, Optical Spectrum Analyzer, 600-1750 nm
Anritsu MS9601A, Optical Spectrum Analyzer, 1200-1700 nm
Coherent 251, Spectrum Controller & Analyzer (2)
S46 999 W30 A1, Optical Reflectometer
Agilent 4156C, Precision Semiconductor Parameter Analyzer
HP 8110A, Programmable Current Pulse Generator, 10V 1 Hz-150 MHz
HP54750A Digitizing Oscilloscope with TDR Module HP54754A
HP8563E, Spectrum Analyzer, 27GHz
Burster 6426, Precision Current Source, 100 mA (2)
HP8168D, Narrow Linewidth Tunable Laser Source, Linewith 100 kHz 1490-1565 nm -10 to -4 dBm
ILX LDC-3722, Laser Diode Controller, 50 mA
ILX LDC-3742, Laser Diode Controller, 3000 mA
ILX LDC-3900, Modular Laser Diode Controller, 3000 mA
ILX Lightwave LDX 3412, 200mA Precision Laser Current Source
AM-3500, Optical Power Meter
Newport 1835-C, Optical Power Meter, 100 fW-300W
Cascade 9652-URF, Wafer Probestation

Computer Equipment

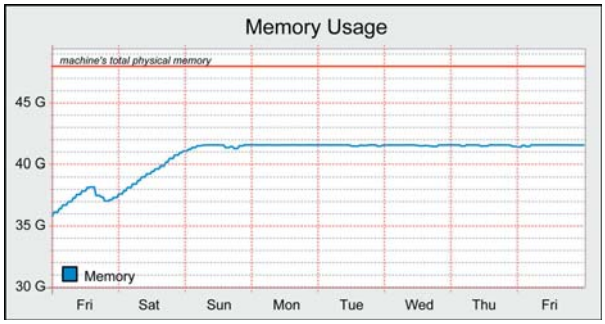
Computers are most relevant tools in teaching and research at IIS. Examples are design of integrated circuits, simulation of circuits, devices and technologies for microelectronics and microsystems, development of application software, and information transfer.

Besides optimal reliability and uncompromising performance, homogeneity of the computing environment and user friendliness are also important. To meet these goals, the computing environment uses the operating system Unix (Solaris, True64, Debian Linux), networking with TCP/IP and NFS, the X-Window System, and the programming languages C, C++, and Fortran 90/95. Besides the Unix machines in the scientific and technical area, Macintosh computers are widely applied for administration and presentation tasks. A Windows 2000 terminal server for mainly office applications is also provided. Several PCs are installed for controlling measurement equipment, for lab classes, and for other special applications.



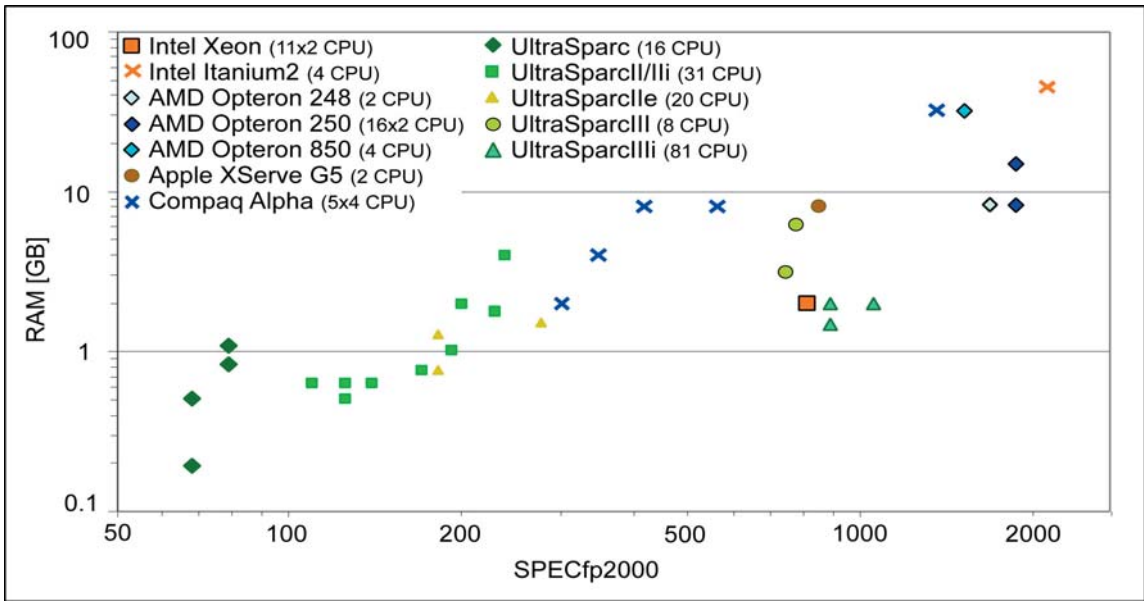
Load of a 4-CPU Intel Itanium2 Server
('Load' = number of processes in running queue)

Since the teaching and research activities span many areas, computer systems of various vendors are utilized. They range from file servers to standard workstations, compute servers, and workstations with specialized dedicated hardware. All Unix computers run SVR4 or BSD, or variants thereof. The file systems of all computers are assembled via NFS into what appears to the user as a single file system. The networking of IIS computers and external computers is based on switched 100 Mbit and Gigabit Ethernet, and on the TCP/IP protocol. Important applications in the technical area are ECAD (Modelsim, Synopsys, Cadence, Protel, Mentor Graphics), TCAD (Synopsys/ISE AG), as well as publishing and office applications on Macintosh computers.

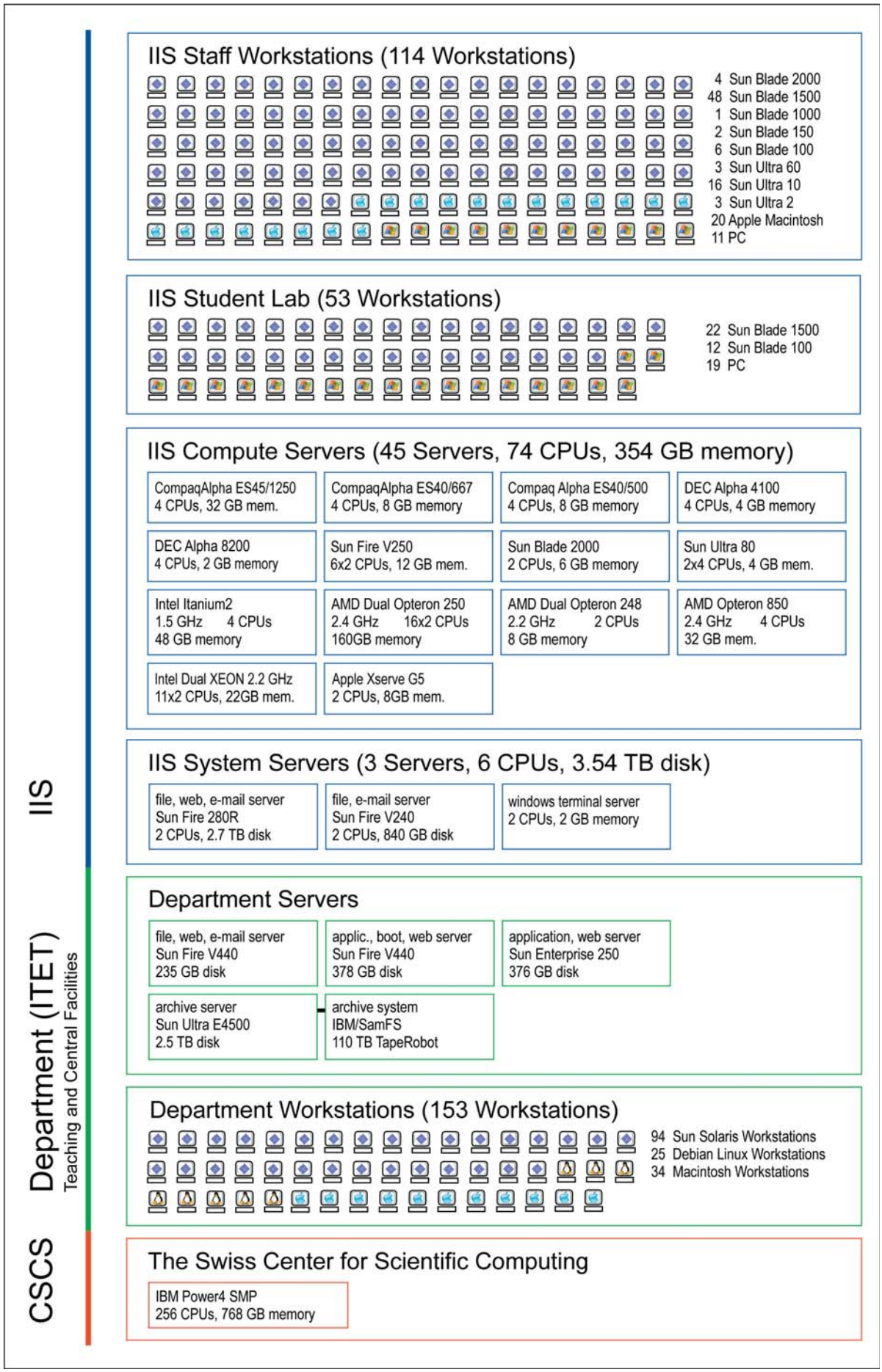


Memory usage of a 4-CPU Intel Itanium2 Server:
total physical memory allocation of all processes.
Values are average values of two data points collected within 100 minutes

The computing equipment of IIS counts two Unix file server, 117 Unix workstations, 20 Macintosh computers, 30 PCs and furthermore 45 powerful shared-memory compute servers including AMD Opteron and Intel Xeon based Linux-clusters for physical simulations. The detailed configuration of computers at the Integrated Systems Laboratory, the Department of Information Technology and Electrical Engineering (D-ITET), and the high-power and parallel computing facilities of CSCS (The Swiss Center for Scientific Computing in Manno/Ticino) is shown on the following page.



Representative figures of performance of computers at the Integrated Systems Laboratory: Floating-point performance per CPU (SPECfp2000 benchmark) and memory size (GBytes) of compute servers and Unix workstations.


IIS
Department (ITET)
Teaching and Central Facilities
CSCS
IIS Staff Workstations (114 Workstations)
4 Sun Blade 2000
48 Sun Blade 1500
1 Sun Blade 1000
2 Sun Blade 150
6 Sun Blade 100
3 Sun Ultra 60
16 Sun Ultra 10
3 Sun Ultra 2
20 Apple Macintosh
11 PC
IIS Student Lab (53 Workstations)
22 Sun Blade 1500
12 Sun Blade 100
19 PC
IIS Compute Servers (45 Servers, 74 CPUs, 354 GB memory)
CompaqAlpha ES45/1250
4 CPUs, 32 GB mem.
CompaqAlpha ES40/667
4 CPUs, 8 GB memory
Compaq Alpha ES40/500
4 CPUs, 8 GB memory
DEC Alpha 4100
4 CPUs, 4 GB memory
DEC Alpha 8200
4 CPUs, 2 GB memory
Sun Fire V250
6x2 CPUs, 12 GB mem.
Sun Blade 2000
2 CPUs, 6 GB memory
Sun Ultra 80
2x4 CPUs, 4 GB mem.
Intel Itanium2
1.5 GHz 4 CPUs
48 GB memory
AMD Dual Opteron 250
2.4 GHz 16x2 CPUs
160GB memory
AMD Dual Opteron 248
2.2 GHz 2 CPUs
8 GB memory
AMD Opteron 850
2.4 GHz 4 CPUs
32 GB mem.
Intel Dual XEON 2.2 GHz
11x2 CPUs, 22GB mem.
Apple Xserve G5
2 CPUs, 8GB mem.
IIS System Servers (3 Servers, 6 CPUs, 3.54 TB disk)
file, web, e-mail server
Sun Fire 280R
2 CPUs, 2.7 TB disk
file, e-mail server
Sun Fire V240
2 CPUs, 840 GB disk
windows terminal server
2 CPUs, 2 GB memory
Department Servers
file, web, e-mail server
Sun Fire V440
235 GB disk
applic., boot, web server
Sun Fire V440
378 GB disk
application, web server
Sun Enterprise 250
376 GB disk
archive server
Sun Ultra E4500
2.5 TB disk
archive system
IBM/SamFS
110 TB TapeRobot
Department Workstations (153 Workstations)
94 Sun Solaris Workstations
25 Debian Linux Workstations
34 Macintosh Workstations
The Swiss Center for Scientific Computing
IBM Power4 SMP
256 CPUs, 768 GB memory