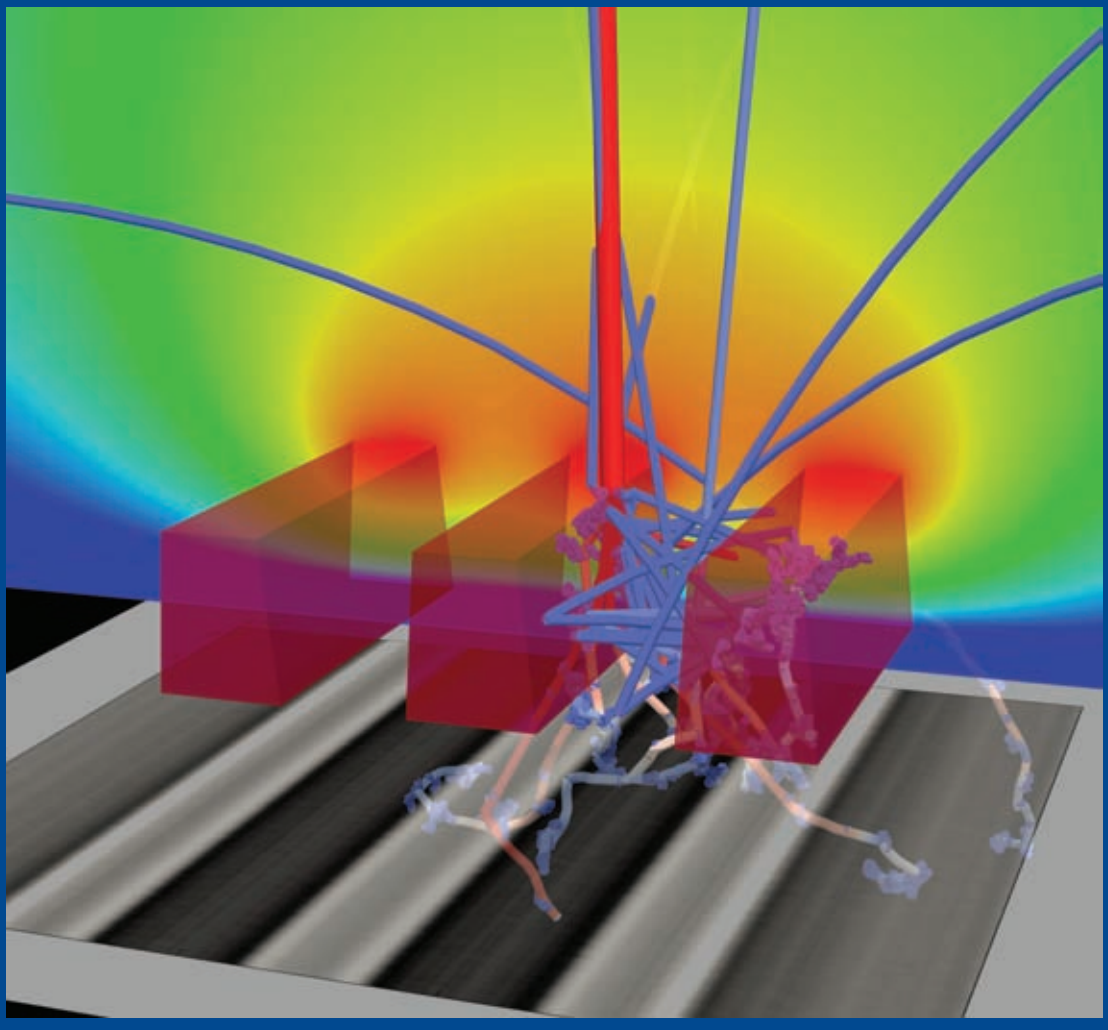
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Integrated Systems Laboratory
Microelectronics Design Center

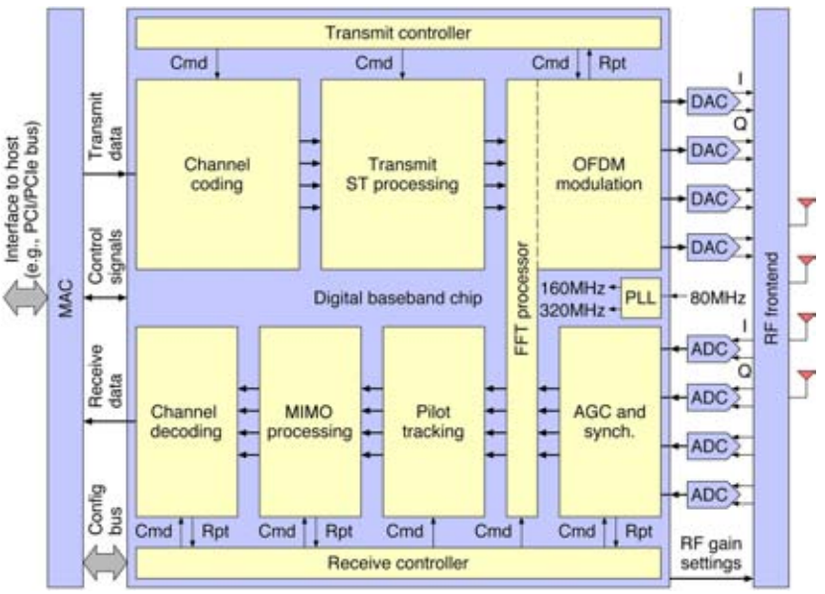
Research Review 2009



Cover Image:
MIMO 4-Stream Baseband Transceiver ASIC for IEEE 802.11n

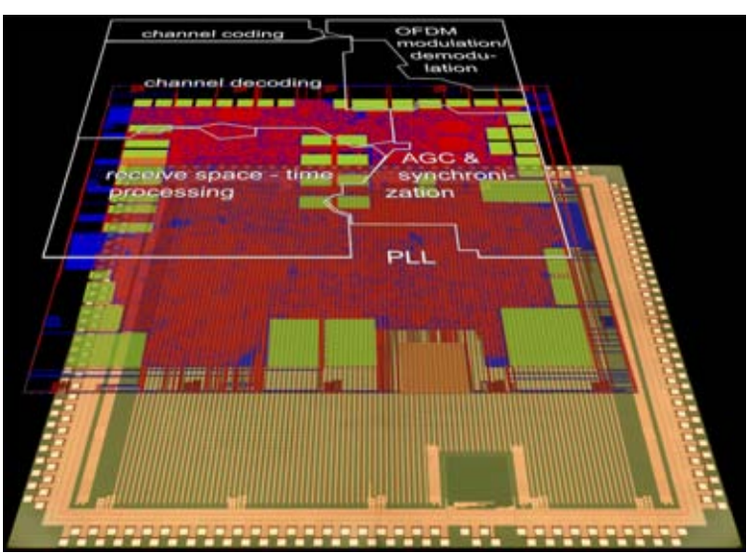
IEEE 802.11n is the most popular emerging standard for wireless local area networks. Compared to its predecessors (IEEE 802.11a/b/g), this new standard achieves larger range, better reliability, and up to 10x higher data rates. To achieve this significant improvement, IEEE 802.11n employs multiple-input multiple-output (MIMO) technology with up to four spatial streams. Unfortunately, the complexity of the baseband processing increases rapidly with the number of spatial streams. Hence, present commercial implementations of the standard support only up to two streams, employing 2 or 3 antennas.

The application-specific integrated circuit (ASIC) developed in this research project is the worldwide first 4-stream IEEE 802.11n baseband transceiver. With 4 transmit and 4 receive antennas, the MIMO-OFDM modem reaches peak over-the-air data rates of up to 600 Mbps in 40 MHz bandwidth, or 289 Mbps in 20 MHz. To support the high number of transmission modes and to provide maximum flexibility for future extensions, the first two levels of hierarchy of the developed VLSI architecture are partitioned into two types of components: processing elements (PEs) perform signal processing but are mostly agnostic about the details of the standard. Data path controllers orchestrate the operation of the PEs. A handshake protocol controls the exchange of data between PEs and the exchange of commands and reports between datapath controllers and the associated PEs. Thanks to this structure, the timing of the data flow is completely self-organizing and individual PEs can easily be modified, exchanged, or added without the need to modify other blocks or the datapath controllers.



The block diagram on the top right of this page shows the first level of hierarchy with 7 PEs and 2 datapath controllers. The PEs in the transmit data path handle the channel coding, the space-time coding, and the MIMO-OFDM modulation which is partially shared with the receiver to reduce silicon area. In the receive data path, the first PE controls the analog gain stages in the RF and performs various synchronization tasks. The subsequent MIMO-OFDM demodulation (shared with the transmitter) and the pilot tracker obtain the frequency-domain representation of the received signal and correct residual frequency and timing offsets. Next, the MIMO processing estimates the channel's frequency response and separates the spatially multiplexed data streams using a linear MMSE detector. Soft-information is then provided to the channel decoding which employs two 300 Mbps Viterbi decoders to recover the transmitted data.

The above described architecture was implemented in a 130 nm CMOS technology, using a standardcell-based design methodology to facilitate process migration. In addition to the 1.1 M gate equivalents for the standardcells in the data path and the control logic, a total of 595 kbit of on-chip memory was used. This memory is distributed across 49 macro cells. A phase-locked-loop generates the 160 MHz and the 320 MHz internal clock signals from an external 80 MHz reference clock. The final layout of the circuit occupies a core area of 14.4 mm^2, which is comparable to the area required by commercial 2-stream implementations. Including the pads, the manufactured ASIC occupies an overall area of 25 mm^2. For more information, please look up pages 40ff.



The cover image shows the 4x4 MIMO Transceiver ASIC. Modern chip technologies provide rather unattractive chip photographs. In order to illustrate more details, two images have been overlaid over the chip micrograph: The first is a plot of the layout data with selected metal connections, all memories, and the PLL. The second indicates the contours of he most important building blocks. The layout constraints for optimal speed and area results lead to this arrangement realized by the automatic place-and-route tools.

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ETH Zurich

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Analog and Mixed-Signal IC Design Group

Research Data Converters for Communications

In the past decade, portable battery-operated devices have reached enormous popularity. The mobile phone industry has bypassed car and traditional computer industry in annual sales and has exceeded the billion-phone-a-year mark. The advent of the iPhone has finally ushered in an era of wireless internet and other non-voice applications. New high-end devices have led to an enormous need for power-efficient digital data processing as well as sophisticated radio front ends to ensure high-quality data transmission and reception at minimum power. In the design of the latter, data converters remain one of the key elements that govern the front-end performance and are thus still an active research topic, especially in combination with the advanced CMOS technologies in which circuits for mobile handsets are designed.

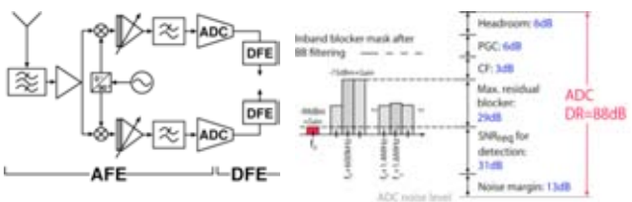


Fig. 1 ADC dynamic range design with EDGE as an example.

We take a terminal EDGE receiver as an example to derive the ADC requirements. The left side of Fig. 1 shows a direct-down-conversion receiver. The RF-preselect filter and the analog base-band filter limit the dynamic range in front of the ADC. Both are complemented by filtering in the digital front end (DFE). The right side of Fig. 1 illustrates the ADC dynamic range calculation for such a receiver. A total range of 88 dB is derived from headroom, programmable gain control (PGC) to follow channel fluctuations, the crest factor (CF) to link peak signal amplitude to power, the amount of unwanted signals (blockers) that are tolerated, the SNR requirement for detection of the signal, and finally the margin of the converter noise vs. the received signal noise in front of the ADC. In such a setup, an ADC with higher dynamic range can absorb more blocker power and have higher margins so that the amount of analog filtering can be reduced in favor of filtering in the DFE. The progress in ADC power efficiency and scaling of digital signal processing implementations has shifted optimum system design towards concepts with reduced complexity in the analog part and high dynamic range ADCs.

Wireless Standards:

	GSM/ EDGE	UMTS/ HSPA	UMTS-LTE	WiMAX	IEEE 802.11n
Bandwidth	200kHz	3.84MHz	1.25 – 20MHz	3.5 – 10MHz	20/40MHz
Resolution	≈12-14bit	≈11-13bit	≈11-13bit	≈11bit	≈11bit

Wire Line Standards:

	ADSL	VDSL	Universal TV	DVB-C	Gigabit Ethernet
Bandwidth	1.25MHz	12.5MHz	8.5MHz	2-10MHz	62.5MHz
Resolution	≈13-15bit	≈14bit	≈9-10bit	≈10-12bit	≈7-8bit

Fig. 2 ADC requirements for Wireless and Wireline Standards (Terminal Side).

The ADC requirements for different wireline and wireless standards (Fig. 2) have to be seen in this light, as such requirements always reflect the feasibility at the time when a standard was defined together with system optimization considerations as outlined above. Consequently, much of the research these days goes into more power-efficient design rather than design for raw performance.

Realizations of ADCs for a given set of performance requirements are illustrated in Fig. 3, which shows the bandwidth-resolution ranges for the pre-dominant converter types. Delta-sigma converters employ oversampling and spectral shaping of quantization noise. These converters thus dominate the high resolution low-speed side of the chart. Without oversampling, circuit thermal noise is the main limiting factor to obtain higher resolutions. Pipelined converters distribute the conversion process topologically as well as in time over many stages that then can use a simple and high-speed circuit structure, leading to medium speed/medium resolution and high speed/low resolution solutions in Fig. 3. The third architecture is folding and interpolating converters which are centered in the high speed/lower resolution region in Fig. 3. These converters distribute the conversion over typically two stages to achieve much smaller latency than pipelined converters and obtain their full resolution by folding and interpolating multiple copies of the input signal against a set of reference signals. Since the implementation complexity grows exponentially with the resolution, folding and interpolating converters are commonly designed for 8 to 10 bits. Exploiting the improved speed of smaller transistors, the bandwidth-resolution ranges of the converter types have moved to higher frequencies over time.

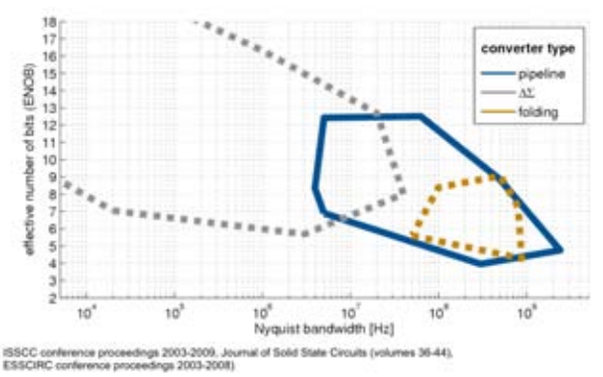


Fig. 3 Bandwidth-Resolution Ranges for Different Converter Types.

Converter design remains one of the core topics in analog and mixed-signal IC design. The AMIC group has published several contributions at ISSCC and in the IEEE JSSC over the past 15 years. Contributions on the above converter types in this report are (section of the AMIC group): from Jürg Treichler on pipelined converters, from Thomas Christen on delta-sigma converters, from Schekeb Fateh on folding and interpolating converters, and from Craig Keogh on high-performance DACs.

Contents

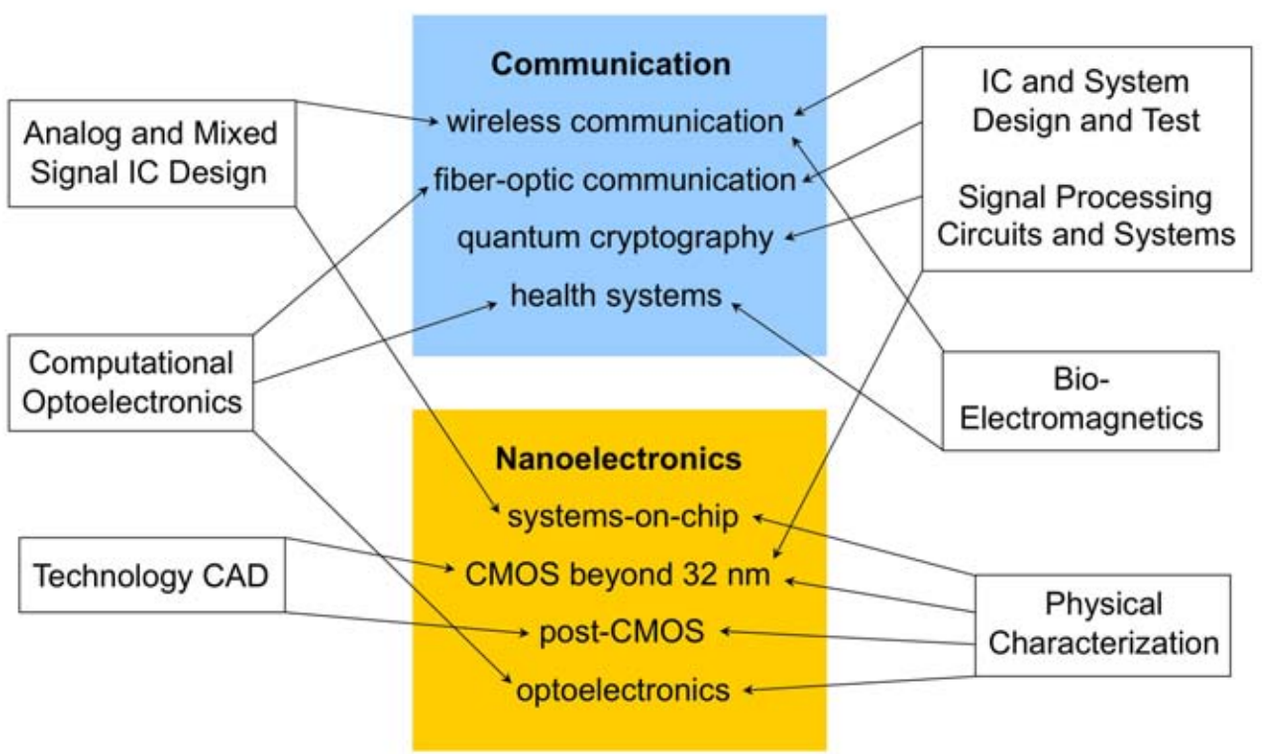
Introduction

This report presents the academic and research activities of the Integrated Systems Laboratory (IIS) and the Microelectronics Design Center (DZ) at the Department of Information Technology and Electrical Engineering (D-ITET) of ETH Zurich for the year 2009.
The IIS staff includes four professors, five research associates, seventeen (17) post docs, twenty six (26) PhD students, three computer system administrators, four persons in administration, and two technicians.
Research topics in digital, mixed, and analog integrated circuit (IC) design range from sensitive sensor interfaces to GHz RF circuits on the analog side, over analog-to-digital converters to the digital field covering projects from low-power design methodologies to complex systems-on-a-chip (SoC). Technology CAD (TCAD), technology and device development, computational optoelectronics, physical characterization, and bio-electromagnetics complement the research fields of IIS towards profes sional tools for modeling and optimizing nanoelectronic and optoelectronic devices and technologies in thenanometer range as well as bio-electromagnetic systems.

Microelectronics Design Center
The Microelectronics Design Center, headed by Dr. H. Kaeslin, with four staff members, is a service organization of the Department of Information Technology and Electrical Engineering. It is closely cooperating with IIS and other D-ITET and ETH Zurich laboratories in their design research and teaching activities for VLSI, analog, and system electronics (see page 121ff.).

Research Projects and Funding
Following the trends of earlier years, our cooperation with national and international partners is at the center of our activities. In 2009, four new research projects started in the fields of complex digital and analog systems-on-chip. One of them is a KTI/CTI (Swiss Commission for Technology and Innovation) project, one an SNF (Swiss National Science Foundation) project and two industrial research cooperations.
Overall, IIS was involved in a total of 23 research projects. Two of them were projects funded by EU, seven by KTI, four by SNF, and ten by industrial partners and research foundations in Switzerland, Europe, and Japan.

PhD Students
In 2009, 12 PhD students finished their doctoral thesis successfully. IIS offers an excellent and highly stimulating research environment that permits PhD students to work on very attractive topics and, nevertheless, to finish their thesis in a comparatively short time. However, it is still an ambitious challenge to find very qualified PhD students from all over the world. We try our best to overcome this situation by an appropriate salary policy and by focusing the student activities on scientific work in order to reduce the administrative and educational overhead.



Research at the Integrated Systems Laboratory: From Devices to Systems
The scientific work of the seven research groups surrounds technologies, devices and systems in communication and nanoelectronics. Fundamentals are semiconductor physics, electronic circuit technology, electromagnetics, physical characterization technology and computational science.

IC and System Design and Test Group

One main activity of the IC and System Design and Test Group in 2010 was in multi-antenna communications (MIMO). Multi-user MIMO communication has been demonstrated on the ETHZ Testbed at the ISCAS 2009 conference. The algorithms that perform complex operations have been trimmed to low circuit complexity and implemented in FPGAs and dedicated ASICs.

Compressed sensing, a new field of research which investigates signals that are sampled at sub-Nyquist rate, could be applied to channel estimation, a crucial task for MIMO communications which is expected to become faster through this new technique.

The third active research topic concerns high-data-rate encryption systems with quantum key distribution. The running KTI/CTI project will be complemented by a nanotera project which will enable further research together with the the quantum research group of the University of Geneva (Prof. Nicolas Gisin) and the Swiss company idQuantique. More cryptographic activities aim at optimal hardware implementations of new stream ciphers for the SHA-3 Competition, and an FPGA implementation of so-called Cube Testers could be successfully applied to uncover weaknesses of the stream cipher Grain-128.

Analog and Mixed Signal IC Design Group

For the Analog and Mixed Signal Integrated Circuit Design (AMIC) Group of Prof. Huang, the year 2009 has shown a continuation of work around the group's focus in the field of RF and base-band circuit design for telecommunications applications. Main research outcome have been three analog-to-digital converters based on pipe-lined, folding and sigma-delta principle, each showing very competitive performance (see inside cover of this report as well). Another high-light of the Group is again a digital base-band signal processing circuit: the 4.5 mW digital base band receiver for Level-A Evolved Edge that sets a new benchmark for this type of application and has been presented at ISSCC 2010.

In 2009, the AMIC group has been successful in obtaining two project grants from the national initiative Nano-Tera with focus in bio-medical monitoring and advanced circuits for telecommunication systems. Beside these new projects the AMIC Group has been partner in several national projects with research focus around circuit design for wireless applications and implementation in deep-submicron CMOS technologies at the 130 nm node and beyond, mainly in collaboration with its spin-off ACP.

Signal Processing Circuits and Systems

In its first year, the Signal Processing Circuits and Systems group under Prof. Andreas Burg has grown from initially three to six PhD students. Thanks to contributions from the Hasler Foundation and from our industry partners, we have been able to expand our research activities into different areas related to wireless and wireline communication.

The highlights of our work in 2009 are mostly in the areas of circuits and systems for multiple-input multiple-output (MIMO) communication and in the design of VLSI circuits for channel coding. In the area of MIMO, our research builds on a physical layer modem for IEEE 802.11n. For this modem, we develop high-performance and low-power algorithms and corresponding VLSI architectures. In particular, during the last year, we have been able to improve on various circuits for MIMO signal detection and we have investigated the impact of RF impairments on MIMO receivers. In the area of channel coding, we have realized several circuits that explore two extremes of the VLSI design space: ultra-low power and very high throughput (collaboration with LSM-EPFL). Corresponding ASICs in a 90nm technology have been sent for fabrication.

In addition to our work on MIMO, we have worked on improving the efficiency of storage devices for signal processing applications, where on-chip memory often accounts for a significant part of the silicon area and the power consumption. Furthermore, new projects have been initiated that look at communication over polymer optical fibers (collaboration with Innodul AG) and at the design of low-power circuits for Wireless Body Area Sensor networks (collaboration with ESL-EPFL).

Technology CAD Group

Research in the **Device Physics Group** focused on quantum transport and new methods to solve the Boltzmann transport equation. The simulation package SIMNAD (SIMulator for NAnoDevices) has experienced several improvements related to the underlying physical models and the numerical methods. The implementation of the more generic non-equilibrium Green's function (NEGF) formalism was extended and improved.

Advanced features in quantum transport solvers

The main extension is an iterative solution procedure using NEGF which allows the treatment of scattering in a perturbational way up to any order. The impact of electron-phonon scattering on device characteristics was investigated together with a new type of boundary conditions for the quantum transport equations. These boundary conditions model the incoherent injection of carriers from the contacts resulting in a continuous density of states across the contact-channel interface, removing this way artificial effects on the potential and enabling convergence. The mobility and the conductivity in silicon resistors and nanowire FETs were studied as a function of confinement and doping concentration. The empirical pseudo-potential (PP) method was implemented and band structures of wires and wells were computed and compared with tight-binding results and phenomenological nonparabolicity models.

Direct solver of the Boltzmann equation

The development of new FEM sparse grid techniques to solve six-dimensional transport equations like Boltzmann or Wigner-Boltzmann was started. As the high dimensionality results in huge stiffness matrices, existing direct solvers are currently restricted to devices with one space dimension. To overcome the problem, a hierarchical basis and the construction of a multidimensional basis by tensor products of lower dimensional bases are key ingredients. Calculations in the Device Physics Group have shown that direct numerical solutions become feasible when adapting these techniques for TCAD.

Impact from international projects

In a research project with Toshiba Corporation the effect of inhomogeneous strain on transport was investigated for state-of-the-art devices developed by the industrial partner. The in-house Monte Carlo simulator was re-written for strain applications. During the device analysis it turned out that the strain gradient in the channel region is negligible due to the already saturated strain level there. However, the accuracy of the calculated band structures becomes increasingly important with rising strain. This calls for a new sparse-grid based interpolation method for

the six-dimensional strain space.
The group participated actively in the EU-IST project NANOSIL (Silicon-Based Nanostructures and Nanodevices) with Monte Carlo and leakage simulations of template devices of the 32, 22, and 16 nm technology nodes. Defect-assisted gate tunneling was studied for a variety of trap configurations in hafnium-oxide based gate stacks and compared to temperature-dependent data provided by experimental partners in the project. A closer collaboration with Tyndall Cork (Ireland) was started on the exploration of CV data of InGaAs capacitors with Al2O3 gate oxide.
The activities of the **Atomistic Simulation Group** are centered on multiscale simulation of dopant diffusion and activation in strained and unstrained silicon. Diffusion and clustering parameters were calculated with ab-initio calculations based on density functional theory and then used as input in a state-of-the art process simulator based on the kinetic Monte Carlo approach. The selection of defect species was made according to the needs of model development for process simulation, taking into account the availability of experimental data, model sensitivity and the capabilities of current ab-initio methods. To ensure a suitable selection of defect species and a correct transfer of the results based on first-principle physics to the kinetic Monte Carlo simulator, the close collaboration with Synopsys was essential. The systematic database of ab-initio results was extended to more than 200 defects species, including mixed clusters with arsenic, phosphorus, antimony, indium, boron, fluorine and carbon. Special emphasis was put on the investigation of stress effects on diffusion and clustering in strained silicon. The computationally extremely demanding calculations (more than 10,000) were performed at the Swiss National Supercomputing Centre CSCS.

Computational Optoelectronics Group
The COE group has focused on both the development of novel simulation models, as well their application to the design and analysis of semiconductor optoelectronics devices. In the domain of nano-scale light emitters, research has been undertaken with the aim to model the physical properties of optical cavities with high quality factors in connection with quantum dots/wires and wells. These emitters are envisioned to approach ultrahigh efficiencies. In the field of gallium-nitride materials for visible light sources, a microscopic model for gain and luminescence in disordered materials has been developed, that, for the first time, matches measured data for quantum wells emitting in the blue and green in a consistent manner. In collaboration with an industrial partner, a high sensitivity and high speed avalanche photo diode for fiber to the home (FTTH) applications has been developed leveraging the insight gained from Monte Carlo simulations using a custom-developed software. The COE group is the primary contributor to the simulation efforts within a project investigating third generation nanowire solar cells as sustainable sources of renewable energy. A novel frequency domain simulator for vertical external cavity surface emitting lasers was developed making novel insights accessible that were previously beyond the boundary of computational feasibility.

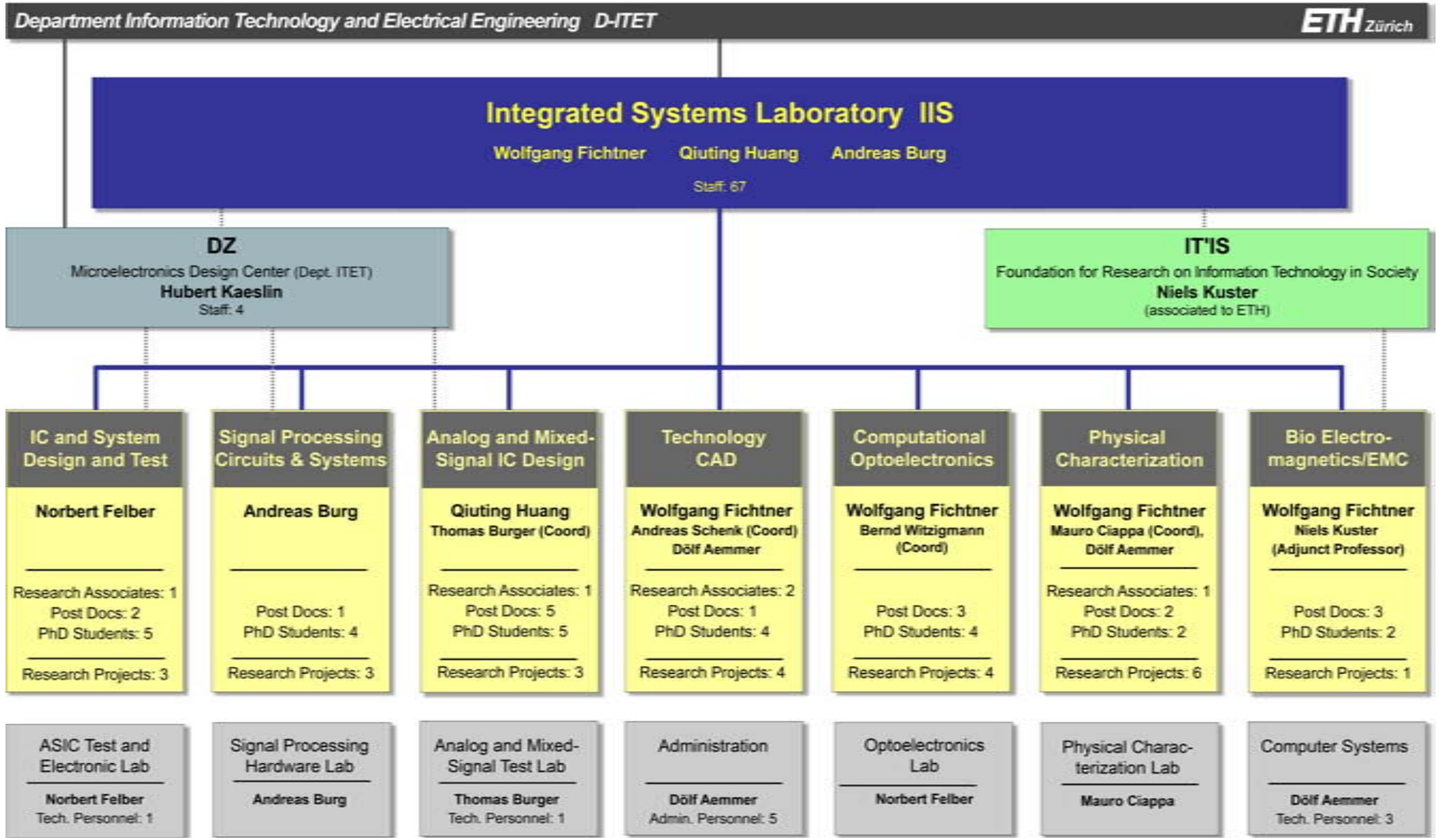
Physical Characterization Group
In 2009, the activities continued according to the planning for the projects initiated in the previous year. Referring to the project with Infineon Technologies, the new concepts for the screening of gate oxide and crystal defectivity in smart power ICs for automotive applications have been integrated into circuits with enhanced testing capabilities. A rigorous analysis demonstrated the advantages of the proposed approach and its suitability for the integration in commercial products. In addition, the philosophy of on-chip defect screening has been extended to cover circuits like analog-to-digital converters, which are very relevant in the automotive field. The activities in the modeling and simulation of scanning electron microscopy images for the quantification of critical dimensions in advanced CMOS processes has progressed along two main directions. Firstly, important results have been obtained in conjunction with the Kessler Foundation in the modeling the secondary electron yield in dielectric materials at very low energies by Monte Carlo techniques. In a second step, these models have been implemented into a dedicated tool for the simulation of linescan produced by 3D probes in the presence of electrostatic fields. The project with HUBER+SUHNER resulted into the development of a 1D and 3D Monte Carlo simulator for the dose prediction during electron beam processing of polymers in the manufacturing of electrical cables and optical fibers. Based on these calculation tools new criteria have been introduced to define the optimum processing conditions and specific dosimetry tools have been conceived. The research also continued in the field of the Micro-Electro-Mechanical Systems (MEMS). In a co-operation with Toshiba Corporation a multi-scale model has been developed to predict the mechanical behavior of macroscopic thin film structures from the morphology at nanoscale, with the scope to ensure the long-term reliability of MEMS products. Finally, in a second co-operation with NTT a systematic flow to design CMOS circuits integrated in MEMS has been defined and demonstrated in the case of technology-relevant examples.

Bio-Electromagnetics Group
IT'IS, the "Foundation for Research on Information Technologies in Society" (headed by ETH adjunct Prof. Niels Kuster), a non-profit research institution supported by ETH Zurich, established its scientific and technical work in close collaboration with our laboratory.
The research activities of IT'IS are in the domain of the interaction of electromagnetic radiation with biological organisms, in advanced measurement equipment for electromagnetic radiation, and health risk assessment. Research projects and PhD students at IIS are funded by the global wireless communications industry, several governmental agencies, and the Commission of the European Union. The collaboration with IT'IS is very fruitful and a benefit for both institutions (see page 124).

Education
Next to research, teaching occupies a central role in our activities. Our staff is responsible for several core lectures in Information Technology and Electrical Engineering as well as in other departments (see page 113). The chapter on student projects (page 91) gives an overview on the manifold diploma theses and semester projects. Several outstanding student semester and master projects contribute to our research projects. The descriptions of exceptional contributions can be found on pages 33 (right), 35 (left), 41 (right), 43 (left). They often lead to accepted presentations at international conferences.

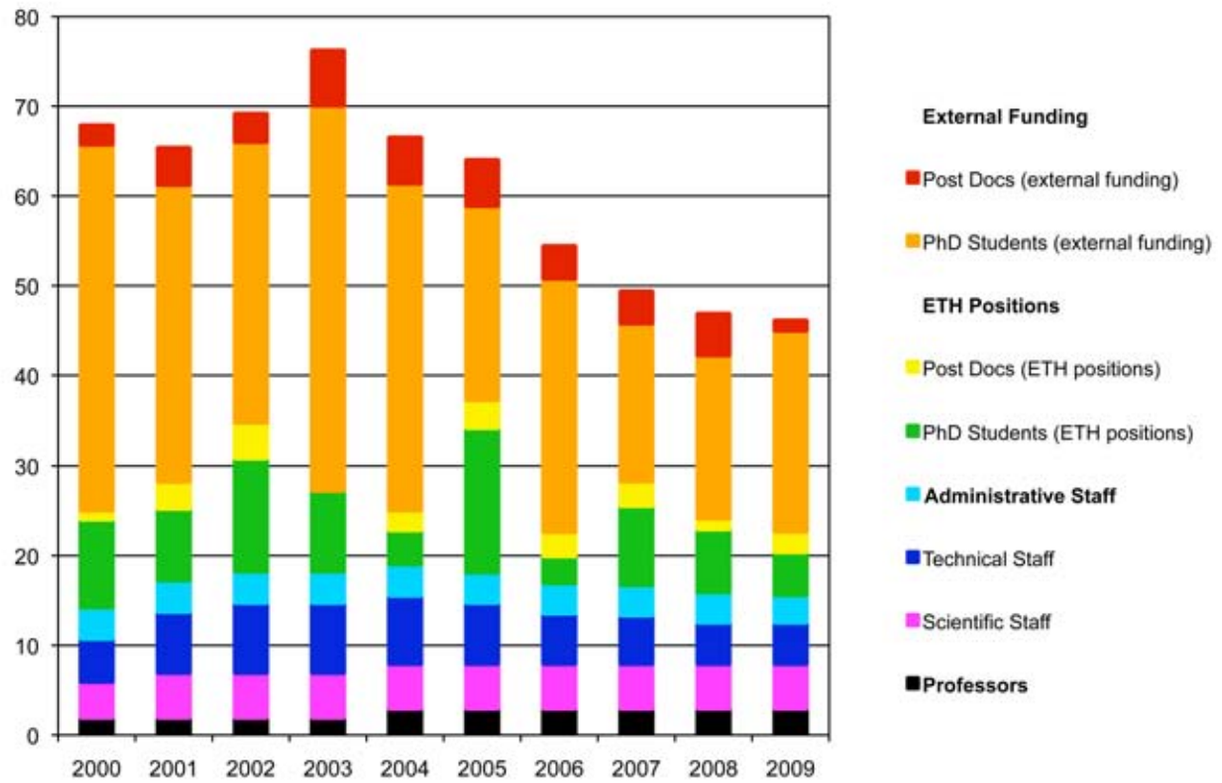
Partners and Funding Agencies
The activities of our laboratory were only possible through the support from the governing board of our university, and several national and international institutions and industrial parties. Special thanks go to our school, to the computing services of ETH Zurich, as well as to the Department of Information Technology and Electrical Engineering and its services and administration.
Finally, we would like to express our gratitude to the Swiss Commission for Technology and Innovation (KTI/CTI), the Swiss National Science Foundation (SNF), the Swiss State Secretariate for Education and Research (SER), the Commission of the European Union and the Hasler Stiftung Switzerland, for their financial support. Just as much, we would like to thank our partners ACP Switzerland, Alstom France, AMAT USA, Anagram Switzerland, austriamicrosystems Austria, BridgeCo Switzerland, Celestrius Switzerland, ECPE Germany, Enablence Switzerland (former Albis Optoelectronics Switzerland), FH Windisch Switzerland, Fondazione Bruno Kessler Italy, Fujitsu Japan, Huber+Suhner Switzerland, IBM Research Switzerland, id Quantique Switzerland, IMEC Belgium, Infineon Austria, IT'IS Foundation Switzerland, NEC Japan, NTT Japan, Osram Germany, Samsung Korea, SPEAG Switzerland, ST Microelectronics France and Italy, Synopsys Switzerland LLC, Synopsys, Inc. USA and Germany, Toshiba Japan, Technical University Graz Austria, University of Bologna Italy, University of Bordeaux France, University of Cagliari Italy, University of Kassel Germany, University of Linz Austria, Loughborough University England, Lund University Sweden, University of Nottingham England, University of Parma Italy, University of Pisa Italy, University of Purdue USA, University of Regensburg Germany, VEST Corp. France, VSEA USA, Zurich MedTech Switzerland, the EPFL laboratories IQEP, LPN, LSM, QP-NCCR in Lausanne Switzerland, the ETH Zurich laboratories CGL, HVL, IfA, IfE, IBT, IFH, IKT, IQE, IWR, and Vision Laboratory for the fruitful cooperation in research projects as well as for their financial support.

Organization



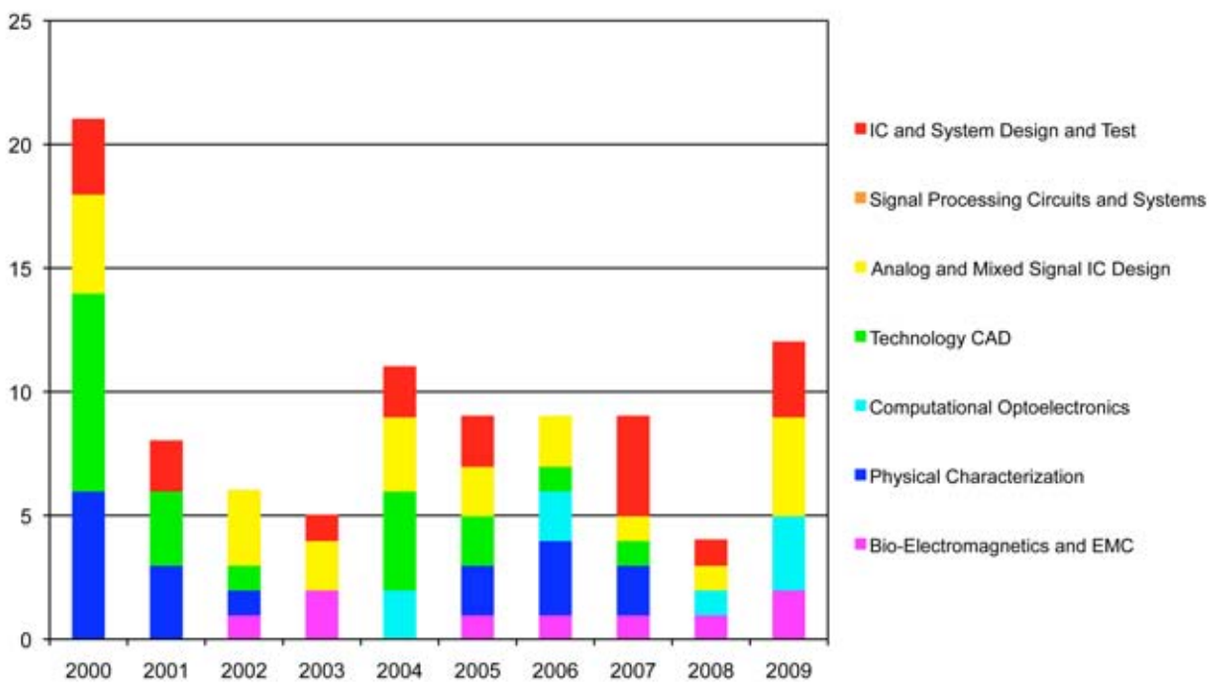
Representative Figures

Staff



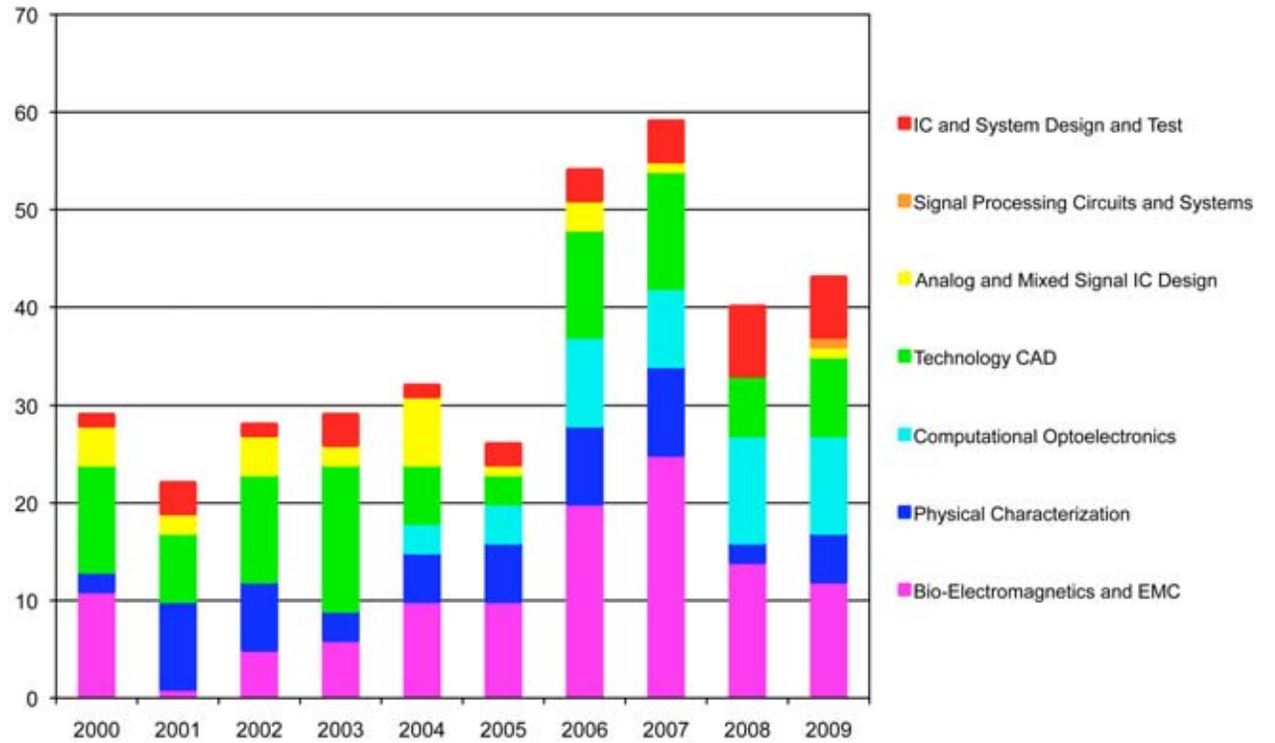
Number of FTE (full-time equivalent) job positions at the Integrated Systems Laboratory from 2000 to 2009.

PhD Theses



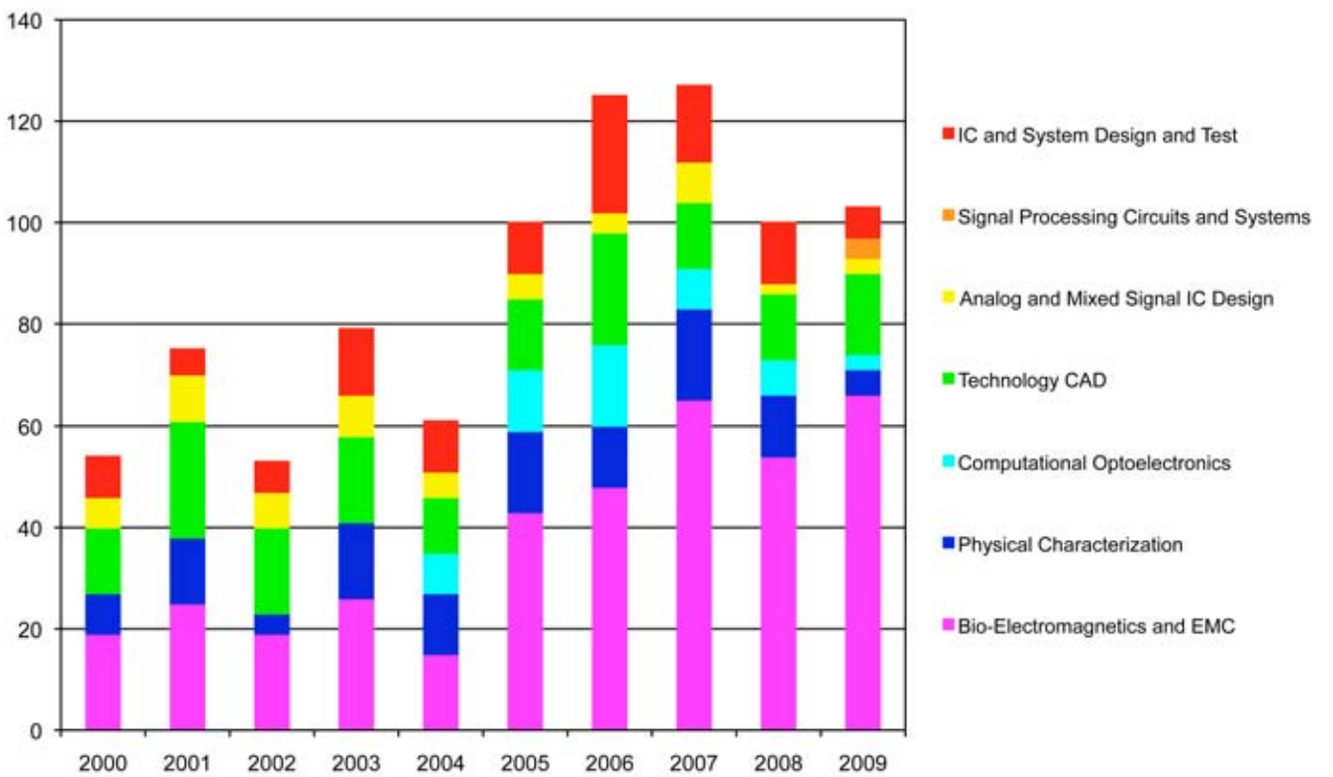
Number of completed PhD theses per year at the Integrated Systems Laboratory from 2000 to 2009. Abstracts of PhD theses: see page 105.

Journal and Book Publications



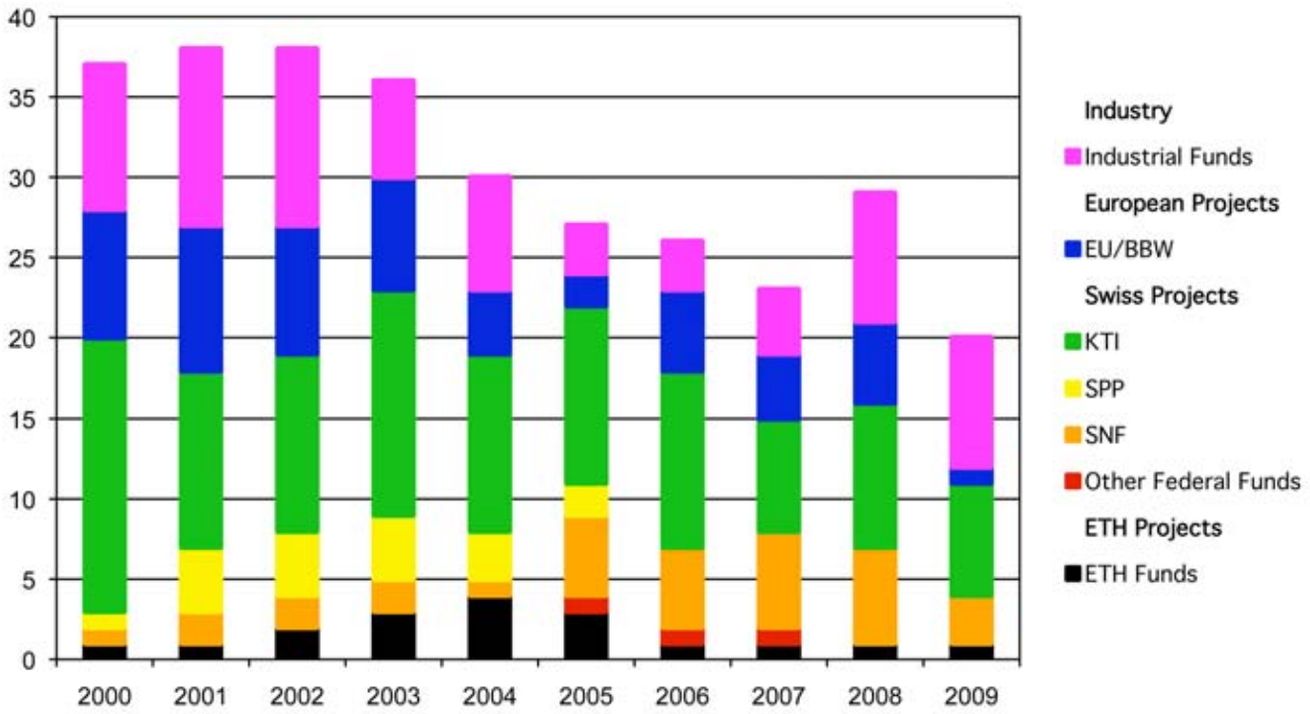
Number of journal and book publications by the Integrated Systems Laboratory from 2000 to 2009. References: see pages 125ff.

Conference and Workshop Presentations



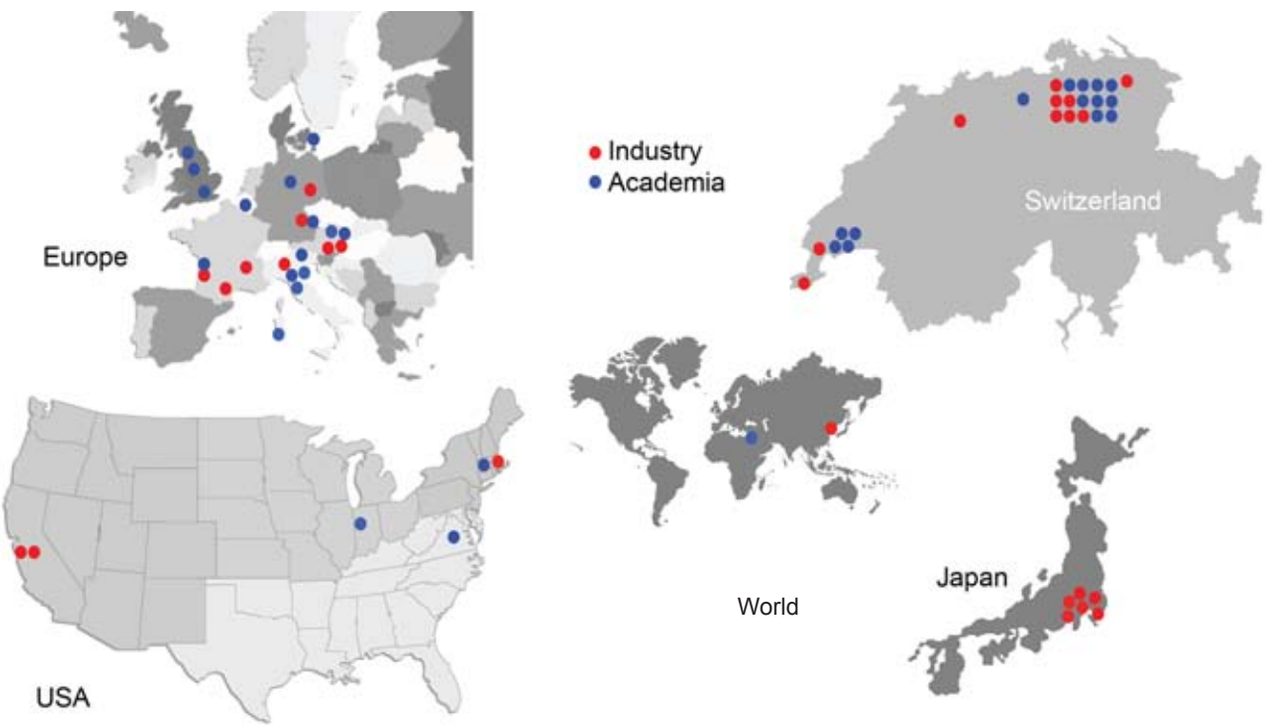
Number of conference and workshop presentations by the Integrated Systems Laboratory from 2000 to 2009 References: see pages 132ff.

IIS Research Projects



Number of research projects with external funding at the Integrated Systems Laboratory from 2000 to 2009. Overview of research projects: see pages 118ff. Partners and funding agencies: see pages 24ff.

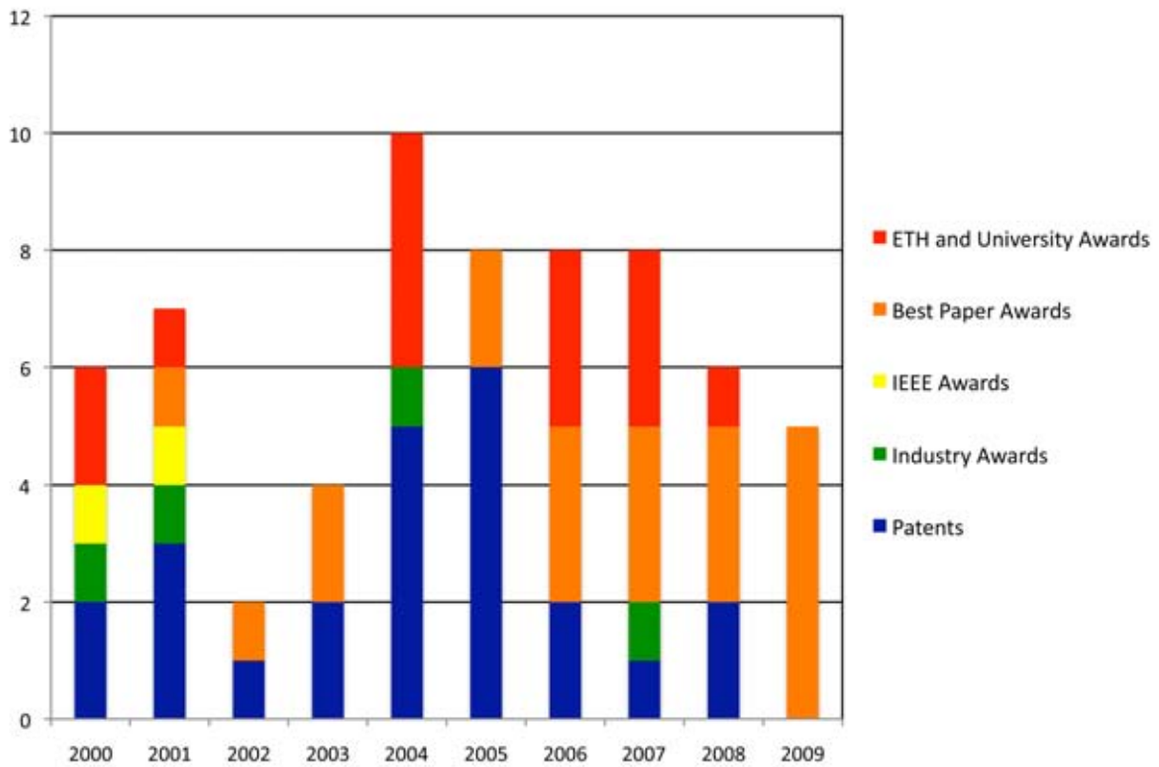
Research Partners of IIS



	CH	Europe	USA	Japan	Others	World
Industry	10	6	3	6	1	26
Academia	10	18	3	0	1	32

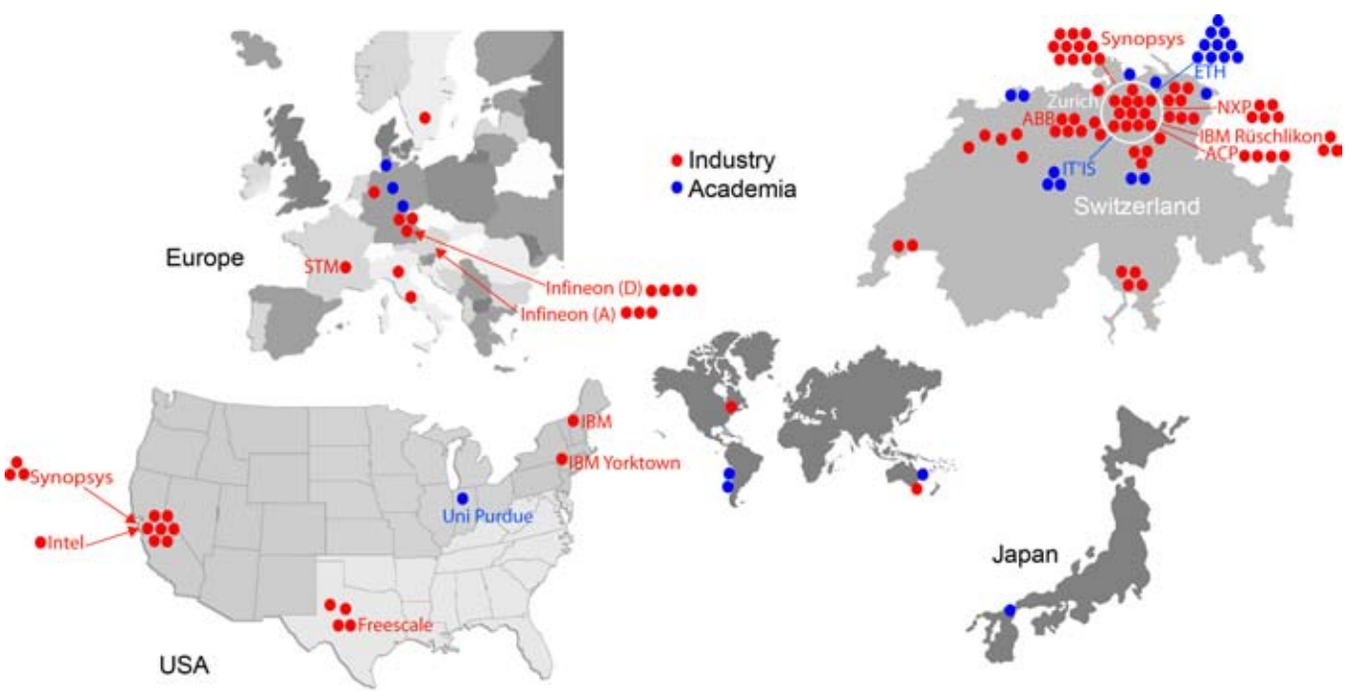
Research partners of the Integrated Systems Laboratory in Switzerland (CH), Europe, and worldwide. Addresses of partners: see pages 24ff.

Awards and Patents



Academic & industrial awards and patents received by Integrated Systems Laboratory staff from 2000 to 2009. References for 2009: see pages 28ff.

Former PhD Students



Working places in industry and academia of 138 former PhD students graduated at Integrated Systems Laboratory in Switzerland, Europa, USA, Japan and worldwide. Addresses of former PhD students: see pages 17ff.

Staff

Professors

Fichtner Wolfgang, Dr., Professor for Electronics, Head	since	1 Sep	1985			
Huang Qiuting, Dr., Professor for Electronics	since	1 Jan	1993			
Burg Andreas, Prof., Dr. Dipl. El.-Ing. ETH	since	1 Jan	2009			
Schenk Andreas, Prof., Dr., Dipl.-Phys., Senior Scientist	since	1 Aug	1991			

Microelectronics Design Center

Kaeslin Hubert, Dr., Dipl. El.-Ing. ETH, Head	since	1 Jan	1986			
Gürkaynak Frank, Dr., Dipl. El. Ing	since	1 Jun	2008			
Köppel Rudolf, FEAM		1 Apr	1995	–	31 Dec	2009
Muheim Beat, Dipl. El. Ing. ZHAW	since	1 Aug	2008			
Schöni Daniel, Ing. für elektronisches Design	since	1 Oct	2009			

Scientific Staff

Aemmer Dölf, Dr., Dipl. Phys. ETH, Senior Scientist	since	1 Sep	1985			
Bäcker Alexandra, Dr., Dipl.-Ing.		1 Oct	2004	–	31 Mar	2009
Benkeser Christian, Dr., Dipl. El.-Ing. ETH	since	15 Sep	2004			
Blattmann René, Dipl. El.-Ing. ETH	since	1 Apr	2008			
Bruderer Lukas, M. Sc. ETH Zurich	since	20 Apr	2009			
Burger Thomas, Dr., Dipl. El.-Ing. ETH	since	1 Oct	1994			
Carnelli Dario Albino, M. Sc. EE	since	15 Nov	2008			
Chen Yihui, M. Sc. EE		1 Aug	2005	–	31 Jul	2009
Chen Yangjian, Dr., El.-Ing.	since	1 Oct	2007			
Ciappa Mauro, Dr., Dipl. Phys.	since	1 Jan	1998			
Del Castillo Guillermo, Dr., M. Mech. Engineer		1 Mar	2005	–	30 Apr	2009
Dolgos Denis, Dipl. Phys	since	1 Jan	2008			
Eberli Stefan, Dr., Dipl. El.-Ing. ETH	since	1 Dec	2003			
Esposito Aniello, Dipl. Phys. ETH	since	15 Aug	2005			
Fateh Schekeb, Dipl. El.-Ing. ETH	since	6 Jun	2009			
Felber Norbert, Dr., Dipl. Phys. ETH, Senior Scientist	since	1 Jul	1987			
Frey Martin, Dipl. Phys. ETH	since	15 Aug	2005			
Greisen Pierre, Dipl. El.-Ing. ETH	since	1 Jan	2009			
Haene Simon, Dr., Dipl. El.-Ing. ETH		1 Jul	2008	–	31 Mar	2009
Henzen Luca, Dipl. El.-Ing. ETH	since	1 Aug	2007			
Holzer Stefan, Dr. techn., Dipl.-Ing.		1 Dec	2008	–	30 Nov	2009
Keogh Craig Brendan, M. Sc. EE	since	1 Apr	2005			
Koch Thomas, M. Sc. EE ETH		1 Mai	2008	–	30 Apr	2009
Koschik Alexander, Dr. techn., Dipl.-Ing.	since	15 Mai	2008			
Kreuter Philipp, Dipl.-Ing. Elektro- u. Informationstechnik	since	1 Oct	2005			
Kühn Sven, Dr., Dipl. Ing. Informationstechnik		1 Mar	2005	–	31 Jul	2009
Kupec Jan, Dipl.-El.-Ing.	since	1 Jan	2008			
Li Chung-Huan, M. Sc. EE	since	5 Apr	2007			
Lüthi Peter, Dr., Dipl. El.-Ing. ETH		1 Nov	2003	–	31 Dec	2009
Mächler Patrick, Dipl. El.-Ing. ETH	since	1 Sep	2008			
Malandruccolo Vezio, Dipl. El.-Ing.	since	1 Mar	2008			
Mangiacapra Luigi, Dipl. Phys.	since	1 Sep	2008			
Martelli Chiara, Dr., Dipl. El.-Ing.	since	17 Jan	2001			
Meier Hektor, Dipl. El.-Ing. ETH	since	1 Apr	2007			
Meinerzhagen Pascal, ing.él. dipl. EPFL	since	1 Jan	2009			

Nadakuduti Jagadish, M. Sc. EE	since	8 Jun	2009			
Peikert Vincent, Dipl. Phys. ETH	since	1 Feb	2009			
Roth Christoph, M. Sc. EE ETH	since	1 Sep	2009			
Sahli Beat, Dr., Dipl.-Phys.		1 Jun	2000	–	30 Jun	2009
Senning Christian, M. Sc. EE ETH	since	1 Mar	2008			
Stefanski Tomasz, Dr., El.-Ing.	since	1 Sep	2009			
Steiger Sebastian, Dr., Dipl. Phys. ETH		1 Nov	2005	–	30 Jun	2009
Treichler Jürg, Dr., Dipl. El.-Ing. ETH	since	1 May	2003			
Ulrich Roger, Dipl. El.-Ing. ETH	since	1 Aug	2009			
Veprek Ratko, Dr., Dipl. Rech. Wiss. ETH		1 Aug	2005	–	31 Jul	2009
Vollenweider, Dipl. Phys. ETH	since	1 Jan	2007			
Wenk Markus, Dipl. El.-Ing. ETH	since	1 Jan	2006			

Computer Staff

Feigin, Adam, Dipl. El.-Ing.	since	1 May	2006			
Kunz Fredi, Reallehrer	since	15 Aug	2009			
Richardet Christoph, Oberstufenlehrer		10 Mai	2000	–	31 Mai	2009
Wicki Christoph, Dipl. El.-Ing. ETH	since	1 Oct	1985			

Technical Staff

Gisler Hansjörg, Industriespengler	since	1 Aug	1989			
Kleier Thomas, Dipl.-Ing. (FH) Nachrichtentechnik	since	1 Jun	2005			

Administrative Staff

Fischer Bruno, Dipl. El.-Ing. HTL	since	14 Apr	1992			
Haller Christine, Betriebsökonomin HWV (95%)	since	8 Mar	1993			
Müller Claudia (35%)		1 May	2006	–	31 Aug	2009
Plank Eva (60%)	since	1 Jul	1998			
Roffler Verena (50%)	since	1 Sep	1999			

Former PhD Students

Name	Year	Now with
Bach Carlo	1993	Interstaatliche Hochschule für Technik (NTB) Werdenbergstrasse 4, CH-9471 Buchs, Switzerland
Bäcker Alexandra	2009	Fürstentum Liechtenstein
Balmelli Pio	2003	Silicon Laboratories 7000 West William Cannon Drive, Bldg. 1, Austin, TX 78735, USA
Basedau Philipp	1999	NXP Semiconductors Switzerland AG Binzstrasse 44, CH-8045 Zürich, Switzerland
Benkeser Christian	2009	Integrated Systems Laboratory, ETH Zürich CH-8092 Zürich, Switzerland
Benkler Stefan	2006	SPEAG Zeughausstrasse 43, CH-8004 Zürich, Switzerland
Berdinas Veronika	2007	EMPA Überlandstrasse 129, CH-8600 Dübendorf
Bonnenberg Heinz	1993	ESPROS Photonics AG Lindenstrasse 10, CH-6340 Baar, Switzerland
Bösch Thomas	2004	STMicroelectronics N.V. Via Cantonale 16 E, CH-6928 Manno, Switzerland
Brenna Gabriel	2004	McKinsey & Company, Inc. Alpenstrasse 3, CH-8065 Zurich
Brugger Simon	2005	
Burg Andreas	2005	Integrated Systems Laboratory, ETH Zürich CH-8092 Zürich, Switzerland
Burger Thomas	2002	Integrated Systems Laboratory, ETH Zürich CH-8092 Zürich, Switzerland
Bürgin Felix	2008	ESPROS Photonics AG Lindenstrasse 10, CH-6340 Baar, Switzerland
Bürgler Josef	1990	Hochschule Technik+Architektur Luzern Technikumstrasse 21, CH-6048 Horw, Switzerland
Buzzo Marco	2006	Infineon Technologies AG Siemensstrasse 2, A-9500 Villach, Austria
Carbognani Flavio	2007	V. le della Villetta 6/1, I-43100 Parma, Italy
Chavannes Nicolas	2002	IT'IS Foundation Zeughausstrasse 43, CH-8004 Zürich, Switzerland
Chen Xinhua	2007	Marvell Switzerland Sarl Route de Pallatex 17, CH-1163 Etoy, Switzerland
Chen Yihui	2009	Professur Biosystems Engineering, ETH Zürich Mattenstrasse 26, 4058 Basel
Christ Andreas	2003	IT'IS Foundation Zeughausstrasse 43, CH-8004 Zürich, Switzerland
Christen Thomas	2009	Integrated Systems Laboratory, ETH Zürich CH-8092 Zürich, Switzerland
Ciampolini Lorenzo	2001	STMicroelectronics, Front-End Technology and Manufacturing 850, Rue Jean Monnet - BP16, F-38926 Crolles Cedex
Ciappa Mauro	2000	Integrated Systems Laboratory, ETH Zürich CH-8092 Zürich, Switzerland
Conti Paolo	1991	Glasmalergasse 2, CH-8004 Zürich, Switzerland
Corvasce Chiara	2006	ABB Semiconductors AG R&D Lb2, Fabrikstrasse 3, CH-5600 Lenzburg, Switzerland
Curiger Andreas	1993	Omnisec AG Rietstrasse 14, CH-8108 Dällikon, Switzerland
Deiss Armin	2002	Microtune, Inc. 2201 10th Street, Plano, TX 75074, USA
Dettmer Hartmut	1994	Infineon Technologies AG Siemensstrasse 2, A-9500 Villach, Austria

Doswald Daniel	2000	Seeweg 4, CH-6330 Cham, Switzerland
Eberli Stefan	2009	Integrated Systems Laboratory, ETH Zürich CH-8092 Zürich, Switzerland
Ebert Sven	2009	Kronenstrasse 25, 8006 Zürich, Switzerland
Eicher Simon	1996	ABB Semiconductors AG R&D Lb2, Fabrikstrasse 3, CH-5600 Lenzburg, Switzerland
Esmark Kai	2001	Infineon Technologies IFAG AIM AP D TD M, Am Campeon 1-12, D-85579 Neubiberg, Germany
Etherton Melanie	2005	Freescale Semiconductor, Inc. 3501 Ed Bluestein Blvd. MD:K10, Austin, TX 78721, USA
Fillo Marco	1993	Quadrics Supercomputers World Ltd. Via Marcellina 11, I-00131 Roma, Italy
Francese Pier-Andrea	2005	National Semiconductor GmbH, Data Conversion Systems Group Livry-Gargan-Str. 10, D-82256 Fürstenfeldbruck, Germany
Gappisch Steffen	1996	NXP Semiconductors Switzerland AG Binzstrasse 44, CH-8045 Zürich, Switzerland
Garreton Gilda	1998	Sun Microsystems Laboratories Asynchronous Group, 16 Network Circle, Menlo Park, CA 94025, USA
Geelhaar Frank	2004	Globalfoundries 1050 E. Arques Ave, Sunnyvale CA 94085, USA
Glaser Ulrich	2006	Infineon Technologies IFAG AIM AP D TD M, Am Campeon 1-12, D-85579 Neubiberg, Germany
Gull Ronald	1996	Synopsys Switzerland LLC Thurgauerstrasse 40, CH-8050 Zürich, Switzerland
Gürkaynak Frank	2005	Integrated Systems Laboratory, ETH Zürich CH-8092 Zürich, Switzerland
Häne Simon	2007	IM Ingegneria Maggia SA Via S. Franscini 5, 6601 Locarno
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Hammerschmied Clemens	2000	Maxim Integrated Products 120 San Gabriel Drive, Sunnyvale, CA 94086, USA
Heeb Hansruedi	1989	Im Tiergarten 9, CH-8055 Zürich, Switzerland
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Heiser Gernot	1991	University of New South Wales, School of Computer Science & Engineering P.O. Box 1, Sydney, 2052 NSW, Australia
Herkersdorf Andreas	1991	TU München, Institute for Integrated Systems Arcisstr. 21, D-80290 München, Germany
Herrigel Alexander	1990	Bergstrasse 62, CH-8706 Meilen, Switzerland
Hertle Jürgen	2004	Miromico AG, Sonneggstrasse 76, CH-8006 Zürich, Switzerland
Heusler Lucas	1990	IBM Zurich Research Division Zurich Research Laboratory, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland
Hitschfeld Nancy	1993	Departamento de Ciencias de la Computación, Universidad Católica de Chile Blanco Encalada 2120, Santiago, Chile
Höfler Alexander	1997	Freescale Semiconductor Inc. 6501 West William Cannon Drive, Mail Drop OE341, Austin, TX 78735, USA
Höhr Timm	2005	Robert Bosch GmbH D-72703 Reutlingen, Germany
Humbel Oliver	2000	Infineon Technologies Austria AG AI PL T PI 32 HV, Siemensstrasse 2, A-9500 Villach, Austria
Kells Kevin	1994	Synopsys, Inc. 700 East Middlefield Road, Mountain View, CA 94043, USA
Körner Thomas	1999	
Kouchev Ilian	2006	Advanced Circuit Pursuit AG Zwischenweg 2, CH-8702 Zollikon, Switzerland
Krause Jens	2001	Trithor GmbH, D-5339 Rheinbach, Germany

Krumbein Ulrich	1996	Infineon Technologies WS SD D Tr MOS, Postfach 80 09 49, D-81609 München, Germany
Kühn Sven	2009	IT'IS Foundation Zeughausstrasse 43, CH-8004 Zürich, Switzerland
Kuratli Christoph	1999	EM Microelectronic Marin SA Sensor & Actuator Interfaces, Rue des Sors 3, CH-2074 Marin, Switzerland
Laino Valerio	2006	
Lamb Peter	1990	55 Gilbert ST, Hackett 2602, Canberra, Australia
Lendenmann Heinz	1994	ABB Corporate Research Dept. G, SE-721 78 Västerås, Sweden
Leonhardt Götz	2000	Synopsys, Inc. 700 East Middlefield Road, Mountain View, CA 94043, USA
Liegmann Arno	1995	Rüti 18, CH-8357 Guntershausen, Switzerland
Litsios James	1996	Actant AG Bahnhofstrasse 10, CH-6300 Zug, Switzerland
Loeser Martin	2008	ZHAW, Institute of Computational Physics Wildbachstrasse 21, 8401 Winterthur, Switzerland
Luisier Mathieu	2007	Network for Computational Nanotechnology, Purdue University 465 Northwestern Avenue, West Lafayette, IN-47907, USA
Lüthi Peter	2009	Integrated Systems Laboratory, ETH Zürich CH-8092 Zürich, Switzerland
Martelli Chiara	2006	Advanced Circuit Pursuit AG Zwischenweg 2, CH-8702 Zollikon, Switzerland
Menolfi Christian	2000	IBM Zurich Research Laboratory Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland
Mergens Markus	2001	QPX GmbH Lincolnstrasse 54/II, D-81549 München, Germany
Müller Christoph	2004	Rahn & Bodmer Talstrasse 15, CH-8022 Zürich, Switzerland
Müller Stephan	1994	Sun Microsystems Santa Clara, CA-95054, USA
Muttersbach Jens	2001	Zühlke Engineering AG Wiesenstrasse 10a, CH-8952 Schlieren, Switzerland
Neeracher Matthias	1998	Binzwiesenstrasse 25, CH-8057 Zürich, Switzerland
Nussbaum Miguel	1988	Departamento de Ciencias de la Computación, Universidad Católica de Chile Casilla 6177, Santiago, Chile
Oberle Michael	2002	SPEAG AG Zeughausstrasse 43, CH-8004 Zürich, Switzerland
Odermatt Stefan	2006	Synopsys Switzerland LLC Thurgauerstrasse 40, CH-8050 Zürich, Switzerland
Oesch Walter	2005	Ammann Aufbereitung AG Eisenbahnstrasse 25, CH-4901 Langenthal, Switzerland
Omura Ichiro	2001	Department of Electrical and Electronical Engineering, Kyushu Institute of Technology Sensui-cho, Tobata-ku, Kitakyushu, 804-8550, Japan
Orsatti Paolo	2000	NemeriX SA Stabile Gerre 2000, Casella postale 425, CH-6928 Manno, Switzerland
Papadopoulos Dimitris	2008	Marvell Switzerland Sarl Route de Pallatex 17, CH-1163 Etoy, Switzerland
Perels David	2007	Phonak AG Laubisrütistrasse 28, CH-8712 Stäfa
Pfaff Dirk	2003	Diablo Technologies Inc. 290 Boulevard St-Joseph, Suite 200, Gatineau, Quebec, J8Y 3Y3, Canada
Pfäffli Paul	1999	Synopsys Switzerland LLC Thurgauerstrasse 40, CH-8050 Zürich, Switzerland
Pfeiffer Michael	2004	Vela Solaris AG Herrenberg 35, CH-8640 Rapperswil, Switzerland
Piazza Francesco	2000	NemeriX SA Stabile Gerre 2000, Casella postale 425, CH-6928 Manno, Switzerland

Pommerell Claude	1992	ABB (Switzerland) Ltd. CH-I Information Technology, Brown Boveri Strasse 6, CH-5400 Baden, Switzerland
Rogenmoser Robert	1996	1633 Benton Ct, Sunnyvale, CA 94087, USA
Rogin Jürgen	2004	Advanced Circuit Pursuit AG Zwischenweg 2, CH-8702 Zollikon, Switzerland
Röllin Stefan	2004	Schindler Aufzüge Zugerstrasse 13, CH6030 Ebikon, Switzerland
Roth Eric	2004	Esmertec AG Lagerstrasse 14, CH-8600 Dübendorf, Switzerland
Rothacher Fritz	1995	Infineon Technologies Communication Solutions, Am Campeon 1-12, D-85579 Neubiberg, Germany
Röwer Thomas	2000	1 Pilgrim Drive, Danbury, CT 06811, USA
Rühl Roland	1992	PDF Solutions, Inc. 333 West San Carlos Street, San Jose, CA 95110, USA
Ryter Roland	1996	NXP Semiconductors Switzerland AG B137, Binzstrasse 44, CH-8045 Zürich, Switzerland
Saad Yves	2007	Synopsys Switzerland LLC Thurgauerstrasse 40, CH-8050 Zürich
Sahli Beat	2006	Integrated Systems Laboratory, ETH Zürich CH-8092 Zürich, Switzerland
Schenk Olaf	2000	University of Basel, Department of Computer Science Klingelbergstrasse 50, CH-4056 Basel, Switzerland
Schenkel Michael	2002	Synopsys Switzerland LLC Thurgauerstrasse 40, CH-8050 Zürich, Switzerland
Schmithüsen Bernhard	2001	Synopsys Switzerland LLC Thurgauerstrasse 40, CH-8050 Zürich, Switzerland
Schneider Lutz	2006	Synopsys Switzerland LLC Thurgauerstrasse 40, CH-8050 Zürich, Switzerland
Scholze Andreas	2000	IBM Systems & Technology Group, Semiconductor Research and Development Center Essex Junction, VT 05452, USA
Schönbächler Edgar	1998	Bien-Air Dental SA Länggasse 60, Case Postale 6008, CH-2500 Bienne 6, Switzerland
Schuderer Jürgen	2003	ABB Corporate Research Applied Physics & Materials, Segelhof 1, CH-5405 Baden-Dättwil, Switzerland
Schuster Christian	2000	TU Hamburg-Harburg, Institute of Electromagnetic Theory Harburger Schloss Str. 20, D-21079 Hamburg, Germany
Seda Steven	1993	Zurich Financial Services Mythenquai 2, CH-8022 Zürich, Switzerland
Sponton Luca	2007	Synopsys Switzerland LLC Thurgauerstrasse 40, CH-8050 Zürich, Switzerland
Stadler Manfred	2000	Winernstrasse 20, CH-5430 Wettingen, Switzerland
Stangoni Maria	2005	Huber+Suhner AG Wire + Cable Division, Tumbelenstrasse 20, CH-8330 Pfäffikon, Switzerland
Steiger Sebastian	2009	
Streiff Matthias	2004	Sensirion AG Laubisruetistrasse 50, CH-8712 Stäfa, Switzerland
Stricker Andreas	2000	MAXIM Integrated Products 3725 N First Street, San Jose, CA 95134, USA
Studer Christoph	2009	Communication Technology Laboratory, ETH Zürich CH-8092 Zürich, Switzerland
Thalheim Jan	2003	CT-Concept Technologie AG J. Renfer-Strasse 15, CH-2504 Biel, Switzerland
Thalmann Markus	2000	Stapferstrasse 25, CH-8006 Zürich, Switzerland
Treichler Jürg	2009	Integrated Systems Laboratory, ETH Zürich CH-8092 Zürich, Switzerland
Tschopp David	2005	Advanced Circuit Pursuit AG Zwischenweg 2, CH-8702 Zollikon, Switzerland
Veprek Ratko	2009	

Villablanca Luis	2000	Synopsys, Inc. 700 East Middlefield Road, Mountain View, CA 94043, USA
Villiger Thomas	2004	NXP Semiconductors Switzerland AG Binzstrasse 44, CH-8045 Zürich, Switzerland
von Arx Christoph	1996	cva technical consulting ag Geissfluhweg 30, CH-4600 Olten, Switzerland
Wassner Jürgen	2001	Hochschule Luzern, Technik & Architektur Technikumstrasse 21, CH-6048 Horw
Wegmüller Marc	2007	Zühlke Engineering AG Wiesenstrasse 10a, CH-8952 Schlieren
Westermann Marc	1995	Logismata AG Hardturmstrasse 76, CH-8005 Zürich, Switzerland
Wettstein Andreas	2000	Synopsys Switzerland LLC Thurgauerstrasse 40, CH-8050 Zürich, Switzerland
Wikström Tobias	2000	ABB Switzerland Ltd., Semiconductors Fabrikstrasse 3, CH-5600 Lenzburg, Switzerland
Witzig Andreas	2002	Vela Solaris AG Herrenberg 3, CH-8640 Rapperswil, Switzerland
Witzigmann Bernd	2000	University of Kassel, Computational Electronics and Photonics Institute Wilhelmshoeher Allee 71, D-34121 Kassel, Germany
Yun Chan-Su	2000	Synopsys, Inc. 700 East Middlefield Road, Mountain View, CA 94043, USA
Zahir Rumi	1991	428 Glenwood Avenue, Menlo Park, CA 94025, USA
Zelenka Stefan	2001	
Zimmermann Reto	1997	Synopsys Switzerland LLC Thurgauerstrasse 40, CH-8050 Zürich, Switzerland

Academic Guests

Dr. Miao Peng	Southeast University, Nanjing, China	15 Sep 2008 - 30 Jun 2009
Prof. Dr. Shahriar Mirabbasi	University of British Columbia, Vancouver, Canada	1 Oct 2008 - 31 Mar 2009
Haruka Kubo	Toshiba Corporation, Yokohama, Japan	11 Oct 2008 - 14 Oct 2009
Yuji Sasaki	Toshiba Corporation, Yokohama, Japan	since 10 Oct 2009
Dr. Norio Sato	NTT Corporation, Kanagawa, Japan	17 Nov 2008 - 15 Nov 2009
Hiroyoshi Togo	NTT Integrated Information & Energy Systems Labs,Kanagawa, Japan	14 Jan 2009
Dr. Maurizio Dapor	Center for Materials and Microsystems, Povo Italy	2 Feb - 6 Feb 2009
Mikhail Alekseev	Cadence Design Systems, Zelenograd, Russia	16 Feb - 18 Feb 2009
Prof. David Atienza	EPFL Lausanne, Switzerland	23 Feb 2009
Ahmed Noeman	Cadence Design Systems GmbH, Feldkirchen, Germany	25 Feb - 27 Feb 2009
Prof. Dr. Katsumi Kishino	Sophia Univesity, Tokyo, Japan	2 Mar 2009
Dr. Maurizio Dapor	Center for Materials and Microsystems, Povo, Italy	2 Mar - 6 Mar 2009
Prof. Dr. Heinrich Meyr	RWTH Aachen, Aachen, Germany	3 Mar 2009
Martin Feldhofer	TU Graz, Graz, Austria	17 Mar - 18 Mar 2009
Dr. Felix Lustenberger	Espros Photonics AG, Baar, Switzerland	15 May 2009
Dr. Maurizio Dapor	Center for Materials and Microsystems, Povo, Italy	11 May - 15 May 2009
Dr. Thomas Haustein	TU Berlin, Berlin, Germany	18 Mai 2009
Dr. Othman Sidek	Universiti Sains Malaysia, Penang, Malaysia	25 May 2009
Alessandro Cevrero	EPFL Lausanne, Switzerland	2 Jun - 26 Oct 2009
Prof. Pierre Fazan	EPFL Lausanne, Switzerland	5 Jun 2009
Dr. Cedric Bassin	EPFL Lausanne, Switzerland	5 Jun 2009
Prof. Dr. Dimitri Y. Antoniadis	MIT, Cambridge, MA, USA	12 Jun 2009
Prof. Dr. Aldi di Carlo	Universita di Roma, Roma, Italy	12 Jun 2009
Prof. Dr. Ichiro Omura	Kyushu Institute of Technology, Kitakyushu, Japan	19 Jun 2009
Dr. Satoshi Matsumoto	MIT, Cambridge, MA, USA	19 Jun 2009
Prof. Dr. Emanuele Viterbo	Universita della Calabria, Rende, Italy	10 Jul 2009
Dr. Maurizio Dapor	Center for Materials and Microsystems, Povo, Italy	13 Jul - 17 Jul 2009
Prof. Dr. Heinrich Meyr	RWTH Aachen, Aachen, Germany	31 Aug 2009
Dr. Takejisa Seino	Toshiba Corporation, Yokohama, Japan	21 Sep 2009
Satoshi Sumida	Toshiba Corporation, Yokohama, Japan	21 Sep 2009
Dr. Maurizio Dapor	Center for Materials and Microsystems, Povo, Italy	12 Oct - 16 Oct 2009
Louise Bradley	ST Microelectronics	21 Oct 2009
Bruno Cavalli	ST Microelectronics	21 Oct 2009
Guido Keel	Fachhochschule Nordwestschweiz, Brugg, Switzerland	21 Oct 2009
Marc Kristol	HMT Microelectronic AG	21 Oct 2009
Alex Huber	Fachhochschule Nordwestschweiz, Brugg, Switzerland	21 Oct 2009
Gerard Mc Glew	HMT Microelectronic AG	21 Oct 2009
Milen Penev	Fachhochschule Nordwestschweiz, Brugg, Switzerland	21 Oct 2009
Pavle Petrovic	ST-Ericsson	21 Oct 2009
Christoph Rüegg	ST Microelectronics	21 Oct 2009
Prof. Dr. Yusuf Leblebici	EPFL, Lausanne, Switzerland	16 Nov 2009
Prof. Dr. Bernhard Boser	Berkeley University of California, USA	5 Dec 2009
Ms. Gao Sumei	Ministry of Industry and Information Technology, Beijing, China	10 Dec 2009
Ms. Wang Xiaoping	Ministry of Industry and Information Technology, Beijing, China	10 Dec 2009
Mr. Gao Yuqi	Ministry of Industry and Information Technology, Beijing, China	10 Dec 2009
Mr. Shi Iijun	China National Tendering Center of MACH.&ELEC Equipment, Beijing, China	10 Dec 2009
Mr. Chen Xiaoxing	Hainan Communicatins Administration, Hainan, China	10 Dec 2009
Ms. Li Wei	Qinghai Communications Administragion, Qinghai, China	10 Dec 2009

Mr. He Wei	Shanghai Municipal Economic Informization Commision, Shanghai, China	10 Dec 2009
Ms. Zhang Rongkun	The Center for Vocational Ability Identification of Hebei Communication, Hebei, China	10 Dec 2009
Mr. Zhang Xiaohui	Jiangxi Industry and Information Technology Commission, Jiangxi, China	10 Dec 2009
Mr. Zhang Baicheng	Informatization Office of Inner Mongolia Autnomous Region Gov, China	10 Dec 2009
Mr. Yu Pengchao	China Telecommunications Corp., Beijing, China	10 Dec 2009
Ms. Jin Huagang	Nanjing Research Institute of Electronics Engineering	10 Dec 2009
Prof. Dr. Heinrich Meyr	RWTH Aachen, Aachen, Germany	16 Dec 2009
Dr. Takamoto Watanabe	DENSO Corporation, Aichi-ken, Japan	18 Dec 2009
Dr. Mathieu Luisier	Purdue University, West Lafayette, IN, USA	18 Dec 2009
Dr. Takamoto Watanabe	DENSO Corp., Aichi-ken, Japan	18 Dec 2009

Partners and Funding Agencies

ACP	ACP Advanced Circuit Pursuit AG Alte Landstrasse 101, CH-8702 Zollikon ZH, Switzerland
Alstom	• Alstom Transport S.A. 3 Avenue André Malraux, F-92300 Levallois-Perret, France • Alstom Transport Composants Rue du Docteur Guinier - BP 4, F-65600 Semeac, France
AMAT	Applied Materials, Inc. 974 E. Arques Avenue, M/S 81157, Sunnyvale, CA 94086, USA
Anagram	Anagram Technologies SA Zl Le Trési 6A, CH-1028 Préverenges, Switzerland
austriamicrosystems	austriamicrosystems AG Schloss Premstätten, A-8141 Unterpremstätten, Austria
BBT	Bundesamt für Berufsbildung und Technologie (Federal Office for Professional Education and Technology, a Swiss Government Agency) Effingerstrasse 27, CH-3003 Bern, Switzerland
BCI	BCI Group Moosstrasse 68-78, CH-2540 Grenchen, Switzerland
BridgeCo	BridgeCo AG Ringstrasse 14, CH-8600 Dübendorf, Switzerland
Celestrius	Celestrius AG Hochstrasse 60, CH-8092 Zurich, Switzerland
CGL-ETHZ	Computer Graphics Laboratory ETH Zürich, Haldeneggsteig 4, CH-8092 Zürich, Switzerland
ECPE	ECPE Engineering Center for Power Electronics GmbH Landgrabenstrasse 94, D-90443 Nürnberg, Germany
Enablence	Enablence Switzerland AG (former: Albis Optoelectronics AG) Moosstrasse 2, CH-8803 Rüschlikon, Switzerland
EPFL	Ecole Polytechnique Fédérale de Lausanne EPFL, CH-1015 Lausanne, Switzerland
ETHZ	Eidgenössische Technische Hochschule Zürich (Swiss Federal Institute of Technology Zürich) ETH Zürich, Rämistrasse 101, CH-8092 Zürich, Switzerland
FBK	Fondazione Bruno Kessler Via S. Croce N. 77, I-38100 Torino, Italy
FHNW Windisch	Fachhochschule Nordwestschweiz Klosterzelgstrrasse, CH-5210 Windisch, Switzerland
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Hasler	Hasler Stiftung Hirschgraben 6, CH-3011 Bern, Switzerland
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IBM Research	IBM Research GmbH Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland
idQ	id Quantique S.A. Chemin de la Marbrerie 3, CH-1227 Carouge, Switzerland
IIS-ETHZ	Integrated Systems Laboratory ETH Zürich, Gloriastrasse 35, CH-8092 Zürich, Switzerland (i.e. the publisher of this “Research Review 2008”)
IKT-ETHZ	Institut für Kommunikationstechnik (Laboratory for Communication Technology) ETH Zürich, Sternwartstrasse 7, CH-8092 Zürich, Switzerland
IMEC	Interuniversity Microelectronics Centre Kapeldreef 75, B-3001 Leuven, Belgium
Imperial College London	Imperial College London South Kensington Campus, London SW7 2AZ, United KIngdom
Infineon	Infineon Technologies Austria AG Siemensstrasse 2, A-9500 Villach, Austria

IPEQ-EPFL	Institut de Photonique et Electronique Quantique, Quantum Devices Group, EPFL, CH-1015 Lausanne, Switzerland
IQE-ETHZ	Institut für Quantenelektronik (Laboratory for Quantum Electronics) ETH Zürich, Wolfgang Pauli-Strasse 16 , CH-8093 Zürich, Switzerland
IT'IS	• IT'IS Foundation for Research on Information Technologies in Society ETH Zürich, Gloriastrasse 35, CH-8092 Zürich, Switzerland • Zeughausstrasse 43, CH-8004 Zürich, Switzerland
IT'IS Partners	AGC Automotive, Ypsilanti, USA Antia Therapeutics, Switzerland Asher Sheppard Consulting, Redlands, USA ARCS, Seibersdorf, Austria Aristotle University of Thessaloniki, Thessaloniki, Greece BAG, Bern, Switzerland BASEXPO Consortium, Europe BfS, Salzgitter, Germany BORL-USZ, Zürich, Switzerland Boston Scientific Corporation, USA Campus of Ravenna, University of Bologna, Bologna, Italy Cancer Research UK, Beatson Laboratories, Glasgow, UK Chalmers University, Gothenburg, Sweden Charité, Berlin, Germany CTIA, Washington DC, USA Department Clinical Research and Veterinary Public Health EPFL, Lausanne, Switzerland Erasmus MC Rotterdam, Rotterdam, The Netherlands Exponent Inc., Menlo Park, CA, USA FAU Erlangen, Erlangen, Germany FDA, Washington DC, USA Forschungsgemeinschaft Funk e.V., Bonn, Germany Fraunhofer ITEM, Hannover, Germany GSM-Association, Genève, Switzerland Health Protection Agency, Chilton, London, UK IBT-ETHZ, Zürich, Switzerland IFA = Automatic Control Laboratory, ETHZ, Switzerland IITRI = Illinois Institute of Technology Research Institute, Chicago, USA Imricor Medical Systems, USA IMTEK, Freiburg, Germany Incos Boté Cosmetic GmbH, Mainz, Germany INTEC, Gent, Belgium IPM, Stockholm, Sweden IPT-UNIZH, Zürich, Switzerland ISTB, University of Bern, Bern, Switzerland Karolinska Institute, Huddinge, Sweden Laboratoire IMS, Uni Bordeaux, Bordeaux, France Laboratoire Clarins, Paris, France McGill University, Montreal, Canada MCL, London, UK MIT, Massachusetts Institute of Technology, Cambridge, USA MMF, Brussels, Belgium Motorola, Ft. Lauderdale, USA National Technical University of Athens, Athens, Greece NCCR Co-Me, Zurich, Switzerland NIEHS, Research Triangle Park, USA NIST, Gaithersburg, USA NOKIA NRC, Helsinki, Finland Philips Medical Systems, Best, The Netherlands Phonak Communications AG, Murten, Switzerland SECO, State Secretariat for Economic Affairs, Switzerland Siemens Medical Solutions AG, Erlangen, Germany SPEAG, Schmid & Partner Engineering AG, Zurich, Switzerland Toronto University, Toronto, Canada Tox Uni ZH, Institute for Pharmacology & Toxicology, Zürich, Switzerland ULP, Strasbourg, France Uni Athens, Technical University of Athens, Athens, Greece University of Basel, Basel, Switzerland University of Bern, Bern, Switzerland University of Geneva, Geneva, Switzerland

	University of Gent, Gent, Belgium University of Uppsala, Uppsala, Sweden University of Zürich, Zürich, Switzerland Zejiang University, Hangzhou, China ZMT Zurich Med Tech, Zurich, Switzerland ZonMW, The Hague, The Netherlands
KTI	Kommission für Technologie und Innovation (Commission for Technology and Innovation, a Swiss Government Agency) Effingerstrasse 27, CH-3003 Bern, Switzerland
LSM-EPFL	Microelectronic Systems Laboratory EPFL, CH-1015 Lausanne, Switzerland
MASCOT Consortium	Forschungszentrum Telekommunikation Wien Betriebs-GmbH, Wien, Austria Eidgenössische Technische Hochschule Zürich, ETH, Zürich, Switzerland Fraunhofer Institute for Telecommunications, Germany Fundació Barcelona Media, Universitat Pompeu Fabra, E-08002 Barcelona, Spain Politecnico di Torino, Torino, Italy Nokia Corporation, Finland Technische Universität Wien, Wien, Austria
MIT	Massachusetts Institute of Technology Research Laboratory of Electronics 50 Vassar Street, Cambridge, MA 02139, USA
NANOSIL Consortium	INPG Entreprise S.A., Seyssinet Pariset, France Institut Polytechnique de Grenoble, Grenoble, France The University of Warwick, Coventry, United Kingdom Rheinisch-Westfälische Technische Hochschule Aachen, Aachen, Germany Kungliga Tekniska Hogskolan, Stockholm, Sweden Consorzio Nazionale Interuniversitario per la Nanoelettronica, Bologna, Italy Universite Catholique de Louvain, Louvain-La-Neuve, Belgium Interuniversitair Micro-Electronica Centrum Vzw, Leuven, Belgium Commissariat a l'Energie Atomique, Paris, France ST Microelectronics Crolles, Crolles, France Institut Superieur d'Electronique et du Numérique, Lille, France Université Paris-Sud, Orsay, France Gesellschaft für Angewandte Mikro- Und Optoelektronik mbH, Aachen, Germany Forschungszentrum Jülich GmbH, Jülich, Germany Qimonda Dresden GmbH & Co. OhG, Dresden, Germany Technische Universität Braunschweig, Braunschweig, Germany Universität Stuttgart, Stuttgart, Germany National Centre for Scientific Research Demokritos, Aghia Paraskevi Attikis, Greece University College Cork - National University of Ireland, Cork, Ireland Politechnika Warszawska, Warszawa, Poland Universidad Rovira i Virgili, Tarragona, Spain Chalmers Tekniska Hoegskola Aktiebolag, Göteborg, Sweden Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland Eidgenössische Technische Hochschule Zürich, Zürich, Switzerland Synopsys Switzerland LLC, Zürich, Switzerland The University of Glasgow, Glasgow, United Kingdom University of Liverpool, Liverpool, United Kingdom The University of Newcastle Upon Tyne, Newcastle upon Tyne, United Kingdom
NEC	NEC Corporation System Devices Research Laboratories 1120 Shimokuzawa, Sagamihara, 229-1198, Japan
NTT	NTT Corporation Microsystem Integration Laboratories 3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-0198, Japan
QP-NCCR	The Quantum Photonics National Center of Competence EPFL, CH-1015 Lausanne, Switzerland
Samsung	Samsung Electronics Co., LTD. San 24 Nongseo-Ri, Giheung-Eup, Yongin-City, Gyeonggi-Do, Korea
SNF	Swiss National Science Foundation Wildhainweg 20, CH-3012 Bern, Switzerland
STM	• ST Microelectronics SA 850 Rue Jean Monnet, F-38921 Crolles, France • ST Microelectronics SRL Via Carlo Olivetti 2, I-20041 Agrate Brianza (MI), Italy

Synopsys	• Synopsys Switzerland LLC Thurgauerstrasse 40, CH-8050 Zürich, Switzerland • Synopsys Inc. 700 East Middlefield Road, Mountain View, CA 94043, USA • Synopsys Inc. (former SIGMA-C GmbH) Thomas Dehler-Strasse 9, D-81737 München, Germany
Toshiba	• Toshiba Corporation 1-1. Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan • Toshiba Corporation 2-5-1, Kasama, Sakae-ku, Yokohama 247-8585, Japan • Toshiba Corporation 1, Komukai, Toshibacho, Saiwai-ku, Kawasaki 210, Japan
TU Berlin	Technische Universität Berlin Strasse des 17. Juni 135, D-10623 Berlin, Germany
TU Graz	Technische Universität Graz Institute for Applied Information Processing and Communications (IAIK) Infeldgasse 16a, A-8010 Graz, Austria
Uni Bologna	Università degli Studi di Bologna Dipartimento di Elettronica Informatica e Sistemistica Via Zamboni 33, I-40126 Bologna, Italy
Uni Bordeaux	Université de Bordeaux Laboratoire de l'Intégration du Matériau au Système 351 Cours de la Libération, F-33405 TALENCE CEDEX, France
Uni Cagliari	Università degli Studi di´Cagliari Dipartimento di Ingegneria Elletrica et Elettronica Piazza d' Armi, I-09123 Cagliari, Italy
Uni Kassel	University of Kassel Computational Electronics Institute Wilhelmshoeher Allee 71, D-34121 Kassel, Germany
Uni Linz	Johannes Kepler University Altenberger Str. 69, A-4040 Linz, Austria
Uni Loughborough	Loughborough University Electronic & Electrical Engineering Department Leicestershire, LE11 3TU, United Kingdom
Uni Lund	Lund University, Lund University Box 117, S-221 00 Lund, Sweden
Uni Nottingham	University of Nottingham Department of Electrical and Electronic Engineering University Park, Tower Building, Nottingham, NG7 2RD, United Kingdom
Uni Parma	University of Parma Dipartimento di Ingegneria dell'Informazione Viale G.P. Usberti, I-43100 Parma, Italy
Uni Pisa	Università di Pisa Dipartimento di Ingegneria dell'Informazione Via Caruso 2, I-56122 Pisa, Italy
Uni Purdue	Purdue University West Lafayette, Indiana 47907, USA
Uni Regensburg	Universität Regensburg, Institute for Experimental and Applied Physics D-93040 Regensburg, Germany
Uni Virginia	University of Virginia Computer Science Department 151 Engineer's Way, Charlottesville, VA 22904, USA
VEST	VEST Corporation, Le Manoir, F-14480 Lantheuil, France
Vision-ETHZ	Computer Vision Laboratory ETH Zürich, Sternwartstrasse 7, CH-8092 Zürich, Switzerland
VSEA	Varian Semiconductor Equipment Associates, Inc. 35 Dory Road, Gloucester, MA 01930-2297, USA
Weizmann	Weizmann Institute of Science PO Box 26, Rehovot 76100, Israel
Zurich MedTech	ZMT Zurich MedTech AG Zeughausstrasse 43, CH-8004 Zürich, Switzerland

Awards

Markus Wenk, Peter Lüthi, Thomas Koch, Patrick Mächler, Michael Lerjen, Norbert Felber, Wolfgang Fichtner

received the

“Best Live Demonstration Award”

for their conference demonstration

“Hardware Platform and Implementation of a Real-Time Multi-User MIMO-OFDM Testbed”

at the 2009 IEEE International Symposium on Circuits and Systems (ISCAS), Taipei, Taiwan, May 24-27, 2009.

Haruka Kubo, Mauro Ciappa, Takayuki Masunaga, Wolfgang Fichtner

received the

“Best Paper Award”

for

“Multiscale simulation of aluminum thin films for the design of highly-reliable MEMS devicess”

at the 20th European Symposium on Reliability of Electron Devices Failure Physics and Analysis (ESREF), Arcachon, France, October 5-9, 2009.

Manuel Murbach, Sven Kühn et al.

received the

“Best Student Platform Presentation Award”

for their conference paper

“Evaluation of artifacts by EEG electrodes during RF exposures”

at the BioEM 2009 Meeting, Davos Switzerland, June 15 - 19, 2009.

Marie-Christine Gosslin, Sven Kühn et al.

received the

“Best Student Poster Presentation Award”

for their conference poster

“Correlation of the exposure of mobile phones assessed in SAM by applying standard procedures with the SAR in anatomical human heads”

at the BioEM 2009 Meeting, Davos Switzerland, June 15 - 19, 2009.

Sven Kühn

received the

“Best Student Poster Presentation Award”

for his conference poster

“Assessment of the SAR from hands-free kits for mobile phones”

at the BioEM 2009 Meeting, Davos Switzerland, June 15 - 19, 2009.

News 2009 and History of the Integrated Systems Laboratory (IIS)

News 2009

IC and System Design and Test

The worldwide first implementation of a multiple-input multiple-output (MIMO) 4-stream (4 transmit and 4 receive antennas) iterative soft-input soft-output (SISO) detector in an application-specific integrated circuit (ASIC) has been demonstrated. With 4 iterations, it gives more than 8 dB SNR improvement over state-of-the-art MIMO detectors at 757 Mbps data rate.

Analog and Mixed-Signal Design

A highly power-efficient and linear multi-mode sigma-delta analog-to-digital converter suitable for cellular communications including 4G. The circuit achieves 86 to 70dB of dynamic range over a 0.1 to 20 MHz bandwith.

BioEM and IT'IS Foundation

The newly established subgroup of BioEM and IT'IS Foundation in Computational Life Sciences was selected as research partner by FDA (USA) to investigate the diagnostic options of magneto-hydrodynamic (MHD) for the assessment of heart failure conditions.

Event organized by IT'IS Foundation and the BioEM Group

The IT'IS Foundation and the BioEM Group organized the BioEM2009 Congress with various satellite meetings during June 14 - 19 in Davos with over 400 abstracts and more than 500 participants from around the world.

New equipment

The IT'IS Foundation with participation of the BioEM Group established the first independent laboratory for testing implants for MRI safety based on MITS 1.5, MITS 3.0, MITS Gradient and DASY52NEO.

History

1985 Appointment of Wolfgang Fichtner, Professor for Electronics, Department of Electrical Engineering, ETH Zurich.
Formation of the research group "VLSI" in the Electronics Laboratory.

1986 Foundation of the "Integrated Systems Laboratory" by merging of the research groups of Prof. Wolfgang Fichtner (Department of Electrical Engineering) and Prof. Martin Morf (Department of Computer Science).
Start of the lecture series "VLSI I: Architectures", "VLSI II: Design", and "VLSI III: Test and Fabrication" (graduate EE, CS, and physics students).

1988 Foundation of the Microelectronics Design Center (Department of Information Technology and Electrical Engineering, associated to the Integrated Systems Laboratory).

1990 Start of the lecture "Semiconductor Devices: Physical Principles and Simulation".
Start of the project "Education and Research in Microelectronics", generous funding by the board of ETH Zurich for IC integration and measurement equipment.
Prof. Wolfgang Fichtner elected IEEE Fellow for the "application of numerical modeling to device scaling and submicron transistor optimization".

1993 Appointment of Qiuting Huang, assistant professor for Analog Integrated Circuits, Department of Information Technology and Electrical Engineering, ETH Zurich.
Foundation of the IIS spin-off "ISE Integrated Systems Engineering AG" Zurich by IIS members (scope of business: software and application support in Technology CAD). Location for the first one and a half years at IIS with support of ETH Zurich.
Start of the lecture "Analog Integrated Circuits" (graduate EE students).

1996 Start of the Swiss priority program "MINAST – Micro and Nano System Technology", program director Prof. Wolfgang Fichtner (1996–1997), program direction established at IIS, total 56 Mio CHF granted by Swiss authorities and more than 60 Mio CHF contributions from Swiss industrial enterprises; IIS research projects: two in the module "Integrated Microsystems Technology", four in the module "Design, Simulation and Engineering of Microsystems", and one in the module "Microsystems Applications".

1998 Promotion of Qiuting Huang to Professor for Electronics, Department of Information Technology and Electrical Engineering, ETH Zurich.

1998 Accommodation of the research group "Physical Characterization", including well known experts and advanced equipment from the former Reliability Laboratory at the Department of Information Technology and Electrical Engineering, ETH Zurich.

1999 Accommodation of the research group “Bioelectromagnetics/EMC” from the Electromagnetic Fields and Microwave Electronics Laboratory at the Department of Information Technology and Electrical Engineering, ETH Zurich. Election of Prof. Wolfgang Fichtner as head of the Department of Information Technology and Electrical Engineering (holding this position from Oct 1999 until Sep 2004).Establishment of the “Foundation for Research on Information Technologies in Society IT’IS” (Zurich, director Dr. Niels Kuster). Associated to ETH Zurich and a close research partner of the IIS research group Bio Electromagnetics/EMC.

2000 IEEE Andrew S. Grove Award of the Year 2000 to Prof. Wolfgang Fichtner “for outstanding contributions to semiconductor device simulations”.
Evaluation of the Department of Information Technology and Electrical Engineering, ETH Zurich, by a group of international experts with high scientific reputation. Overall qualification: “The international standing of Integrated Systems Laboratory regarding its core activities is definitely among the best of the world.”

2001 Prof. Qiuting Huang elected IEEE Fellow for outstanding contributions to integrated circuits for wireless communications.
Start of the lectures “Semiconductor Devices” and “Communications Electronics” (undergraduate EE students).

2002 “International Conference on Numerical Simulation of Semiconductor Optoelectronic Devices NUSOD-02”, 25–27 September 2002, organized by IIS at ETH Zurich, 111 participants from Europe, USA, and Japan, 13 invited talks by well known experts from USA and Europe, 19 talks, 10 posters, and 5 company presentations.

2003 ETH Zurich established the assistant professorship Computational Optoelectronics. Dr. Bernd Witzigmann was elected and has taken up this position at the Integrated Systems Laboratory on 1 March 2004.

2004 The Optoelectronics Laboratory (OptoLab) was founded as a common research instrument between IIS-ETHZ, IfE-ETHZ and IFH-ETHZ to support scientific work in fundamental and applied research projects with industrial partners.
Spin-off ISE AG was acquired by Synopsys, Inc. and became Synopsys Switzerland LLC. It is a Swiss based subsidiary and the headquarter of Synopsys TCAD activities. It is partner in ISE’s and in future European and national research projects.
Start of the lecture series “Advanced Optoelectronics” (graduate EE students).
“15th European Symposium Reliability of Electron Devices, Failure Physics and Analysis (ESREF) 2004”, 4-8 October 2004, organized by IIS at ETH Zurich, 234 participants from Europe, USA, and Far East, 7 invited talks by well known experts from Europe, Far East, and USA, 52 talks, 40 posters, and an exhibition with 16 companies.

2006 The National Institute of Health NIH (USA) has granted a research contract worth USD 5.6 Million in a single source procedure to the IT’IS Foundation and the BioEM group. This grant is part of the largest single experiment of NIH and includes several endpoints relevant for the health risk assessment of mobile communication systems.

2007 Appointment of Professor Qiuting Huang as Cheung Kong Seminar Professor by the Chinese Ministry of Education.

2008 Leave of Assistant Professor Bernd Witzigmann. Since November 2008, Prof. Witzigmann is full professor and head of the Computational Electronics and Photonics Laboratory at the Electrical Engineering and Computer Science Department of the University of Kassel in Germany. Prof. Witzigmann supports PhD students in computational optoelectronics at Integrated Systems Laboratory until conclusion of the doctorate.
A research team in computational electron beam physics was established. Scientific topics concern sub-nanometer measurement of critical dimensions for wafer and mask-level scanning electron microscopy (SEM) of the 32 nanometer node and beyond as well as modeling and correction of the enhanced proximity effects occurring in high-resolution direct writing of wafers by electron beam lithography at low beam energies.

Research Projects

IC and System Design and Test

Coordinator:

Norbert Felber

Multi-User Real-Time MIMO-OFDM Testbed Demonstration

Personnel: Markus Wenk, Patrick Mächler, Peter Lüthi, Thomas Koch

Funding: EU-IST-26905 MASCOT

Partners: IKT-ETHZ, MASCOT Consortium

References: [D12]

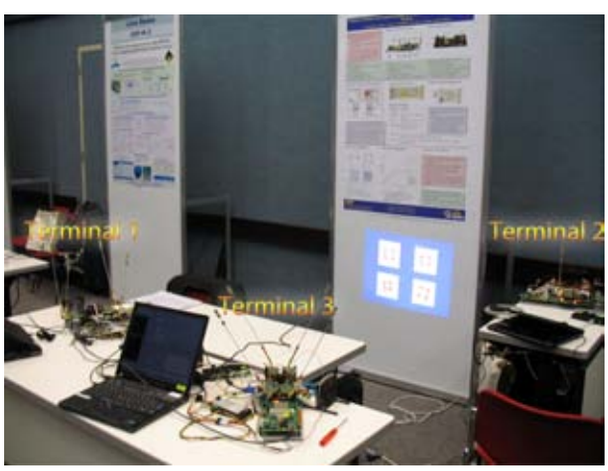
The multi-user real-time MIMO-OFDM testbed has been demonstrated at several occasions. It visualizes MIMO-OFDM communication in terms of throughput, link reliability and live display of real-world constellation diagrams. The setup consists of two or more MIMO-OFDM terminals whereof one acts as access point and the others as clients. Several demonstration scenarios exist:

A real-time movie demonstration has been set-up to stream a video from one terminal to the other. Frame errors appear as artifacts in the received video.

The difference of various MIMO detection algorithms can be experienced by changing the active MIMO detection algorithm. It can be chosen from linear detection successive interference cancellation (SIC), conditioned ordered successive interference cancellation (COSIC), hard-output sphere decoding (SD), and soft-output minimum mean squared error (MMSE) detection. The differences are visualized by the actual frame error rate (FER).

A real-time simultaneous multi-user uplink demonstration set-up is also available. To this end, several users are transmitting simultaneously to the same base station. Currently, a common clock source for all users is required.

All demonstration scenarios are supported by specific user interfaces realized in Matlab. They also allow to change the modulation scheme, the number of transmit or receive antennas, the frame length and other communication parameters.



Demonstration setup at the live demonstration session of ISCAS 2009. The real-time constellation diagram is projected onto the closer board.

From Linear Detection to Sphere Decoding: Algorithms for the ETH MIMO-OFDM Testbed

Personnel: Hannes Friederich (student); Markus Wenk, Peter Lüthi, Christoph Studer

Funding: EU-IST-26905 MASCOT

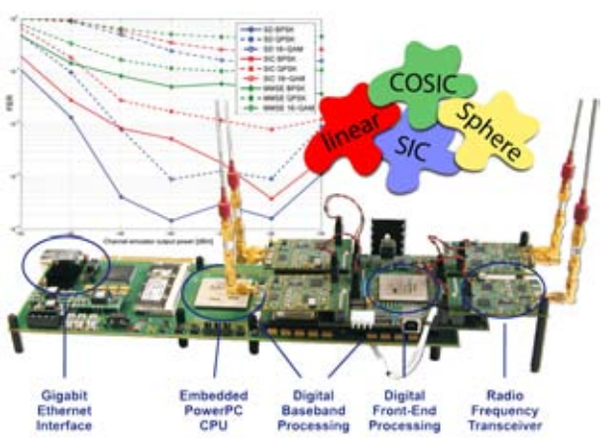
Partners: IKT-ETHZ, MASCOT Consortium

Different data detection algorithms for multiple-input multiple output (MIMO) communication exist. They differ in terms of error-rate performance, implementation complexity, and run-time. In this project, linear detection, successive interference cancellation (SIC), conditioned ordered successive interference cancellation (COSIC), and hard output sphere decoding (SD) were implemented on the ETH MIMO-OFDM testbed. Furthermore, first measurements and demonstrations using these algorithms were carried out.

Particular care has been taken to the implementation of the SD algorithm. To reduce implementation complexity, a new low-complexity enumeration strategy has been developed. Furthermore, interleaved pipelining has been applied to increase hardware efficiency. The resulting SD implementation significantly outperforms previous implementations in terms of circuit area and throughput.

To integrate the implemented detection algorithms into the existing MIMO-OFDM testbed, system-level considerations were carried out. To keep latency low, two detection cores operate in parallel. A scheduling algorithm is responsible for balancing the variable run-time of SD and feeds the cores with the received data.

Both measurements over-the-air and through a channel emulator proofed that the implemented algorithms work. However, the performance figures were not as good as expected. Transmit impairments could be localized which deteriorate the performance of SD. These findings triggered new research activities.



Linear, SIC, COSIC and sphere decoding were implemented on the testbed. The frame error rate (FER) performance measured over the channel emulator is shown on the background figure.

Iterative MIMO Decoding: Algorithms and VLSI Implementation Aspects

Personnel: Christoph Studer

Funding: ETHZ

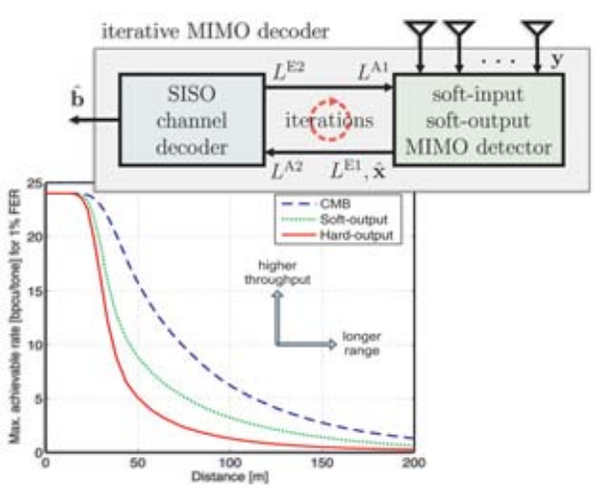
Partners: IKT-ETHZ

References: [D9]

The key requirements of modern wireless communication systems are throughput, coverage and range. Multiple-input multiple-output (MIMO) wireless technology in combination with iterative MIMO detection and channel decoding (known as iterative MIMO decoding) is one of the most promising methods to improve these requirements, without sacrificing spectral efficiency or transmit power.

This dissertation focused on the design and optimization of algorithms for iterative MIMO decoding and presents corresponding VLSI implementations. The main contributions of this work are the development and implementation of novel low-complexity and high-performance soft-input soft-output (SISO) detection algorithms for MIMO systems. The developed algorithms base on minimum mean-square error (MMSE) parallel interference cancellation (PIC), and on single tree-search sphere decoding (SD). In addition, implementation results for SISO decoding of convolutional, low-density parity check (LDPC), and turbo codes are presented.

The algorithms and circuits provided in this work give reference for the performance and silicon complexity associated with iterative MIMO decoding. Finally, it is shown that iterative MIMO decoding can be implemented in practical systems and enables significant performance gains in terms of signal-to-noise ratio; this gain translates to higher throughput, better coverage, and longer range compared to state-of-the-art (hard-output and soft-output) MIMO detection schemes.



Top: Illustration of iterative MIMO decoding. Bottom: With the number of iterations, starting from hard-output or soft-output MIMO decoding error rates, iterative MIMO decoding approaches the theoretical performance bound (CMB).

Soft-Input Soft-Output MIMO Detection using Parallel Interference Cancellation

Personnel: Christoph Studer, Schekeb Fateh, IKT-ETHZ : Dominik Seethaler

Funding: ETHZ

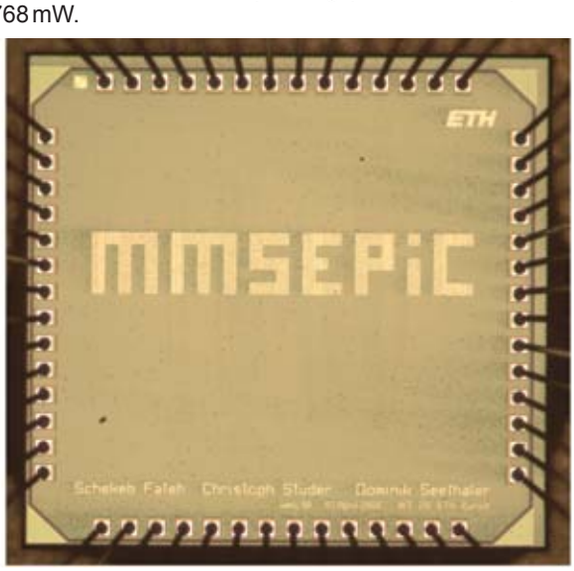
Partners: IKT-ETHZ

Iterative soft-input soft-output (SISO) detection and channel decoding is the key to achieve near-ideal capacity in multiple-input multiple-output (MIMO) wireless communication systems. In this project, we develop the first VLSI implementation reported in the literature of a 4-stream SISO detection algorithm for iterative MIMO decoding.

To this end, a reduced-complexity minimum mean-square error (MMSE) parallel interference cancellation (PIC) algorithm has been developed. The main complexity of the resulting algorithm is required by one matrix inversion per received vector. Efficient matrix inversion is achieved by performing an LU-decomposition followed by forward- and back-substitution procedures.

We developed a systolic network of dedicated processing units (PUs), which processes six receive vectors concurrently and in a pipelined manner. Each PU performs the assigned tasks in 18 cycles. Matrix inversion requires division operations, which are performed in custom units that meet the throughput and precision constraints.

The ASIC was fabricated in 90 nm CMOS technology. The implemented SISO MMSE PIC decoder, which covers 1.5 mm^2 core area, performs 4-stream SISO detection with more than 8 dB SNR improvement over state-of-the-art MIMO detector implementations, when performing four iterations. The detector achieves a maximum clock frequency of 568 MHz, leading to 757 Mb/s throughput per iteration. The corresponding power consumption is 768 mW.



Chip photo of the SISO MMSE PIC detector. The 90 nm CMOS ASIC performs SISO detection for iterative MIMO systems. The die size is 1.9 mm by 1.9 mm, from which only 1.5 mm^2 are used by the detector.

High-Throughput Low-Power Turbo Decoding for 3GPP-LTE

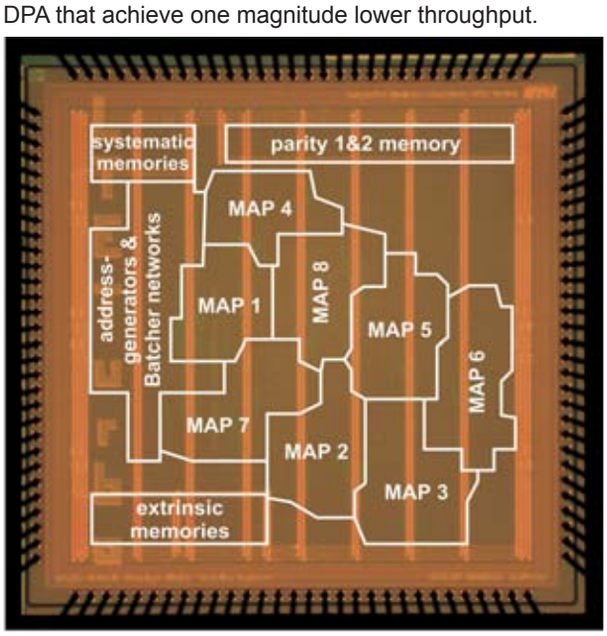
Personnel: Sandro Belfanti (student);
Christoph Studer, Christian Benkeser

Funding: ETHZ

Recent popularity of smart phones, netbooks, and other mobile broadband devices has vindicated 3G (HSDPA) as an enabling technology for main-stream high-speed data and has given fresh impetus to its 4G successor LTE (long-term evolution). LTE achieves up to 326.4 Mb/s throughput, which leads to more than 20 times higher complexity for turbo decoding (compared to HSDPA).

In this project, a low-power turbo decoder implementation for LTE, which is able to achieve the LTE peak throughput, has been developed. To this end, we designed a high-performance contention-free interleaver architecture, which contains two Batcher sorting networks to perform 8-fold parallel interleaving, i.e., the architecture enables interleaved memory access to eight log-likelihood ratio (LLR) values per clock cycle. By instantiating eight parallel radix-4 maximum a-posteriori (MAP) decoder cores, the LTE peak throughput could be achieved.

Measurement results of the fabricated chip show that the 130 nm CMOS ASIC achieves a maximum clock frequency of 302 MHz, ultimately leading to peak throughput of 390.6 Mb/s at 5.5 iterations. The theoretical LTE maximum throughput can therefore be achieved with margin. At more realistic 100 Mb/s throughout, the measured power consumption is only 68.6 mW, which is comparable to that of state-of-the-art low-power turbo decoders for HSDPA that achieve one magnitude lower throughput.



ASIC micrograph of the 3GPP-LTE turbo decoder. The main components of the decoder are indicated. They use a core area of 3.57 mm^2.

Compressed Sensing for Sparse Channel Estimation

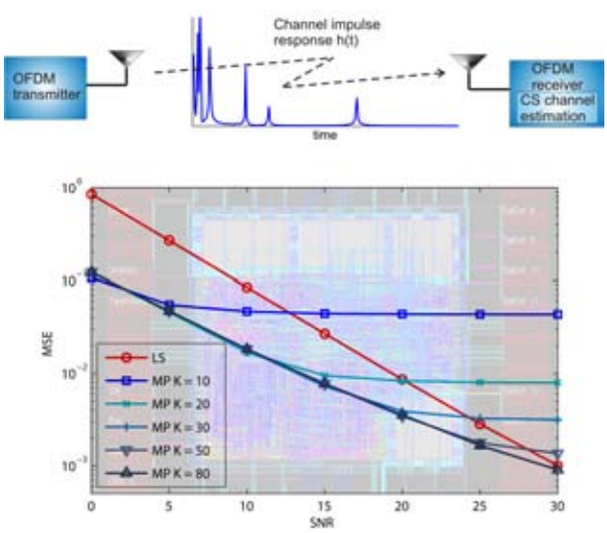
Personnel: Patrick Mächler, Pierre Greisen

Funding: ETHZ

Broadband wireless channels often show sparse characteristics in time domain, which means that their channel impulse response consists of few peaks and is otherwise almost zero. The reason is that the individual propagation paths of the transmitted signal are typically small in number and clustered. The emerging research field of compressed sensing (CS) offers a framework which can exploit sparsity in signals. CS allows to achieve better signal reconstruction from fewer measurements, even below Nyquist rate. A large number of algorithms have been developed lately to reconstruct the original signal out of fewer measurements. All the reconstruction algorithms have high computational requirements which makes them hard to use in real-time applications.

The goal of this work is to asses the complexity of CS algorithms for the application of channel estimation in long-term evolution (LTE) mobile communication systems. LTE can use large bandwidths with up to 2048 OFDM subchannels.

The first algorithm implemented is the matching pursuit algorithm, which is especially suitable for implementation on an ASIC since it can efficiently be parallelized and has low complexity. The reconstruction complexity depends on the sparsity of the signal, i.e. the number of non-zero elements. Thus, the lowest possible sparsity of a signal was used to determine the computational complexity of its reconstruction and finally the chip area of its VLSI implementation.



Top: OFDM system transmitting over a sparse channel. Bottom: Plot showing the mean-squared error of the matching pursuit algorithm with maximal K iterations, compared to least-squares estimation (over chip layout).

Dictionary-based Program Code Compression for Fixed-VLIW-Format Processors

Personnel: Stefan Eberli

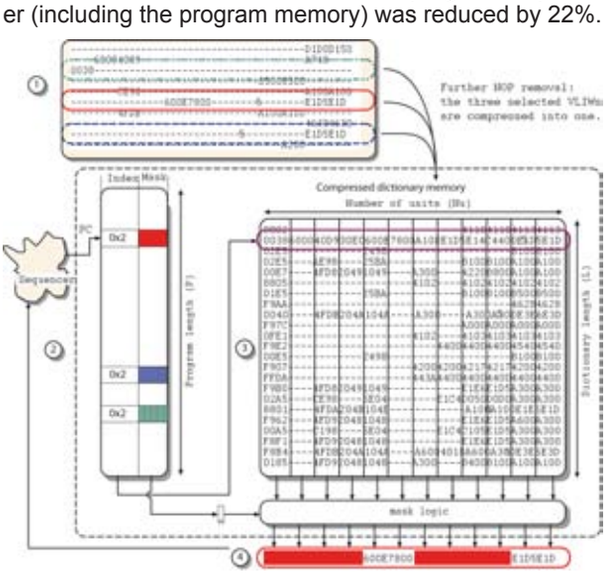
Funding: EHZ, KTI-8537 NMPP MIMO2, BridgeCo

Partners: BridgeCo

Very-long-instruction-word (VLIW) processors can exploit the instruction-level parallelism inherent to data processing algorithms by operating the function units allocated inside their datapath concurrently. Unfortunately, the implemented application often does not require to run all available units concurrently, and therefore the program code contains many no-operations (NOPs) for the unemployed units. This means that the code density is low, especially for processors that store the entire VLIW in one program memory word (i.e., fixed-instruction-format VLIW processors). Moreover, the application may require one VLIW to be repeated several times inside the program memory, resulting in large programs.

In this project, dictionary-based program code compression (DBCC) is implemented to alleviate for this inefficiency. DBCC schemes collect at compile-time all unique instructions of a program into a dictionary memory. Then, at run-time, the dictionary entries are indexed through a much narrower, but deeper memory, which eventually allows to reconstruct the original program flow. Motivated by the observation that the dictionary memory still contains a significant number of NOP CWs in this project, the dictionary memory is further compressed.

This enhanced DBCC algorithm was applied to the ASPE VLIW processor developed at IIS-ETHZ. It achieves average compression ratios close to 30% of the initial program size. In addition, the silicon area of the program sequencer (including the program memory) was reduced by 22%.



Enhanced DBCC method: An algorithm starts from the uncompressed memory (1), and extracts the index and bitmasks memory (2), and the compressed dictionary (3). The original VLIW is reconstructed by the aid of the bitmask (4).

Quantum Cryptography based Point-to-Point Secure Data Communication System

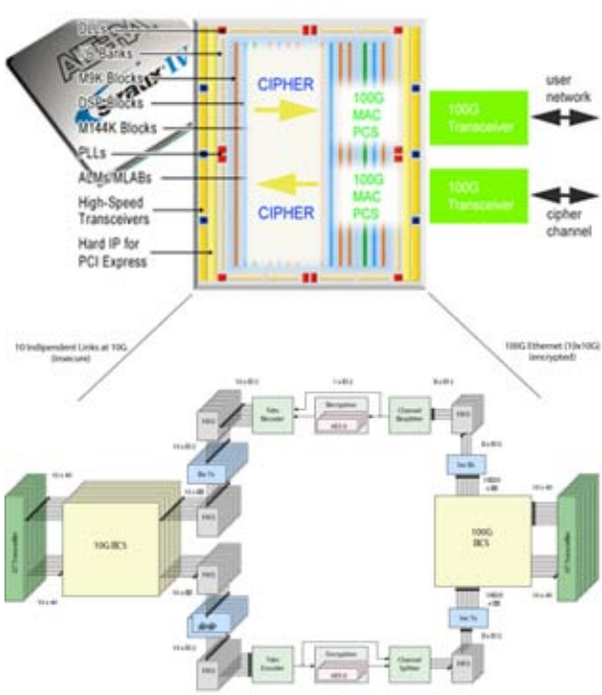
Personnel: Luca Henzen

Funding: KTI-9821.1 NMPP ESCRYPT2, idQ

Partners: idQ

The forthcoming Ethernet standard for high-speed network communication IEEE 802.3ba will support frame transmission at 40 and 100 Gigabits per second (Gbps). The goal of this project is, in collaboration with the network-security company idQuantique, to develop a high-speed Ethernet encryptor. Three main security features should be provided by the system:

- Highly secure cipher key exchange based on Quantum Key Distribution (QKD).
- Secure payload encryption at 40 and 100 Gbps with the Advanced Encryption Standard, a worldwide accepted block cipher.
- Secure authentication: A received message must be guaranteed to stem from the right sender. While so far, this authentication is mostly done on a high communication layer by the application or the user, authentication by the encryption system itself drastically increases the speed of the computation process. However, the algorithmic effort of authentication becomes extremely high for 40 and 100 Gbps rates. Modern FPGA chips supporting multiple 10 Gbps transceivers are thus used.



Top: Channel configuration of an FPGA chip in order to support bidirectional 100Gbps encryption.
Bottom: Block diagram of the 100Gbps Ethernet encryptor.

FPGA Implementation of High-Dimensional Cube Testers on the Stream Cipher Grain-128

Personnel: Luca Henzen;
FHNW Windisch: Jean-Philippe Amasson, Willi Meier
Weizmann: Itai Dinur, Adi Shamir

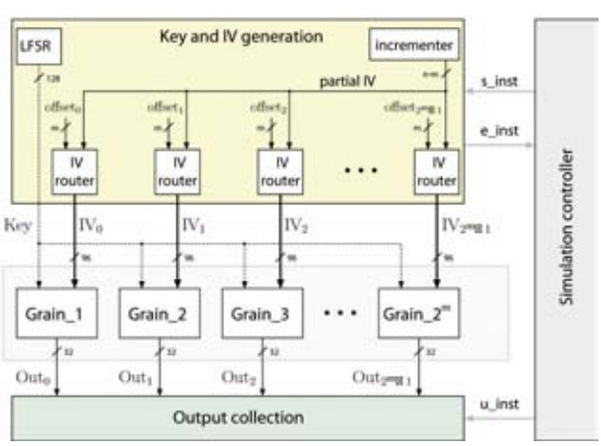
Funding: ETHZ

Partners: FHNW Windisch, Weizmann

References: [D8]

The stream cipher Grain-128 was proposed by Hell, Johansson, Maximov, and Meier. It is a variant of Grain-v1 and accepts keys up to 128 bits, instead of up to 80 bits. Grain-v1 has been selected in the eSTREAM portfolio of promising stream ciphers for hardware, and Grain-128 was expected to retain the merits of Grain-v1. In this project, its cryptographic security was investigated.

Cube testers are a generic class of cryptographic methods used to attack stream ciphers and hash functions in order to uncover security weaknesses. They are based on cube attacks and on algebraic property-testers. In this project, we developed an efficient FPGA implementation of cube testers and used it to attack Grain-128. Our best result (attack on Grain-128, reduced to 237 rounds out of 256) was achieved after a computation involving 254 iterations of Grain-128, with a 256×32 parallelization. An extrapolation of our results with standard methods suggests the possibility of an attack on the full Grain-128 in time 283, which is well below the complexity 2128 of exhaustive search. We also developed a specific method, based on an evolutionary algorithm, for finding good cubes. For instance, running a 30-dimensional cube tester on Grain-128 takes 10 seconds with our FPGA machine, compared to about 45 minutes with a bit-sliced C implementation, and more than a day with a straightforward C implementation in state-of-the-art PCs.



Architecture of the cube module implemented in a Xilinx Virtex-5 FPGA. The system clock frequency has been set to 200 MHz.

Research Projects

Signal Processing Circuits and Systems

Coordinator:

Andreas Burg

Transmit Noise in MIMO Communications under Real-World Conditions

Personnel: Markus Wenk

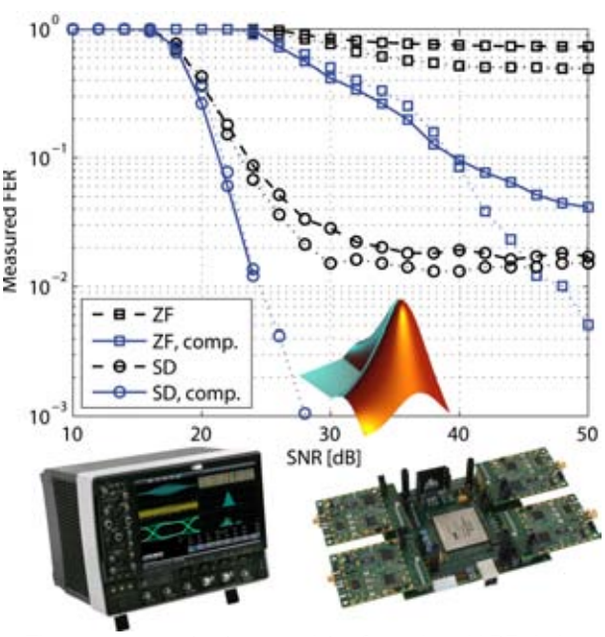
Funding: IIS, EU-IST-26905 MASCOT

Partners: IKT-ETHZ, MASCOT Consortium

For simulations of multiple-input multiple-output (MIMO) systems, usually only noise in the receive path is considered. However, recent simulations that also include impairments in the transmit path showed a significant performance degradation in error-rate performance. This observation was confirmed by measurements on the testbed platform.

The characterization of the transmit impairments was carried out by stimulating the testbed RF chain with MIMO-OFDM frames from the FPGA and recording the output of the RF chain on a high-end oscilloscope. Afterwards, the recorded data is loaded into Matlab and the error vector magnitude (EVM) is computed. An analysis of the EVM revealed that the impairments in the transmitter can be modeled as independent and identical distributed (i.i.d.) Gaussian noise.

With the same measurement setup, the impact of transmit noise on different MIMO detection algorithms was measured. It confirmed the simulation results in that the error-rate performance of certain MIMO detection algorithms (e.g., sphere decoding) heavily suffers under transmit noise. Furthermore, it was shown that the impact of transmit noise can be reduced by noise whitening. To this end, a noise whitening filter is computed and applied to the received signal.



The measurement set-up consists of a real-world RF chain, a high-end oscilloscope, and Matlab. The measured and simulated (dotted lines) error-rate performance is shown without and with compensation (noise whitening).

Implementation of Noise Whitening for MIMO Wireless Communication

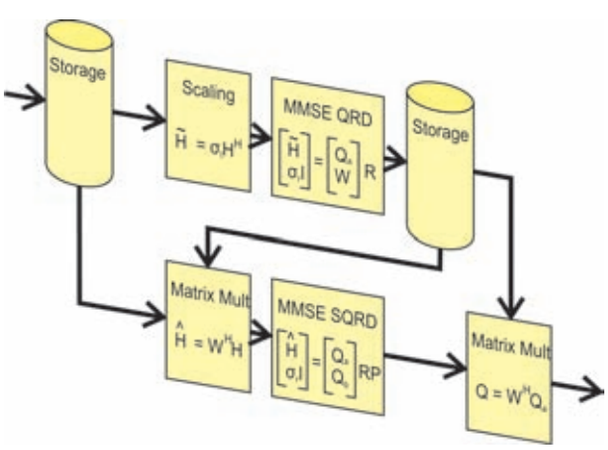
Personnel: Christian Senning, Christoph Studer

Funding: Hasler

Physical transceiver (Tx) radio-frequency (RF) implementations for multiple-input multiple-output (MIMO) wireless communication systems suffer from residual impairments that are located at the transmitter. These residual distortions result in colored noise at the receiver, which severely degrades the performance of (near-)optimal MIMO detection algorithms, such as the soft-output single tree search (STS) sphere decoder (SD), for example.

In order to mitigate this performance loss, an efficient algorithm that whitens the colored noise in the receiver has been implemented. The algorithm is based on a suitably modified regularized QR-decomposition of the channel matrix, which is performed prior to the QR-decomposition required for the detection algorithm. Since noise whitening is performed in the preprocessing unit, symbol rate processing (e.g., MIMO detection) is not affected, which ultimately leads to low implementation complexity.

Both QR-decompositions have been implemented using systolic arrays, that provide a sustained throughput of 20 million QR-decompositions per second for 4x4-dimensional channel matrices. In addition, memories based on FIFOs are required for storage and to provide the corresponding matrices to the associated systolic arrays. In summary, noise whitening roughly increases the silicon complexity of the preprocessing unit by a factor of two, i.e., from 200 kGE for an implementation without noise whitening to about 500 kGE. The maximum clock frequency of the resulting chip in 130 nm CMOS technology (in fabrication) is 320 MHz.



Schematic of the noise-whitening implementation for mitigation of residual transmit-RF impairments. The implementation requires 500 kGE and operates at 320 MHz.

Simulation and Emulation of MIMO Wireless Transceivers

Personnel: Pierre Greisen, Simon Haene

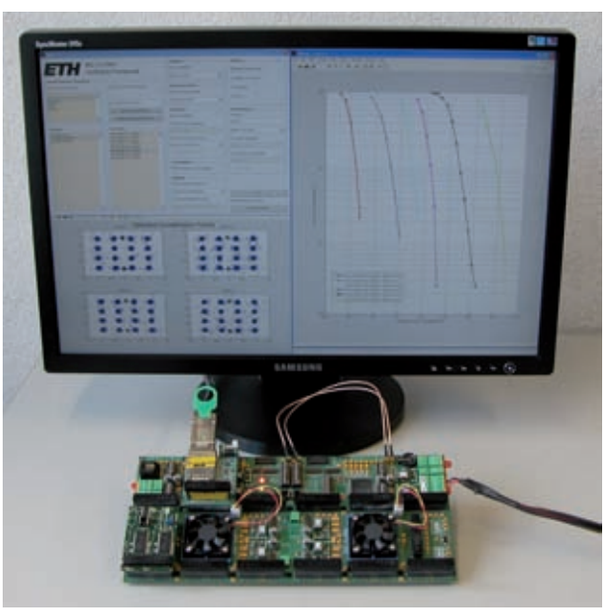
Funding: FESS SNF PP002-11057/1

References: EURASIP Feb 2010

Beside the actual designing process of digital circuits, such as wireless communication transceivers, the simulation and verification procedure remains a time-intensive and challenging task. Growing complexity of designs and standard-conformity requirements amplify this effect even more.

In this work, a complete design, verification, and performance characterization methodology that is tailored to the needs of the development of the baseband part of state-of-the-art wireless transceivers, for both research and industrial products, was developed. Contrary to research testbeds following a proof-of-concept approach, the design flow from this work focuses on the different steps, from system specifications to a final ASIC implementation. One main contribution is the integration of different design representations into one consistent framework: possible design representations are floating-point and software fixed-point models, as well as an RTL model targeted for different platforms (HDL simulation, FPGA emulation, and ASIC implementation).

This framework has been successfully employed for the development and verification of an industrial-grade, fully standard-compliant, 4-stream IEEE 802.11n MIMO-OFDM transceiver.



Picture of the FPGA emulation environment, together with the software environment (Screen: GUI, real-time constellation plots, and bit-error-rate curves).

Performance Assessment of an MMSE-based 802.11n Transceiver

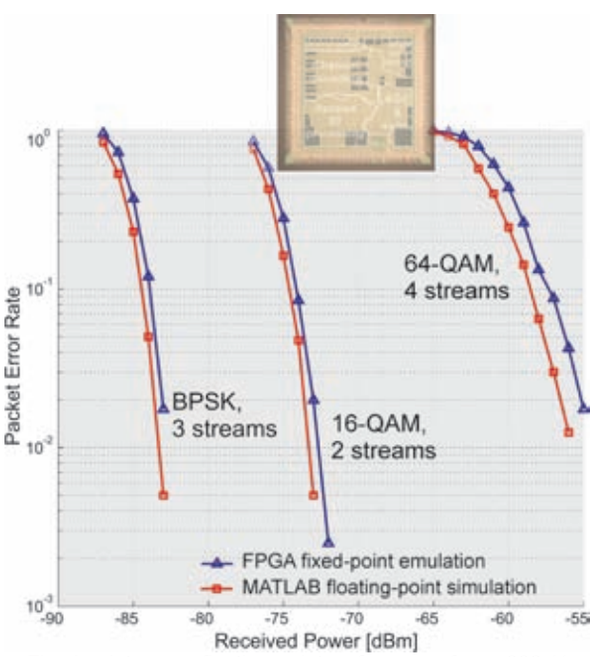
Personnel: Pierre Greisen, Christian Senning

Funding: FESS SNF PP002-11057/1

The quality of a communication circuit is determined by its final performance compared to an ideal reference. The gap between obtained performance and reference performance defines the implementation loss, which is largely due to the impact of using a fixed-point arithmetic instead of floating-point precision.

This project aimed at fine-tuning an existing IEEE 802.11n transceiver with a soft-output MMSE MIMO detector, using an FPGA emulation platform. The goal was to get good accordance between floating-point and fixed-point performance. One example for optimization is the scaling of the output of the MMSE detector: initial floating-point to fixed-point performance comparison revealed a substantial gap for certain modes. With a consistent parameter setting a significant improvement was achieved.

The figure below shows the outcome for three characteristic 802.11n modulation and coding schemes (MCS): BPSK (3 streams), 16-QAM (2 streams), and 64-QAM (4 streams) with physical layer throughput of 40.5 Mbps, 162 Mbps, and 432 Mbps, respectively. A TGn-type-D channel model has been used together with 40 MHz transmission bandwidth. The gap between fixed-point and floating-point is below 1 dB SNR for all mandatory 802.11n modes.



Fixed-point versus floating-point performance for an 802.11n physical layer transceiver. The floating-point curves are obtained through MATLAB simulations, the fixed-point curves are obtained through FPGA emulation runs.

Single-Tree-Search Sphere Decoder for MIMO

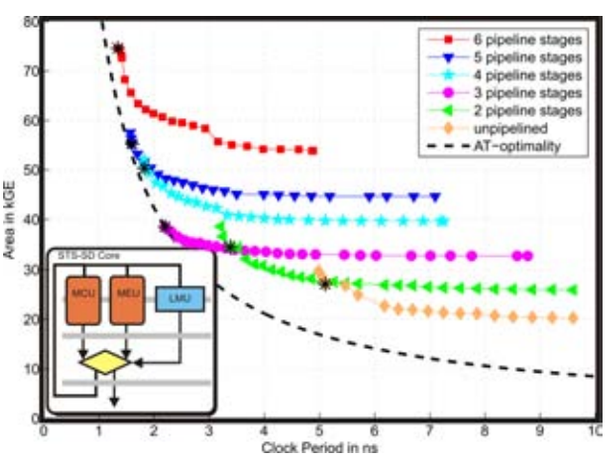
Personnel: Lukas Bruderer, Markus Wenk

Funding: FESS SNF PP002-11057/1

Soft-output detection in multiple-input multiple-output (MIMO) wireless systems based on sphere decoding (SD) yields superior error-rate performance compared to that of linear soft-output MIMO detection. SD-based MIMO detection is key to enable the high-throughput modes of modern wireless communication standards. In particular, soft-output MIMO detection based on single-tree-search (STS) SD was shown to achieve near-optimal error-rate performance at low computational complexity and enables the peak throughput of 600 Mbit/s in IEEE 802.11n.

In this project, the STS-SD algorithm has been optimized for soft-output detection in the IEEE 802.11n physical layer (PHY). In view of integration of this STS-SD design into a PHY, sustaining a high throughput was the main design goal. To this end, a novel symbol-enumeration scheme was implemented. This scheme allows to shorten the critical path and also lowers the number of iterations required to decode a symbol. Additionally, the efficiency of the STS-SD design was increased by selecting an optimal number of pipeline stages and optimizing the architecture for the different transmission schemes of the IEEE 802.11n standard.

The STS-SD core, mapped onto a 130 nm process, operates at a maximum clock frequency of 400 MHz and occupies a total area of around 85 kGE. Compared to previous realizations, this implementation is highly efficient in terms of throughput and area, and enables the use of the high-throughput modes of the IEEE 802.11n standard.



Impact of various number of pipeline stages on the area-time efficiency for the SD with the novel enumeration scheme in a 130 nm CMOS process. Bottom left: high-level block diagram of the implemented STS-SD algorithm.

Low-Power VLSI Implementation of a Reconfigurable LDPC Decoder

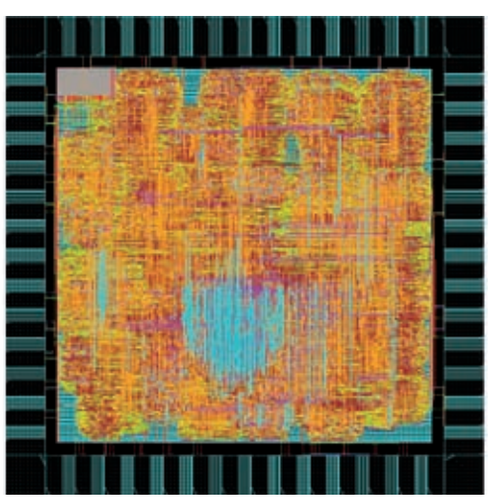
Personnel: Christoph Roth (student);
Pascal Meinerzhagen, Christoph Studer

Funding: FESS SNF PP002-11057/1

The high throughput and quality-of-service requirements of today's wireless communication systems require high-performance error-correction schemes. Low-density parity-check (LDPC) codes are widely used due to excellent error-correction capabilities. Especially, quasi-cyclic (QC) LDPC codes offer high decoding throughput at relatively low implementation complexity. Mobile applications ask for low-power VLSI implementations of LDPC decoders which do still achieve the high throughputs.

In this project, various low-power strategies ranging from the arithmetic level down to the gate level have been applied to an existing LDPC decoder design: Introduction of an adapted layered offset min-sum (L-OMS) decoding algorithm, replacement of SRAM macrocells by latch arrays, change of number representation format from two's complement to sign-magnitude, and memory bypassing. The initial power consumption and the power consumption after each optimization step have been determined by means of an automated power flow, considering both nominal supply voltage and scaled supply voltages.

With respect to the original design, the total power consumption could be reduced by nearly 72 %. The high achievable throughput of approximately 1.5 Gbit/s allows to extensively use voltage scaling while still fulfilling the throughput requirements. The design supports all QC-LDPC standards, the code blocks and matrix prototypes fit which fit into the allocated memories. The decoder has been implemented in 90 nm CMOS technology.



Physical-layout view of the low-power QC-LDPC decoder VLSI implementation in 90-nm CMOS technology. The chip is in fabrication.

Systematic Sign-Magnitude Implementation

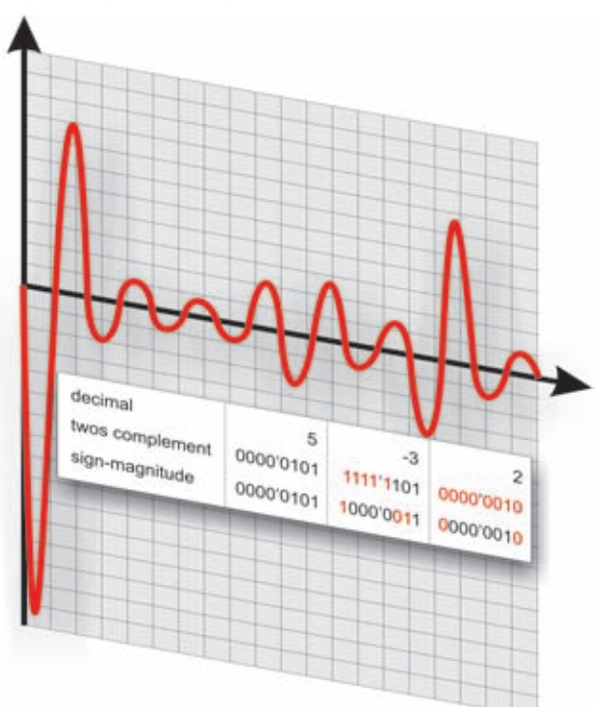
Personnel: Christian Senning

Funding: Hasler

Power consumption has become an important issue for ASIC implementations. Reduction of the dynamic power consumption can be achieved by system-level optimization, architectural changes, arithmetic improvements, and by applying newer CMOS technologies.

Depending on the signal characteristics, the number format has a tremendous impact on the power efficiency of a digital circuit. For zero-mean signed signals with a potentially high dynamic range, where the amplitude only temporally utilizes all available bits, changing the number format from standard two's complement to sign-magnitude may result in an enormous reduction of the dynamic power consumption. Typical signals with this characteristic are recorded voice audio streams.

In this project, a library providing sign-magnitude arithmetic which is bit-true for Matlab and VHDL has been implemented. The library provides real-valued and complex-valued arithmetic operations, such as multiplication or shifting. It as well adds conversion functions from two's complement to sign-magnitude format and vice versa in order to enable mixing of both number format in the same circuit. The word width can generically be adjusted to the required dynamic range and precision.



Example of switching bits for two's complement and sign-magitude signal representations.

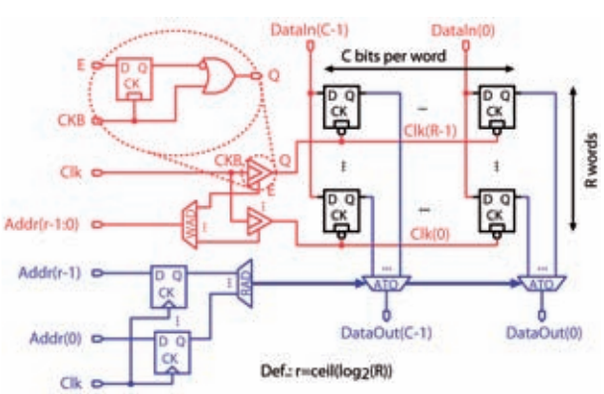
Low-Power Area-Efficient Standard-Cell-based Memory Architectures

Personnel: Pascal Meinerzhagen

Funding: FESS SNF PP002-11057/1

Virtually any CMOS chip manufactured nowadays includes some form of memory. The major options for on-chip memory implementations are: (1) registers built from flip-flops or latches, and (2) SRAM macrocells. SRAM macrocells are compatible with standard CMOS circuits. For most technologies, SRAM macrocell generators are available. For reasonably small storage capacities, flip-flop/latch arrays might be an interesting alternative to SRAM macrocells in order to improve area and energy efficiency, amongst others.

In this project, investigations on several state-of-the art CMOS technologies have been conducted, which show that, compared to SRAM macrocells, flip-flop/latch arrays can bring various benefits, such as ease of portability and modifications at design time, ability to merge storage with logic, potentially less routing, no need of separate voltage supply rings, and more flexibility for fine-granular memory organizations. The write logic of flip-flop/latch arrays, which use basic flip-flops or latches as storage cells in conjunction with clock gates, leads to smaller area and lower power consumption than a solution with flip-flops or latches with enable. The read logic of multiplexer-based implementations leads to smaller area than tri-state-buffer-based implementations. Latch arrays are only slightly smaller than flip-flop arrays. Flip-flop arrays, however, are more convenient for high-speed applications. For applications requiring a memory capacity <1 kbit, replacing SRAM macrocells by latch arrays can be profitable for both area and power.



Schematic view of a latch array with clock gates for the write logic and multiplexers for the read logic.

Embedded Many-Bit-per-Cell Gain-Cell-based DRAM Design

Personnel: Onur Andiç (student);
Pascal Meinerzhagen

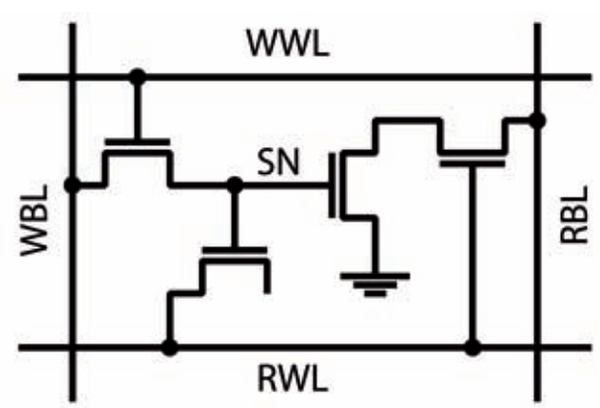
Funding: FESS SNF PP002-11057/1

The major options for on-chip memory integration are dynamic random access memory (DRAM) and static random access memory (SRAM) macrocells. DRAM typically uses special technology options to build high-density stacked or trench capacitors and is therefore not logic compatible. SRAM is compatible with standard logic CMOS technologies, but has, with a minimum of 6 transistors per cell, a relatively large cell size.

In gain cells, charge is stored on the gate of a transistor, whose transconductance gain is used to yield a high sensing current. This leads to a fast and non-destructive read-out operation. Furthermore, gain-cell-based DRAM can be logic-compatible and smaller than SRAM. Various gain-cell-based DRAMs have been proposed to date.

In order to trade data retention time for storage density, many bits can be stored in a single dynamic cell. This approach requires digital-to-analog and analog-to-digital converters for the write and read operations, respectively. Various multilevel DRAMs using a conventional 1T-1C storage cell have been proposed to date.

In this project, the multilevel approach is applied to gain cells. To sense different levels, the drain current of the storage transistor is modulated by means of its gate voltage. If desired, the stored voltage level can be boosted during the read-out operation to ease the design of sensing circuits. Different leakage reduction techniques will be applied to maintain reasonable data retention times even at advanced technology nodes.



4-transistor gain cell suited for multilevel operation. By activating the write word line (WWL), different voltage levels can be transmitted from the write bit line (WBL) to the storage node (SN).

LDPC Decoder for Gigabit Ethernet in 90 nm CMOS

Personnel: LSM-EPFL: Alessandro Cevrero;
Andreas Burg

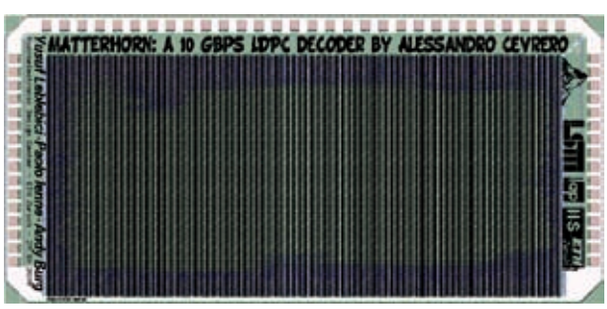
Funding: FESS SNF PP002-11057/1

Partners: LSM-EPFL

Low density parity check (LDPC) codes are very powerful forward-error-correcting codes that enable digital communication systems to operate extremely close to the Shannon Limit. The basic idea of these codes and a possible approach for the decoding was discovered as early as in the 1960s by Gallager. Unfortunately, at that time, the decoding process was considered to be too complex for implementation, and the codes received only very little attention. With the advent of very large scale integration, LDPC codes were rediscovered in the 1990s, and the parallel nature of the message passing algorithms used for decoding turned out to be well suited for deep-submicron integration of decoders for high-speed applications.

In this work, we consider the problem of realizing LDPC decoders for optical networking appliances with a throughput above 10 Gbps. In this first project, an LDPC decoder for 10 Gbps Ethernet was realized in a 90 nm process together with the Microelectronic Systems Laboratory of the EPFL. The various challenges in this project relate to the selection of the decoding algorithm, to the choice of the fixed-point implementation parameters, the design of the register-transfer-level implementation, and especially to the physical implementation. The main problem driving most of the design decisions was the fact that the usual parallel LDPC implementations would occupy a prohibitive active silicon area and would suffer from a very poor area utilization due to the significant amount of routing that is required to connect thousands of mostly identical building blocks.

This challenge was met by employing a layered decoding strategy, combined with an innovative interconnect architecture that reduces the amount of wiring significantly to enable an area utilization above 90% for the final design and to provide a throughput above 10 Gbps.



Layout of the 10 Gbps LDPC decoder sent for fabrication in a 90 nm technology. The area of the overall ASIC is 1.8 mm x 3.6 mm. More than 36 pins are reserved for providing the power supply for an expected power consumption of 2.5 W.

Research Projects

Analog and Mixed-Signal IC Design

Coordinator:

Qiuting Huang

Linearity Correction Techniques for High-Speed Folding and Interpolating A/D Converters

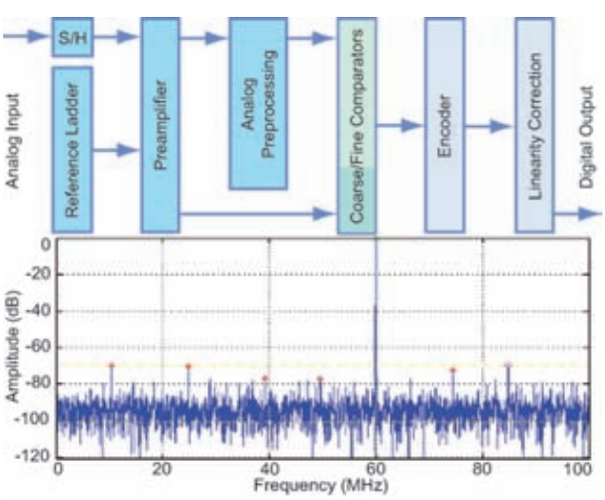
Personnel: Schekeb Fateh

References: [A3]

The demand for high-speed and high-resolution analog-to-digital converters (ADCs) has increased in recent years since ADC specifications are largely determined by communication systems, and these integrated system-on-chips (SoCs) require high throughput and a resolution above 10 bits.

Flash architectures achieve high conversion rates due to their parallel signal processing. However, the disadvantage of these converters is that the power consumption, input capacitance, and production costs grow exponentially with their resolution. To overcome these short-comings, analog preprocessing is used, consisting of folding and interpolating circuits, which reduce the number of comparators and the input capacitance. These techniques are combined to create a folding and interpolating high-speed ADC with limited power consumption.

Poor matching properties of CMOS technology degrade the linearity of the pre- and folding amplifier and thus decrease the resolution of the ADC. This project aims to increase the effective number of bits (ENOBs) at the output of the ADC by applying linearity correction techniques in the digital domain. In order to find an efficient correction circuit, different algorithms are analyzed to achieve a speed-accuracy tradeoff.



Top: Architecture of the folding and interpolating A/D converter. Bottom: Dynamic performance of ADC after linearity correction at 200 MHz sampling frequency for a 60 MHz sinusoidal signal.

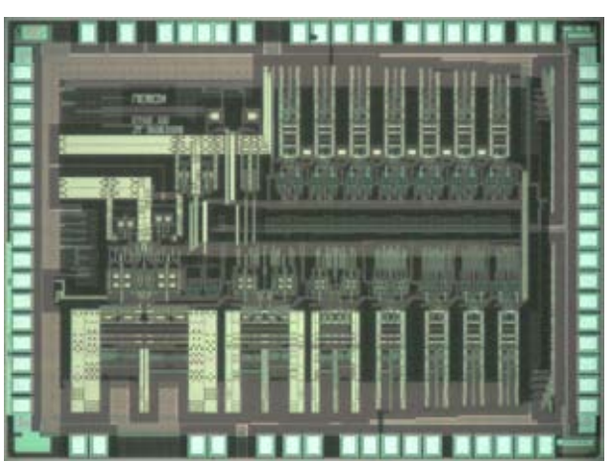
High-Speed Pipelined A/D Converters in Deep-Submicron CMOS Technology

Personnel: Jürg Treichler

The demand for high data rates and high resolutions remains the driving force behind the development of analog-to-digital converters (ADCs). While oversampling ADCs offer high resolutions at moderate bandwidths and flash converters are used to achieve very high conversion speeds, successive approximation register (SAR) converters allow within limits for a continuous trade-off between resolution and bandwidth. Pipelined ADCs have the potential for large bandwidths at considerable resolutions with sampling rates up to several hundreds of megasamples per second (MS/s), and thus offer an adequate solution especially for wireline communication systems.

The ongoing reduction of minimum feature sizes of CMOS processes presents new challenges to the design of converters. While the feasibility of low-resistance switches allows for higher settling speeds in switched capacitor applications, increasing leakage currents severely impact the achievable resolution. Wiring parasitics also begin to play an important role.

Contrary to the observed trend in many recent publications on pipelined ADCs with low supply voltages, the implemented chip aims at a high resolution. This is made difficult by signal-to-noise ratio degradation, caused by the reduced signal swing. Measurements confirm that the resolution of the realized ADC is well above 11.1 bits (effective) for sampling rates up to 50 MS/s, and exceeds 11.6 ENOB at lower signal frequencies at a supply voltage of 1.2 V.



Photomicrograph of the Nemox ADC chip, fabricated in a 1-P 6-M 0.13 µm CMOS process with MiM capacitors.
The front stage is located in the bottom left corner, while several reference voltage buffers occupy the upper left.

A/D Conversion for Multi-Standard Wireless Receivers

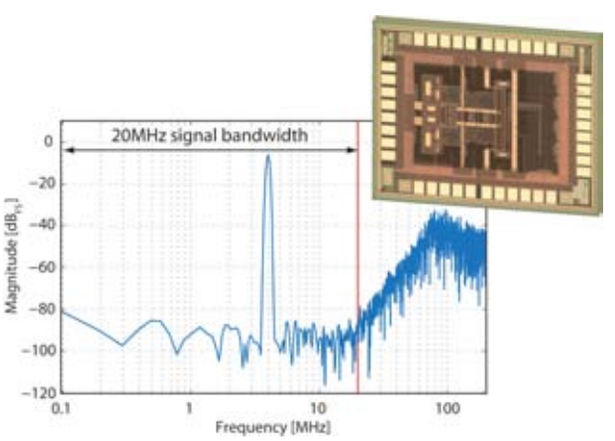
Personnel: Thomas Christen

References: [A4]

As data-centric application proliferate in both cellular and local area networks, higher data-rate expectations continue to precipitate newer wireless standards, while popular incumbent standards must be retained. From the user's point of view, the current trends call for designs that allow convergence of wireless services, allowing access to different standards from the same wireless device and cost effective solutions for intercontinental roaming. For space and cost reasons, hardware has to be shared as much as possible in this devices.

Reconfigurability of wireless radios, or software defined radio (SDR), has therefore become a focus of recent research. Analog hardware is generally seen as an impediment to adaptability and its reduction a desirable outcome in the quest for SDR, especially as scaling of CMOS down to 100 nm and below increasingly favors digital design over analog. High-performance ADCs are therefore an enabling component in the design of multi-standard radios.

In this research project, a reconfigurable tri-level/multi-bit multi-mode $\Delta\Sigma$ modulator has been implemented in 0.13 μm CMOS. The implemented $\Delta\Sigma$ modulator covers signal bandwidths up to 20 MHz making it suitable for cellular applications including 4G radio systems, also known as IMT-Advanced, which support scalable RF bandwidths up to 40 MHz. With a maximum sampling rate of 400 MHz, the modulator achieves a DR between 86 dB and 70 dB for signal bandwidths between 100 kHz and 20 MHz, respectively, at a scalable power consumption between 2 mW and 34 mW from a 1.2 V supply.



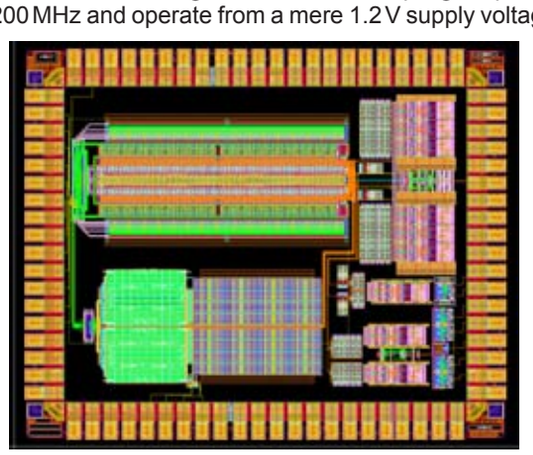
Chip photo of implemented multi-mode $\Delta\Sigma$ modulator together with measurement of output spectrum in LTE-Advanced mode (20 MHz signal bandwidth).

High-Resolution Digital-to-Analog Conversion using a Hybrid Architecture

Personnel: Craig Keogh

As well as being important in its own right, the digital-to-analog converter (DAC) is an increasingly used building-block in modern electronic systems ranging from advanced communication devices to high-performance analog-to-digital converters. The design of such DACs in a standard sub-micron CMOS technology using a low-supply voltage remains a challenging task. The majority of DAC architectures in deployment today are predominantly one of two types: current-steering or switched-capacitor. The current steering architecture consists of an array of current sources that are switched to the output node. Due to the inherently fast speed at which these currents can be switched, this topology is favourable in high-speed applications such as modern communication systems. Switched-capacitor DAC topologies rely on charge redistribution and are realised using a network of switches and capacitors. Although they cannot reach the high-speeds attained by current-steering designs, they have the advantage of delivering good linearity and accuracy. Hence they find widespread use in sampled-data systems requiring a DAC such as $\Sigma\Delta$-modulators, pipeline and successive approximation ADC architectures.

This research project has culminated in the development of a high-resolution hybrid DAC. The DAC targets a resolution of 15 bits by merging a calibrated 6 bit switched-capacitor MSB sub-DAC with a 9 bit current-steering LSB array. The reference current for the LSB array is generated on-chip using dedicated circuitry in conjunction with one of the MSBs from the switched-capacitor sub-DAC. A general-purpose 0.13 μm CMOS technology featuring MIM capacitor option is used in the implementation of the chip. The DAC is designed to run at a sampling frequency of 200 MHz and operate from a mere 1.2 V supply voltage.



Snapshot taken from the EDA tool showing the complete layout of the 15 bit hybrid DAC. The entire chip (including pads) occupies an area of approximately 4 mm^2.

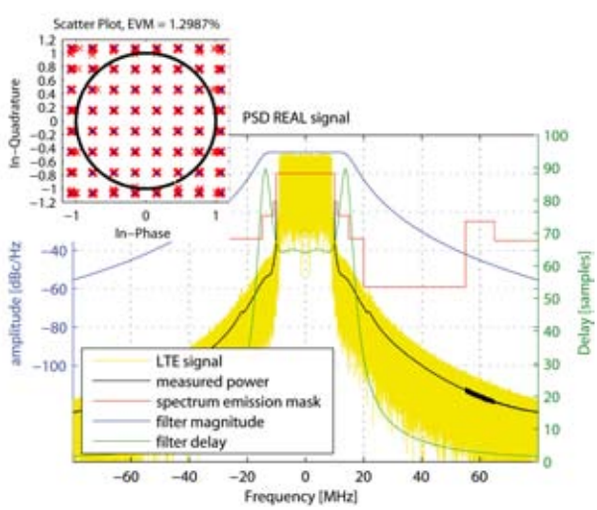
Multi Band Transmitter Design for LTE Mobile Communications

Personnel: Dario Albino Carnelli

In the information era we are living communication has become one important aspect of everyday life. The need of enhanced communication experience led to the technology evolution of mobile communication systems. With the introduction of multimedia services and mobile internet connection there has been a shift from voice- to data-oriented systems.

Although the last generation of standards (3G) for mobile communication provides high data rates, the data rate demand is expected to increase significantly in the next few years, therefore a new standard called Long Term Evolution (LTE) is currently specified for introduction in the coming years. Advantages of this new standard are the increased spectral efficiency due to the use of a new modulation scheme, OFDM-based for transmission, combined with flexible bandwidth and high order modulation.

The RF transmitters play an important role in this scenario since their performances strongly impact coverage, battery life and maximum transmission rate. Goal of this project is the design of an LTE-compliant Direct Conversion Transmitter (DCT) architecture, in a 130 nm technology, with a closer look to critical aspects which will restrain the DCT performance characteristics in a 4G system framework.



Simulated Tx LTE signal spectrum with baseband filter response.
Top left: 64 QAM constellation (red) with Zadoff-Chu sequence (black).

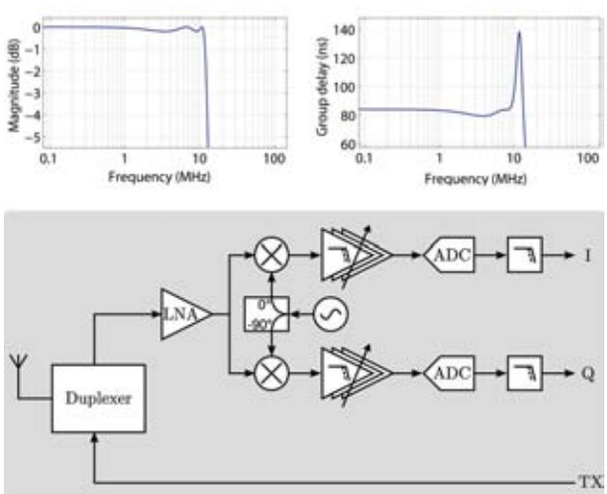
Multi Band Receiver Design for LTE Mobile Communications

Personnel: René Blattmann

Wireless mobile communication data rates have been continuously increased with third generation networks like UMTS and its upgrade HSPA. But the growing number of mobile internet users and new applications such as video streaming and Web 2.0 still ask for even higher data rates. To meet these requirements, the 3rd Generation Partnership Project (3GPP) has developed the 3G Long Term Evolution (LTE) as a new standard.

LTE introduces Orthogonal Frequency Division Multiplexing (OFDM) to increase the spectral efficiency. Flexible bandwidth allocation, modulation schemes up to 64 QAM and MIMO operation allow meeting the required data rates. Nevertheless, increasing the signal bandwidth and the modulation order introduces new challenges for the radio receiver circuit. Tight EVM specifications force the analog receiver front-end to have high linearity and good noise performance. Since LTE supports 6 different signal bandwidths, the baseband signal processing circuit has to be programmable. Additionally, LTE operates in new bands with higher carrier frequencies to enable large channel bandwidths.

The aim of this project is to investigate the challenges a modern mobile radio receiver faces and to find solutions for the analog receiver front-end to cope with the increasing demand for higher data rates while keeping the power consumption low. An integrated LTE receiver front-end circuit will be designed and implemented in standard CMOS technology.



Top: 5th-order Chebyshev baseband filter characteristic: magnitude response (left) and group delay (right).
Bottom: Schematic of the direct conversion receiver.

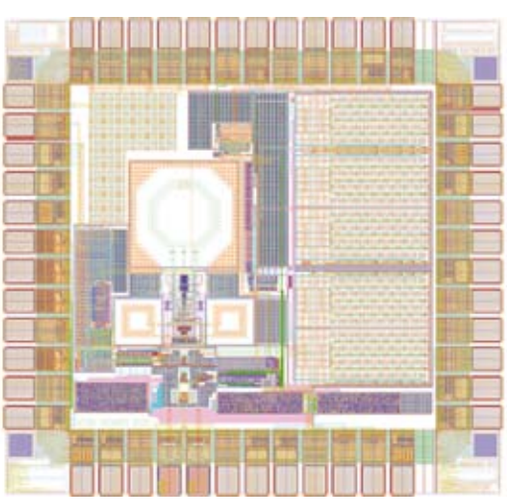
RF Frequency Synthesizer for Wireless Communications

Personnel: Yangjian Chen

Frequency synthesizers serve as vital building blocks in modern wireless communication systems. As local oscillators in conventional RF transceivers, they directly define key performances such as Error Vector Magnitude (EVM) and Adjacent Channel Leakage Ratio (ACLR). In novel polar transmitters, frequency synthesizers literally become the transmitters/modulators as phase modulations happen completely within the loop.

With the introduction of 4G standards like Long Term Evolution (LTE) , maturing 3G standards like WCDMA, and 2G standards (GSM) still holding a large market share, a single frequency synthesizer is required to support all the standards and frequency bands, which puts stringent requirements on almost every aspect of its performances.

This project involves the design, implementation and fabrication of a high performance low-power fractional-N frequency synthesizer. This synthesizer employs sigma-delta modulation to curb the quantization noise in the output spectrum. A Voltage Controlled Oscillator (VCO) using noise filtering technique ensures low-phase noise to meet the stringent GSM requirement. It is capable of support the current (GSM, UMTS etc.) and future wireless standards (WiMAX, LTE etc.). This frequency synthesizer is implemented in a 1-poly, 6-metal CMOS 0.13 um technology.



Layout view of the implemented multi-mode fractional-N frequency synthesizer.

RF CMOS Receiver for Evolved EDGE

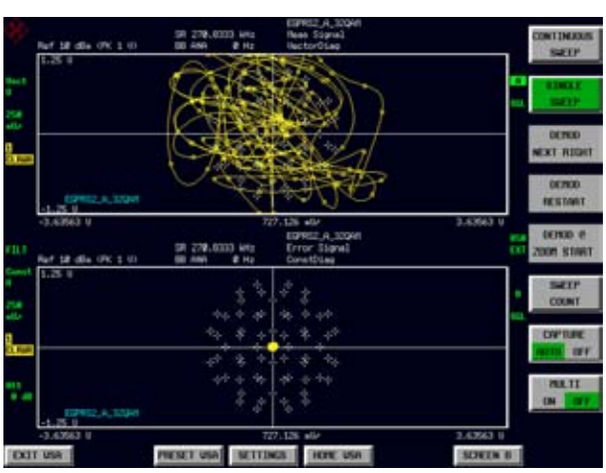
Personnel: Thomas Dellsperger

References: ISSCC 2010

Mobile broadband devices like smart phones, netbooks, and cellular modems have been the only growth sector during the global recession in the past two years. Key enabler for those high-end devices are the high data rates provided by 3G standards, particularly by HSDPA. A good user experience, however, crucially depends on service continuity when 3G networks are absent. Even in western Europe, where 3G networks have been deployed relatively early, 3G coverage is still very patchy. In many cases, travelling from one city into another will result in a loss of 3G connectivity along the way. GSM / EDGE is used as a fallback technology in such cases. While EDGE provides a respectable substitute where HSDPA is absent, an enhanced EDGE is deemed desirable to lessen the data rate disparity between upcoming 3.75G / 4G technologies and the fallback technology. Evolved EDGE (E-EDGE) is an extension of GSM / EDGE that aims to quintuple the peak data rate of EDGE to 1.2 Mbps, thereby serving as a respectable fallback technology for HSDPA+ and beyond.

E-EDGE is phasing in a set of additional technical features that ultimately will include higher modulation order up to 32QAM, higher symbol rate, downlink dual carrier, mobile station receive diversity, and latency reductions in higher protocol layers.

The goal of this project was to design and implement an E-EDGE receiver supporting all of the features mentioned above.



EVM measurement at the receiver output of an E-EDGE 32QAM signal. The upper part shows the measured signal trajectory. The lower part depicts the measured error vectors, displayed in proportion to the 32QAM constellation.

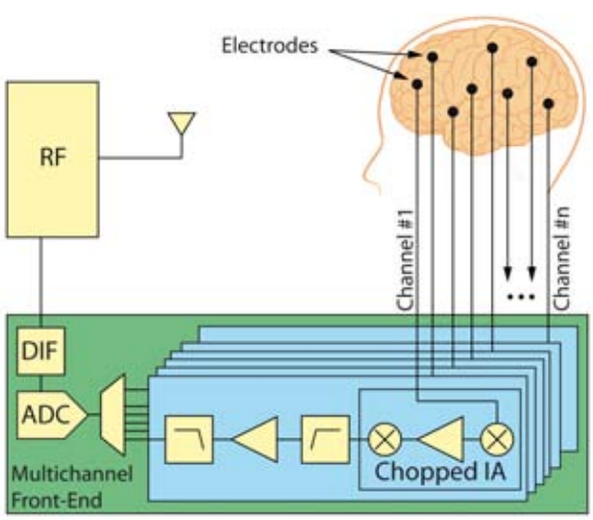
Multichannel Front-End for Biomedical Applications

Personnel: Roger Ulrich, Thomas Burger

Recording data for epilepsy or sleep monitoring as well as non-clinical applications like Brain to Computer Interface (BCI) requires analog multichannel readout front-ends, which amplify and digitize very small signals with low bandwidth.

The signal level for Electroencephalography (EEG) is typically around 100 μV_{PP} within 100 Hz bandwidth, while the number of channels can be up to 128 or even more for clinical research. At this small signal level, any interferer like 50/60 Hz supply tone or differential electrode offset (DEO) could potentially be larger than the measured signal. Those effects and many more like the unknown electrode high impedance up to two Mega ohm for dry skin-electrode contacts demand for an Instrumentation Amplifier (IA) with high CMRR, high input impedance and low noise. The latter one is more challenging to achieve due to the low frequency noise in CMOS technology known as flicker and popcorn noise. Chopper stabilization is a proven technique to mitigate the low frequency noise contribution in a preamplifier for biomedical application and has therefore been applied to the design. Moreover, the DEO limits the preamplifier gain and has to be removed by a high pass filter at a very early stage. After further amplification and low pass filtering, the signal is sufficient conditioned for multiplexing and digitizing.

The aim of this project is to develop a multichannel front-end for biomedical applications in 130 nm CMOS technology with primary focus on EEG measurements for BCI.



Simplified diagram for EEG measurement: Multichannel Front-End is highlighted.

An Equalizer-Based Digital Baseband Receiver for Evolved EDGE

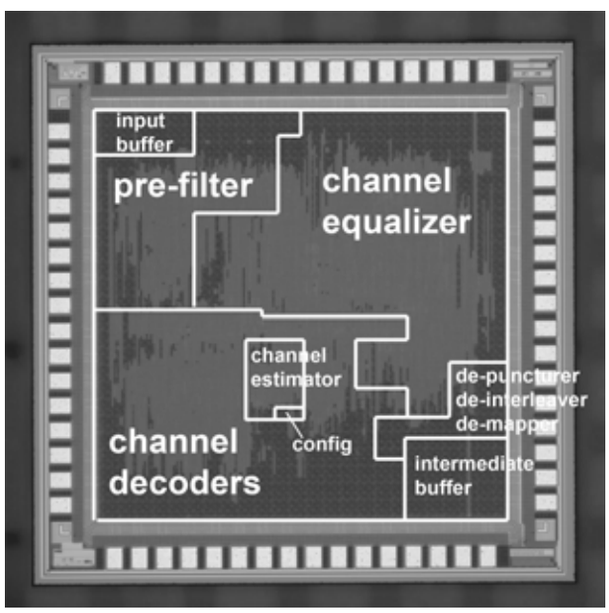
Personnel: Christian Benkeser

References: ISSCC 2010

EDGE Evolution as the latest TDMA based communication standard offers a simple solution to increase the spectral efficiency of GSM mobile communication systems. This standard offers sufficient performance for most mobile applications and the benefit of reusing the existing hardware for mobile operators. This can be interesting for rural areas and developing countries, where large cell areas and low infrastructure costs are demanded by the communication services companies.

Evolved EDGE introduces several new technical features which require new sophisticated solutions, as e.g. transmission modes with higher modulation orders. These exacerbate the channel equalization and demodulation of the received signals.

In this project the digital baseband for Evolved EDGE has been explored with a focus on channel equalization. The most promising algorithms have been used for the realization of a receiver ASIC which supports 4 modulation types and 23 different coding schemes, as required for GSM, GPRS, EDGE and Evolved EDGE. With a measured power consumption of less than 5 mW in all modes, this prototype shows that Evolved EDGE can be realized at preserving the low-power attribute of 2G/GSM devices.



Photograph of the implemented digital baseband receiver ASIC. The different functional blocks are marked to show the relative silicon area requirements. The chip has been implemented in 0.13 µm CMOS with a die size of 2 mm^2.

Research Projects

Technology CAD

Coordinators:

Wolfgang Fichtner
Andreas Schenk
Dölf Aemmer

Boundary Conditions for Quantum Transport

Personnel: Martin Frey

Funding: EU-IST-216171-NANOSIL

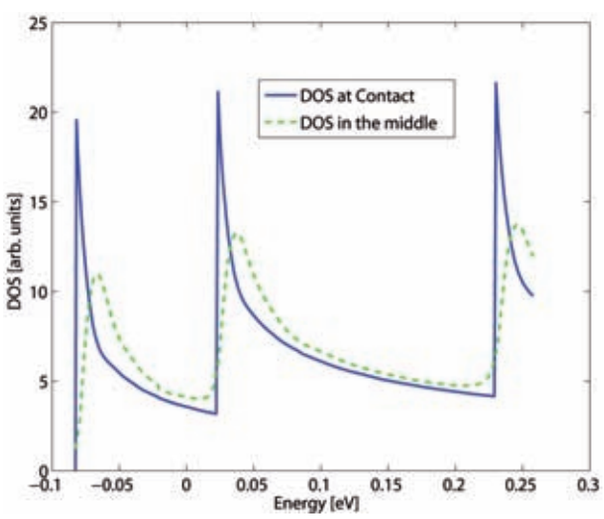
References: [T5]

The non-equilibrium Green's function (NEGF) formalism provides an elegant framework for coherent and incoherent quantum transport device simulations.

With shrinking device length, the effect of the contacts on the device becomes increasingly important. When the device length is of the same magnitude as the coherence length of the carriers, contacts should be considered as reservoirs of incoherent carriers, if scattering is considered in the device.

The influence of coherent and incoherent boundary conditions for quantum transport through silicon nanowires including electron-phonon scattering was studied, using a new iteration scheme to compute an approximate self-energy in the contact. This is done by approximating the retarded Green's functions in the contact with the help of analytical expressions, i.e. the Green's function for an infinite and a semi-infinite system. These two expressions are used in a self-consistent iteration to compute the scattering self-energy in the contacts. With this procedure, an educated guess for the self-energy and the density of states in the contact is gained.

Using the appropriate boundary conditions, the artificial band bending arising from a mismatch of the density of states at the interface between the contact and the device is removed. This results in an increased convergence speed for triple gate silicon nanowires and allows the investigation of transport parameters in simple devices such as one-dimensional resistors.



In a homogeneously doped equilibrium system, the mismatch of the density of state (DOS) arising from unsuitable boundary conditions results in a non-homogeneous density and potential.

Nonparabolicity and Phonon Scattering

Personnel: Martin Frey, Aniello Esposito

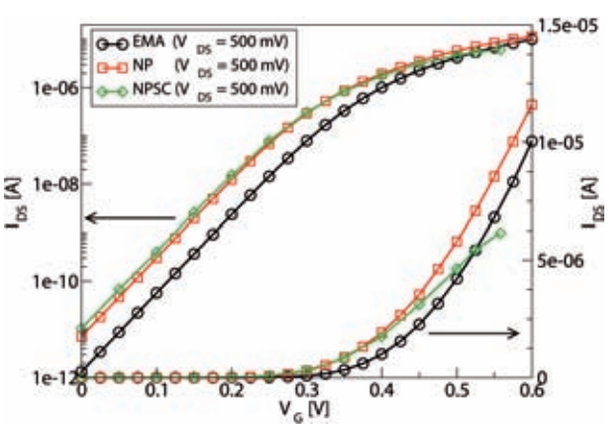
Funding: EU-IST-216171-NANOSIL

References: [T3]

Simulation approaches to predict the behavior of CMOS devices usually consist of an iterative solution scheme, where the Schrödinger and the Poisson equation are solved in a self-consistent way. In the simplest form, the Schrödinger problem is formulated in the effective mass approximation (EMA), which is intended for problems whose external perturbations are smooth compared to the lattice constant of the considered material. Thus, for devices involving confinements down to the nanometer length scale, the EMA becomes questionable.

A remedy is provided by nonparabolicity, which has the same computational advantages as the EMA, but incorporates a large part of the band structure effects as far as the currents are concerned. The parameters for NP are obtained from a comparison with data from a tight binding band structure.

The separate and combined effects of nonparabolicity and phonon scattering have been studied for triple gate silicon nanowires. The observed shift in the threshold voltage was identified as a band structure effect. The ON-current, on the other hand, is mainly determined by scattering. The remaining influence of nonparabolicity on the ON-current strongly depends on the kinetic energy of the carriers in the drain extension, which is a function of the source-to-drain voltage. The higher the source-to-drain voltage, the higher is the kinetic energy of the carriers in the drain and, therefore, the influence of nonparabolicity on the ON-current.



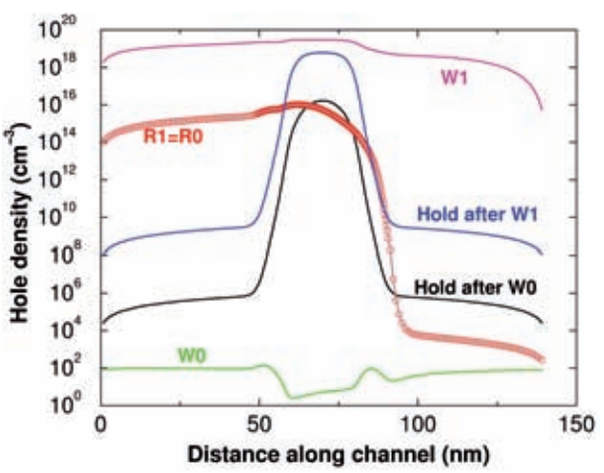
The current of a triple gate silicon nanowire FET with a gate length of 15 nm. Nonparabolicity (NP) results in a threshold shift, while phonon scattering (SC) reduces the ON-current.

Scalability Study of Floating Body Memory Cells

Personnel: Andreas Schenk

Funding: ETHZ

A TCAD study on the scalability of impact-ionization based floating-body memory cells to fully depleted short-channel devices was performed. Only the energy-balance transport model allows for transient simulations of realistic voltage wave forms. To attain qualified predictions, impact ionization rates were calibrated by full-band Monte Carlo simulations. Inclusion of band-to-band tunneling is crucial, although junction profiles were optimized for minimal gate-induced drain leakage. In partially-depleted FETs, two operation modi exist: the steady-state avalanche mode which makes use of the soft breakdown of the body-drain junction, and the bipolar mode where the collector current of the parasitic bipolar decays in time due to the loss of stored holes in the base. It was found that in fully-depleted ultra-thin body FETs the common kink effect is absent. Although a large amount of excess holes can be created during WRITE1 (W1) and hold relatively steady in the body, this charge is always lost when switching to READ1 (R1). At sub-threshold gate voltages, the R1 current becomes self-determined by band-to-band tunneling, which also fixes the READ0 (R0) current to the same value. Above threshold, stored holes are either swept out to the source or their electrostatic impact is negligible compared to the injected charge from the source. No wave form could be found that results in a R1/R0 > 1 programming window in the case of fully-depleted ultra-thin body FETs.



Hole excess density profiles along the channel of the fully-depleted ultra-thin body FET at a depth of 0.5 nm from the interface. The R1 and R0 states are equal as consequence of the predominance of band-to-band tunneling.

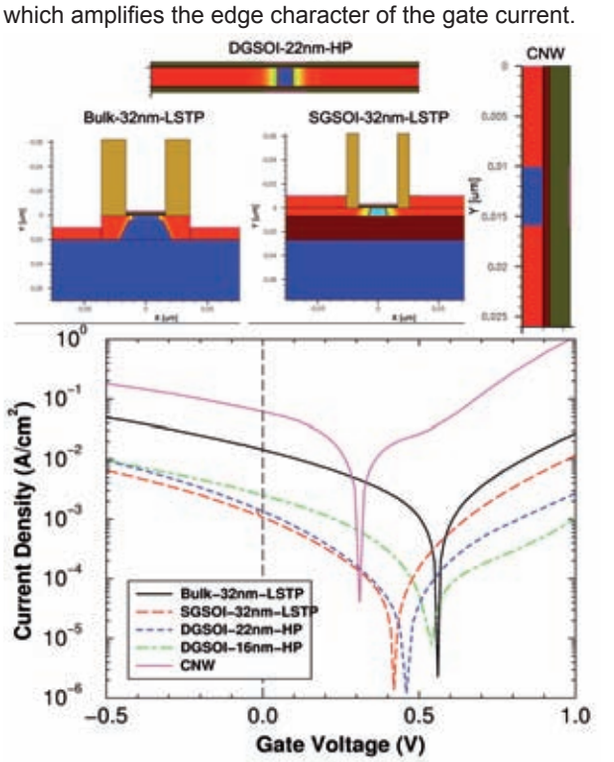
Gate Currents in Future FET Architectures

Personnel: Andreas Schenk

Funding: EU-IST-216171 NANOSIL

Partners: NANOSIL Consortium

In the "Joint Characterization and Modeling Platform" of the European NANOSIL project the direct tunneling gate leakage was studied by advanced simulation for five template FETs with high-*K* gate stacks. A direct comparison of the different architectures is not straightforward, because in the OFF-state the gate current is an edge current (quasi-1D along the gate edges). Whereas the width of all planar FETs was 1 µm, the effective gate edge length of the CNW FET is only $2\pi R$, where R is either the inner or the outer radius. If one uses the outer radius, the effective gate edge length becomes 34 times shorter than the edge length of the planar devices. Scaling the CNW device by this factor, its OFF-current increases to the value of the bulk-32nm-LSTP FET. The latter has the strongest gate current, about one order of magnitude more than all other planar FETs which exhibit the same leakage current of about 3×10^{-13} A/µm. Plotting current densities (A/cm^2) instead, takes the effect of the gate edge length into account as well. Then the CNW FET has the highest OFF-state leakage density. The physical reason for this behavior is given by the gate-all-around architecture which amplifies the edge character of the gate current.



Top: Examples of the template FETs. LSTP=Low Stand By Power, HP=High Performance, SOI=Silicon On Insulator, DG=Double Gate, CNW=Cylindrical Nano Wire. Bottom: Direct gate current densities.

Improvement of the Effective Mass Approximation for Silicon Nanowires

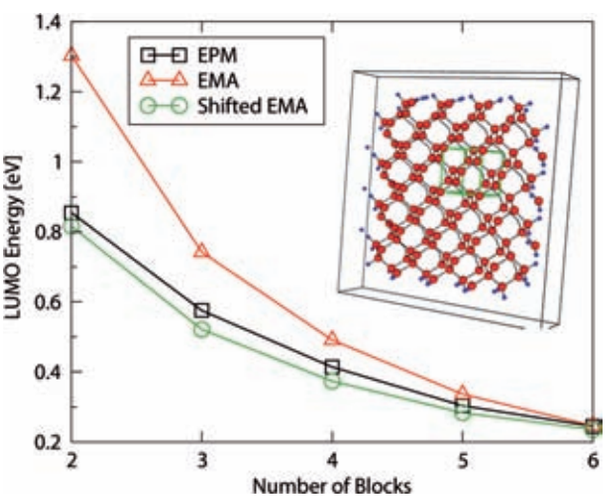
Personnel: Aniello Esposito, Martin Frey, Andreas Schenk

Funding: EU-IST-216171-NANOSIL

References: Schweizer Numerik Kolloquium 2009

In this work, the impact of a weak external perturbation on silicon nanowires is investigated. In particular, the shortcomings of the effective mass approximation (EMA) in reproducing the energy of the lowest unoccupied molecular orbital (LUMO) are addressed. The Hamiltonian of the nanostructure passivated by hydrogen is expressed within an empirical plane wave pseudopotential (EP) framework. Initially, no perturbations are taken into account. In this case the LUMO energy computed by the EMA is found to be considerably larger than the corresponding energy in the EP case. This result is a consequence of the EMAs key ingredient, i.e. the parabolic approximation of the bulk bandstructure. For an increasing wire width the discrepancy between the EMA and the EP method diminishes as the parabolic approximation becomes more realistic.

In a second step, a weak harmonic perturbation is added to the pseudopotential and both the EMA and EP calculations are repeated for the same set of wire widths. The energy overestimation caused by the EMA is found to be close to the one of the free case addressed above. Indeed, by adding the energy shifts from the free case to the EMA Hamiltonian, the discrepancy to the EP energies is considerably reduced as shown in the figure. Such a simple improvement is particularly interesting for quantum transport simulations of small nanowires, where the EMA considerably reduces the computational burden.



LUMO energies for different wire widths. The width is expressed in terms of blocks, i.e. the green cells highlighted in the inserted figure. Data is shown for EMA, EP, and the shifted EMA (see text).

Transport in Inhomogeneously Strained Silicon

Personnel: Vincent Peikert, Andreas Schenk

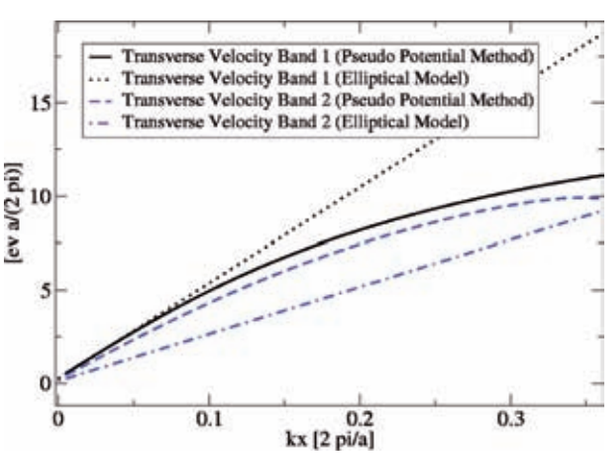
Funding: ETHZ, Toshiba

Partners: Toshiba

Recently, stress engineering attracted a lot of attention and is now already widely used in the semiconductor industry. The reason is that the band structure of semiconductors changes under application of strain. This way, the mobility can be enhanced significantly. As a side effect of recently developed cap layer technologies, the stress is inhomogeneously distributed along the devices. In this project, the effect on transport had to be investigated for state-of-the-art devices developed by Toshiba corporation.

In order to treat strained silicon, the ETH Monte Carlo simulator (EMC) had to be rewritten to simulate with 1/2 of the Brillouin zone instead of 1/8 as before. Furthermore, the EMC had to be extended to local band structures, a concept where every cell of the real space mesh has its own strain-dependent band structure.

However, MC simulations show that it is numerically still sufficient to apply any stress value from the channel region homogeneously to the whole device. This is due to the vanishing strain gradient in the channel region, as well as due to saturation effects. On the other hand, the accuracy of the calculated band structures becomes important with increasing stress level. Hence, a new sparse-grid based interpolation method for the 6D strain space is suggested.



Group velocities of the first two silicon conduction bands in transverse transport direction. The elliptical models are not precise enough in transverse direction. Hence, under stress induced valley splitting, interpolations become necessary.

Analysis of a New Fixed Point Equation for the Boltzmann Transport Equation

Personnel: Vincent Peikert, Andreas Schenk

Funding: ETHZ, Toshiba

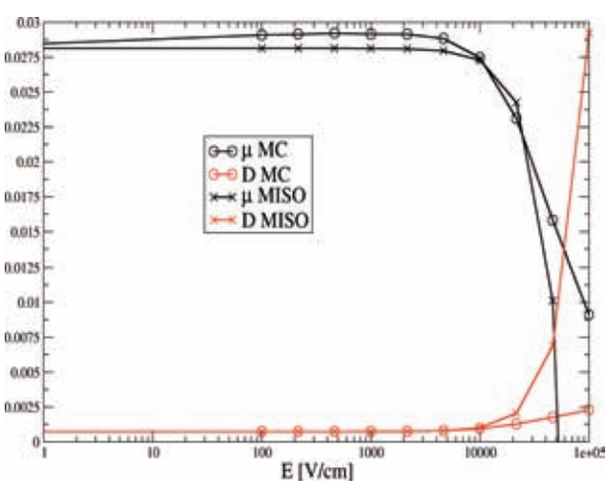
Partners: Toshiba

References: [T12]

The Boltzmann transport equation (BTE) describes the particle probability density f(r,k) in semiconductor devices and forms the basis to design new semiconductor nano devices with TCAD. The solution of the BTE is still an open issue: Monte Carlo approaches are noisy, unacceptably slow and cannot simulate rare events. Direct solvers can not cope with the “curse of dimensionality” of the six-dimensional simulation domain. Therefore, a new method has been developed at our laboratory: by inverting the scattering operator of the BTE and by rearranging the terms, a new fixed point equation for the density f(r,k) arises. The iteration does neither result in a long simulation time nor a high memory consumption.

Depending on the convergence properties of this fixed point equation, three cases are thinkable:

- In the best case this scheme could form a new method to solve the BTE.
- The second best case would be a coupling with the Monte Carlo method.
- In the worst case, the convergence is too slow or the scheme doesn’t converge at all. It turns out that the fixed point equation only converges, if the ratio of the scattering rate and the driving fields is large and that the speed of convergence is ruled by these ratios. This renders the application hard in inhomogeneous semiconductors.



Mobilities and diffusion constants: comparison between Monte Carlo (MC) and the second order iteration (MISO) for bulk silicon with $10^{18}\,cm^{-3}$.arsenic doping concentration.

A New Sparse Grid Based Approach to Solve the Boltzmann Transport Equation Directly

Personnel: Vincent Peikert, Andreas Schenk

Funding: ETHZ, Toshiba

Partners: Toshiba

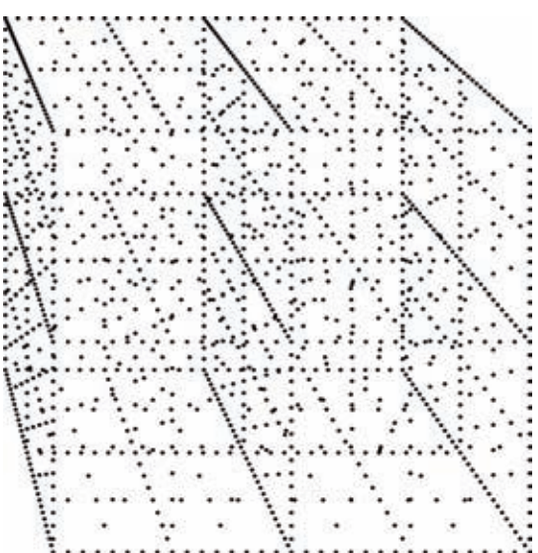
Six-dimensional transport equations (Boltzmann, Wigner) describe the flow of charge carriers in semiconductors. However, these high-dimensional equations result in huge stiffness matrices so that existing direct solvers are restricted to devices with one space dimension so far.

New FEM sparse grid techniques which are currently under development can overcome this “curse of dimensionality” up to a certain degree. The two main ingredients in these concepts are

1) a hierarchical basis and
2) the construction of a multidimensional basis by tensor products of lower dimensional bases.

This way it is possible to save the smallest coefficients from the tensor product expansion a priory, which reduces the number of coefficients drastically. Calculations at our laboratory show, that the numerical solutions of six-dimensional transport equations become feasible when adapting these techniques for TCAD.

The first results of this ongoing project are theoretical investigations and key implementation concepts regarding the following topics: adequate wavelet bases, stable variational formulations, stiffness matrix compression techniques based on the vanishing moments of wavelets, pre-conditioning based on multilevel norm equivalences of wavelets, and matrix-vector multiplications with sophisticated data structures (generalized trees, hash tables).



Sketch of a three-dimensional sparse grid in a cube. In contrast, in a full grid the density of points would be homogeneous which causes the curse of dimensionality.

Diffusion Mechanism of the Arsenic Vacancy Pair in Silicon

Personnel: Kilian Vollenweider, Beat Sahli

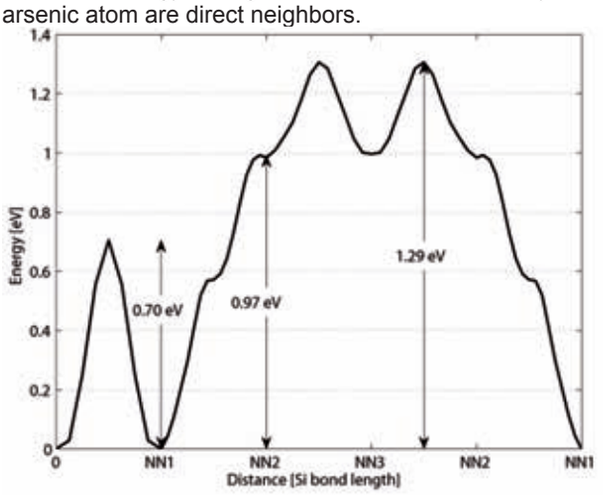
Funding: KTI 8349.1 NMPP-NM ATOMDIFF, Synopsys

Partners: Synopsys
Pilot Users: AMAT, Fujitsu, NEC, Samsung, STM, VSEA

The diffusion mechanism of the arsenic vacancy pair (AsV) in crystalline silicon was investigated with molecular dynamics (MD) simulations. The simulation was performed with the Vienna Ab-Initio Simulation Package (VASP) at a temperature of 1000° C and the total simulated time was 170 ps. In the observed ring mechanism vacancy and neighboring arsenic atom first exchange their positions and subsequently the vacancy migrates around a hexagonal silicon ring from the first nearest neighbor position (NN1) to the second (NN2) and third (NN3) nearest neighbor positions, ending in another first nearest neighbor position.

The local minimum energy configurations of the ring mechanism were determined with relaxations of MD configurations. The corresponding migration energy barriers between these configurations were calculated with nudged elastic band simulations and the overall barrier was found to be 1.29 eV.

The analysis of the diffusion statistics shows that the exchange of vacancy and arsenic atom happens most frequently. The defect spent most of the time (164 ps) in the minimum energy configuration where the vacancy and arsenic atom are direct neighbors.



Mechanism	Number of events	Configuration	Time [fs]
Exchange	8	NN1	164050
NN1 to NN2 (NN2 to NN1)	6 (6)	NN2	4550
NN2 to NN3 (NN3 to NN2)	1 (1)	NN3	1400

Top: The calculated energy barriers for the ring diffusion mechanism of the AsV pair.
Bottom: Diffusion statistics of the MD simulation.

Ab-Initio Calculation of Poisson's Ratio of Crystalline Silicon

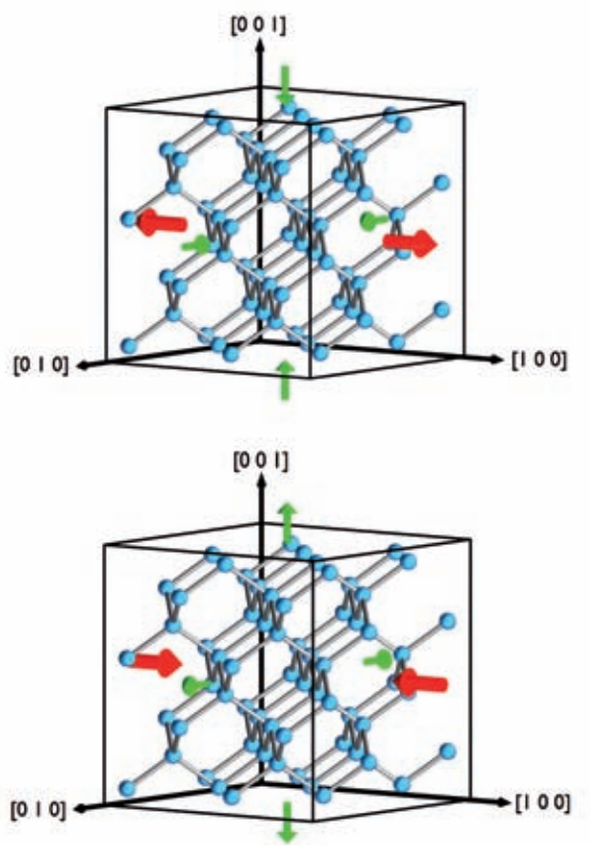
Personnel: Kilian Vollenweider, Beat Sahli

Funding: KTI 8349.1 NMPP-NM ATOMDIFF, Synopsys

Partners: Synopsys
Pilot Users: AMAT, Fujitsu, NEC, Samsung, STM, VSEA

The elastic behavior of crystalline silicon under uniaxial strain in <100> direction has been studied with ab-initio simulations in supercells with 216 atoms. The Poisson's ratio (ν) was calculated, which is defined as the ratio of the applied (ε_{100}) and the resulting perpendicular strains (ε_{010} and ε_{001}). Because of the symmetric equivalence of the two perpendicular strains, they were considered to be the same.

First, the total energy for a set of crystalline silicon under uniformly distributed strain was determined with static simulations. The considered strain values were between -0.014 and +0.014, which corresponds to stress between -1 GPa and +1 GPa. In a second step, the calculated energies were fitted with a quadratic function of ε_{100} and ε_{010}. The minimization of the fit function to ε_{010} for fixed ε_{100} leads to a linear relation between parallel and perpendicular strain. The gradient of this relation is exactly the Poisson's ratio, which was determined to 0.26.



Tensile (top) and compressively (bottom) strained silicon. Applied and resulting strain are indicated with red and green arrows, respectively.

Formation Energies of Defects in Strained Silicon

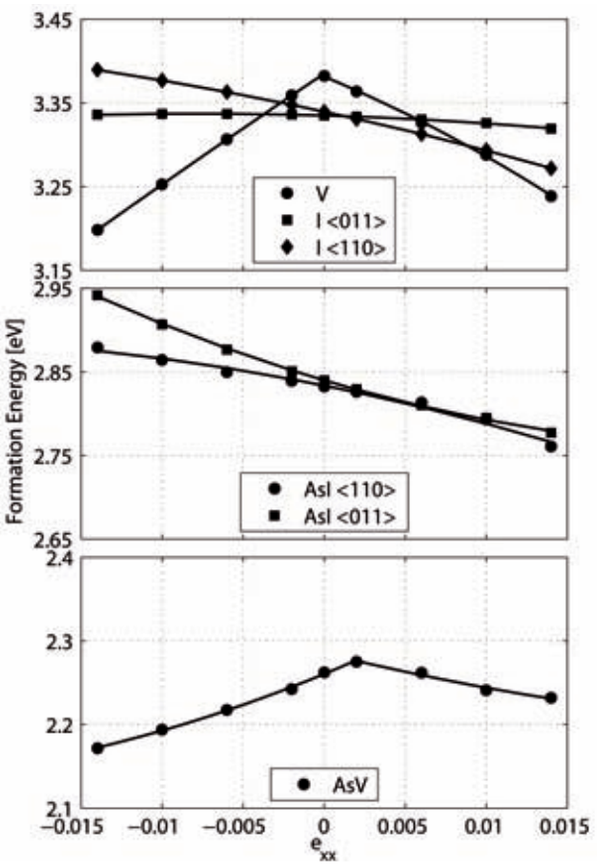
Personnel: Kilian Vollenweider, Beat Sahli

Funding: KTI 8349.1 NMPP-NM ATOMDIFF, Synopsys

Partners: Synopsys
Pilot Users: AMAT, Fujitsu, NEC, Samsung, STM, VSEA

The formation energy of a defect is essential to understand its formation and diffusion in silicon. Furthermore, these properties of defects are of great interest in strained silicon. Therefore, the formation energies of the silicon self-interstitial (I), the vacancy (V), the arsenic interstitial (AsI) and the arsenic vacancy pair (AsV) were calculated in uniaxially strained silicon. In the perpendicular directions, the structure was relaxed. For the interstitial defects I and AsI, the calculations were performed for the two nonequivalent split orientations <110> and <011>. No other orientations have been considered, because all of the four remaining orientations are symmetrically equivalent to one of these two.

The calculated formation energies were quadratically fitted. In the cases of V and AsV two fits were required because strain dependent minimum energy configurations were found.



The calculated formation energies (marker) of four mobile defects in uniaxially strained silicon with quadratic fits (line).

Ab-Initio Calculations of Defect Clustering with Co-Dopants in Silicon

Personnel: Beat Sahli, Kilian Vollenweider

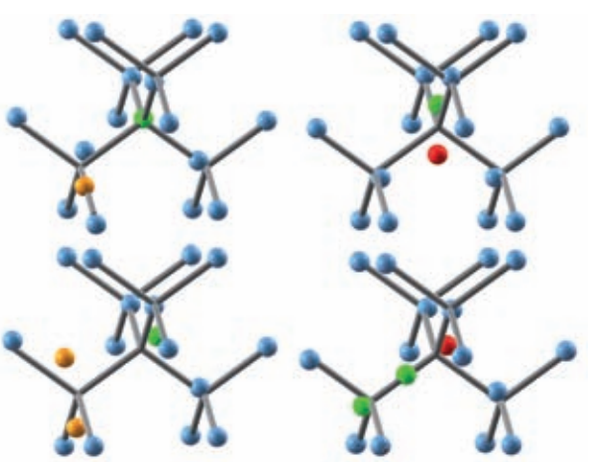
Funding: KTI 8349.1 NMPP ATOMDIFF, Synopsys

Partners: Synopsys
Pilot Users: AMAT, Fujitsu, NEC, Samsung, STM, VSEA

Co-dopants such as fluorine and carbon are used to achieve the stringent requirements on semiconductor technology for the ongoing downscaling of MOSFET devices. Consequently, process simulators must accurately model the interactions of these co-dopants with each other, with the intrinsic point defects and of course with the standard dopants. In particular, such models must describe the formation of pairs and clusters. The required binding energies are very hard to determine experimentally. Ab-initio calculations provide a powerful alternative to experimental methods.

Defect configurations, formation energies and binding energies were calculated for a family of more than 60 different cluster species containing fluorine, carbon, boron, interstitials and vacancies. The calculations were based on density functional theory in the generalized gradient approximation and were performed with the Vienna Ab-Initio Simulation Package (VASP). The setup and analysis of several hundred simulations was performed with a software environment developed for previous calculations for other cluster families. The numerical settings of the VASP calculations were optimized and coordinated in order to obtain a consistent database of clustering energies, allowing the reliable identification of general trends.

The calculated formation and binding energies are used by Synopsys for the development of improved continuum and kinetic Monte Carlo models for dopant clustering and diffusion.



The atomic configurations of four clusters from the investigated defect family: BFI. BCI, BF2I and B2CI. Silicon (blue), boron (green), fluorine (orange) and carbon (red) atoms are shown as spheres. A reference lattice is shown in gray.

Molecular Dynamics Simulation of Defect Configurations and Diffusion

Personnel: Beat Sahli, Kilian Vollenweider

Funding: KTI 8349.1 NMPP ATOMDIFF, Synopsys

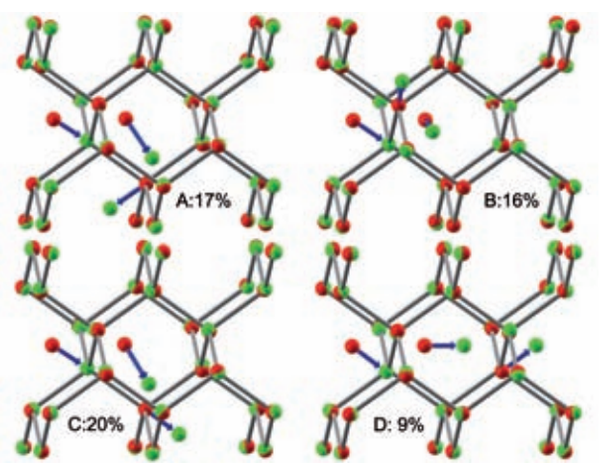
Partners: Synopsys
Pilot Users: AMAT, Fujitsu, NEC, Samsung, STM, VSEA

Ab-initio calculations are a powerful tool to investigate point defects in semiconductors. There are two major methods to sample the potential energy in the high dimensional configuration space and extract defect properties such as formation energies or diffusion barriers:

1) searching for minima and transition states in the potential energy with local optimization methods,
2) calculating particle trajectories with full molecular dynamics simulation.

While molecular dynamics simulation is more robust and delivers more reliable results than the optimization based approach, it also requires a much higher computational effort. However, for a growing range of simulation projects (especially for point defects in crystalline solids), the true bottleneck is no longer the computational cost, but the human work for setup and analysis.

To remove this bottleneck, we have developed a simulation and analysis method that allows the fast and reliable extraction of quantitative information on defect configurations and diffusion mechanisms. It requires a combination of both sampling methods and is based on multivariate statistics (dimensionality reduction, clustering) and time series analysis (segmentation). From particle trajectories and a corresponding series of minimum energy positions, the statistics of defect configurations and diffusion mechanisms are calculated. In contrast to our previous approach, this method is completely general and can be applied to any point defects in silicon.



The four most frequent diffusion mechanisms of the self-interstitial in silicon: The initial (red) and final (green) atom positions are shown, connected by blue arrows. A reference lattice is shown in gray.

Research Projects

Computational Optoelectronics

Coordinators:

Bernd Witzigmann
Wolfgang Fichtner

Monte Carlo Simulation of Avalanche Photodiodes

Personnel: Hektor Meier, Denis Dolgos

Funding: KTI 8894.1 PONDETECT

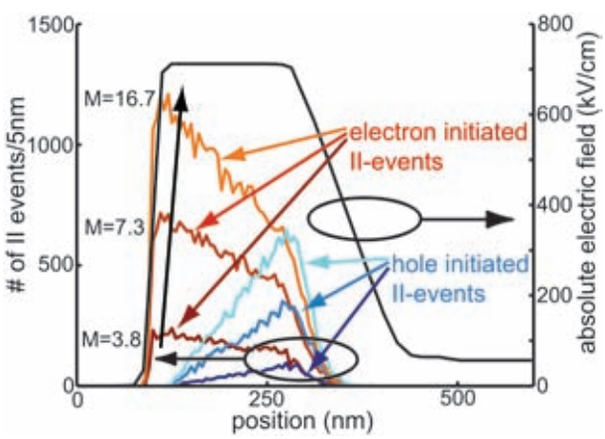
Partners: Enablence

Modern avalanche photodiodes (APDs) can be found as part of optical receiver circuits in fiber optical networks, such as fiber-to-the-home (FTTH) passive optical networks (PON). APDs are operated close to their breakdown voltage and provide signal gain due to avalanche multiplication.

Common drift-diffusion (DD) device simulators with local impact ionization (II) models fail to describe the physics in small scale APDs. First, DD cannot correctly describe the spatially strongly varying non-equilibrium carrier distribution. Hence, DD is unable to predict the correct dynamics of the carrier energies and velocities. Second, the carriers require a certain distance before they acquire enough energy from the electric field to generate a new electron-hole pair by means of II. The so-called dead-space can be several tens of nm. This effect can not be described by local II models where the II-rate depends on local quantities, such as the local electric field.

Non-equilibrium carrier transport and non-local II is accurately modeled using a Monte Carlo (MC) procedure. Below the non-locality of the II-events within a separated absorption, charge and multiplication APD is shown.

Using a one-dimensional, frozen field MC device simulator the breakdown behavior and the bandwidth limitations of state-of-the-art APDs have been analyzed. The optimized simulator allows a time-efficient analysis and predictable improvements of the device structure.



Right axis: Typical electric field profile in a separated absorption, charge and multiplication avalanche photodiode. Left axis: Number of electron and hole initiated impact ionization events for a multiplication gain of 3.8, 7.3 and 16.7.

High Field Carrier Transport in III-V Heterostructures Using Monte Carlo Methods

Personnel: Denis Dolgos, Hektor Meier

Funding: KTI 8894.1 PONDETECT

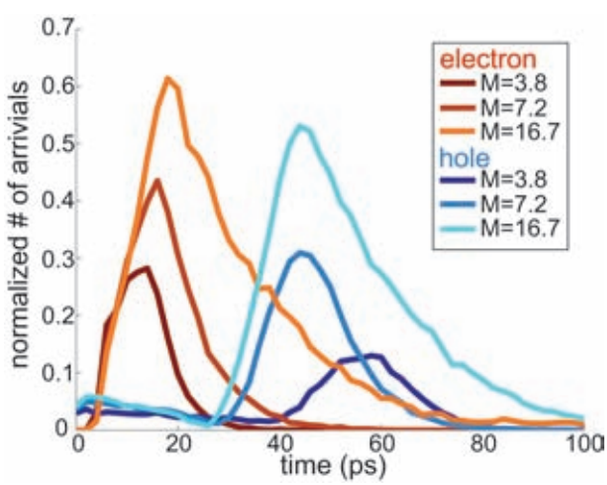
Partners: Enablence

The simulation of carrier transport in modern semiconductor devices operating at far non-equilibrium conditions requires the solution of semi-classical Boltzmann transport equations (BTEs). A stochastic solution technique called Monte Carlo (MC) method is used. Electrons and holes are propagated in time, real- and momentum-space using Newtonian dynamics and quantum mechanics. From an ensemble of charge carriers relevant data like distribution functions and mean values can be gained.

Within this project a MC simulator is being developed to compute the transport properties of state-of-the-art avalanche photodiodes (APDs). An analytical multi-valley non-parabolic band model is used for scattering mechanism calculations and equation of motion solutions. All relevant scattering mechanisms for III-V semiconductors like phonon scattering (acoustic, non-polar optical, polar optical), ionized impurity scattering, alloy scattering and non-local impact ionization are incorporated.

A separated absorption, charge and multiplication APD (SACM APD) has been simulated. The diagram shows the histogram of electron and hole arrival times at the n- and p-side of the device, respectively, as a response to optically generated electron-hole pairs.

In future, the high-field transport of carriers will be modeled using ab-initio full-band structures. The Poisson equation will be coupled to the BTEs.



Histogram of electron and hole arrival times at depletion layer boundaries as a result of photon generated electron-hole pairs within the absorber region for different gains M.

Frequency Domain Simulation of VECSELs

Personnel: Philipp Kreuter

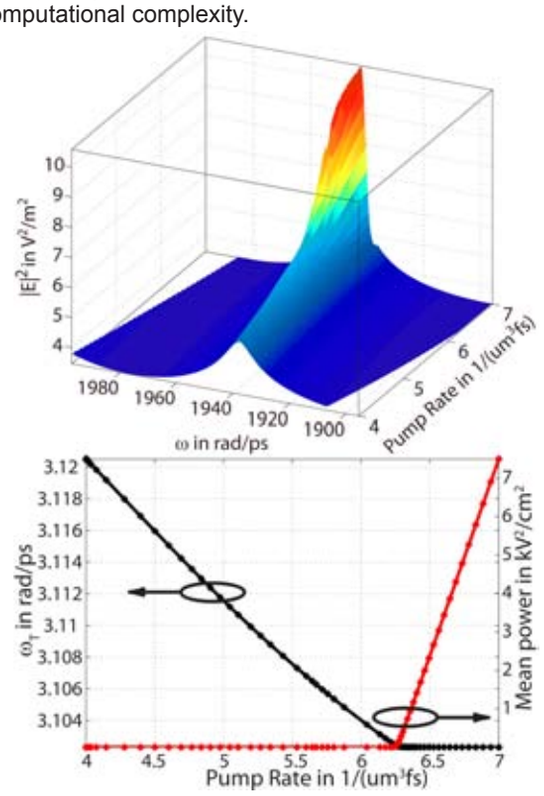
Funding: ETHZ

Partners: IQE-ETHZ

Mode locked vertical-external-cavity surface-emitting lasers (VECSELs) have been studied intensively in the past decade. Commonly, time domain models are used for their numerical simulation. The large separation of timescales combined with the weak damping of the system, however, renders this approach computationally very demanding.

In order to avoid any transients in the simulation, a novel frequency domain approach has been derived to directly determine the periodic steady state solution. The large geometry is discretized with a combined FEM-TMM method by separating linear and nonlinear device domains. Nonlinear light-matter interaction is incorporated as an IIR filter. The solution period is an additional unknown.

The novel approach has been validated by the simulation of a superluminescent light emitting diode. It has been found to be capable of describing the nonlinear dynamics in semiconductor lasers while reducing the computational complexity drastically. The frequency domain method clearly outperforms time domain methods in terms of computational complexity.



Top: Output power spectrum as a function of the pump rate.
Bottom: Mean electric facet power as well as periodic angular frequency as a function of the carrier pump rate.

Dispersion, Wave Propagation and Efficiency Analysis of Nanowire Solar Cells

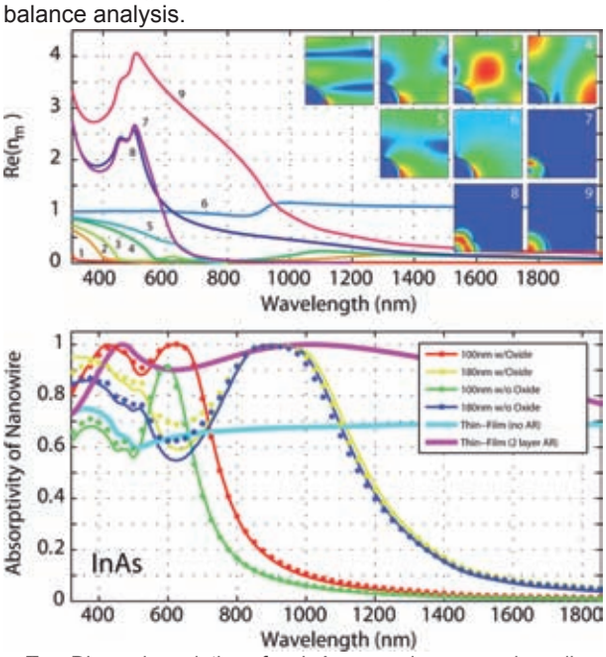
Personnel: Jan Kupec

Funding: ETHZ

References: [O3]

The average rate of solar energy incident on earth is approximately 80,000 TW while the human average rate of energy consumption of all primary energy carriers is circa 13 TW. To harvest a fraction of the power need from the sun high efficiency is paramount. To do so, solar cells based on nanostructured active regions are under intense research.

In the present context, nanowires of dimensions on the length scale of the incident light are employed to convert light into electrical current. In contrast to thin film and bulk solar cells light propagation is not straight-forward to calculate. 3D FEM is used to solve Maxwell's equations and to simulate the absorptivity of selected designs. The absorptivity of the structures does not reflect the absorption properties of the bulk material. The results obtained from 3D analysis were explained by a 2D modal analysis of the structure. By calculating the dispersion relation of the nanowire array, it was demonstrated that large fractions of the light are travelling in discrete modes. Simultaneously, it was shown that effective refractive index approaches based on geometric considerations are not adequate. Quantitative agreement between 3D and 2D modal analysis was achieved, the resulting efficiency limits of the designs were determined by a modified detailed balance analysis.



Top: Dispersion relation of an InAs nanowire array solar cell, real part of the modal refractive index along with the corresponding modal field distributions.
Bottom: Comparison between 3D and 2D modal analysis for various designs.

Finite Element Calculation of Semipolar and Nonpolar GaN Laser Diode Waveguides

Personnel: Jan Kupec

Funding: ETHZ

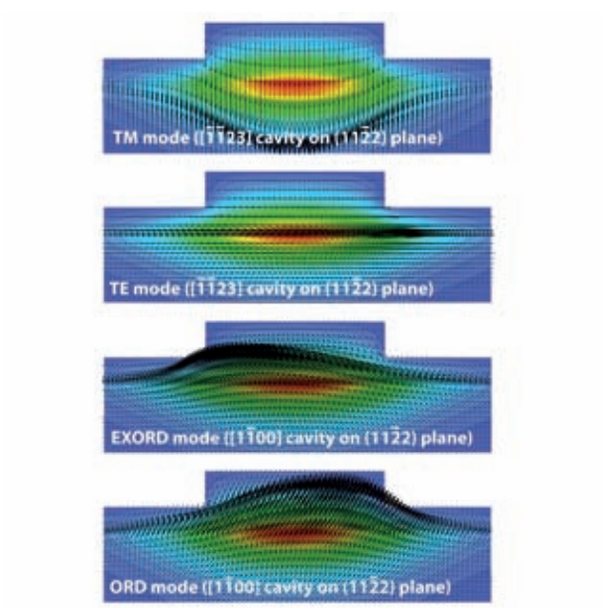
Partners: TU Berlin

References: [O5]

The optical properties of laser diode cavities grown on semipolar GaN are significantly influenced by their orientation with respect to the semiconductor surface. Cavities along the nonpolar direction exhibit birefringence in the plane orthogonal to the direction of wave propagation. As the interfaces of the various layers of the laser heterostructure are neither normal nor parallel to the axis of birefringence, the modal field patterns are influenced by the interplay of birefringence forcing the electric field to be oriented along the ordinary and extraordinary axis as well as by the continuity conditions for the electromagnetic fields across material interfaces. This circumstance leads to a qualitatively different modal characteristic compared to the behavior of cavities grown along the semipolar directions where TE and TM modes exist.

These observations have to be incorporated into the design of a laser diode device as the orientation of the modal electric field ultimately determines threshold.

We employed the finite element method for solving the eigenvalue problem derived from Maxwell's equations for ridge waveguides oriented in both semipolar and nonpolar direction. We observed that due to the low refractive index contrast of the heterostructure layers, the modes for nonpolar oriented cavities are closely oriented along ordinary and extraordinary directions.



Fundamental modes for laser diode ridge waveguides oriented along both semipolar and nonpolar directions. In cavities oriented along the semipolar direction, TE and TM modes can propagate.

Physical Characterization

Coordinators:

Wolfgang Fichtner
Mauro Ciappa
Dölf Aemmer

Monte Carlo Modeling of the Secondary Electrons Yield at Low Energies for SiO_2 and PMMA

Personnel: Mauro Ciappa;
FBK: Maurizio Dapor

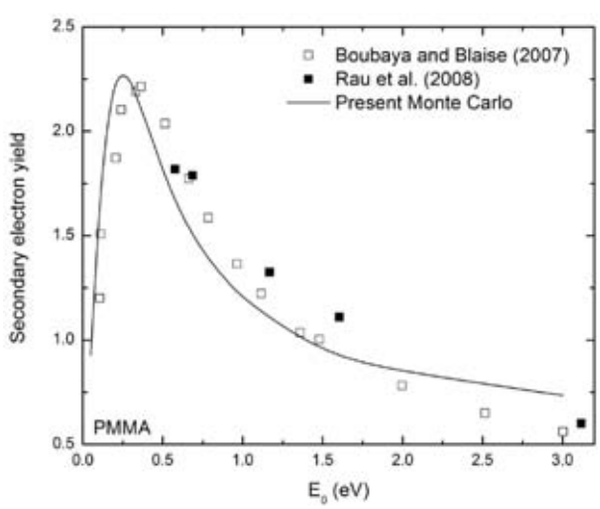
Funding: ETH

Partners: FBK

References: Journal Micro-Nanolithography 2010

Polymethyl Methacrylate (PMMA) and SiO_2 are relevant dielectrics for microelectronics. In particular, they are largely used either as a resist or as masks in optical and electron beam lithography for the fabrication of integrated semiconductor devices down to the nanometer scale. With the most advanced patterning techniques, critical dimensions (CD) measurements with sub-nanometer uncertainty must be performed beyond 22 nm. This task is still carried out by high-resolution CD scanning electron microscopy (CD-SEM). Even with the best available equipment, accurate nanometrology requires that the electron beam interactions are understood and that the image formation process is modeled to deconvolute the relationship between the sample and the SEM image. At present, Monte Carlo simulation of the generation and transport of secondary electrons in materials is still the most straightforward approach to the solution.

In this project, the main scattering mechanisms governing the transport of electrons in PMMA and SiO_2 in an energy domain ranging from the energy of the primary electron beam down to few hundreds of milli-electronvolts are identified. In particular, electron energy loss mechanisms like electron-to-electron scattering, scattering with phonons and scattering with plasmons have been modeled quantitatively. Furthermore, a dedicated Monte Carlo simulation scheme for the emission of secondary electrons has been developed to be applied for the extraction of critical dimensions in scanning electron microscopy.



Secondary electron yield of PMMA as a function of the primary beam energy E_0 at normal incidence. The solid line shows the accuracy of present model after implementation in the Monte Carlo tool. Symbols are experimental data.

Monte Carlo Simulator for Critical Dimension SEM Metrology

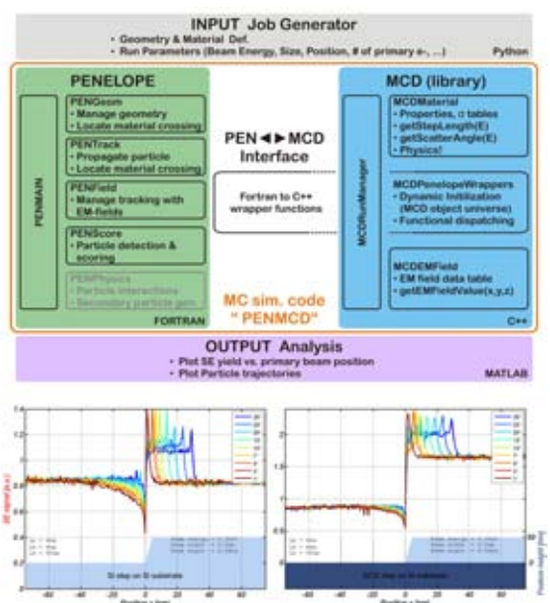
Personnel: Alexander Koschik, Stefan Holzer,
Mauro Ciappa;
FBK: Maurizio Dapor

Funding: ETHZ

Partners: FBK

Quality control in latest CMOS technologies requires critical dimension (CD) measurements during the manufacturing process with sub-nanometer uncertainty in order to avoid yield loss. Besides the use of the most advanced equipment, accurate nanometrology requires that the physics of image formation in scanning electron microscopy (SEM) is accurately modeled to extract the relevant quantitative information. Present CD extraction techniques for linewidth measurement of photoresist lines (e.g. PMMA) that are largely used in optical and electron beam lithography for device integration down to the sub-16 nm scale, can not meet the tight uncertainty requirements.

For the design of novel CD extraction and surface reconstruction methods, a MC simulator has been developed to provide the necessary secondary electron (SE) yield information. Most recent models for the low-energy electron scattering processes permit the accurate treatment of SE generation. Particular attention has been paid to the implementation of a fully discrete interaction scheme based on the straggling principle, as well as of efficient tracking and ray tracing functions of SE in 3D geometries with arbitrary shape and in the presence of electromagnetic fields. At present time-invariant electrostatic fields (steady-state charging conditions) are assumed, which are provided by external Poisson solvers.



Top: Block structure of novel MC simulator based on the code PENELOPE.
Bottom: Simulated linescan signals for step-geometries with varying angle, Si/Si (left), Si/SiO2 (right).

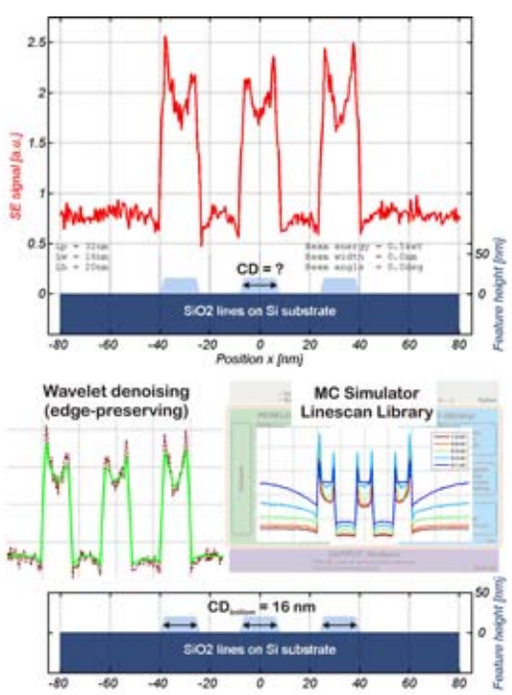
Digital Filter Methods for CD Extraction of SEM Linescan Signals

Personnel: Alexander Koschik, Stefan Holzer, Mauro Ciappa

Funding: ETHZ

Critical dimension (CD) extraction from high resolution scanning electron microscope (SEM) images is a powerful approach but it is time consuming. Therefore, alternative strategies have been explored with the scope to process directly raw one-dimensional linescans of photoresist lines or vias in thick dielectric layers as they are acquired by the instrument.

Digital filters have shown to be very promising in solving this class of problems. In this project, several deconvolution methods have been developed, which are based both on stable numerical procedures, and on the calculation of the transfer functions by Monte Carlo simulation from some basic structures. This enables to account for the complex physics that governs formation of a SEM image. As the rendering of the sample topography through the collection of secondary electrons is strongly dependent on local characteristics (e.g. material, shadowing, slope, etc.), SEMs generally produce a non-linear response. Therefore, the use of linear deconvolution algorithms has been demonstrated to be feasible in a reduced amount of cases, where local effects just play a limited role and the signal-to-noise ratio of the raw signal is sufficiently high.



During the deconvolution process, the raw signal (top) is first smoothed using a wavelet filter (center left) and then deconvoluted using MC generated library of linescans (center right), delivering the CD information (bottom).

Modeling and Simulation of the Electrostatic Field due to Charging Effects in Scanning Electron Microscopy

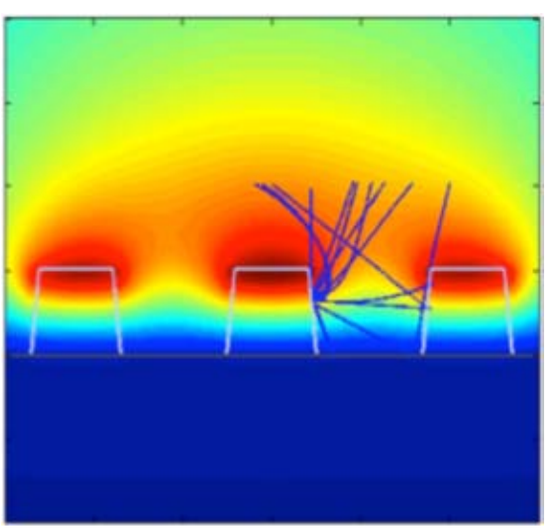
Personnel: Stefan Holzer, Alexander Koschik, Mauro Ciappa

Funding: ETHZ

Electrostatic charging of non-conductive samples in scanning electron microscopy (SEM) degrades the measurement of critical dimensions in the manufacturing of nanometer scale integrated circuits. Modern SEMs mainly operate with primary electrons impinging on the sample surface at energies below 200 eV. Therefore, the presence of electrostatic fields due to self-charging effects can strongly impact the trajectories of both primary and secondary electrons, and ultimately the accuracy of the extracted linewidth.

A simulation tool accounting for charging effects typically includes a Monte Carlo code for the simulation of the electrons interactions within the sample, a code for the transport and the recombination of the deposited charge within the dielectric, a Poisson solver to calculate the electrostatic field as a function among others of the local charge, and a ray tracing code for the calculation of the trajectories of the secondary electrons exiting the sample surface and possibly reaching the detector.

In present project, the 3D device simulator SENTAURUS-DEVICE has been used to simulate the electrostatic field arising from the fixed charge injected and generated in the dielectrics, as well as the electrostatic field produced by charges induced in the underlying semiconductor. Additionally, dedicated tools have been implemented to transfer automatically the field data from the device simulator to the ray tracing tool.



Electrostatic field produced by the charging effects in three adjacent SiO_2 lines on silicon (as simulated by SENTAURUS-DEVICE) and the resulting trajectories of the emitted secondary electrons.

Fine Tuning of Electron Beam Crosslinking of Electrical Cables and Wires by 3D Monte Carlo Simulation

Personnel: Luigi Mangiacapra, Mauro Ciappa; HUBER+SUHNER: Maria Stangoni, Stephan Ott

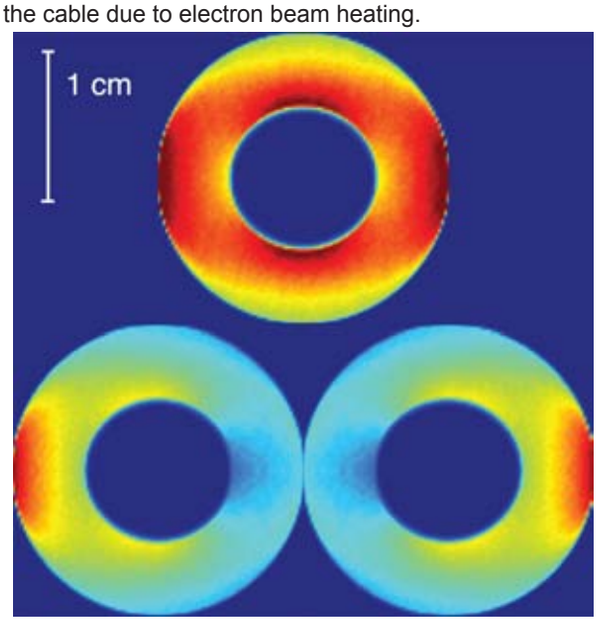
Funding: KTI 9561.1 PFIW-IW

Partners: Huber+Suhner

References: [P2], [P3]

One of the main challenges in electron beam processing of polymers is the setup of optimal irradiation conditions to deliver a uniform dose in the isolation layer of cables. A solution of this problem leads to the best degree of polymer crosslinking and satisfies the required specifications. In the present project, the problem is solved by three-dimensional Monte Carlo simulation.

Together with the accelerator geometry, the electron beam energy is one of the critical parameters that affect the final dose uniformity. During processing, cables are span through dedicated conveyors and pass several times across the irradiation field in different positions and fluence values. This involves several irradiations with different spatial dose distributions. For a fine dose calculation, the simulation has to be subdivided into multiple steps to reproduce the real geometry. Then, all contributions are added to obtain the spatial distribution of the cumulated dose. For this scope, a three-dimensional Monte Carlo simulation flow has been designed to automatically calculate the cumulated dose distribution for accelerator geometries of a given complexity. Through an iterative procedure it is now possible to calculate the beam energy for optimum dose uniformity in a few minutes. The developed tool will be extended for the optimization of multiple process variables, including the temperature increase of the cable due to electron beam heating.



Partial dose distributions in the Polyethylene isolation of a copper cable crossing the radiation field in the center of the conveyor (top) and at both sides (bottom), respectively. The most homeogeneous dose is obtained for an electron beam energy of 2.1 MeV.

Quantitative Three-dimensional Modeling and Simulation of Electron Beam Accelerators for Material Processing

Personnel: Luigi Mangiacapra, Mauro Ciappa; HUBER+SUHNER: Maria Stangoni, Stephan Ott

Funding: KTI 9561.1 PFIW-IW

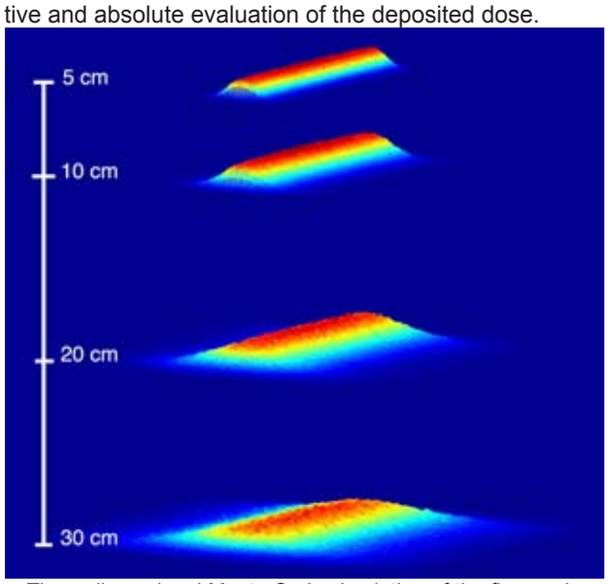
Partners: Huber+Suhner

The quantitative characterization of the irradiation field in industrial electron accelerators is critical to the accurate calculation of the dose delivered during radiation processing.

High-energy (up to 5 MeV) high-current (up to 100 mA) electron beams are collimated and scanned over large working fields (up to 0.3 m^2) by suitable electromagnetic optical systems. Before reaching the target to be irradiated, the electron beam has to cross the accelerator thin window, as well as several centimeters of air. The resulting interactions have a relevant impact on the angular distribution of the electrons and finally on the spatial distribution of the fluence. Thus, this effect needs to be modeled properly, in order to predict the irradiation characteristics of every single accelerator.

In this project, electron beam straggling has been estimated by three-dimensional Monte Carlo simulation in conjunction with targeted measurements by thin films dosimetry, for calibration purposes.

Unfortunately, the existing dosimetry techniques in the 100 kGy range do not provide enough lateral resolution for this scope. Therefore, alternative experimental methods, including special-purpose Faraday cups with complex geometry, have been designed, simulated, and are presently under investigation. Furthermore, additional experimental systems are under development, for quantitative and absolute evaluation of the deposited dose.



Three-dimensional Monte Carlo simulation of the fluence in a single beam electron accelerator operated at 1 MeV. The spatial distribution of the impinging electrons in air has been calculated at 5, 10, 20, and 30 cm distance after the accelerator thin window.

Multi-Domain, Multi-Level Abstraction Modeling of Integrated Power Devices

Personnel: Mauro Ciappa;
Uni Nottingham: Alberto Castellazzi

Funding: ETHZ

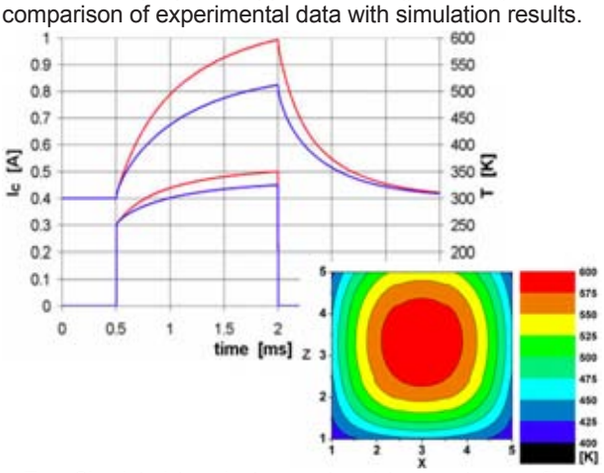
Partners: Uni Nottingham

References: [P1]

The trend in power electronics device development has moved towards structural and functional integration, with a marked tendency towards monolithic solutions. For a given power handling capability, advances in semiconductor technology enable the shrinking of the device dimensions. However, as the volumetric power density increases, the temperature increase during transient operation strongly impacts transistor performance and reliability, as well as that of neighboring components. In addition, solid-state solutions are being used more and more as protective elements in the place of electro-mechanical components: in this case, differently from their usage as high frequency switches, the devices are explicitly intended to withstand energy dissipation.

So, interaction between effects and components traditionally treated independently acquires an increasing relevance. Thus, the availability of a unified platform is gaining interest, in particular if it permits flexible multi-physics and multi-domain solutions. At present, the interconnection of discipline-specialized simulation programs is non trivial, costly and time consuming. On the other hand, the simplifications required by generic circuit simulators are no longer adequate to meet the needs and satisfy the requirements of novel developments.

In this project, the capabilities offered by VHDL-AMS simulation tools have been explored in two case studies. The analytical models of semiconductor components have been coupled with a distributed three-dimensional description of thermal phenomena and with conditional logic statements to render experimental observations. The performance of the proposed approach emerges clearly from the comparison of experimental data with simulation results.



Top: Simulated transient current and temperature profiles for two different cells in the considered PowerMOSFET. Bottom: Corresponding thermal map of the chip surface at the instant of the maximum temperature.

Modeling and Simulation the Degradation of the Thermal Interfaces in Power Module under Cyclic Operation

Personnel: Mauro Ciappa

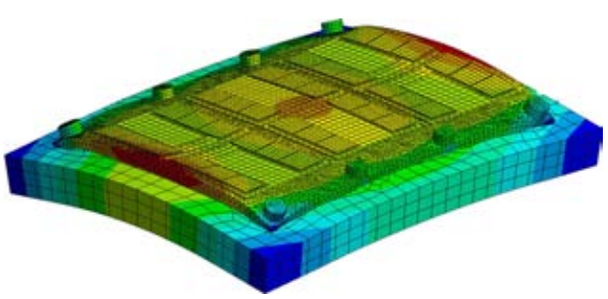
Funding: ECPE

Partners: ECPE

Field experiments show that the thermal management of a power modules and thus their reliability can be strongly influenced by unwanted and sometimes unexpected thermo-mechanical phenomena.

Conventional modules are fixed to the heat sink by bolts placed along the perimeter of the baseplate. In order to reduce the overall thermal resistance of the IGBT the air gap between the baseplate and the heatsink is filled with thermal grease. Due to the mismatch in the coefficient of thermal expansion of the baseplate and of the stiff substrate represented by the heatsink and due to the fact that it is rigidly clamped to the heatsink, the baseplate bends with a radius, which depends on the instantaneous temperature. This effect leads to the formation of a cavity at the interface between the baseplate and the heatsink with a resulting compression and depression of the thermal grease. Over time, the thermal grease is squeezed out of the gap, such that the overall thermal resistance of the power module dramatically increases, worsening the reliability of the system. Finite element analysis of such a problem requires accurate modeling of the stress applied through the bolts, as well as a correct definition of the thermal boundary conditions at the moving interfaces.

The main focus of this project was to model and simulate numerically the reliability aspects related to the interface between the power module and the heat sink under operating conditions. In particular, the issues have been addressed, which predominantly occur during power cycling of the power devices with particular focus on the modelization of complex and large multichip modules mounted on technical heatsinks.



Finite element simulation of the vertical displacement in a power device module as consequence of the pre-tensioning of the bolts and selfheating. The baseplate of the module is pre-bowed to improve the thermal contact resistance.

Implementation of a New Embedded Strategy for Defect Screening of LD-MOS in ICs for Automotive Applications

Personnel: Vezio Malandruccolo, Mauro Ciappa; Infineon: Hubert Rothleitner

Funding: Infineon.

Partners: Infineon

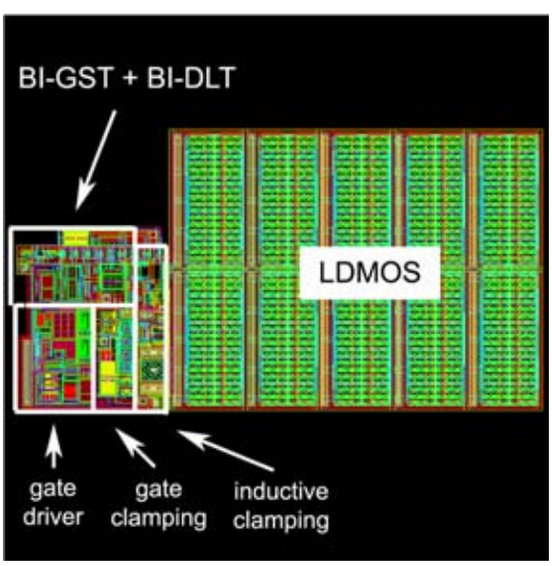
References: [P7], [P8]

Efficient strategies for the control of the defectivity are vital to limit early failures especially in critical automotive applications. In fact, due to the large number and critical functions of integrated devices in a car, random failures occurring in the field may have immediate disastrous consequences as an example in form of safety issues for the car passengers, or expensive recall actions for the manufacturer because of unreliable parts.

Traditional strategies based on burn-in and in-line tests are able to provide the required level of reliability but they are expensive and time consuming. The limitations are mainly due to the fact that they require expensive automatic testers, dedicated contact pads and overhead circuitry, they have very limited parallelization capabilities, they are very cumbersome after device packaging, and finally they need expensive burn-in equipment to perform tests that often exhibit a limited coverage.

In the first phase of this project, a novel built-in approach has been proposed to screen out defective gate oxides and crystals defects in Lateral Diffused MOS transistors in integrated circuits.

In the second phase of the project, the concept has been integrated and tested successfully under realistic operating condition.



Layout of the embedded circuitry performing both gate oxide (BI-GST) and crystal defect built-in screening (BI-DLT). The overhead is less than 7% of the LDMOS area, no increased power consumption, no additional reliability risks.

New Methodology for Built-in Defect Screening of Analog to Digital Converters for Automotive Applications

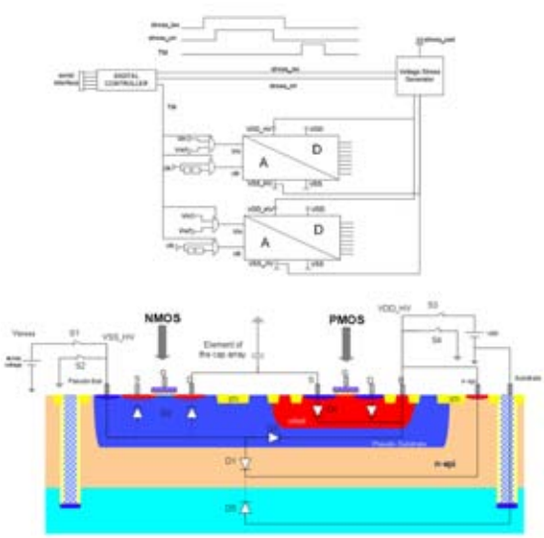
Personnel: Vezio Malandruccolo, Mauro Ciappa; Infineon: Hubert Rothleitner

Funding: Infineon.

Partners: Infineon

References: ETS 2010

Thanks to the variety of devices available for smart power technologies, an increasing number of new features can be added to existing integrated circuits in order to extend their functionalities, reduce their cost, and make them more flexible. This is especially the case of analog-to-digital converters (ADC), which are particularly useful in automotive control systems. As an example, a four-channel airbag driver integrates more than twenty ADCs in the regulation loop of the squib current. Nowadays, a popular architecture for ADC is based on arrays of switched Vertical Parallel Plate Capacitors (VPP). VPP provide high density and the related logic circuitry can be integrated underneath the capacitors. In automotive applications, ADCs accomplish critical functions that have a direct impact on safety of the final system. A major concern in this respect is the integrity of the thick dielectric in VPP capacitor banks. Up to now, capacitor banks could not be directly accessed for testing, such that latent defects in the oxide dielectric could not be screened out. In this project, a novel biasing scheme of the VPP capacitor banks and an embedded circuitry have been designed to screen out in situ defects in the thick oxide of ADCs. This technique presents several advantages. Among these, built-in defect screening is made possible with a very low area overhead, no major design changes are necessary, expensive and long burn-in sessions are no longer needed, and finally the data collected during the back end screening can be profitably used to tune the front-end process.



Top: Working principle of the built-in screening technique. for Vertical Parallel Plate capacitors.
Bottom: Novel biasing scheme to perform the high-voltage stress of the capacitor banks.

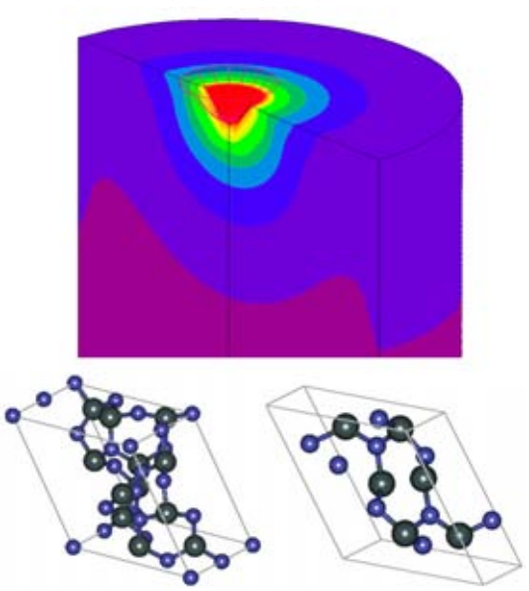
Extraction of the Mechanical Properties in Thin Films by First Principles and Finite Element Simulations

Personnel: Toshiba: Yuji Sasaki, Takayuki Masunaga; Mauro Ciappa

Funding: Toshiba

Partners: Toshiba

The demand of new techniques for accurate extraction of the mechanical properties related to the microscopic structure of thin films used for semiconductor devices and Microelectromechanical Systems (MEMS) is increasing. This is mainly driven by the need to improve the structural design procedures and manufacturing processes by numerical analysis. The mechanical properties of interest are divided into elastic and non-elastic parameters. For example, the simulation of the thermo-mechanical stress caused by the mismatch of thermal expansion coefficients of a thin film on the top of a substrate requires to account for the elastic constants. In converse, the simulation of plasticity and fatigue effects requires to take into consideration the stress-strain curve and the creep behavior of the material. Generally, bulk material parameters can be extracted by tensile and bend tests. However, this is no longer possible in thin films. Usually, the mechanical properties at microscopic level are measured by nanoindentation, i.e. by forcing a diamond probe into the thin film surface in order to acquire the relationship between indentation load and indentation depth (L-D curve). In this project, finite element simulation modeling is used to predict the L-D curve. Special attention is devoted to novel procedures to extract non-elastic material properties from the measured L-D curve as a function of several parameters. At the same time, the elastic constants are calculated independently by first principles simulation techniques.



Top: Nanoindentation measurement as simulated by finite elements.
Bottom: Atomic models of α-Si_3N_4 and β-Si_3N_4 used for first principles simulation.

Multiscale Modeling and Simulation of Grain Boundary Sliding and Diffusion in Aluminum Thin Films for MEMS

Personnel: Toshiba: Haruka Kubo, Takayuki Masunaga; Mauro Ciappa

Funding: Toshiba

Partners: Toshiba

References: [P4]

Deformation by residual stresses, fracturing by thermal processes, and long-term deformation by creeping phenomena are relevant structural issues in the design of advanced MEMS to ensure long-term product reliability. This requires quantitative and predictive simulation methodologies that rely on robust and accurate models of the behavior of thin films materials used in manufacturing and account for their non-continuum properties. The latter is not a trivial task to be solved, since in general thin film material properties are notably different from those of bulk materials. Furthermore, experimental characterization techniques for thin films are inherently more difficult due to the reduced specimen size, load, and deformation range.

In this project a two-dimensional multiscale simulation scheme for aluminum thin films has been developed, which accounts for anisotropic elastic constants depending on the crystal orientation as well as for sliding and diffusion along the grain boundaries. After defining the constitutive equations, the models have been applied to thin films with different textures and stress conditions. An experimental setup including proper test structures has been designed and used to validate the simulation results, which have been shown to be in excellent agreement with the measured data.

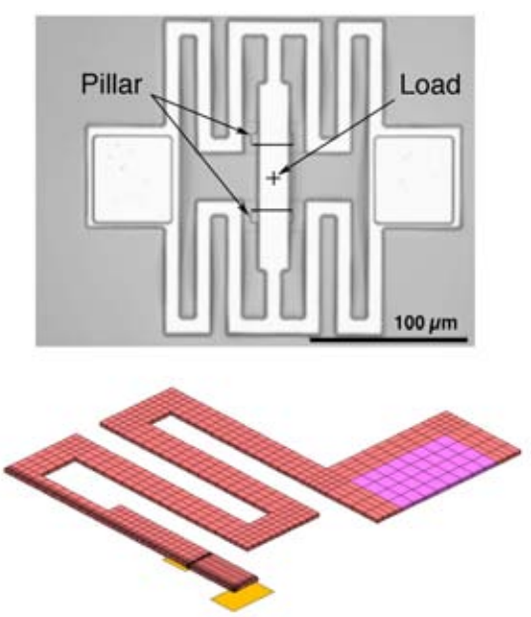


Image of the three points bending structure (top) and the related finite element model (bottom, one quarter) used to validate the models for the polycristalline aluminum thin films.

Design Methodology for CMOS-MEMS Systems

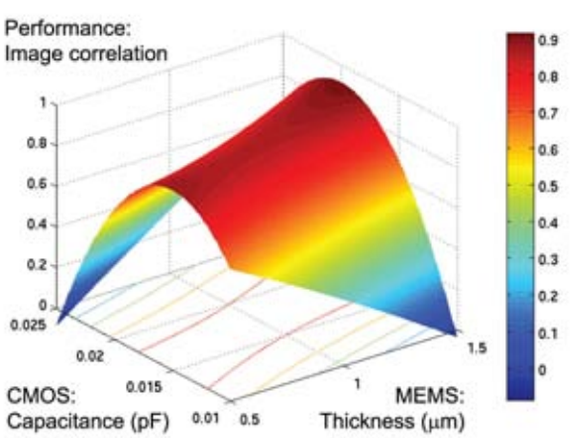
Personnel: NTT: Norio Sato;
Mauro Ciappa, Dölf Aemmer, Hubert Kaeslin

Funding: NTT

Partners: NTT

Integration of microelectromechanical systems (MEMS) and CMOS adds new/high functionality to electronic systems. Compared to individual elements of CMOS circuits or MEMS devices, systems coupling CMOS and MEMS are more complicated. Therefore, a methodology for an efficient design is needed.

The design methodology used in this project has been defined in the first phase. CMOS circuits and MEMS structures are simulated accurately by HDL, SPICE and ANSYS in a bottom-up approach. After selection of important parameters from both CMOS circuits and MEMS structures, all peculiarities due to the coupling of both technologies are extracted by the response surface method. By repeating this procedure over the different abstraction levels of the hierarchy, the system performance at the top level can be described by the design parameters of CMOS and MEMS at the bottom level. Once the complete model is ready, the dependencies of the integrated systems on the individual paramters can be easily derived by a design-space exploration in a top-down approach. This methodology has been applied as a demonstrator to a CMOS MEMS fingerprint sensor. The capability of the system to acquire well-resolved fingerprint images has been assessed by studying the correlation of the output digital images on the input finger morphology. This dependency has then been modeled by the mechanical parameters of a MEMS deformable-plate and by the capacitance of the CMOS sensing circuit. Finally, based on this procedure, the specifications for the fingerprint sensor have been translated into the design space of the CMOS and MEMS components.



Response surface model for the dependency of the system output performance on the design parameters of the CMOS and MEMS components.

Research Projects

Bio-Electromagnetics and Electromagnetic Compatibility

Coordinator:

Niels Kuster

(Adjunct Professor of Information Technology and Electrical Engineering)

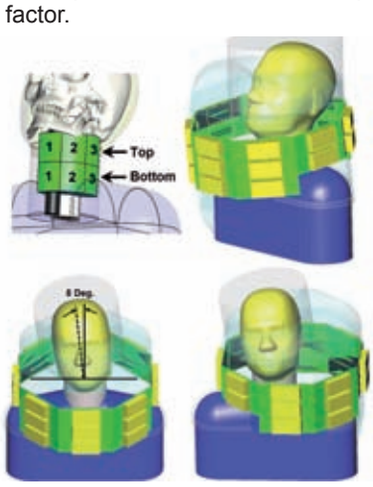
Optimization of the Patient Position in Non-Invasive Hyperthermia Treatment at the Head and Neck Region

Personnel: Chung-Huan Li;
IT'IS: Esra Neufeld, Myles Capstick, Niels Kuster

Funding: CTI 8059.2 LSPP-LS HYCUNEHT

Partners: IT'IS, SPEAG ZMT, Erasmus MC, Hospital La Chaux de Fonds, KS Aarau, Unispital GE, Arkansas Children's Hospital, KispiZH, UniBasel, IBM, BIWI, ERBE, IGT

The objective is to optimize hyperthermia treatments for patients using a novel, next-generation system for regional hyperthermia. Of key importance is to reliably control temperature elevations in cancerous tissues of the head and neck region while the surrounding tissues remain below the threshold for adverse effects. The hyperthermia applicator developed within this study consists of an array of 20 cavity-backed slot antennas configured as 3 stacked rings of antennas with a 40 cm diameter. The system is operated in the European 433.84 MHz ISM band. A water bolus filled with de-ionized water is placed between the applicator and the patient to reduce reflections, miniaturize antenna elements and cool the surface of the patient. Whereas most studies consider the applicator design only, here the patient position is the focus of the research. Therefore, this study has two nested optimizations, the patient position and the amplitude and phase of the array excitation, to achieve optimum SAR performance for each treated zone in the head-and-neck region. The research uses EM simulations using SEMCAD X which uses Finite-Difference Time-Domain algorithm (FDTD). The simulation results showed that the optimization of the patient positions results in an increased quality of treatment as the resolution of EM power deposition is much enhanced. The enhancement comes about when the patient is positioned such that the target tumor region is close to the array centre which results in optimized paths through the patient's healthy tissue. Secondary to this is the fact that more antenna elements also have a significant power contribution so that for a given SAR level amplifiers of lower power output can be utilized, an important hardware cost factor.



Top, left: The three target regions for different tumor locations. Proposed patient positions for the target: location 1 (top, right), location 2 (bottom, left) and location 3 (bottom, right).

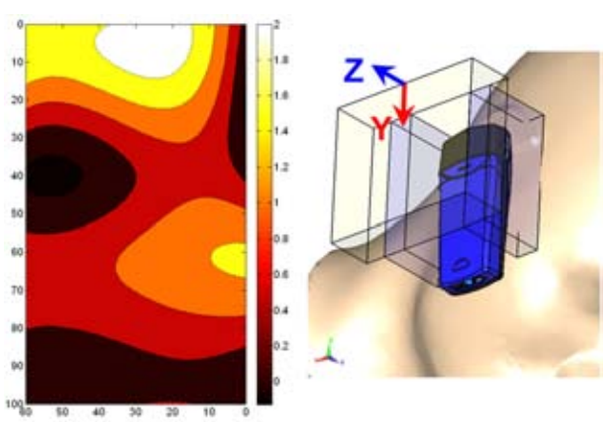
The Effect of the User Hand on Head SAR Using Mobile Phones

Personnel: Chung-Huan Li;
IT'IS: Mark Douglas, Niels Kuster;
SPEAG: Erdem Ofli

Funding: SPEAG

Partners: IT'IS, SPEAG, Field Imaging SARL, Vodafone Group

The objective of this study is to investigate how the Specific Absorption Rate (SAR) in the head of a mobile telephone user is affected by the presence of the user's hand holding it. Current SAR measurement standards IEEE 1528 and IEC 62209-1 state that the presence of the hand lowers the SAR in the head, due to the absorption of radiofrequency energy by the hand. These standards do not include the user's hand in the measurements. However, recent studies demand that the issue be re-investigated. The recent availability of standardized hand phantoms and advancements in numerical modeling (such as posable hand models and hardware acceleration in SEMCAD X) enable the issue to be investigated in more detail than before. In this study, the hand effect is investigated for commercial mobile phones and simplified phone models. Anatomical geometries of the head and hand are used. The hand model is moved to different possible positions for user's hand to find the highest SAR. The results show that the SAR in the head can be significantly increased by the presence of the hand. Worst-case increases of 2.5 dB have been demonstrated at different frequencies and using different mobile telephone models. The results are sensitive to the hand grip, with 3 dB variation of the head SAR observed, depending on the hand location and palm distance. The results of this study provide important information for the development of the SAR measurement standards.



Left: Change in SAR in the head (dB) due to the hand as a function of the hand grip location (vertical) and the palm distance (horizontal).
Right: Generic block hand is shown gripping a mobile phone used against the head.

An EMI Problem on a Real Mobile Phone PCB

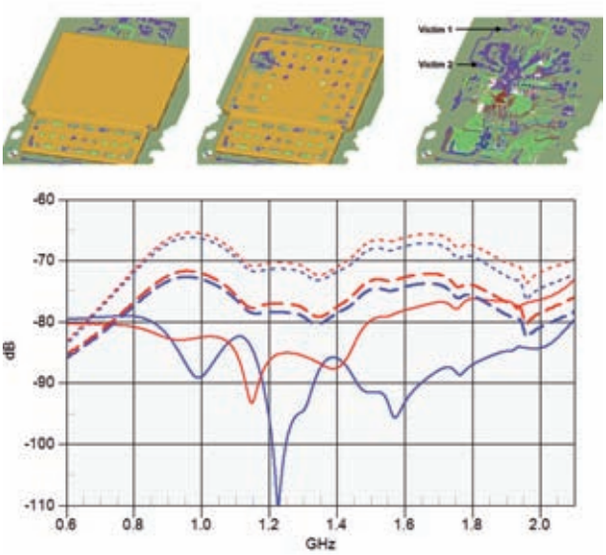
Personnel: Chung-Huan Li;
IT'IS: Nicolas Chavannes, Niels Kuster;
SPEAG: Peter Futter, George Tudosie

Funding: KTI 8969 PFIW-IW LOVESim

Partners: IT'IS, SPEAG, Pfisterer Holding AG

For real-world usage, EMC problems on the PCB-level are always massive and complicated. It is common to design or solve EMC problems on a PCB by following the guidelines based on practical experience or studies. In addition to measurement, numerical simulation also plays an important role in these solutions for reducing the cost and more importantly, gaining more physical insight. For example, simulation can provide some information that is not measureable, such as field distributions in a shielding. However, because of the complexity of practical models, most numerical PCB-level EMC studies are conducted with significantly simplified models. Although those studies can serve as a knowledge base, the simulation results might not reflect the real situation. In this study, both real and simplified PCBs are simulated for respectively obtaining more EM information in reality, and for studying the coupling behavior between the traces.

Shielding is one of the most common and effective ways of suppressing EMI and increasing the isolation between different modules on a PCB. In the meantime, the shielding may also significantly influence the coupling between the traces underneath it. The objectives of this paper are to firstly simulate and validate an EMC problem on a real mobile phone PCB, and secondly, to thoroughly investigate the effect of the shielding on the coupling between the trace and the PCB. Finally, guidelines about the coupling suppression on the PCB are suggested.



Top: the real mobile phone PCB model with three different configurations.
Bottom: the isolation of the two victims simulated with the three configurations.

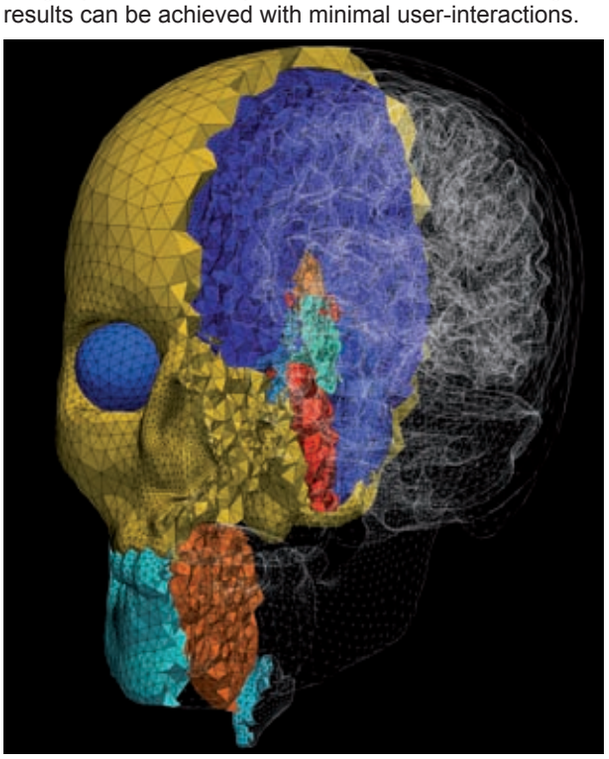
Efficient Generation of Multi-Domain Whole-Body Unstructured Meshes for Multiphysics Biomedical Simulations

Personnel: Tomasz Stefanski;
IT'IS: Dominik Szczerba, Esra Neufeld
Nicolas Chavannes, Niels Kuster

Funding: IT'IS

Partners: IT'IS, Zurich MedTech

Physiological systems are inherently complex, involving multi-physics phenomena at a multitude of spatial and temporal scales. To realistically simulate their functions, detailed high quality multi-resolution and often patient-specific human models are required. Mesh generation has remained a central topic in finite element analysis (FEA) for a few decades now. Recent developments in high performance computing (HPC) driven by the need for multi-physics multi-scale simulations of physiological systems define new challenges in this area. Even though many algorithms have been developed over years and are offered as commercial packages, they are often limited to mechanical engineering applications only. Mesh generation for human anatomical domains requires more effective and flexible techniques to tackle their greater geometrical and topological complexities. We have evaluated several methods to generate unstructured body fitted multi-domain adaptive meshes with geometrically and topologically compatible interfaces from the segmented MR cross-sections of the Virtual Family models for the purpose of large scale whole body simulations. We found that an automated solution is difficult to achieve with real-image qualities, but if optimal methods are selected, good results can be achieved with minimal user-interactions.



Unstructured Mesh Generation From Segmented Medical Images.

Mechanical Contact Simulation for a Pelvis Loading Experiment

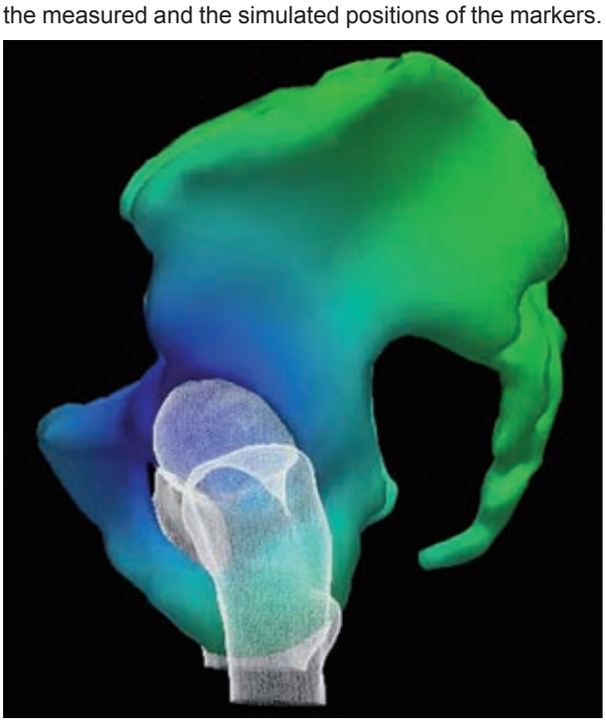
Personnel: Tomasz Stefanski;
IT'IS: Dominik Szcerba; Esra Neufeld, Niels Kuster

Funding: IT'IS

Partners: IT'IS, Zurich MedTech

Bone cancer can lead to resection of a large part of the human pelvis. Implants are necessary to recover basic mechanical functions like walking. Ensuring it is long lasting after such an invasive procedure is a challenging task. Not only must the material be durable, the implant itself must be properly designed and fixed and its integration with the hosting bone has to be stimulated. Currently, serious corrections - or even replacements - are needed 1-3 years after implantation. Therefore, techniques from material engineering sciences are gradually attracting interest from the orthopedics community. Of particular interest are finite element models whereby various implant designs can be efficiently evaluated and their fixation and subsequent performance can be simulated.

To evaluate this technology in a real clinical case, a study has been carried out to compare simulation results with an experiment where a cadaver pelvis was subject to a gait-mimicking oscillatory load. A critical issue in this comparison was proper modeling of the hip joints. The femurs were fixed during the experiment but the pelvis was not, which led to its non-trivial oscillatory movement. Special markers were placed onto the pelvis and a camera tracking system was used to record their positions in real time. A very good agreement has been found between the measured and the simulated positions of the markers.



Contact simulation of human pelvis.

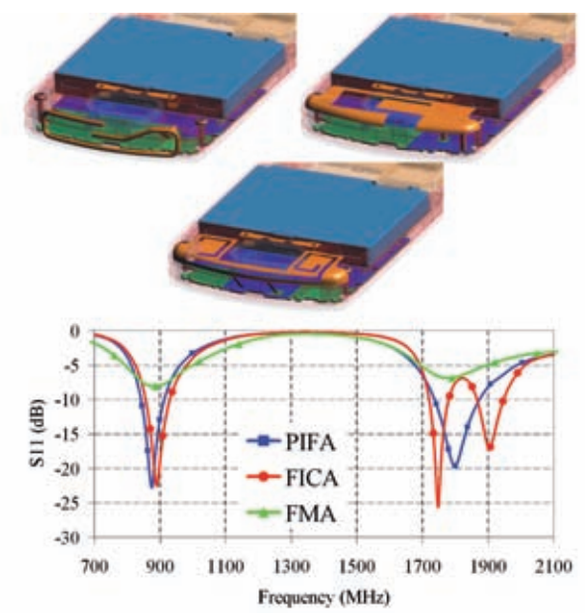
Virtual Prototyping of Mobile Phone Antennas with Genetic Algorithms and Network Parallelization

Personnel: Chung-Huan Li;
IT'IS: Vick Chen; Nicolas Chavannes, Niels Kuster;
SPEAG: Erdem Ofli, Francisco Nunez

Funding: CTI 8969 PFIW-IW LOVESim

Partners: IT'IS, SPEAG, Pfisterer Holding AG

In this study, the virtual prototyping and optimizations of mobile phone antennas was demonstrated with electromagnetic numerical techniques and network parallelized Generic Algorithms. Due to the evolution-like nature of the Generic Algorithms, an antenna optimization process can be performed concurrently on multiple workstations through network parallelization; hence this results in a tremendous reduction in the required optimization time. The design and optimization of mobile phone antennas was executed in a Computer Aided Design (CAD) derived environment. On the basis of an up-to-date commercial mobile phone CAD model, three types of internally embedded multi-band antenna were designed and optimized within a fixed volume. The objective was to achieve optimum antenna performance for all three designs efficiently by employing a well-devised optimization approach. The simulation time required for an optimization task is reduced proportionally by the number of workstations utilized. The optimized antennas were compared in terms of their respective far-field (TRP) and near-field (SAR, HAC) performances. All three designs were successfully optimized towards multiple goals, each task finished within a time duration of 20 hours. The aforementioned numerical technique and optimization scheme are proven to be efficient and effective for RF design optimization tasks.



Top: three optimized internal antenna designs based on same antenna volume and mobile phone structure.
Bottom: S_{11} plots of the three designs in free space.

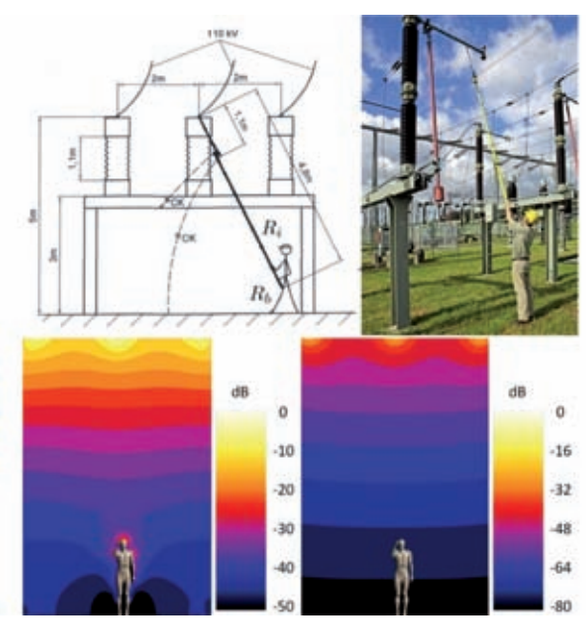
Full Human Body Exposure Assessment for Low Frequency EM Fields

Personnel: Jagadish Nadakuduti;
IT'IS: Vick Chen, Nicolas Chavannes, Niels Kuster;
SPEAG: Stefan Benkler

Funding: KTI 8969 PFIW-IW LOVESim

Partners: IT'IS, SPEAG

This project investigates the electric field and current density induced in a human body when exposed to low frequency electromagnetic fields. A numerical technique based on the Finite Element Method and electromagnetic quasistatic approximations was developed to compute both the fields generated by low frequency sources and the fields induced inside a human body from low frequency exposure. A high resolution MRI scan-based anatomical whole-body model was used in the computations to achieve a detailed representation of the human biological structure. In addition, skeleton-based deformation of the body model was implemented that allows realistic body postures to be included in exposure evaluations. While various biological effects caused by the exposure to low frequency electromagnetic fields have already been established, more in-depth research is still required to gain a comprehensive understanding of the interactions between low frequency electromagnetic fields and biological tissues. In this project, case studies were conducted to investigate exposure situations pertaining to the safety of human beings in the vicinity of high intensity low frequency electromagnetic fields. A numerical technique is demonstrated to provide insightful information for the investigation of induced fields in a human body under various exposure scenarios caused by low frequency electromagnetic fields.



Top: direct and indirect exposure scenario depicting a worker operating a voltage detector in a substation.
Bottom: incidient electric and Magnetic fields for the exposure set up.

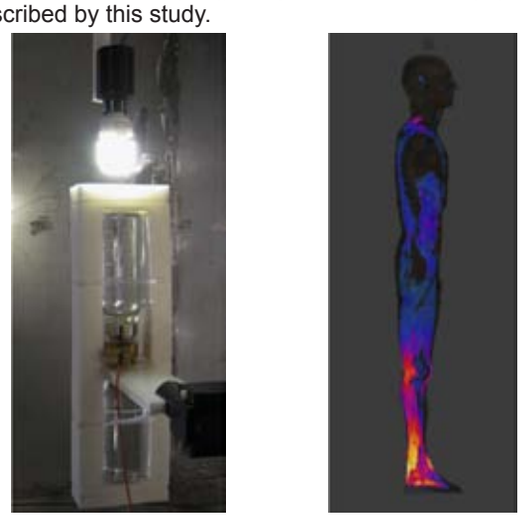
Assessment of EM Exposure of Energy-Saving Bulbs & Possible Mitigation Strategies

Personnel: Jagadish Nadakuduti, Sven Kühn;
IT'IS: Mark Douglas, Myles Capstick, Niels Kuster;
SPEAG: Stefan Benkler

Funding: BAG/08.004316/434.0001/-13 & BFE/15350

Partners: IT'IS, SPEAG

The objective of this project is the development of scientifically sound instrumentation, methods and procedures for the EM exposure assessment of energy-saving bulbs (ESBs). Previous investigations and our initial incident field measurements have demonstrated that compliance tests cannot be performed using standard free-space equipment, since the reference levels are exceeded in the close vicinity of the light bulbs and the measurement uncertainty is large. The recently defined standard IEC 62493 is also inadequate since it is based on incident fields at an arbitrary larger distance from the bulbs and does not provide any correlation to the exposure in people. In order to obtain a sound testing of compliance with the basic restrictions in the safety guidelines, novel equipment was developed for the measurement of the field values induced inside the human body. The authors have also established a relationship between the measured induced current densities and the values induced in different human bodies and in various postures. The field levels in eleven compact fluorescent ESBs, two long fluorescent tube lights, two incandescent bulbs and two LED bulbs have been measured. The worst-case exposure of all investigated bulbs at a separation of 20mm were within the ICNIRP limits, the majority of which with large margins. However, based on the observed large variations between the bulbs, it cannot be concluded that energy saving bulbs are intrinsically compliant with the ICNIRP recommendations. The IEC 62493 standard can be improved by adopting the procedures and equipment described by this study.



Left: Current density probe (including phantom, current clamp and optical transmitter) for exposure measurement from ESBs;
Right: peak current densities in a human model under a charged sphere representing a light bulb.

Investigating the MHD Effect of Aortic Flow

Personnel: Tomasz Stefanski;
BiWi: Adam Kyriacou;
IT'IS: Esra Neufeld, Dominik Szczerba, Niels Kuster;
SPEAG: Stefan Benkler

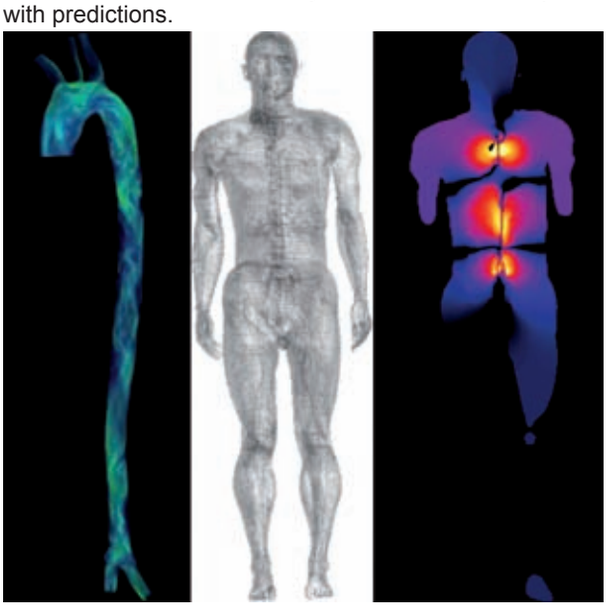
Funding: FDA

Partners: IT'IS, SPEAG

The objective is to develop a method to non-invasively characterize cardiac blood flow, including stroke volume and cardiac output along with spatial resolution of flow characteristics in order to evaluate heart failure conditions. This information is based on a physiological marker called the magneto-hemodynamic (MHD) signal. The MHD signal can be recorded as a distortion of the electrocardiogram (ECG) signal while the patient is exposed to a strong static magnetic field (e.g., MRI magnet). This distortion is caused by induced electrical currents in the blood flow. Modeling can be used to identify suitable ECG measurement locations and to study how the recorded signal can be interpreted.

Flow and electromagnetic (EM) simulations have been carried out using the MRI based *'Virtual Family'* male model. MRI flow measurements of the same volunteer have been generated to obtain suitable boundary conditions as well as a validation base for the flow simulations. To obtain the flow distribution the Navier-Stokes equation is solved using an own parallelized FEM solver with a Schur complement preconditioner. The resulting EM surface potential is determined using a quasistatic solver which is part of our *SEMCAD X* simulation platform.

The MHD simulation platform has been validated experimentally for simple setups with excellent agreement. ECG measurements of the MHD effect will now be performed on the *'Virtual Family'* volunteer and compared with predictions.



Left: aortic flow
Middle: segmented *'Virtual Family'* male model
Right: MHD induced EM potential distribution.

Simulation of Neuromotoric Incapacitation, Neuro-Stimulation and Neuro-Prosthesises

Personnel: Tomasz Stefanski;
BiWi: Adam Kyriacou;
IT'IS: Esra Neufeld

Funding: IT'IS

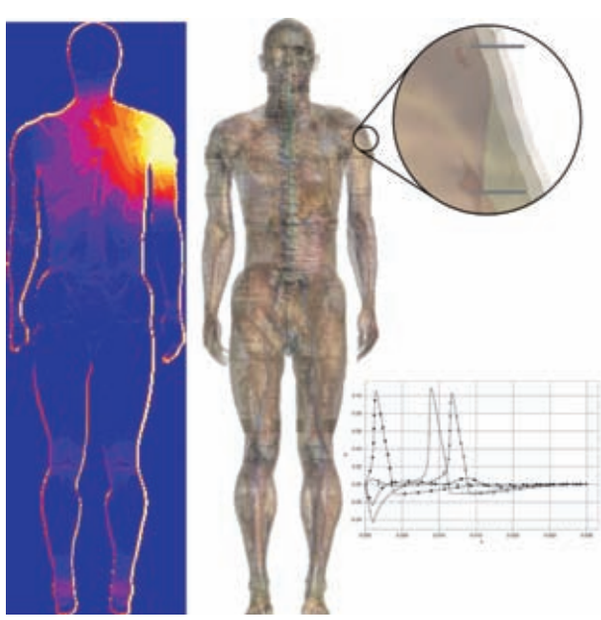
Partners: IFA, MIT, FDA

There are many areas where the interaction of EM fields and neurons are important, including neuro-prosthetics (direct activation of neurons by external EM fields or activation of prosthesis by neural signals), neuro-motoric incapacitation (e.g., *TASER*), MRI safety assessment (e.g., for gradient coil), and neuro-stimulation (e.g., deep brain stimulation).

Our *SEMCAD X* platform is optimized for the simulation of EM tissue interactions in complex tissue distributions and complete human body models. Multiple full body models with more than 200 distinguished tissues have been constructed based on MRI images of volunteers (different age classes, weights, sexes, etc., and even pregnant women models at different stages of gestation). This allows safety and efficacy assessments covering a large part of the human population to be performed.

Different cable theory based approaches of axon and neuron modeling have been implemented to study EM induced nerve excitation and signaling inhibition. The implementation enables consideration of the thermal effects on channel activity. It is intended to extend this to the modeling of neural networks and to provide a Python interface to the widely used *NEURON* simulation platform.

In addition the interaction with neurons at the (sub-)cellular level are being investigated by combining our EM solvers with equivalent network based models of pore formation from our collaborators at the *MIT*. Furthermore, this research can be applied to study electroporation as a means to increase drug uptake.



Computing Farming Based on Microsoft WCF Applied to EM Optimization Problems

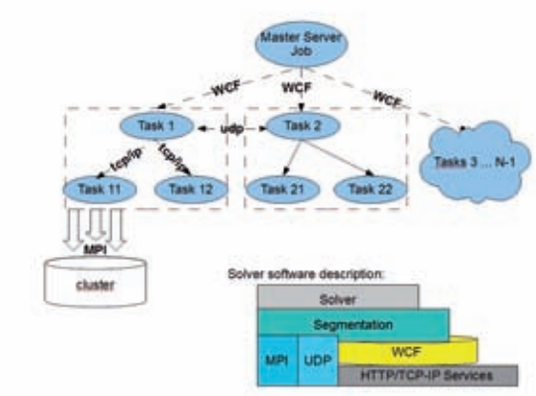
Personnel: Tomasz Stefanski, Guillermo del Castillo; IT'IS: Nicolas Chavannes, Niels Kuster; SPEAG: Francisco Nunez

Funding: KTI 8969 PFIW-IW LOVESim

Partners: IT'IS, SPEAG, Pfisterer Holding AG

The main goal of this study is the usage of all computational resources available within a network (intranet) to perform heavy computational tasks, such as simulation of large electromagnetic (EM) structures or the optimization of complex EM problems requiring large amounts of evaluations of parametrized geometries. The implemented software architecture, described in the figure, can be summarized as follows: When a solver receives a job to be simulated (e.g: waveguide filter), a segmentation algorithm performs the division of the main problem into a series of independent subproblems or tasks. Each task is submitted in parallel to other available solvers located within the intranet. This action is performed using Microsoft .NET WCF, implemented within each solver at one of the communication layers available. At this stage each solver holds the host and client instances of a WCF service, in order to send and receive messages as well as transferring the required files through the net to other solvers. Each submitted task can be further parallelized by either repeating the process described above or by spreading the computational work among multiple computation nodes using the MPI protocol. In our specific implementation all solvers had CUDA accelerated routines as well as multicore architectures compatibility through MPI. An extra communication layer based on multicast datagrams (UDP) was also implemented to allow communication among all the solver instances in order to notify available partial results on child nodes from the distribution tree as depicted in the figure here below

When a task finishes, it submits its results to its parent node (see tree depicted in the figure), each parent node is responsible for assembling all parts of the task.



Network distribution tree representing how a job is segmented and distributed among different tasks. Below the tree the software components embedded in each solver are depicted.

Distributed Database Architecture for Computational Resources Management

Personnel: Tomasz Stefanski, Guillermo del Castillo; IT'IS: Nicolas Chavannes, Niels Kuster; SPEAG: Francisco Nunez

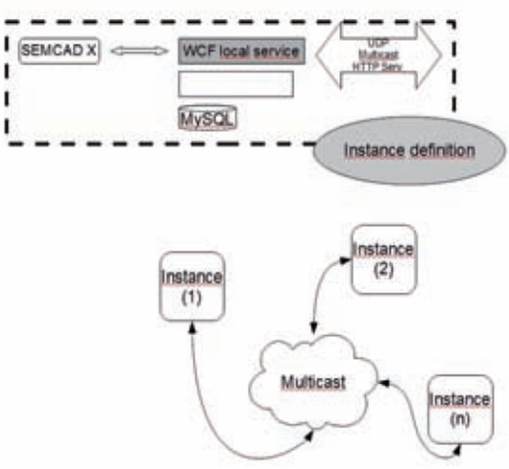
Funding: KTI 8969 PFIW-IW LOVESim

Partners: IT'IS, SPEAG, Pfisterer Holding AG

This work covers the implementation of a distributed resources manager responsible for allocating computational resources in the network (intranet), distributing computational tasks according their complexity, memory allocation etc. This resource manager has been implemented under the SEMCAD X platform, and has been used to address the distribution of electromagnetic simulations over the available SEMCAD X instances running in the same intranet. The software package, as is depicted in the figure, is composed of:

- A WCF service, running in local mode, which is responsible for communicating with the SEMCAD X instances and for providing information on the available machines on the network.
- This WCF service is connected to DB manager components which gives full access to a running MySQL server instance.
- The MySQL server instance contains the database of all the resources in the network, describing computational capacity (such as CUDA capable, multicore platform etc.), the queue of jobs waiting to be run, speed of the ethernet connection, available solvers, available simulation results etc.

Each instance of SEMCAD X running on the intranet, can be run as service provider, and under this situation, it connects to the local WCF service, and its data is inserted into the MySQL service.



Software architecture for resource manager. Within the slotted rectangle the components installed per computer are depicted. The figure below shows the interconnection of true multicast UDP among the instances.

Uncertainty Assessments of OTA Hand Phantom Fixture in Talk and Data Mode

Personnel: Chung-Huan Li;
IT'IS: Nicolas Chavannes, Niels Kuster;
SPEAG: Erdem Ofli

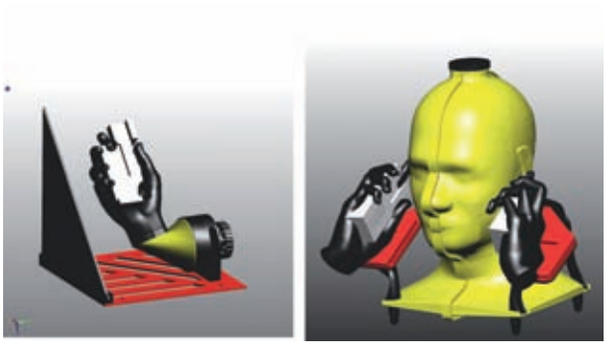
Funding: SPEAG

Partners: IT'IS, Motorola, SPEAG, ERP CTIA

Uncertainty assessments are always relative evaluations and therefore well-suited for numerical simulation tools which provide the most appropriate technique to compare different configurations. It can be guaranteed that the relative accuracy is significantly better than 0.1 dB. The purpose of this project is to describe the concept of uncertainty assessment using simulation tools and to carefully assess the uncertainties arising from talk mode and data mode mounting fixtures.

The hand phantom fixture uncertainty is the effect of the hand phantom fixtures on the TRP/NHPRP/UHRP/PGRP compared to the standard configuration with an ideally RF transparent fixture. The effect of the fixture is frequency dependent and is evaluated at the middle channel of the PCS and Cell bands in order to estimate the uncertainty of the 1500-2200 MHz and the 700-900 MHz bands, respectively. The selected phones used in the evaluation enables the uncertainty to be extrapolated to the entire phone population. The number of phones should be at least six and include at least two monoblock phones (fixed or sliders), two fold phones, two with antennas at the top, and two with antennas at the bottom of the phone.

The evaluation was conducted using the electromagnetic simulation tool SEMCAD X. Each phone is simulated with and without mounting structures and the maximum of each TRP/NHPRP/UHRP/PGRP delta across all phones is determined to estimate the standard measurement uncertainty for the fixture.



Hand phantom fixtures for talk and data modes.

New Hand Grip Investigations for Different Mobile Phone Applications

Personnel: Chung-Huan Li;
IT'IS: Nicolas Chavannes, Niels Kuster;
SPEAG: Erdem Ofli

Funding: SPEAG

Partners: IT'IS, Motorola, SPEAG, ERP CTIA

CTIA-The Wireless Association has recently introduced four standard hand phantoms for each phone form factor (Monoblock, Fold, Narrow Data and PDA) to use in over-the-air (OTA) testing of both talk (head and hand, voice call) and data (hand only, browsing grip) modes. Most of the mobile phone devices currently available in the market fit in one of these hand phantoms. However, alternative hand phantoms (grips) are required for some other popular usages such as two-hands (gaming) mode. In this project, new hand phantoms together with positioning requirements are proposed for OTA testing of mobile phone devices with two hands (in gaming mode).

The size and dimensions of the new hand phantoms are based on the existing parameters defined in the CTIA Test Plan. Human factor studies are performed to determine the positioning of the fingers (grip) with respect to the mobile phone device. The right hand phantom is built using the data obtained from these studies. The left hand phantom is then obtained by mirroring the right hand phantom.

The mobile phone is mounted between right and left hand phantoms and oriented such that the device's main display is tilted 45 degrees from vertical. The test will be performed without any head phantom to simulate two-hands mode (gaming, browsing, navigation). New hand phantom mounting fixtures and spacers were also developed to position the hand phantoms and the device accurately.

Right and left hand phantoms for gaming mode.

FDTD Solver Portable Between Modern HPC Architectures

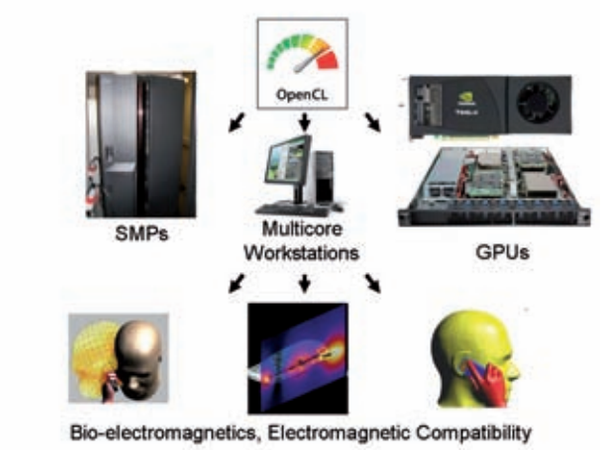
Personnel: Tomasz Stefanski;
IT'IS: Nicolas Chavannes, Niels Kuster;
SPEAG: Stefan Benkler

Funding: KTI 8969 PFIW-IW LOVESim

Partners: IT'IS, SPEAG, Pfisterer Holding AG

Parallel implementations of the computational electromagnetics schemes are required not only to speed up computations but also to increase the maximum solvable problem size. In spite of advancement in the computer processing power, simulations of the real-life problems of bio-electromagnetics and electromagnetic compatibility can still exhaust any currently existing computational resources.

The purpose of this project is to develop a numerically efficient parallel finite-difference time-domain (FDTD) solver in Open Computing Language (OpenCL) which will be portable between modern high performance computers, e.g. based on multicore processors, graphics processor units, and Cell Broadband Engines. Due to scaling of the processor parallelism according to Moor's law, it is quite a challenge to develop scientific codes which are not only portable between existing machines but will also transparently scale its parallelism in the future. OpenCL seems to be a suitable platform for overcoming this challenge maintaining portability between hardware architectures and efficiency of the close-to-the-metal programming interface. On the other hand, the FDTD method is very well suited for parallelization on heterogeneous systems due to high spatial locality of data and resulting efficient use of the cache memory. Therefore, a combination of the FDTD method with OpenCL may result in development of the novel massively parallel code facilitating researchers investigating problems of the computational electromagnetics.



OpenCL (Open Computing Language) is an open framework for parallel programming of heterogeneous systems consisting of multicore CPUs and GPUs.

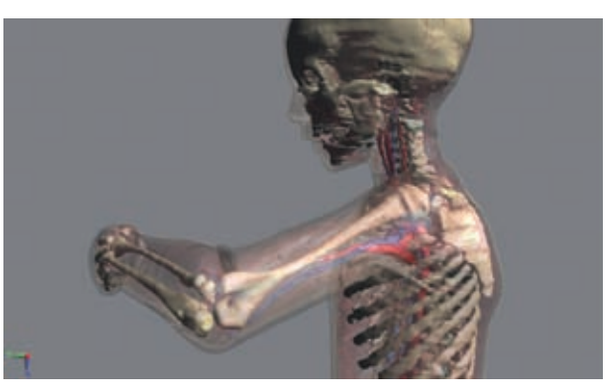
Poser: A Realistic Posture Tool For 3D High-Resolution Anatomical CAD Data

Personnel: Tomasz Stefanski;
IT'IS: Nicolas Chavannes, Niels Kuster;
SPEAG: Emilio Cherubini

Funding: KTI 8969 PFIW-IW LOVESim

Partners: IT'IS, SPEAG, Pfisterer Holding AG

The work presented here extends and combines techniques to deal with high-resolution full-body anatomical models, including deformation of all tissues and organs surrounding the rigid bones in an efficient way. This work also focused on a visual system to setup the hierarchical structure of bones that drive the anatomical deformation in a simple way, taking into account user-defined constraints on the bone articulation. The goal of this work was the development and integration into an existing TCAD package of a framework which takes a high-resolution anatomical model and which allows visual configuration of the influencing bones, including their anatomical constraints. The bone hierarchy allows propagation of transformations through a whole limb if the user moves the parent bone, on the other side the tool makes use of known methods to solve the Inverse Kinematics problem to achieve a desired pose of the bone structure while satisfying user defined joint constraints. The next step is the actual computation of the deformation with immediate visual feedback to the user. The resulting volume-preserving transformation of an element of the model is computed using a method which creates a divergence-free deformation field. To ensure a more realistic deformation, the rigidity of the bone is considered and a simple spring correction is used on the non-rigid parts of the model. Finally, the posed anatomical models can be used to simulate exposure to- and interaction with electromagnetic radiation.



A posed full body model.

Recent GPU-Based Cluster Architectures: Implementation and Application

Personnel: Tomasz Stefanski, Guillermo del Castillo; IT'IS: Nicolas Chavannes, Niels Kuster

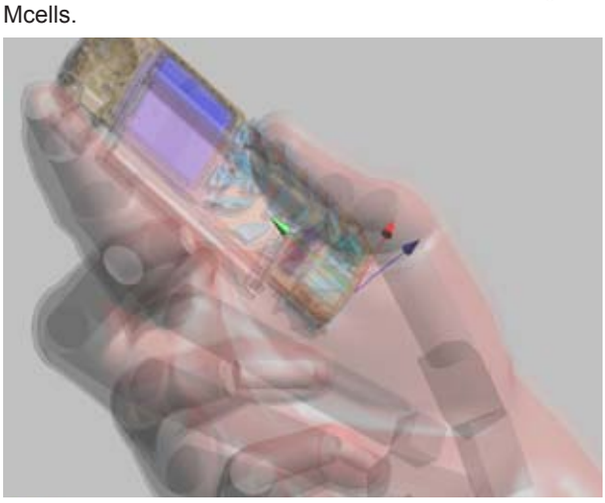
Funding: KTI 8969 PFIW-IW LOVESim

Partners: IT'IS, SPEAG, Pfisterer Holding AG

There is an increased interest in numerical solutions implemented on graphic board architectures for engineering and scientific purposes. The high memory bandwidth of graphics boards makes them ideally suited to the task of accelerating computationally intensive applications. Graphics cards possess much greater computational parallelism than single or multi-core CPU-based systems, and high parallelism results in higher solver speeds.

The FDTD method applied to Maxwell's equations has the characteristic that the x, y and z components of the electric and magnetic fields can be integrated independently for each time-step. This feature makes the method particularly suitable for a parallelizing approach using graphic processing units (GPUs). However, the limit in domain size is determined by the on-board RAM.

In CPU-based systems, a possible solution to expand the simulation size beyond the RAM of one single machine is to have a series of cores in a globally shared memory network (using MPI, for instance). This approach can be applied also to GPU-based systems, with some extra considerations. The current project at IT'IS uses NVIDIA graphics processing units and hardware designed by Acceleware, a partner company of SPEAG, to test the viability of a system that combines the advantage of a having a globally shared network memory for large sized simulations, with the gain of using GPU-based components for high solver speeds. These solver speeds can be in excess of 3 Gcell/s with model sizes of more than 700 Mcells. In contrast, single GPU systems can achieve about 500 Mcell/s and simulation sizes not exceeding 100 Mcells.



Highly detailed model used for benchmark calculations.

GPU-Based High-Speed Computations of Large Scale Problems

Personnel: Tomasz Stefanski, Guillermo del Castillo; IT'IS: Nicolas Chavannes, Niels Kuster

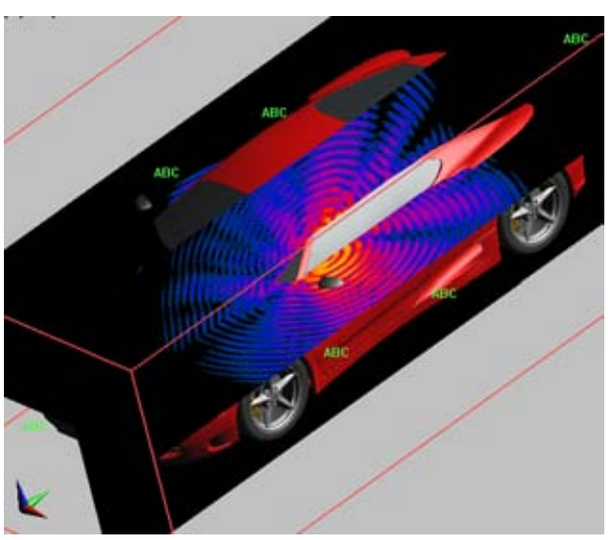
Funding: KTI 8969 PFIW-IW LOVESim

Partners: IT'IS, SPEAG, Pfisterer Holding AG

The Finite Difference Time Domain (FDTD) method applied to Maxwell's equations is ideal for distributed computing since the spatial components of the electric and magnetic fields can be integrated independently for each time-step.

One approach takes advantage of the high memory bandwidth of graphics boards to accelerate computational intensive applications. Graphics cards possess much greater computational parallelism than single or multi-core CPU-based systems. This is especially useful while using the FDTD method, since this particular scheme is very dependent on memory access. The downside is the maximum size of simulations that can be executed is fixed, and such systems are not easily scalable.

The current project at IT'IS tests a system built in-house that combines the advantage of a globally shared network memory (enabling large size simulations) with the gain of using GPU-based components (resulting in high solver speeds). Benchmarks and test have been calculated for very large-sized domains (>700 Mcells) with solver speeds exceeding 2 Gcells/s. Non-clustered GPU systems typically can not handle simulation sizes larger than 380 Mcells or have solver speeds higher than 1.6 Gcell/s.



H-field distribution in a highly detailed car-antenna model.

Extension of the Common FDTD Material Averaging to Dispersive Media

Personnel: Tomasz Stefanski;
IT'IS: Nicolas Chavannes, Niels Kuster;
SPEAG: Stefan Schild

Funding: KTI 8969 PFIW-IW LOVESim

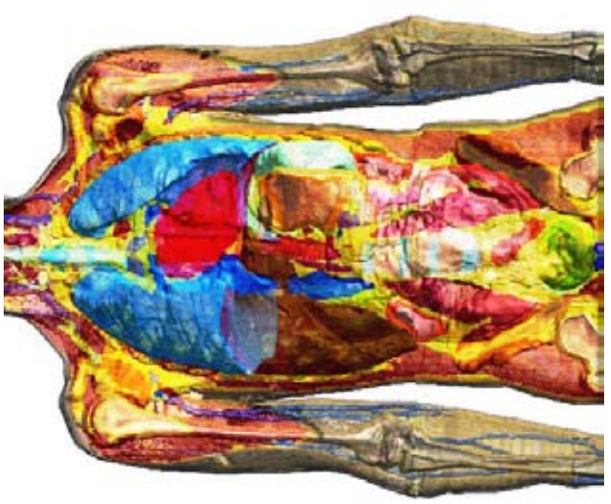
Partners: IT'IS, SPEAG, Pfisterer Holding AG

Dielectric material properties are imbued in the voxels of an FDTD grid, i.e. the FDTD cells whose sides are defined by the rectilinear grid lines. The perfect electric and magnetic conductor approximation for metals (PEC/PMC) as well as the lossy metal material types can be viewed as being assigned on the grid edges directly, due to the fact that PEC or PMC cannot be averaged with dielectric materials and must take precedence.

In conventional FDTD, dielectric edges, i.e. non-metallic edges that are adjacent to dielectric voxels only, are assigned the averaged material properties of their neighboring voxels. It has been shown that this leads to superior accuracy.

A novel implementation now allows the averaging between voxels containing dispersive susceptibilities. By mapping the conventional dispersive types Drude, Lorentz and Debye to a generalized rational form in ω, the approach allows the averaging between all types and combinations of dispersive poles. It is shown that accurate averaging can be achieved by weighing only the amplitudes of the poles while combining the poles themselves.

This approach leads to multi-pole susceptibilities at the boundary of dispersive media, but these surfaces constitute a small subset of all edges in a 3D FDTD simulation, and modern solvers including hardware accelerated solutions are capable of handling inhomogeneous memory needs in a 3D simulation domain.



Human full body model with a highlighted cross-section showing the different tissues. The highly frequency dependent tissue parameters and the complex material distribution require dispersive media with accurate averaging.

A Novel Parallelization Algorithm for the Yee-FDTD Update Coefficients Calculation

Personnel: Tomasz Stefanski;
IT'IS: Nicolas Chavannes, Niels Kuster;
SPEAG: Stefan Schild

Funding: KTI 8969 PFIW-IW LOVESim

Partners: IT'IS, SPEAG, Pfisterer Holding AG

The first step during preprocessing in an FDTD simulation is the computation of update coefficients. For highly complex and very large simulations, this can be a time-consuming step. Mainly, this includes material averaging, stability assessment, and time-step computations.

In modern FDTD simulations containing hundreds of millions of cells and complex geometries such as human full body models, this pre-processing step can be a significant part of the entire computation. In the case of hardware accelerated kernels, cases have been observed where a non-optimized coefficient computation could use more time than the actual FDTD computation itself.

A novel, parallelized implementation can speed up the coefficient calculation by several orders of magnitude. This result has been achieved by utilizing modern threading technology and libraries, intelligently splitting the computational domain into independent parts, and a thorough assessment of recurring computations during the coefficient calculation for typical use cases. It has been shown that such computational steps that are identical for large numbers of cells can be effectively identified and performed before the coefficient calculation.

Human head and mobile phone. The FDTD grid contains about 700 million edges, but the update coefficient calculation completes in less than 1 minute. The highlighted cross-section shows part of the discretization.

A Unified Material Treatment for FDTD

Personnel: Tomasz Stefanski, Guillermo del Castillo; IT'IS: Nicolas Chavannes, Niels Kuster; SPEAG: Stefan Schild

Funding: KTI 8969 PFIW-IW LOVESim

Partners: IT'IS, SPEAG, Pfisterer Holding AG

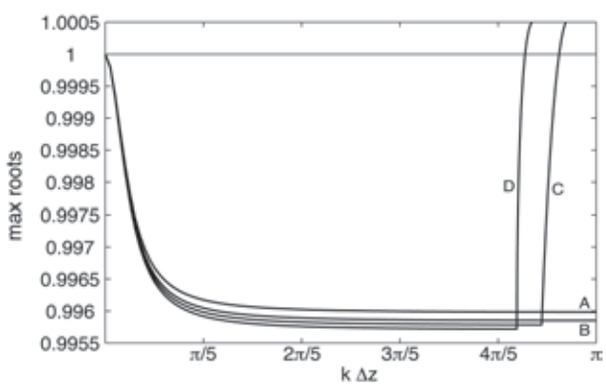
Advanced material models are gaining in importance due to today's increased computational power. At the same time, state-of-the-art research demands the investigation of such materials in very complex simulations. This creates new challenges for FDTD solvers which need to be able to successfully simulate multiple material types in one simulation.

A novel FDTD framework allows an arbitrary combination of the following material types to be present in a simulation:

- Lossy dielectrics
- Perfect metallic/magnetic conductors
- Lossy metallic conductors
- Thin conductive sheets
- Generalized dispersive media (Drude, Debye, Lorentz)
- Nonlinear media (Kerr, Raman)

The framework includes a novel stability analysis engine that finds potential stability problems due to material definitions such as unstable dispersive poles. In order to ease the use of the nonlinear media, the framework uses an estimation of the maximum field strength (saturation) inside nonlinear materials, either given by the user or based on previous simulations, to assess the stability.

Moreover, maximal and minimal wavelength for each material are computed using dispersive pole definitions and nonlinear saturation estimation to ensure adequate grid resolution and simulation setup.



Maximal roots vs wave vector times grid step of four different FDTD media (A,B,C,D) with multiple dispersive poles. If all roots are smaller than one, the FDTD update is stable. Here, the analysis detects that C and D are unstable.

State of the Art Computational SAR Averaging: Requirements and Limitations

Personnel: Tomasz Stefanski, Guillermo del Castillo; IT'IS: Nicolas Chavannes, Niels Kuster; SPEAG: Pedro Crespo

Funding: KTI 8969 PFIW-IW LOVESim

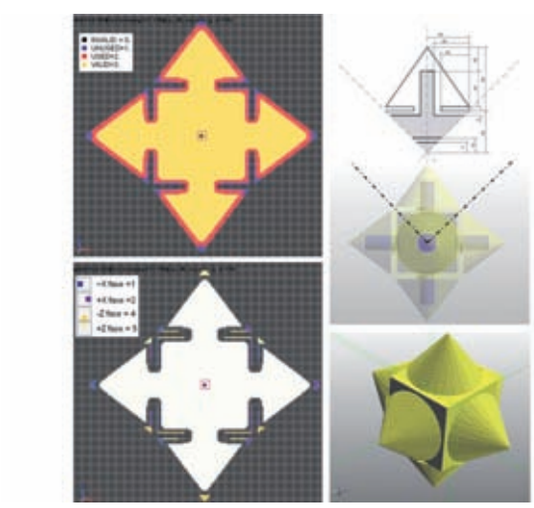
Partners: IT'IS, SPEAG, Pfisterer Holding AG

Radiation dosimetry in biological tissue is evaluated in terms of Specific Absorption Rate (SAR), expressed in W/kg. This quantity is normally not computed at a single point but rather, averaged over a volume of lossy tissue with a constant mass (typically, 1 g or 10 g). The shape of this volume is defined differently depending on the scientific or standardization group, leading to a variety averaging schemes as contiguous, spherical, adjacent and cubic, with the latter being most widely used.

SAR averaging using cubic volumes has been recently defined in the IEEE-1528.1 standard (Annex C). The choice of this shape is mainly due to historical reasons since it naturally fits into a FDTD grid. As concluded in previous works, most of the computational effort is required when the algorithm calculates the averaging volume and "grows" around a reference point.

IEEE-1528.1 introduces 2 different types of averaging procedures that adds a new level of complexity. It defines the so-called centered-volume or centered-face averaging cubes, depending on the location of the cube with respect to the reference point. This distinction introduces an additional computational burden since all voxels in the model must be dynamically labeled during averaging routine.

This study overcomes this drawback by combining efficient techniques for "volume growing" and segmentation methods that take advantage of multiprocessor architectures. This has been applied to benchmarks, proposed by IEEE, providing promising results.



Evaluation of the SAR star benchmark from IEEE-1528 with uniform grid. On the top-left image, the labels assigned to the voxels; the bottom-left image shows the center-face (colored) and center-volume locations.

High Level Automation for Numerical Device design in Industrial Environments

Personnel: IT'IS: Nicolas Chavannes, Niels Kuster;
SPEAG: Pedro Crespo, Wayne Jennings

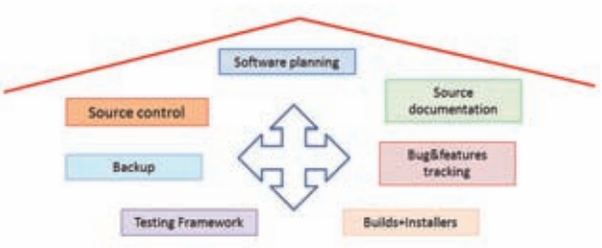
Funding: KTI 8969 PFIW-IW LOVESim

Partners: IT'IS, SPEAG, Pfisterer Holding AG

In an industrial environment, reducing the time-to-market is a key issue for the success of any product. The development of professional software for numerical simulation is no exception. Released versions of numerical packages must be ready in time and must fulfill high quality standards. These two requirements are particularly difficult to accomplish simultaneously in numerical software development. Firstly, the natural flexibility of software, when compared to hardware, produces a highly dynamic environment that is in rapid and continual flux: a method used today is not valid tomorrow. Due to this complexity, code management is error prone and cannot be tackled effectively by humans. Secondly, if the software is used to simulate engineering or medical problems, incorrect results could endanger life. This requires that the released code must fulfill the highest quality standards in terms of accuracy and efficiency.

In this work, we have designed a framework that gathers a collection of processes required for software development. Each module addresses a particular process, such as source control and bug-tracking, and should provide tools to fully, if possible, or else partially automate its development. We have investigated several open-source projects that provide professional solutions to some of these modules, selecting those that suit integration into the framework best. Some other modules, such as backup, testing, building and packing have been developed in-house using Python.

The progress and operations performed within each module during the development of the software can be monitored either via a custom interface (provided by the module itself) or through a website that gathers and centralizes all the relevant information. The result is a framework that can perform automated control and execution of complex and highly dynamic operations such as coding, testing, bug-tracking and implementation of features.



Conceptual representation of a development framework for an industrial environment.

Assessment of the SAR from Hands-Free Kits for Mobile Phones

Personnel: Sven Kuehn;
IT'IS: Eugenia Cabot, Niels Kuster

Funding: BfS

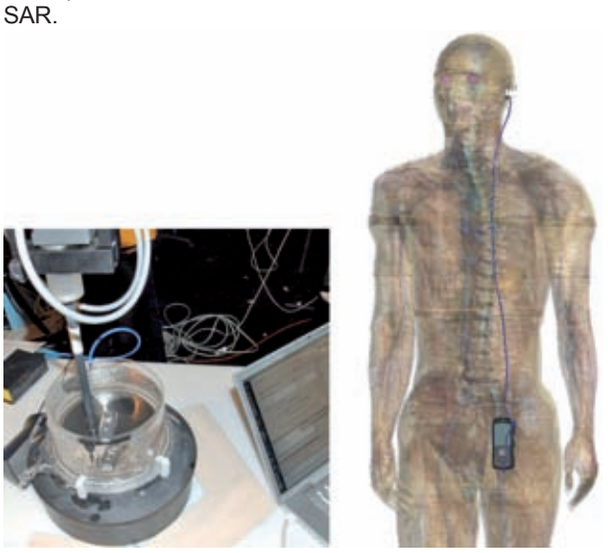
Partners: IT'IS, SPEAG

There has been debate on whether the use of hands-free kits (HFK) with mobiles phones could lead to an increased amount of absorbed radio-frequency energy in the users head. The confusion has mostly arisen due to methodically problematic studies using unrealistic compliance test scenarios. Studies that reported a higher exposure, for instance, often neglected the attenuation along the cable of wired HFKs. However, uncertainty still remains about the actual exposure when using wired and wireless HFK, and sound compliance test procedures are required.

The most important questions discussed in this study are whether separate compliance testing is required for HFK and the extent to which the use of wired and wireless HFKs can reduce human exposure.

The SAR from wired HFKs was evaluated experimentally while connected to mobile phones (GSM900/1800, UMTS1950) under maximized current coupling onto the HFK cable and various cable routing configurations along the absorbing bodies. The SAR from wireless HFKs was also measured. A novel phantom for devices that are partially surrounded by tissue has been developed. Simulations were performed for a HFK and a mobile phone being operated on anatomical whole-body models.

In conclusion, wired HFKs reduce the exposure of the head region considerably compared to the phone operated at the head. Wired HFKs may cause a localized increase in the exposure in the inner ear. Wireless HFKs show a lower SAR.



Left: SAR measurement of a wireless HFK in a novel vacuum phantom for devices partially surrounded by tissue. Right: Virtual Family Duke model with mobile phone and wired hands-free kit as used in the FDTD simulation in order to estimate human exposure in anatomically correct models.

Power Control of Multi-Band, Multi-System Mobile Phones in Real Networks

Personnel: Sven Kuehn;
IT'IS: Niels Kuster

Funding: SNF NFP57

Partners: IT'IS, UniBa

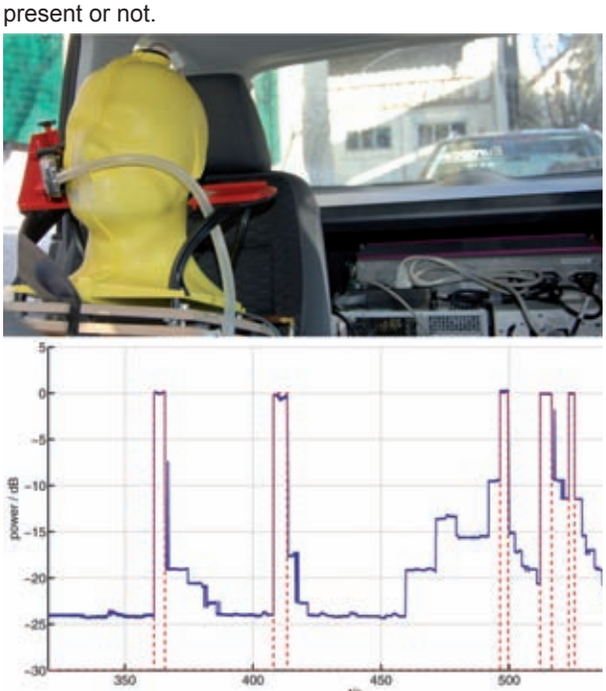
The cumulative dose of electromagnetic fields from cellular phones absorbed in the human head during usage in a network is a function of the specific absorption rate strength and distribution at maximum power level, the average power control level depending on the corresponding transmission mode and the duration of the exposure.

This study aimed at evaluating the power control behavior from multi-system mobile phones (GSM, UMTS) in real networks.

A novel mobile phone field test setup simulating realistic usage at the user's head has been developed and applied in field tests of mobile phones operated in various geographical environments. The developed system is able to measure the mobile phone output power communication band and system for any marketed mobile phone, and does not require modifications to the phone.

The collected data has been statistically evaluated with respect to communication system, usage time, frequency, and the cumulative dose of fields induced in the head.

The results show that the communication system used is the strongest predictor of the exposure. The geographical location defines whether a communication system is present or not.



Top: Developed mobile measurement system for mobile phone output power in real networks.
Bottom: Power control behavior in a GSM1800 network with peak power excursions during handovers.

Organ and CNS Tissue Evaluation of the Time-Averaged Far-Field Exposure in Various Human Body Models

Personnel: Sven Kuehn;
IT'IS: Marie-Christine Gosselin, Roxana Djafarzadeh, Marcel Zefferer, Andreas Christ, Niels Kuster;
SPEAG: Pedro Crespo-Valero

Funding: SNF NFP57

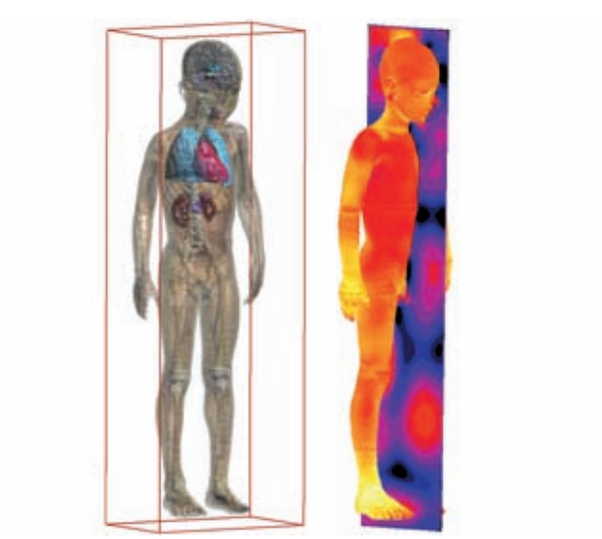
Partners: IT'IS, UniBa

In the past, epidemiologic research on possible health effects from human exposure to radio frequency (RF) electromagnetic fields (EMF) applied very simplistic exposure metrics. These metrics range from simple distance metrics, over wireless propagation modeling, to more recent work performing in-situ exposure assessments and also taking background fields into account. A correlation to induced fields, however, is missing. Since the levels of RF EMF for the considered cases are far below possible effects due to temperature increase, the only plausible metric is a correlation with functional regions, first of all the central nervous system (CNS) and then other organs of the human body.

Thus, the aim of our study was the evaluation of the tissue and functional body region specific absorption in various human body models.

We used the members of the Virtual Family for the evaluation of the absorption characteristics in various body and brain regions. We performed the simulations using the FDTD method and implemented novel region specific post-processing algorithms. We exposed the models to plane-waves incident from all major sides, simulating movement in a multi-path environment. Our evaluation covered the frequency range from 50 MHz to 6 GHz.

The results of the study provide a novel metric to estimate the everyday exposure from fixed base station transmitters taking into account brain and body regions.



Left: Virtual Family Thelonius model inside a wave source box.
Right: Thelonius model surface SAR and incident E-field view frorn a isotropic field incidence.

Correlation of the Exposure of Mobile Phones Assessed in SAM in Anatomical Human Heads

Personnel: Sven Kuehn;
IT'IS: Marie-Christine Gosselin, Marcel Zefferer, Andreas Christ, Niels Kuster

Funding: SNF NFP57

Partners: IT'IS

Epidemiologic research on possible health effects from human exposure to radio frequency electromagnetic fields from mobile phones requires scientifically sound and robust exposure metrics. Typical end-points of epidemiologic research in this field are carcinogenic effects in the tissues that are dominantly exposed. Nevertheless, the difference of the power absorption in different tissues in the head can vary strongly between different types of mobile phones. Currently, only the maximum exposure in terms of the peak spatial average SAR is reported for mobile phones during compliance testing. For epidemiologic research and for better information for health agencies and the public, it would be beneficial to also extract the head and brain region-specific exposure from the compliance scan data.

The aim of this study was to correlate the region-specific absorption in the anatomical heads of the Virtual Family to the one in the homogeneous SAM head. Virtual tissues, such as cheek, inner-ear, eye, and brain, were created in the SAM head, based on an anatomical head. The region specific absorption was assessed using an FDTD method. A brain region specific post-processing was implemented. The correlation in the region specific absorption, as well as the uncertainties and limitations of this approach were determined in the study. The region-specific evaluation will be implemented in the commercial SAR scanner DASY5 and thus become available for routine mobile phone evaluations.

Left: Numerical model of the homogeneous SAM phantom head with a mobile phone attached.
Right: Same SAM phantom with virtual head tissues and regions implemented using morphing techniques.

Hybrid SAR Analysis of Various Human Models in Front of Base Station Antennas in the Range 300 MHz to 5 GHz

Personnel: Sven Kuehn;
IT'IS: Marie-Christine Gosselin, Niels Kuster;
SPEAG: Stefan Benkler

Funding: MMF, GSMA

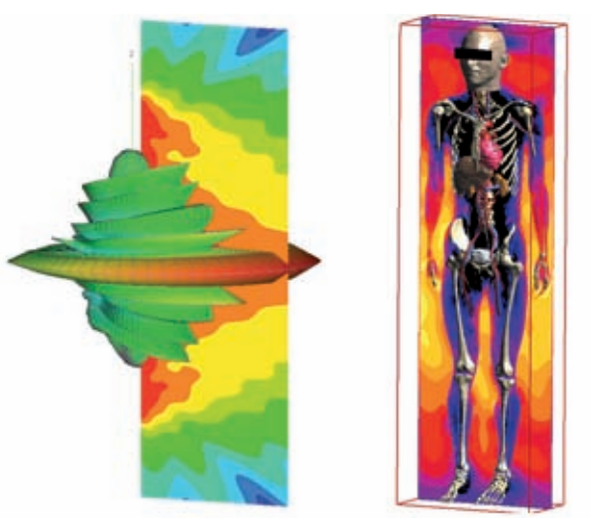
Partners: IT'IS

This study was conducted to support the International Electrotechnical Commission (IEC) in the elaboration of a new international standard. The aim was to develop estimation formulas to easily estimate the specific absorption rate (SAR) in workers in front of base station antennas and to assess the uncertainty by simulating various humans in front of generic base station antennas.

Estimation formulas for the whole-body average SAR and the peak spatial average SAR have been developed. The physical and electrical characteristics of the antennas were used, as well as a homogeneous cuboid as a representation of the human body. The estimation formulas are based on worst-case exposure considerations in order to be conservative.

Twelve different generic base station antennas were modeled and validated with FDTD and MoM for six different frequencies ranging from 300 MHz to 5 GHz. Three human models of the Virtual Family were used: an adult male, an adult female, and a 6-year-old boy. The models were placed at six distances from every antenna, ranging from 10 mm to 3000 mm. The whole-body average SAR and peak spatial average SAR were evaluated. To reduce the computational demands a new generalized Huygens box method was implemented as well as a new algorithm for the fast extraction of the peak spatial average SAR in computationally large models.

The estimation formulas were validated against simulation results and have been implemented in an IEC standard.



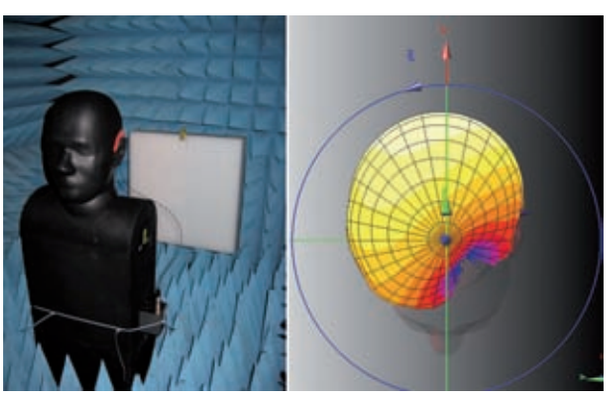
E-field and far-field pattern created by one antenna at 2.1 GHz; E-field around and inside the VFM model.

Instrumentation and Procedure for Characterisation and Optimisation of the RF Link of Hearing Aids

Personnel: Jagadish Nadakuduti;
IT'IS: Myles Capstick, Jagadish Nadakuduti, Vick Chen, Roxana Djafarzadeh, Niels Kuster

Partners: IT'IS, Phonak Communications

This project has conducted the research and data analysis required to determine the size and shape of a measurement phantom head for use with hearing instruments that closely represents the 95th percentile of North American and European populations. Detailed investigations were performed to determine the effect of the ear pinna size on the communications links and a phantom ear was designed with an ear canal suitable for Phonak ITE hearing instruments (HI). CAD files were developed for the production of moulds to allow fabrication of a head with the correct physical size. Most available measurement heads for electromagnetic evaluations have a non-conductive plastic shell filled with a tissue simulating liquid or gel, this configuration cannot simulate the close contact between HI and the lossy head and pinna. Considerable effort went into developing carbon loaded elastomers with appropriate dielectric and loss parameters from which to make the entire head. Methods were developed to make a measurement system with RF transparent connections ensuring that the physical foot print of the HI was not extended perturbing the performance. Small reference receivers and transmitters were manufactured for a validation system which, in conjunction with an independent reference signal recovery method, can be employed to provide reference path loss measurements. Additionally, a measurement protocol was developed that could remove many of the uncertainties from the system by employing a differential technique.



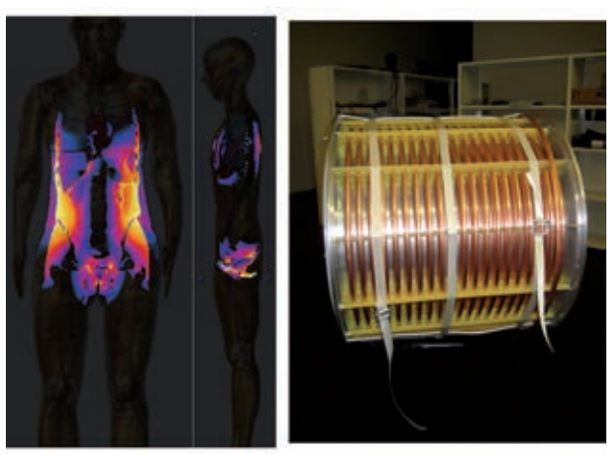
Phantom head and measurement system devices and a simulated hearing instrument radiation pattern.

Injectable Nanocomposite Local Hyperthermia

Personnel: Jagadish Nadakuduti;
IT'IS: Myles Capstick, Niels Kuster

Partners: IT'IS, Antia Therapeutics, EPFL, Uni Geneva

The application of superparamagnetic iron oxide nanoparticles (SPION) for diagnostic procedures has gained wide acceptance in radiology practice (as MRI contrast agent), but therapeutic applications are still under investigation. Such applications have exploited two major advantages of iron oxides: their low toxicity to human beings and their high magnetization. For example, the magnetization is used to target drugs to the tumor area through external static magnetic fields. If exposed to an alternating magnetic field, the harmless iron oxide particles become powerful heat sources by transforming the energy from the magnetic field into heat. Magnetic hyperthermia involves the generation of temperatures up to 43°–48°C with superparamagnetic iron oxides as particles. The treatment works by rendering cells more sensitive to radiation therapy or chemotherapy. The heating of magnetic oxides in an alternating-current magnetic field is due mainly to loss processes during reorientation of the magnetization or frictional losses with particle rotations in low-viscous environments. A large specific heating power is desirable to reduce the material amount to be administered to the patient. Here the IT'IS foundation is performing modelling and human dosimetry of magnetic field applicators to determine the limits of safe operation. Magnetic field applicators are being designed and optimised to provide high field strengths with reduced heating of normal tissues. A second strand is the development of highly efficient switch mode amplifiers for the generation of the magnetic fields required for nano particle heating.



Vitrual family Female exposed to 140 kHz magnetic field and a prototype magnetic field applicator.

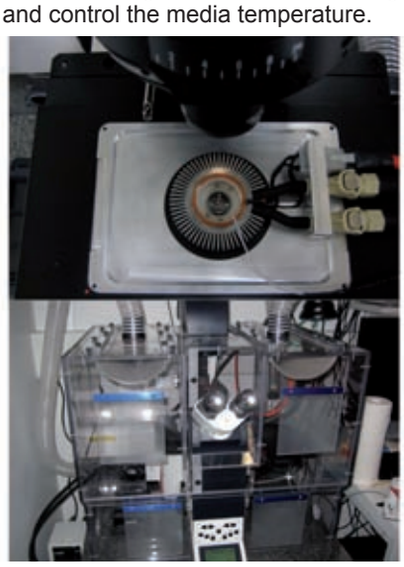
Live Cell Imaging During EMF Exposure

Personnel: Sven Kuehn;
IT'IS: Myles Capstick, Albert Romann, Andreas Christ. Niels Kuster

Funding: SNF NFP57

Partners: IT'IS, UniBa

A considerable variety of exposure setups have been used in the past to investigate the biological effects of the exposure to extremely low frequency (ELF) magnetic fields. Common to all these systems is that the cells are exposed to particular field conditions for defined time periods and the analysis is performed post exposure. The objective of this project was the development of a miniature ELF exposure system that can be integrated with a microscope system, thus enabling live cell imaging and other state of the art microscopic techniques including during the ELF exposure. The setup was optimized for uniform B-field exposure and minimum non-B-field differences between the exposure and sham. It is expected that this system will be an effective tool to study possible athermal interaction mechanisms to EMF. The setup comprises ELF magnetic field coils integrated into a live cell imaging chamber in such a way that it met the requirements for exposure setups in health risk assessment. In addition to the chamber, the setup includes a control computer, a signal source and instrumentation for exposure control and recording of the experimental parameters. The design achieves excellent homogeneity ensuring equal exposure of all cells whatever their location. The experimental setup allows for a frequency range up to several kHz with either pure sinusoidal excitation or arbitrary signal shapes. A temperature controlled water bath circulates water through a heat sinking element and a small temperature sensor is integrated into the live imaging cell to measure and control the media temperature.



Exposure cell for live cell imaging integrated into the conformal imaging microscope.

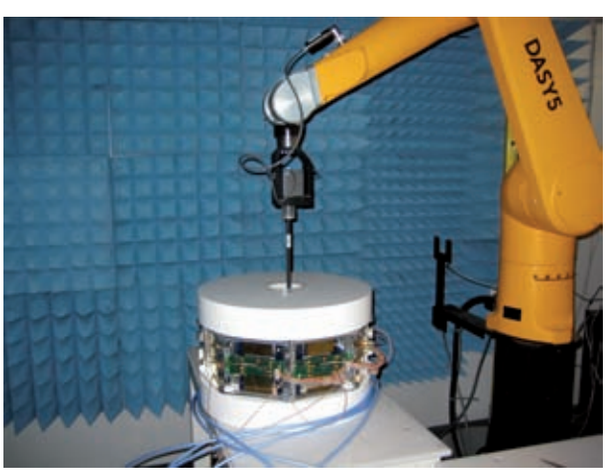
Hyperthermia System Hardware for the Treatment of Neck and Head Tumors Hearing Aids

Personnel: Chung-Huan Li;
IT'IS: Myles Capstick, Esra Neufeld, Niels Kuster

Funding: HYCUNEHT

Partners: IT'IS, SPEAG, Erasmus Medical Centre

The objective is to develop a novel, next-generation system for regional hyperthermia to reliably control temperature elevations in cancerous tissues of the head and neck region, while the surrounding tissues remains below the threshold for adverse effects using an innovative ring applicator. Central to the development is a user-friendly and comprehensive planning tool, enabling physicians to perform routine, safe and effective treatment applications. The clinical utility of the prototype is being assessed at one of the leading hyperthermia centres in the world. This aspect of the project focuses on the power and control electronics system architecture that will allow great confidence that the hyperthermia application delivered to a particular patient is that which was planned. To enable this, a new paradigm for signal monitoring has been developed that directly senses the field radiated from each applicator element thus removing an important source of uncertainty. This monitoring scheme provides enhanced confidence in applied signals and better closed loop control, ensuring patient safety. In addition all the antennas for the phased array applicator have been designed in such a way that they are completely planar with the dimensions defined by photolithographic techniques, ensuring repeatability and consistency. We have also developed microprocessor controllable agile signal sources and power amplifiers for excitation of the phased array that are both cost effective and accurate and when used in combination with the signal monitoring, provide a flexible signal generation frame work.



Testing using DASY 5.

A Radio Frequency Radiation Reverberation Chamber Exposure System for Rodents Hearing Aids

Personnel: Sven Kuehn;
IT'IS: Myles Capstick, Yijian Gong, Niels Kuster

Funding: NIEHS

Partners: NIEHS, IITRI, NIST

Modern society clearly values the role science plays in improving our daily lives. However, society also demands that science provides knowledge about the risks to its citizens posed by those industrial processes, new technologies, improved food, improved drugs, changed life-styles, etc. Science also must play a critical role in developing and implementing strategies to control any risks that are deemed unacceptable. The tool science has developed to satisfy these requirements is called 'risk assessment.' Risk assessment involves the use of scientific evidence to define health effects from the exposure of individuals or populations to hazardous chemicals, physical agents and/or hazardous situations. The scientific evidence must always be underpinned by data and established facts that identify the toxicity and the magnitude of the risk for a given exposure as a function of susceptibilities in the population.

The National Toxicology Program in the USA issued a study to evaluate the potential toxicity and carcinogenicity of cell phone RF radiation in laboratory animals. The system to do these evaluations had been designed, developed, manufactured, installed and characterized by the IT'IS Foundation. The exposure facility for the large scale animal study was installed at IITRI in Chicago in the summer of 2007. The current status is that the results of the thermal pilot study have been reported and based on these findings the prechronic study exposure levels have been defined. The prechronic study will be performed in 2010.

NIEHS, National toxicology program radio frequency exposure facility manufactured and installed by the IT'IS foundation.

System to Study CNS Responses to Radiofrequency ELF Modulation versus Low Frequency Magnetic Exposures

Personnel: Sven Kühn;
IBT: Manuel Murbach;
IT'IS: Maria Christopoulou, Sven Kühn, Esra Neufeld, Andreas Christ, Niels Kuster;
UniZ: Peter Achermann

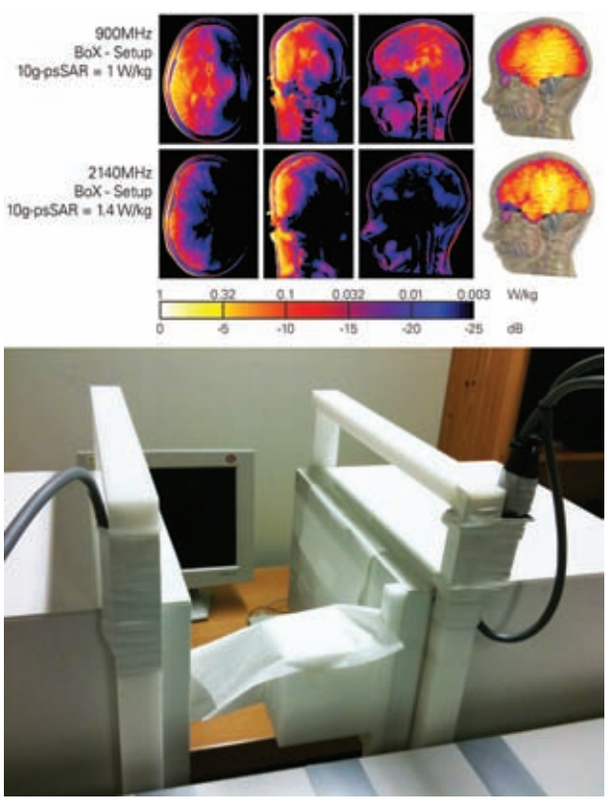
Funding: SNF NFP57

Partners: IT'IS, SPEAG, Uni Zurich

There is increasing evidence that pulse-modulated radio frequency electromagnetic fields (RF EMF), such as those emitted by mobile phones, can alter brain physiology. Changes in EEG, regional cerebral blood flow (rCBF) and cognitive function have been reported.

Current studies about the site of interaction as well as the interaction mechanism have been enhanced by comparing RF exposures to low frequency magnetic field (MF) exposures in the human cortex. The magnetic signal is identical to the RF modulation signal. Similar physiological responses could indicate demodulation abilities of the brain tissues.

The novel exposure system (BoX) incorporates both 900 MHz and 2.14 GHz RF, as well as MF exposures in a double blind manner. Subjects are prevented from having any knowledge about the actual exposure condition.



SAR distributions for 900 MHz and 2.14 GHz, resulting in different penetration depths. BoX Exposure System with Helmholtz coils for magnetic field.

RF Exposure & Risk Evaluations for Patients/Workers within MRI Environments

Personnel: Sven Kühn;
IT'IS: Manuel Murbach, Esra Neufeld, Andreas Christ, Michael Oberle, Niels Kuster

Funding: CTI 9193.1 PFLS-LS

Partners: IT'IS, IBT-ETHZ, Philips, Siemens, Erasmus Medical Center, INTEC, Uni Athens, Charité Berlin, FDA, SPEAG, Zurich MedTech

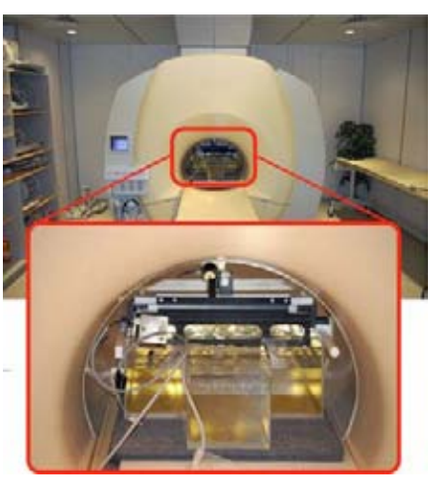
The purpose of this project is to reduce MRI scan times, optimize image quality at lower costs, and increase the safety of patients (with and without implants) and MRI personnel.

The project started with the classification of MRI field generating units. Units from all major manufacturers (Philips, Siemens, GE) have been included.

The completion of anatomical models is one of the key tasks, as it will provide the necessary information to cover the entire patient population for electromagnetic simulations. FDTD (SEMCAD) solvers such as the temperature solver, field optimizer, poser, as well as specific algorithms for tissue damage modeling have been extended or specifically developed for this project.

The development of experimental data/TCAD tools for field and temperature measurements was necessary for accurate measurements within the EM hostile MR environment.

The project results will provide important benefits and economies for society as a whole, including patients and hospitals as a result of better and safer diagnostics and lower costs.



Phantom and SAR measurement equipment placed into an MR scanner.

Exposure of the Fetus to ELF and RF fields in uncontrolled environments

Personnel: Jagadish Nadakuduti;
IT'IS: Andreas Christ, Barbara Bühlmann, Nicolas Chavannes, Stefan Benkler, Marcel Zefferer, Niels Kuster

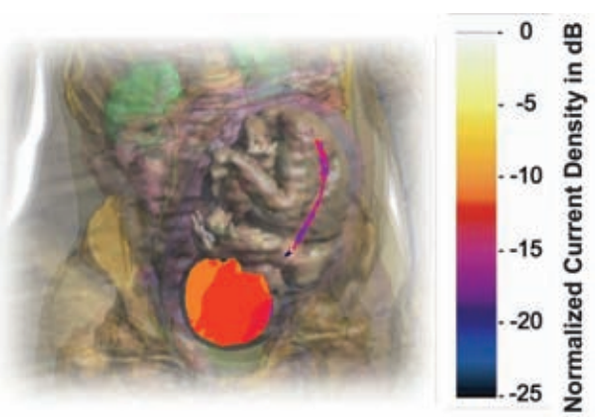
Funding: SNF NFP57

Partners: IT'IS

Latest advances in the anatomical modeling of the human body and in RF and ELF simulation tools permit the efficient analysis of the exposure of the fetus inside the mother's womb taking into account a large number of exposure situations in uncontrolled environments, i.e. during day-to-day life. The WHO has identified a lack of knowledge in this area, and recognizes the need for research.

Within this project, highly detailed anatomical whole body models of pregnant women were developed in the 3rd, 7th and 9th gestational month. The models are based on magnetic resonance images and were complemented by different literature sources. The models are simulated with cell resolutions of less than 1 mm^3. Mesh sizes of several ten million cells can be treated numerically.

The models are exposed to a matrix of generic sources of ELF magnetic fields and RF electromagnetic fields. The matrix can be arranged such that a large number of different exposure scenarios can be evaluated efficiently by superposition of the vector field components. The different exposure scenarios include electronic article surveillance systems, induction cooker hobs, high voltage transmission lines and different personal communication devices operating in the close environment of the body. First results show that the exposure of the fetus can exceed the basic restrictions for the occupational exposure limits.



Normalized current density in the brain and the spinal cord of the fetus exposed to a magnetic field source in its close environment.

Exposure to ELF Fields from Induction Cookers in Professional Environments

Personnel: Jagadish Nadakuduti;
IT'IS: Marcel Zefferer, Niels Kuster
SPEAG: Stefan Benkler
SECO: Rene Guldimann

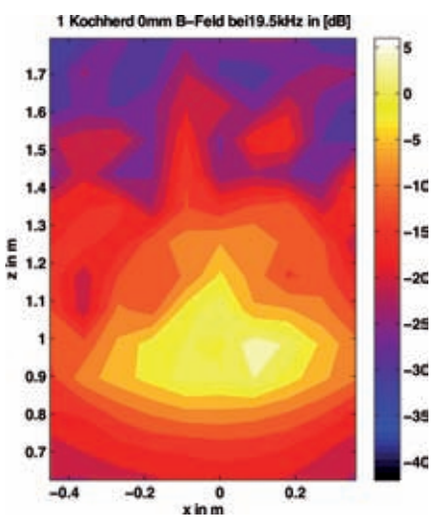
Funding: BAG

Partners: IT'IS, SECO

Previous studies have shown that the present standards for the evaluation of the B-field strength of induction cooking appliances suffer from shortcomings which can lead to potentially significant violation of the exposure of workers in the immediate environment of these devices. For the assessment of the workers' exposure, the magnetic fields of a large series of induction cookers are measured considering different loading conditions. In a second step, the exposure is modeled using the numerical simulation platform SEMCAD X and a set of anatomical high resolution models.

The incident magnetic field of the different cookers is modeled using generic current loops and matched appropriately considering amplitude and spatial distribution of the measured data. For the calculation of the induced current densities, anatomical body models of both sexes ranging from a 14-year-old male (1.65 m, 50 kg) to an obese adult model (1.79 m, 120 kg) are used. The limbs of the models is articulated in typical postures during work in a kitchen.

The results are evaluated with respect to current guidelines on basic restrictions. Improved methods and standardized procedures for the demonstration of induction cookers with the basic restrictions will be developed.



B-field distribution immediately in the front of a professional induction cook top.

Testing the Risk of Tissue Heating of a Generic Brain Stimulator when Exposed to the RF Fields of MR Scanners

Personnel: Sven Kühn;
IT'IS: Eugenia Cabot, Andreas Christ, Mark Douglas, Niels Kuster;
Imricor: Tom Lloyd, Greg Stenzel, Steve Wedan;
FDA: Wolfgang Kainz

Funding: MDRF

Partners: IT'IS, Imricor, FDA

Within the health care and the medical device industry, there is great interest in the evaluation of the risks of Magnetic Resonance (MR) examinations of patients wearing active implantable medical devices (AIMDs). Severe injuries can arise from unintended tissue heating caused by the radio frequency (RF) currents induced on the conducting parts of the implants. Because of the intricate spatial distribution of tissues in the body and their associated dielectric parameters, the E-fields incident on the implant are not easy to quantify. In order to arrive at a conservative and reproducible procedure for the evaluation of the possible risks for the patient, a joint working group of the ISO and the IEC is developing a four-tiered technical specification for implant safety testing for patients undergoing MR exams. At the most accurate tier, the detailed modeling of the implant is required in anatomical body models using numerical techniques for the quantification of the induced tissue heating. The objective of this study is to demonstrate the practicability of the approach by evaluating a generic brain stimulator and to quantify the uncertainty of the temperature increase induced in the patient.

A generic implant of a brain stimulator has been developed. Its leads are designed to yield a reduction in heating by 10 dB and 20 dB with respect to a single straight lead. For the simulations, an electrically equivalent subcell model using lumped elements is developed. The numerical model is validated experimentally using the Medical Implant Test System MITS1.5 (Zurich MedTech). Both the deposited RF energy at the lead tips and the induced temperature increase are evaluated numerically using the FDTD method. The evaluation is complemented by the numerical and experimental evaluation of the induced SAR and temperature rise of the implant.

Generic brain stimulator inserted into the adult male model.

Development of an Anatomical Whole Body Model of an Obese Adult for Dosimetric Simulations

Personnel: Sven Kühn;
IT'IS: Marcel Zefferer, Andreas Christ, Barbara Bühlmann, Niels Kuster

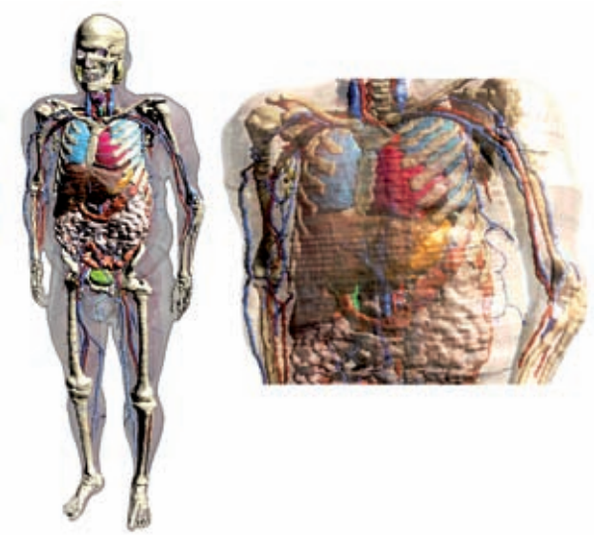
Funding: Zurich MedTech

Partners: IT'IS

Several whole body models of adults and children have been developed by different research groups. The general objective of the development of these models was to create a sample of the population which is representative for most individuals. Body height and weight of these models were therefore chosen according to statistical averages. On the other hand, the actual representativeness of such models cannot be assessed by evaluating a group of models with similar features. The variability must be quantified by including extreme cases, such as highly obese models.

For the dosimetric assessment of the exposure to electromagnetic fields, a model with a high body fat content is of particular interest because the dielectric properties of fat tissue differ distinctly from those of most other soft tissues. The realistic representation of the fat tissue distribution in the body of the model is of highest importance, because the dielectric contrasts are likely to cause hot spots, e.g. because of standing wave effects.

In order to overcome this gap, images of a 37-year-old volunteer of height 1.78 m and body mass 120 kg have been obtained using magnetic resonance tomography, and a highly detailed CAD model has been reconstructed based on this image set. The model distinguishes about 80 different tissues and organs. The limbs of the model can be articulated using the software SEMCAD X. The application range of the model encompasses whole and partial body SAR assessment during exposure to any kind of electromagnetic field sources or the assessment of X-ray doses in radiation physics.



Anatomical model of an obese adult.

Exposure of Children to ELF and RF fields in uncontrolled environments

Personnel: Sven Kühn;
IT'IS: Andreas Christ, Marcel Zefferer, Esra Neufeld, Niels Kuster;
EMC: Jurriaan Bakker, Gerard van Rhoon

Funding: ZonMW

Partners: IT'IS, Erasmus Medical Center

The majority of present studies on the exposure of children to electromagnetic fields deals with the absorption of cell phone radiation in the head or whole body absorption under simple plane wave conditions. Within the framework of this project, the exposure of children to electromagnetic fields in uncontrolled environments is analyzed considering frequencies from the kHz range to the lower GHz bands. Particular attention will be paid to anatomical differences between adults and children and different exposure patterns: for exposure in the kHz range, magnetic fields from induction cooker hobs have their maximum field strength at the height of the heads of children. Passers-by are usually exposed to the near-field of the transmitters of electronic article surveillance systems, and because of their shorter bodies, a strongly different field distribution can be expected in children. These issues must be considered for the accurate modeling of the exposure and require anatomically correct body models. In the frequency bands in the GHz range, which are used by modern short range communication devices, such as mobile phones or laptop computers with wireless data links, the wavelengths are in the order of magnitude of the dimensions of the head or exposed parts of the body. For the accurate simulation of the electromagnetic field distribution in the body considering all anatomical characteristics, different anatomical models have been developed which correctly represent the size and shape of children of different age groups. The simulation of the exposure to the field sources described above will permit the quantification of the SAR and the induced thermal load in the bodies of children.

Anatomical whole body models of children between five and 14 years of age.

Education Program

Student Semester and Master Projects

Coordinator:

Norbert Felber

Teaching microelectronics is one of the core activities of the Integrated Systems Laboratory. Shortly after the laboratory was founded in 1986, it started to offer projects in IC design to master students (during the 7th semester of the studies; in the following, the term “student” is used for students in the Master Course – 7th to 10th semester). Probably as the first European university, ETH Zürich financed the fabrication of student chips. This gave students the opportunity to carry out a VLSI design project from the specification to the test of their own silicon chips. Still today, many of the semester projects at IIS are in practical chip design, and many Master projects include the realization of integrated circuits or the development of components as contribution to research ASICs. Since the first VLSI course offered by IIS, around 580 engineering students have had the chance of designing real silicon. During times of a prospering market, but also during the periodic low-phases, our students had all the chances of finding jobs in- and outside Switzerland. The recent crisis of the electronics industry however, and its consequences to many microelectronics companies in Switzerland, led to a lower interest of the students in VLSI education and projects, but also in the other microelectronics-related fields of our lab, which is mirrored in lower numbers of student projects.

Education in Microelectronics

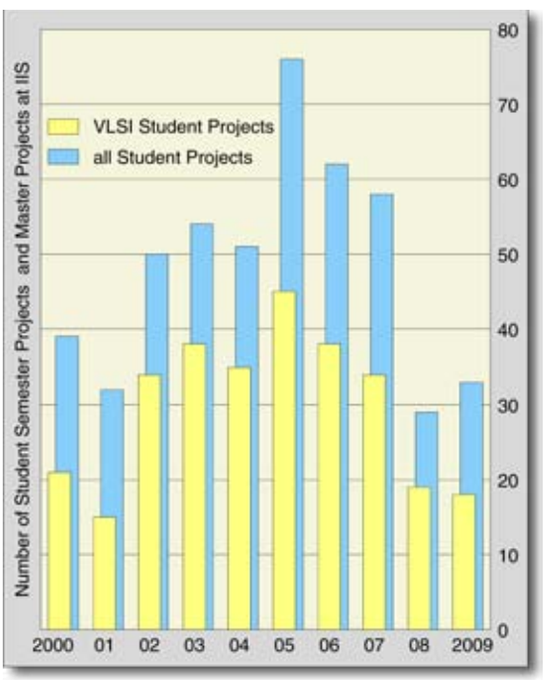
During the first four semesters, students are motivated towards microelectronics by several PPS (Practicals, Projects, Seminars) (http://www.iis.ee.ethz.ch/stud_area/pps.en.html). In semester 5 and 6, practical training (Fachpraktika, http://www.iis.ee.ethz.ch/stud_area/fachpraktika.en.html) offered by IIS aim at the same goal.

The three VLSI lectures from the 6th to the 8th semester, illustrated in the figure on page 111 and described on pages 113ff, form the main block in microelectronics education by the Integrated Systems Laboratory. Students who want to further deepen their experience in microelectronics often choose a Master’s thesis in the framework of a research project of IIS as culmination of their education. Some then stay in these research fields for a PhD thesis.

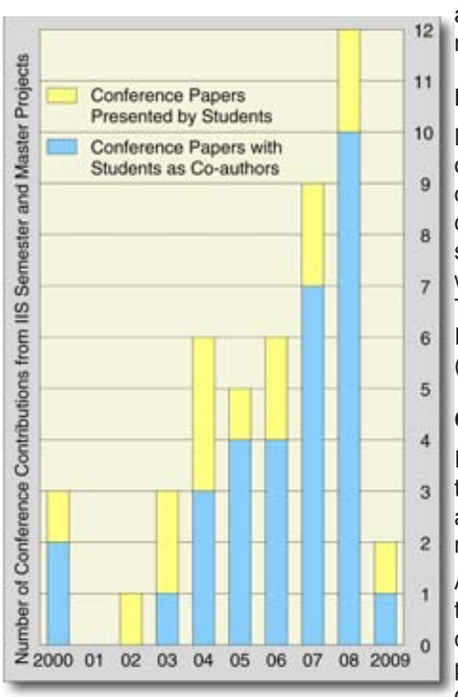
ASIC Design Projects

Students who have decided to realize an integrated circuit will learn a professional design flow with the same tools as used in research and by our main industry partners. They realize an often challenging and complex project. Despite the hard work with many traps and complications, almost all chips finally work as intended.

During the 14 weeks of a semester project, the design students put ‘official’ 50 % of their work load into the realization of the chip, often considerably more. First-time-right digital ICs of industrial complexity level often result: The ones from 2009 are shown on the next page. This is only possible due to the sound VLSI education and an excellent support for design and test offered by the PhD students of our Laboratory and the Microelectronics Design Center of the Department of Information Technology and Electrical Engineering (see pages 121ff and http://dz.ee.ethz.ch).



Student projects at IIS during the last ten years. The yellow bars indicate the number of students which did a digital VLSI project during the indicated year. The blue bars include also the semester and master projects in the other research groups of IIS.



Conference contributions by students from semester and master projects at IIS.

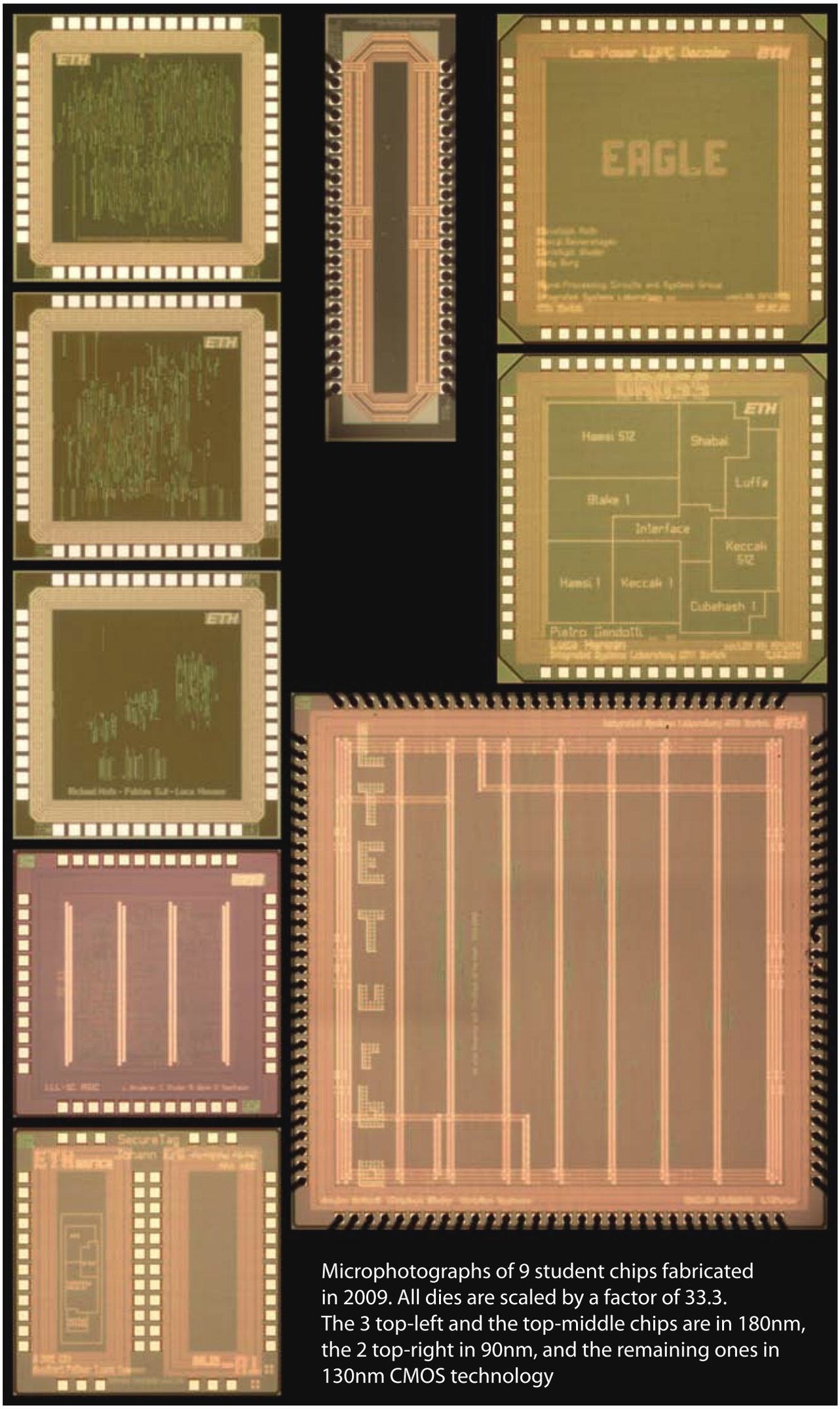
Further Student Projects at IIS

Next to digital ASIC design – mostly for signal-processing tasks –, students are offered projects in HW and SW system design, as well as in the fields of all other research groups of IIS and IT’IS. This regards analog and mixed-signal IC design, TCAD tool development and applications, physical characterization of semiconductor devices, optoelectronics device development and simulation, as well as tool, measurement and experiment contributions in bio-electromagnetics. The graphics above gives an overview over the number of student projects at IIS (blue bars) during the last ten years with emphasis to VLSI student projects (yellow bars).

Organization of this Chapter

In the following pages, student projects are reported in the order mentioned in the paragraph above. A special case are some student projects which are direct and important contributions to research projects. This work is included in the corresponding research sections on pages 33 (right), 35 (left), 41 (right), 43 (left).

As a last remark, it is worth to mention the student papers of some of the projects that have been accepted in international conferences and presented by the students as their first contribution to the research community. In the header of the project descriptions, references to the student’s publications on pages 125ff are given. The figure to the left illustrates the development of the number of papers with major student contributions.



Microphotographs of 9 student chips fabricated in 2009. All dies are scaled by a factor of 33.3. The 3 top-left and the top-middle chips are in 180nm, the 2 top-right in 90nm, and the remaining ones in 130nm CMOS technology

Synchronization-Parameter Estimation for Wireless Multi-User MIMO-OFDM Testbed

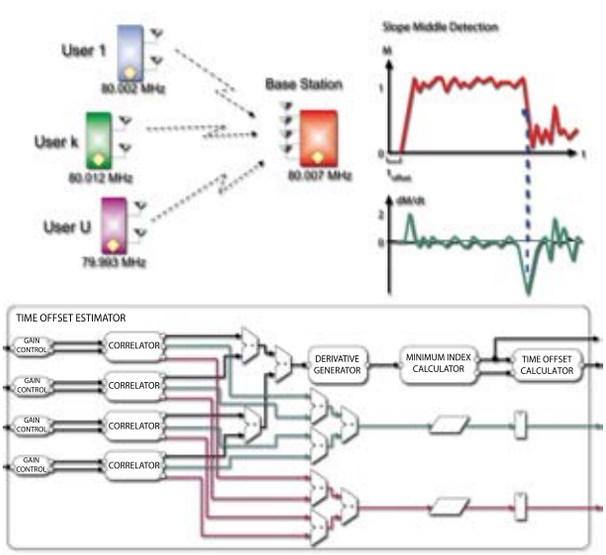
Personnel: Michael Müri;
Assistants: Markus Wenk,
Patrick Mächler

Thesis: Semester Thesis

Multi-user MIMO-OFDM communication needs a different concept for time- and frequency-offset synchronization between users and base-station compared to single-user MIMO-OFDM communication. Each user's MIMO-OFDM terminal is equipped with its own local clock source. In order to communicate with different users simultaneously, each terminal must synchronize on a common clock, e.g., the clock of the base station. Therefore, offset compensation must be carried out in the transmitter.

In this project, different algorithms for synchronization-parameter estimation were revisited and evaluated with real-world data on the MIMO-OFDM testbed. The considered synchronization parameters are carrier frequency offset (frequency difference between transmitter and receiver) and time offset (frame start). The most promising algorithm for frequency- and time-offset estimation was identified with Matlab simulations on real-world data recorded on the testbed, and was afterwards implemented in VHDL for the MIMO-OFDM testbed.

The realized implementation is based on the Schmidl-Cox algorithm for frequency- and time-offset estimation. For the time-offset estimation, the edge of the correlation function was detected by computing the derivative. Then, the maximum value of the filtered derivative is taken for the computation of the time offset. A simplification of the derivative function allowed to reduce circuit complexity.



Top left: In multi-user MIMO communication, new concepts are required for time- and frequency-offset estimation and compensation. Top right: Edge detection on metric function. Bottom: Block diagram for time-offset estimation.

Noise-Whitening Processor for MIMO Communication

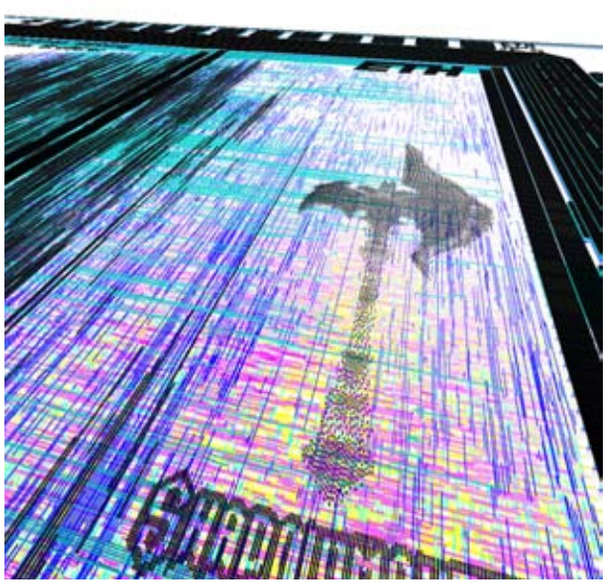
Personnel: Chai Yuning, Manuel Widmer;
Assistants: Christian Senning, Lukas Bruderer

Thesis: Semester Thesis

In state-of-the-art MIMO wireless links, thermal noise is introduced into the transmit and the receive chain. Recently, measurements have shown that transmit-side noise can not be neglected since the assumption of spatially uncorrelated noise at the receiver does no longer hold. Spatially-colored noise has detrimental effects on the error-rate performance of certain (near-) maximum-likelihood decoders (e.g., sphere decoder (SD) and K-best decoder).

The goal of this project was to design the preprocessing stage with noise whitening filter computation for SD-based detectors. Recently, it was suggested that the computation of the whitening filter for the colored noise can be efficiently implemented by a regularized QR decomposition, and two complex-valued matrix multiplications. These three steps have to be done additionally to a sorted QR decomposition of the equivalent channel (i.e., whitened channel) required for the detector. To accommodate the necessary preprocessing steps, a processor architecture capable of QR decomposition based on the modified Gram-Schmidt algorithm was realized.

The design was implemented in a 180 nm (1P/6M) CMOS process and occupies 79 kGE. The resulting ASIC operates at a maximum clock speed of 270 MHz while achieving a sustained throughput of 0.6 million complex-valued 4x4-dimensional channel matrices per second.



Raytraced 3-dimensional view on the GDSII layer information of the implemented noise-whitening processor for MIMO communication systems.

Orthogonal Matching Pursuit for Sparse Channel Estimation

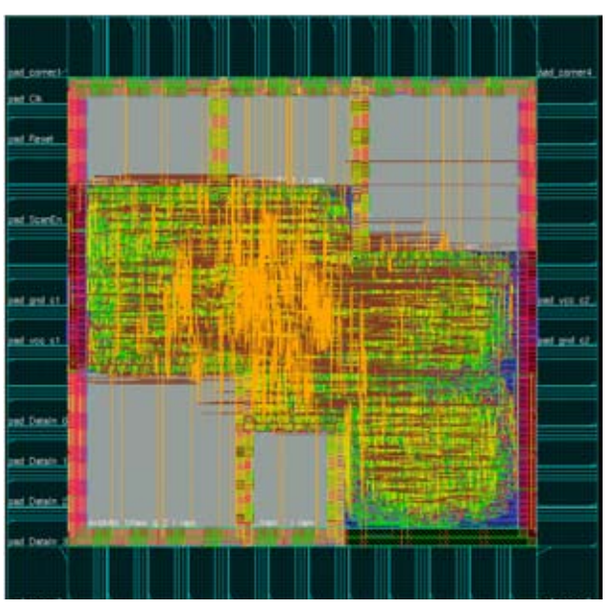
Personnel: Benjamin Sporrer, Sebastian Steiner;
Assistants: Patrick Mächler,
Pierre Greisen

Thesis: Semester Thesis

Broadband wireless channels often show sparse impulse responses and the theory of compressed sensing (CS) allows to exploit this sparsity. In the case of the upcoming LTE standard, CS improves the quality of the channel estimation compared to least-squares estimation.

The goal of this semester thesis was to implement part of the orthogonal matching pursuit (OMP) algorithm for sparse channel estimation. OMP belongs to the class of greedy algorithms, which approximate the ideal solution of the sparse reconstruction problem by iterative processing. OMP extends the more simple matching pursuit algorithm by a least squares optimization step. This additional step leads to better performance and convergence with fewer iterations, which means that not more than one iteration per non-zero component of the sampled impulse response must be performed.

The modified Gram-Schmidt algorithm was found to be the most efficient candidate to perform the necessary QR decomposition. The Gram-Schmidt QR decomposition allows to solve the least squares problem for very tall matrices (this implementation works for matrix dimensions of up to 200x10, which covers 10 MHz LTE channels with up to 10 reflections). The least squares minimization implemented in this work, combined with the functionality of the gradient pursuit implementation from another semester thesis, will result in a full OMP implementation.



ASIC layout of the least squares optimization algorithm for OMP sparse channel estimation, implemented in a 180 nm CMOS technology.

Gradient Pursuit for Sparse Channel Estimation

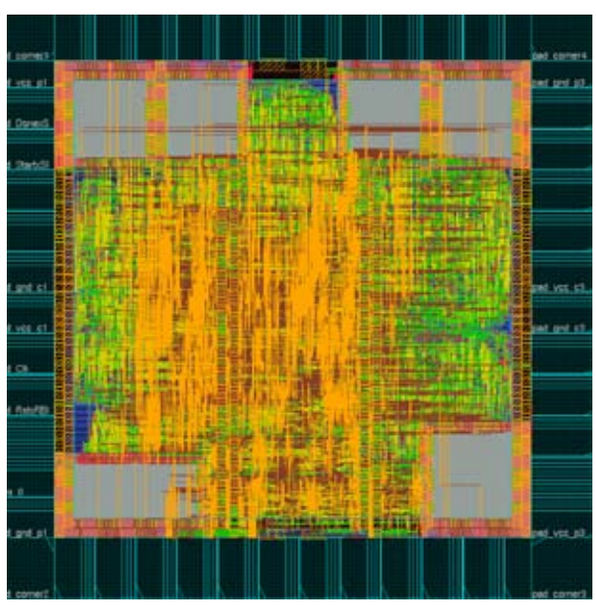
Personnel: Fabian Huber;
Assistants: Patrick Mächler,
Pierre Greisen

Thesis: Semester Thesis

Gradient pursuit (GP) is a greedy algorithm which is able to extract the sparse structure of broadband channel impulse responses from given measurements. GP fills the gap between the computationally simple, but only slowly converging matching pursuit (MP) and the fast converging, but more complex orthogonal matching pursuit (OMP). GP can almost achieve the performance of OMP, while its computational complexity is still comparable to MP.

In this project, the GP algorithm for estimating a sparse channel impulse response was implemented. This algorithm selects one new channel tap in each iteration. Unlike MP, not only the newly selected tap is considered, but all previously selected taps are updated. This is done by computing an optimization direction in the vector space spanned by all previously chosen taps. The benefit of GP compared to OMP is the easier computation of the optimization step.

The hardware implementation uses four parallel multiply-and-accumulate units. This is possible since the GP algorithm is inherently qualified for parallel processing. As the structure is very similar to MP, the design was based on an MP implementation. Besides new control logic and new memories, a divider unit was necessary. To mitigate the high dynamic-range requirements in the divider, pseudo-floating-point structures were added to the divider.



ASIC layout of the gradient pursuit algorithm for sparse channel estimation, implemented in 180 nm CMOS technology.

Hardware-Efficient Matrix Decomposition Processor for MIMO Communication

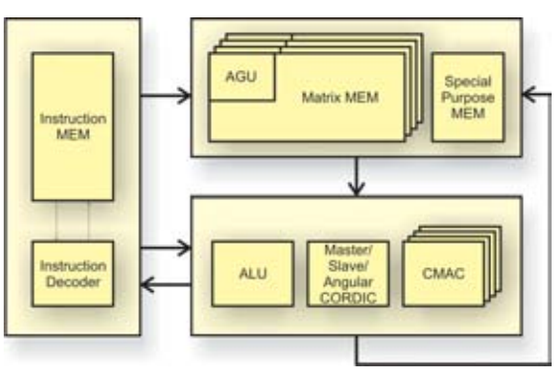
Personnel: Mu Li;
Assistants: Christian Senning, Patrick Maechler

Thesis: Master Thesis

Several multiple-input multiple-output (MIMO) decoders need to compute a decomposition of the channel matrix in a pre-processing step. Examples of such decompositions are the QR decomposition or the singular value decomposition (SVD). Since their computations show similar structures, a processor-like architecture can be designed which is capable of performing all decompositions of interest. Such a processor consists of a number of specialized computation units, a matrix storage, and an instruction code memory. The computation units include a master-slave CORDIC, a complex-valued multiply and accumulate (CMAC) unit, and a general-purpose aritthmetic logic unit (ALU). In a previous implementation of this processor, each of these units were instantiated once which allows computing one data word per cycle.

However, the matrix decomposition algorithms are well suited for parallel processing and could benefit from multiple instances of processing units. The goal of this work was to increase the efficiency in terms of AT product by exploiting this parallelism. Thus, four parallel CMACs were implemented, which was found to be the most efficient configuration to decompose 4x4 matrices. Their implementation required also a fourfold increased memory bandwidth, which was achieved by replacing the RAM-based matrix storage blocks with flip-flop arrays. As a consequence, also more elaborate address generation units had to be designed.

The resulting design requires more than twice the silicon area, but the AT product is enhanced to 72.5% of the original implementation.



Block diagram of the optimized matrix decomposition processor with vector addressing and multiple CMACs.

VLSI Implementation of the SHA-3 Candidates Shabal and CubeHash

Personnel: Markus Bernet;
Assistant: Luca Henzen

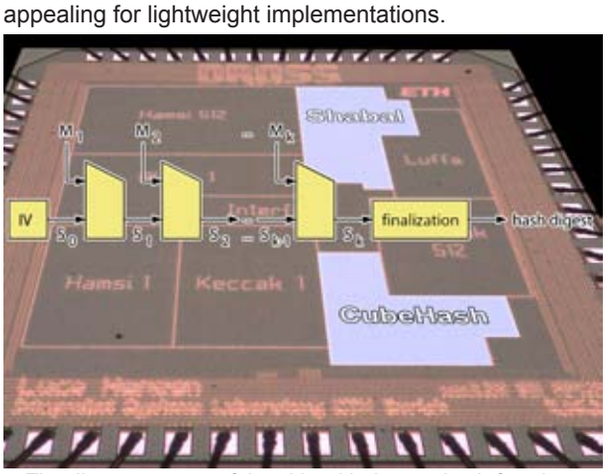
Thesis: Semester Thesis

References: [D2]

In 2005, relatively efficient methods for finding collisions in the former standard SHA-1 have been demonstrated. Although no successful cryptanalytic attacks have been reported yet on the four variants of the current standard SHA-2, they strongly resemble SHA-1 and are thus particularly vulnerable. Since 2007, a public competition organized by the U.S. National Institute of Standards and Technology (NIST), has therefore been underway to design a secure new SHA standard which will be given the name SHA-3. The final selection is scheduled in 2012. Compared to SHA-2, SHA-3 should show better security properties and better or at least equal computational efficiency and memory requirements.

In the first round of the SHA-3 competition organized by the NIST, the 51 accepted candidates for the next-generation cryptographic hash standard SHA-3 have been evaluated in terms of security properties, computational efficiency, and memory requirements. While detailed information about the software performance on various platforms is provided for all candidates, a thorough analysis of the algorithm performance on dedicated hardware is often missing. Nevertheless, hardware efficiency is of substantial importance, as SHA-3 is expected to be implemented in many resource-constrained applications.

This thesis intends to complement the specifications of the candidates Shabal and CubeHash by investigating their suitability for both high-speed and low-area VLSI implementations. Shabal's high-speed core reaches a fairly large throughput of 6.351 Gbps at a complexity of 41.32 k gate equivalents (GE), whereas CubeHash makes do with a complexity of only 7.63 kGE and is thus particularly appealing for lightweight implementations.



The diagram on top of the chip with the two hash functions illustrates the mode of operation of an iterative hash function. The variable-length message is split into k fixed-length input blocks M_i and then compressed into the final digest.

Silicon Implementation of non-AES-based SHA-3 Second Round Candidates

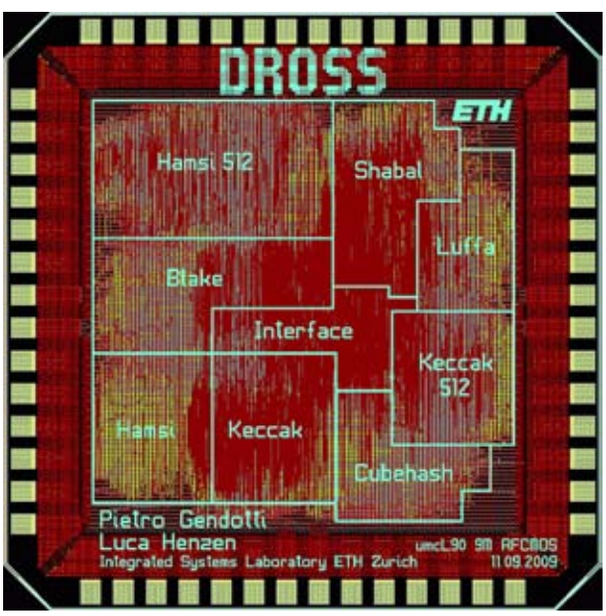
Personnel: Pietro Gendotti;
Assistant: Luca Henzen

Thesis: Master Thesis

During this diploma thesis, ten different architectures of the six non-AES-based SHA-3 candidates BLAKE, CubeHash, Hamsi, Keccak, Luffa and Shabal have been investigated and implemented in VHDL. The decision to take into account only candidates that are not based on the AES block cipher, exlcuding even those using only some steps of it, is mainly due to the fact that AES has already been deeply analyzed both in software and in hardware.

Among the investigated candidates, Keccak and Luffa, are the two algorithms that have shown the best performance, both in terms of area occupation and computational speed. The reason is their simple and compact implementation. In addition, most of the architectures implemented have shown appreciable performance in comparison with other researchers' implementations.

As a proof of concept, eight different architectures have been implemented on a 90 nm CMOS ASIC called *DROSS*. The chip, including the seal ring, has a fixed size of 1.925 mm x 1.925 mm, which limits the logical complexity to approximately 450'000 gate equivalents. The design uses a special-purpose interface to test the algorithms. In total, three clock domains have been specified at 300, 500 and 700 MHz in order to get optimal conditions for each algorithm.



Layout of the *DROSS* chip. The eight algorithms are highlighted in blue. The interface circuit has been placed in the center.

Silicon Implementation of Second-Round SHA-3 Candidates

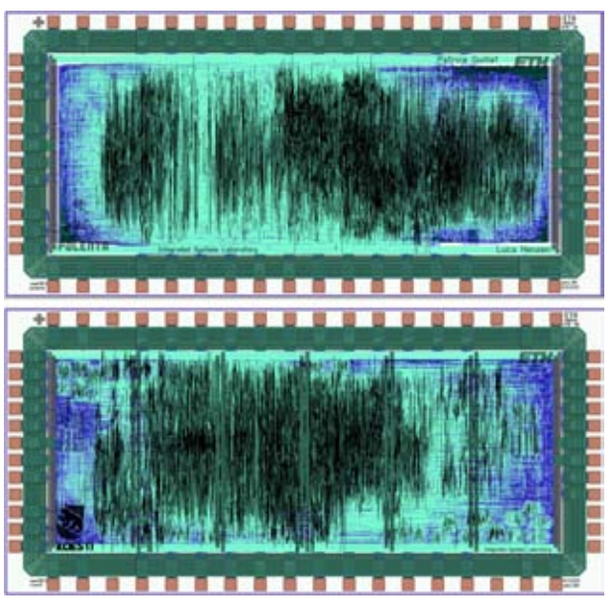
Personnel: Patrice Guillet, Enrico Pargaetzi, Martin Zoller;
Assistant: Luca Henzen

Thesis: Semester Thesis

As a result of the encountered weaknesses of the widely used SHA-1 hash algorithm, and due to concerns on the similarly-structured algorithms of the SHA-2 family, the US NIST has initiated the SHA-3 contest in order to select a suitable drop-in replacement. In round two of the competition, 14 candidates remain for consideration. Apart from the ongoing cryptanalytic efforts, benchmarking of software and hardware implementations of the candidates will be an important part of the evaluation. Software benchmarking is done for example by NIST on their reference platform and by the eBASH project in the context of the ECRYPT II network of excellence.

In order to complete the hardware analysis of the second round SHA-3 candidates, this thesis implemented six further algorithms, i.e. Blue Midnight Wish, Fugue, Grøstl, JH, SHAvite-3,and Skein. The implementations encompass equivalent functionality and interfaces. The design process has been done targeting the UMC 0.18 µm CMOS process technology.

The six architectures have been integrated into two different ASICs. Due to the area requirements of the architectures, the first chip, called *Polenta,* hosts the cores of the hash functions Blue Midnight Wish and Skein, while the functions Fuge, Grøstl; JH and SHAvite-3 have been assembled in the *Roesti* chip.



Chip layout of the *Polenta* (top) and the *Roesti (bottom)* ASICSs. A dedicated interface circuit provides input and output data transfer in both designs.

Low-Power Security-Enhanced Digital Controller ASIC for UHF Radio Frequency Identification Tag

Personnel: Johann Ertl;
Assistants: Norbert Felber, Luca Henzen;
TU Graz: Martin Feldhofer

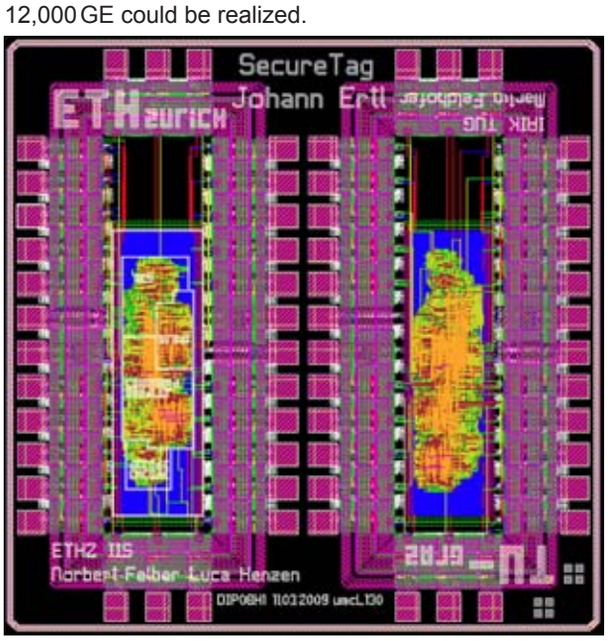
Thesis: Master Thesis

Partners: TU Graz

Radio frequency identification (RFID) tags consist of an integrated circuit (IC) attached to an antenna. The IC combines an analog frontend, a digital controller for the protocol handling, nonvolatile memory for electronic product code (EPC) and password storage, and possibly modules for cryptographic protocols. This work implemented the digital part of an EPC™ standard-compliant tag, extended by cryptographic units in order to implement an authentication protocol.

Since the VLSI process for student projects does not support nonvolatile memory, a test interface has been realized which allows direct access for the initialization of all memories and separate control of the AES and Grain cryptographic modules. The main parts of the device are the controller for the protocol handling, the en/decoder for the data to and from the RF interface, A Grain stream cipher used to generate secure (pseudo) random numbers for the challenge-response protocol, and an encryption-only Advanced Encryption Standard (AES) core.

Special attention was put on enhanced resistance against cryptographic DPA attacks by use of a sophisticated clocking strategy which is also responsible for reaching low power consumption. The power overhead could be limited to less than 0.2 μW of the total 4.8 μW and a silicon overhead of less than 1,000 gate equivalents (GE) of the 12,000 GE could be realized.



Two versions of the RFID digital controller, prototype ASIC with and without DPA-resistance enhancements. The chip microphotograph can be seen on page 93.

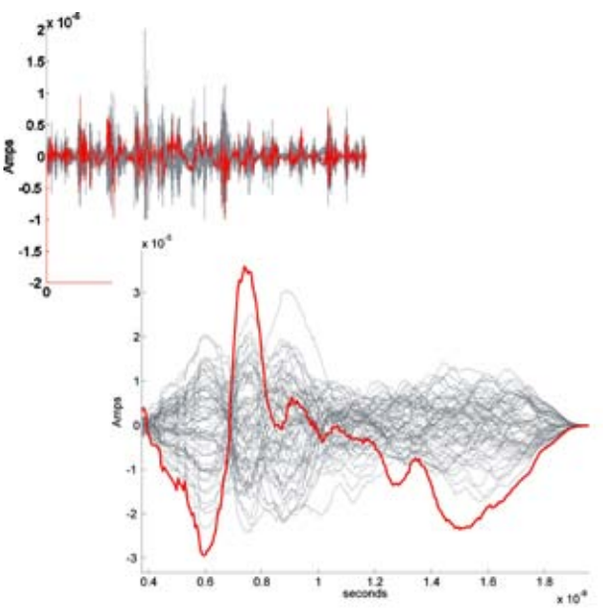
Implementation of a Prototype Board for Power Analysis Attacks

Personnel: Manuel Baumann;
Assistants: Luca Henzen, Markus Wenk

Thesis: Semester Thesis

Nowadays, symmetric and asymmetric ciphers are ubiquitous methods to secure private data transfer. Although modern cryptographic systems can be proven secure, the proof often relies on a simple model of the system and the attacker. The usual assumption is indeed that the attacker knows the cipher and even the algorithm in detail. The only thing the attacker is missing is the key used for the cryptographic operations. This scheme does not take in account the actual implementation of the cryptographic core. Often, implementations of provably secure crypto systems can easily be broken by observing the side information leaked during the secret computation. These leaks can be any physical parameters of an observed crypto system. The power consumption of hardware implementations is in most cases related to the cryptographic key or the incoming plaintext. The process of exploiting the leaking information given by the power traces of a cryptographic system is also referred as power analysis attack.

This project aims to build a system which is able to perform power analysis attacks on cryptographic ASICs. The final goal was to design, fabricate and test an FPGA-based testbed for power analysis. Using a fast analog-to-digital converter, the power traces of a running chip are transmitted and elaborated inside a Virtex-4 FPGA.



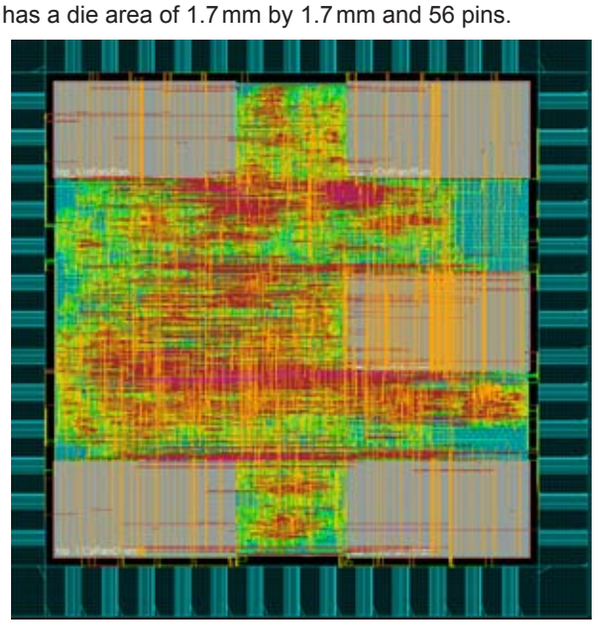
Power analysis of a running ASIC under a set of different keys. The red lines refer to the traces of the matching secret key.

High-Order Low-Latency Audio FIR Filter ASIC using a Novel Time-Domain Parallel Filter Algorithm

Personnel: Christoph Keller;
Assistants: Norbert Felber,
Lukas Bruderer

Thesis: Master Thesis

In this Master Thesis, an ASIC had to be developed which serves to treat audio recordings with extremely long acoustic room responses. Both the computational effort, and the storage requirements for the room response and the audio sequence to be processed, are very large. Algorithms had to be found to reduce the memory interface bandwidth and the number of required multipliers to a manageable amount. The new algorithm makes use of the redundancy in consecutive output samples in order to lower the memory throughput. After simulation and optimization of this algorithm, it was implemented in VHDL with the constraint for the layout to fit on the available silicon area for student designs (90 nm Mini@sic Europractice Multi Project Wafer). The resulting ASIC, connected to an external SRAM, is able to handle an impulse response of 87,300 samples at 48 kHz, corresponding to 1.8 seconds reverberation. A solution was found which allows to multiply this duration by the number of chips connected in a cascade. The latency of the resulting audio stream could be kept as low as 37.5 ms, which enables real-time applications. The chip features a time-domain-multiplexed standard audio interface to be connected to common Digital Signal Processors and audio AD and DA converters. It operates with 10 multipliers at a clock frequency of 245.76 MHz. Audio and impulse response data are 24 bit PCM. The ASIC in UMC L90 CMOS technology has a die area of 1.7 mm by 1.7 mm and 56 pins.



Chip layout of the audio FIR filter of order 87,300. Behind the orange wires, five grey RAMs can be seen. The ASIC is able to treat real-time audio streams with room responses of up to 1.8 seconds per cascadable chip.

Touch-Screen Graphical User Interface for Audio Digital Signal Processing Board

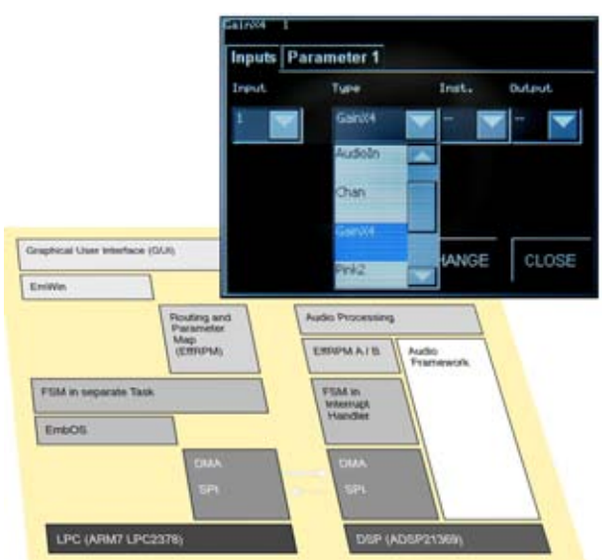
Personnel: David Sele;
Assistants: Norbert Felber,
Steven Müllener

Thesis: Semester Project

For the education of Bachelor students in a so called PPS (Practical training - Projects - Seminars), a versatile signal processing board is used for different digital-audio projects. It consists of a Digital Signal Processor ADSP-21369 (DSP), DA and AD converters for analog and digital inputs and outputs, several digital interfaces, LED bars, and a simple user interface with a 4 x 20 character LCD display.

For several projects, a state-of-the art graphical display – as used on many handheld devices – would be convenient, e.g. for presenting frequency responses of equalizers or measured impulse responses. Such a display with touch-screen facility could also be used to establish a comfortable menu-driven control interface.

In this semester project, a commercial product named BlueScreen with a 240 x 320 point color LCD and an ARM7 microprocessor on a small PCB has been evaluated for this purpose. Based on a real-time operating system EmbOS and a graphical library EmWin (by SEGGER Microcontroller GmbH), a framework has been established, which should students allow to configure the touch-screen interface for their individual requirements without the need to learn the developing environment of the microprocessor, but leaving time for creativity to audio processing on the DSP. While a nice solution for the graphical interface has been realized, the restricted memory of the BlueScreen did not allow to add curve displays.



An audio effect screen on the touch-screen graphical user interface for the PPS Digital Audio for 3rd and 4th semester EE students. Below, the structure of the framework is shown.

Programmable Baseband Filter for an LTE Direct-Conversion Receiver

Personnel: Piotr Gawlicki;
Assistants: Thomas Dellsperger, Thomas Burger

Thesis: Master Thesis

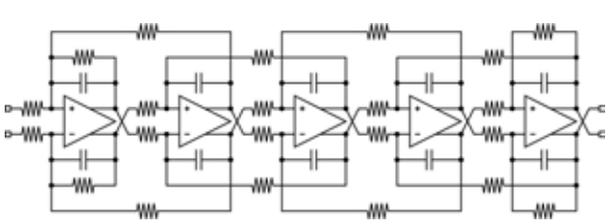
Partners: Imperial College London

Although 3rd generation (3G) mobile communication systems like UMTS are still maturing, 4th generation (4G) systems are already being standardized. LTE (Long Term Evolution), being a standard of the 4G family, is the most likely successor of UMTS. LTE will offer data rates beyond 100 Mbps in the downlink. A major difference compared to 3G standards is the variable channel bandwidth, which can be 1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz, or even 20 MHz.

The goal of this project was to design a baseband filter suitable for an LTE direct conversion receiver. The main purpose of a baseband filter is to attenuate interfering signals to a certain level relative to the wanted signal, such that the latter can be digitized reliably. The baseband filter should be programmable in cut-off frequency such as to cover all LTE channel bandwidths.

Based on specifications, a suitable low-pass filter approximation and filter order was chosen. Given the assumptions made for the remaining receiver blocks, a 5th order Chebychev low pass filter was determined to be suitable by means of MATLAB simulations. To achieve the required linearity, the Chebychev prototype was mapped to a Leapfrog active-RC circuit topology. Cut-off frequency programming was achieved by making the active-RC circuit's resistors and capacitors programmable. Appropriately combining resistor and capacitor values results in the desired cut-off frequency.

Based on a two-stage Miller-compensated opamp, designed to achieve a gain-bandwidth product of close to 1 GHz, the performance of the baseband filter was verified in the circuit simulation package Cadence.



Circuit topology of the implemented 5th order Chebychev Leapfrog filter.

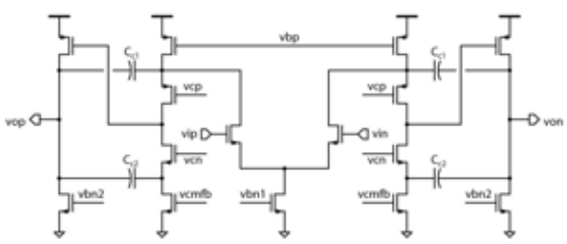
High-Performance Amplifier Design in CMOS for Switched Capacitor Circuits

Personnel: Xiao Liu;
Assistants: Craig Keogh, Schekeb Fateh

Thesis: Master Thesis

Switched capacitor (SC) circuits have proven themselves as excellent candidates for the implementation of critical analogue signal processing blocks such as sampled-data analogue filters and high-resolution data converters. These circuits consist of a network of switches and capacitors where charge is accurately transferred from a signal capacitance (or sampling capacitance) to another circuit capacitance (e.g. a feedback capacitance) via a virtual ground node. In such circuits, a high-performance amplifier or operational transconductance amplifier (OTA) is used to create this virtual ground node, thus ensuring the complete transfer of charge. The design of the OTAs for these SC circuits is no trivial task, especially in modern CMOS processes, where the designer must contend with shrinking supply voltages, reduced transistor intrinsic gain and increased leakage as technology migrates to smaller feature sizes.

This project investigated the design of highly-accurate and fast-settling OTAs for use in switched capacitor data converters. A mathematical analysis of various amplifier topologies was first conducted in order to better understand the relationships between the different parameters. Two candidate OTAs were then chosen and designed at the schematic level. A folded-cascode single-stage OTA and a two-stage compensated OTA were the chosen architectures. Simulations indicate that the two designed amplifiers settle to 14-bits accuracy within 2 ns across all process corners. A CMOS 130nm process was used in the implementation of both amplifiers.



Schematic of the two-stage OTA chosen and designed in 130 nm CMOS. Topology employs cascode compensation.

Real Space Green Solver for Nano Devices

Personnel: Michael, Spreng;
Assistants: Martin Frey, Aniello Esposito

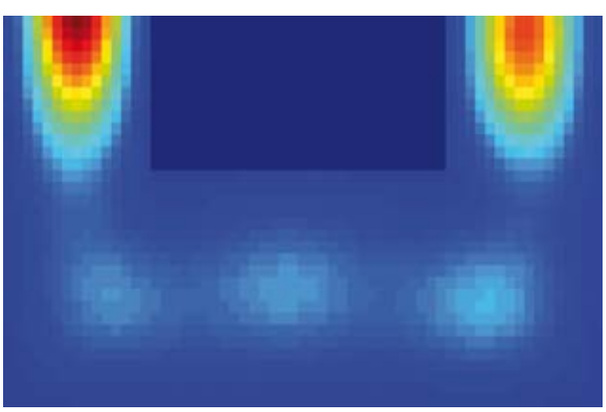
Thesis: Semester Thesis

The simulation package SIMNAD is a Poisson-Schrödinger Solver for nanoscale devices. Realized within the coupled mode approach, devices with a well defined transport direction and <100> crystal orientation can be simulated in an efficient way.

In order to allow simulations of non-idealized geometries, with electronic transport in arbitrary crystal orientation, a real space approach to quantum transport simulations is suitable. Therefore, the existing NEGF solver was generalized in the sense, that Hamiltonians with non-diagonal effective mass tensors can be treated as well.

In addition to the possibility of having an arbitrary crystal orientation in silicon, this generalization step also allows the treatment of other semiconductor materials, as for example germanium. Another advantage of the real space approach is that the gate leakage current can be calculated.

Both the Schrödinger and the Poisson equation were solved using a FD discretization. Only two-dimensional ballistic transport problems were considered in this thesis. The new solver has been successfully applied to test devices. The self-consistent coupling of the two equations and the simulation of realistic devices must be achieved in a follow-up project.



The spectral density in a two dimensional test device without a well defined transport direction. Strong reflections and perfect coherence in ballistic simulations demand an adaptive energy integration routine for the density calculation.

Design and Optimization of a Silicon Electro-Optic Modulator

Personnel: Eugen Zgraggen;
Assistants: Jan Kupec, Denis Dolgos;
MIT: Rajeev Ram

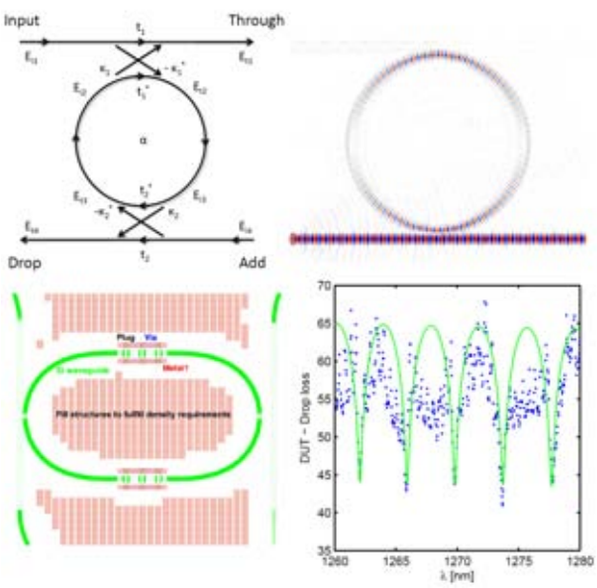
Thesis: Master Thesis

Partners: MIT

The increasing demand for data processing and transfer caused by new applications and growing data volumes drives the efforts of engineers to explore technologies and devices dispite the fact that conventional electronics are reaching their limits. This work focused on the intra-chip communication issue. Higher data volumes that have to be transferred within a chip, e.g. from memory to the processing unit, will no longer be handled by metallic interconnects like copper. Not only bandwidth issues are important, also energy efficiency aspects are limiting copper wires. Optical waveguides offer the bandwidths and promise high energy efficiency to address this problem.

A design and optimization of a silicon electro-optic modulator was performed within the scope of this thesis. To the best knowledge of the author, as of 2009, the literature review showed that there was no modulator design published that met the requirements of a monolithic integration within a scaled CMOS process. Rather, people modified the processes in order to break the limitations that the process puts on the device designer.

The aim within the project was to not make any modification to the mature and highly optimized scaled CMOS fabrication, but instead, the project was pursuing the design of the photonic devices within that framework and applying post processing to increase device performance.



Top left: Schematic of an add-drop single ring resonator. Top right: Field distribution within a ring resonator.
Bottom left: Ring modulator structure compliant with CMOS process. Bottom right: Comparison of simulated and measured drop loss.

Simulation of Nanowire Solar Cells

Personnel: Ralph Stoop;
Assistants: Jan Kupec,
Denis Dolgos

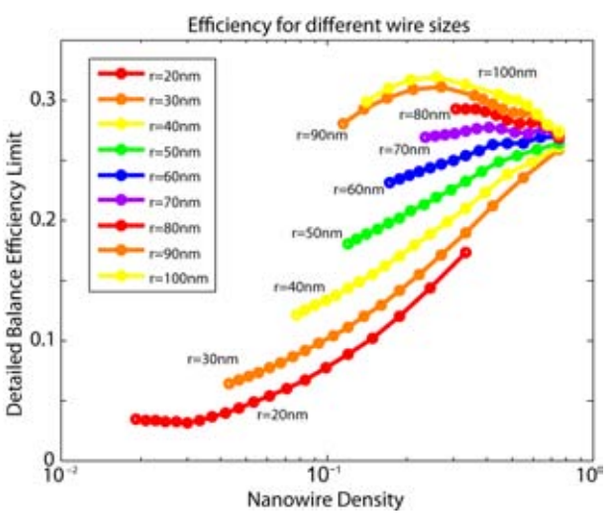
Thesis: Semester Thesis

In this thesis, numerical simulations of nanowire solar cells and calculations of the efficiency by detailed balance calculation were presented. Regarding numerical simulation of nanowire solar cells, a distinct challenge is the light propagation in nano-structured devices. It differs from the straight-forward calculations in the case of thick film devices since the absorption properties are no longer merely determined by the material composition.

In order to investigate the electromagnetic properties of nanowire solar cells, a variety of geometries has been simulated using the Finite Element Method (FEM) and compared in terms of absorption and efficiency using detailed balance calculations constituting a post-processing step of the data originating from FEM.

The obtained results highlight that a sparse nanowire array can absorb nearly all of the incident light, meaning that strain relaxation does not go along with decreased absorptivity. Strongly varying efficiency limits were obtained for constant array density. For certain nanowire diameters, increasing the inter-nanowire distance (i.e. decreasing density and semiconductor material consumption) efficiency could be even increased. The array exhibits intrinsically anti-reflective properties, allowing very efficiency coupling of light into the array.

These observations highlight the importance of rigorous solution of Maxwell's equations and the inapplicability of effective medium or ray optics approaches that are still commonly applied to this class of devices.



Efficiency limits for various nanowire radii at various densities. At low radii, even a dense array yields lower efficiency than a significantly sparser array of thicker nanowires. For thick wires, decreasing density can improve performance.

Biomimetic Solar Cell Design

Personnel: Onur Andiç;
Assistants: Jan Kupec, Denis Dolgos

Thesis: Semester Thesis

The flamboyant colors of butterfly wings are caused by nano-photonic phenomena rather than pigmentation. For the insects, the coloring of their most pronounced and exposed body part serves many purposes, including camouflage and temperature regulation. Many species exhibit perfectly black wings at very small thickness. Electron microscopy revealed the three-dimensional structures composed out of chitin that are responsible for the broadband absorptivity of some species. Yet, those structures are very porous to have low weight.

Although the complexity of the 3D nano-photonic structures is far beyond the limits of semiconductor fabrication, experiments with solar cells with nano-imprinted surfaces using real butterfly wings as stamps showed interesting preliminary results.

Within the scope of this thesis, honeycomb-structure-resembling patterns found on those insects were analyzed. Finite Element (FEM) simulations of a hypothetical indium phosphide nano-structured solar cell were performed to understand the mechanism of absorption. 3D simulations were compared to 2D modal analysis to identify the total absorption as a superposition of the absorption of the eigensolutions of the structure.

The structure exhibits highly absorptive resonances. At the same time those resonances have a low correlation with incident light. Research to increase the coupling efficiencies of predetermined modes could increase the total absorption of sun light and so the performance of solar cells.

Higher order eigenmode of the honeycomb structure. Resonances of the structure that exhibit a high confinement of the optical power in a very porous array of lossy material resulting in highly efficient absorption exist.

Periodic Boundary Conditions with Non-Matching Triangulations

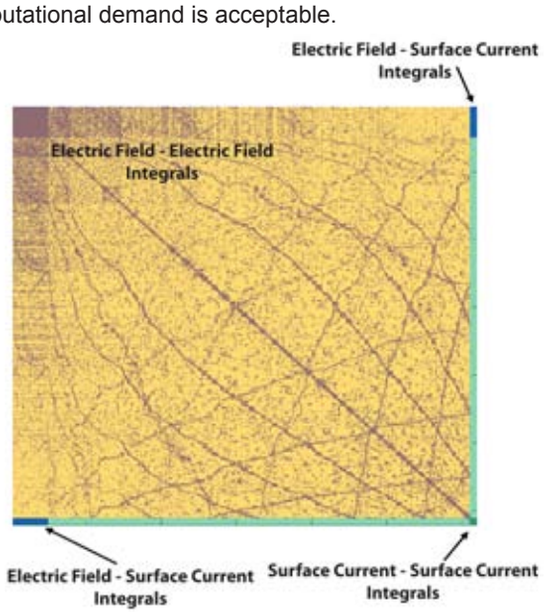
Personnel: Andrin Doll;
Assistants: Jan Kupec, Denis Dolgos

Thesis: Semester Thesis

Periodic boundary conditions (PBC) are essential for modelling a plethora of nano-optical problems. The most common approach to implement this feature in the Finite Element Method (FEM) involves direct mapping of degrees of freedom. This solution, however, requires identical triangulations at the faces where PBC is enforced.

A distinct advantage of FEM is, that the relations between the degrees of freedom are only at a local scope within a small fraction of the entire computational domain, hence, the finite element. This property leads to sparsely populated system matrices of the corresponding linear problem. Only elements sharing an edge share a degree of freedom. The method implemented within the scope of this thesis introduces an additional degree of freedom for every edge of triangular faces of elements at the boundary of the computational domain where PBC is imposed. The new degrees of freedom represent a surface current density expanded in terms of Raviart-Thomas basis functions.

Interaction between the surface current and the adjacent element (cis-boundary), as well as interaction of the surface current within an element, across the boundary (trans-boundary), and with the electric field across the boundary, has to be considered additionally. As the number of edges located on the surface of the convex computational domain is much smaller than within, the additional computational demand is acceptable.



The additional degrees of freedom required to enforce PBC do not alter the sparsity of the problem as the interaction across the boundary remains confined to elements with adjacent faces that have an overlap.

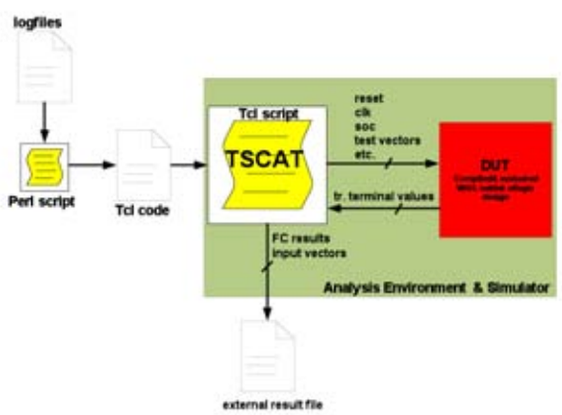
Defect Screening in Charge-redistribution Successive-approximation Register Analog-to-Digital Converter

Personnel: Thomas Kaltenbacher;
Assistants: Vezio Malandruccolo, Mauro Ciappa

Thesis: Master Thesis

Partners: Infineon AG

The scope of this work is to conceive and realize theoretical and experimental tools for the implementation of built-in reliability program for a smart-power technology for automotive applications. Traditional strategies making use of burn-in and high voltage testing are expensive and time consuming. A built-in screening strategy including an embedded circuitry has been designed to apply in-situ a proper stress and to monitor the degradation of sensitive physical parameters related to the defect to be screened out. A commercial charge-redistribution successive-approximation register analog-to-digital converter (SAR ADC) is used as an example circuit to demonstrate the developed screening strategy, both for the analog, as well as for the digital part. Defects to be screened out in the SAR ADC by the proposed technique are gate oxide defects. The screening procedure of the digital part consists of the application of proper logic test vectors at increased supply voltage followed by the measurement of the quiescent supply-current (I_{DDQ}). In this respect, a procedure is presented to define an optimum set of test vectors to grant the required screening coverage. The efficiency of this method has been demonstrated by simulation after implementation of a new plug-in tool called TSCAT. Thin oxide defects in the analog part of the SAR ADC (mainly consisting of stacked capacitors) are screened out by a first phase where a high voltage pulse is applied to the capacitor bank, followed by an electrical test at decreased clock frequency in order to identify possible leakage currents impairing the functionality of the SAR ADC.



Simulation environment developed to simulate the level of test coverage obtained by the different test vectors.

Electro-Thermal Multiscale Simulation of Electronic Devices

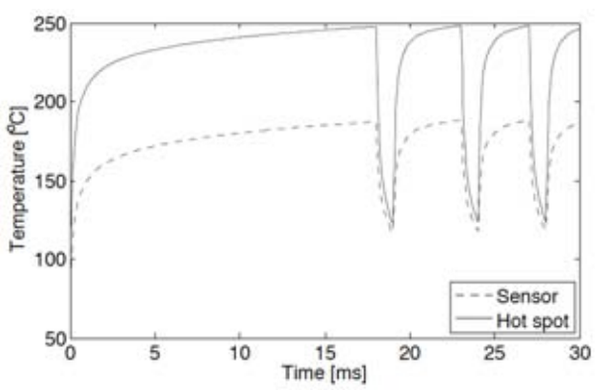
Personnel: Alberto Rizzi
Assistant: Mauro Ciappa

Thesis: Master Thesis

Partners: Uni Parma

Large-scale simulation of electronic systems requires more and more to take into consideration the dependency of the junction temperature described by the semiconductor equations The dependency is particularly relevant in the case of power devices, where in some circumstances the coupling of electrical and thermal parameters can result into a positive feed-back that can turn into catastrophic thermal runaway phenomena. From the modeling point of view, the solution of such a problem presents some basic constraints. In fact, in most cases the temperature-dependent heat sources are extremely concentrated in small space regions, while the local temperature is defined by the heat transport over large distances. This situation requires to use multiscale simulations techniques.

In this master thesis, an innovative approach for electro-thermal simulation of power electronic devices has been explored, which overcomes some major limitations encountered in traditional techniques. The required accuracy has been obtained by means of adaptive meshing strategies. Instead of handling the problems separately, electrical and thermal equations are coupled to calculate the self-heating effects occurring in electronic devices. The simulated value of the junction temperature is then used directly in the Ansys finite element simulator to calculate the instantaneous power dissipated by the power devices. This iteration step has been implemented by the APDL scripting language of Ansys.



Simulation of the temperature evolution in a temperature-controlled switch with hysteresis. The solid curve represents the temperature at the hot spot location, whose final level is defined by the switching algorithm. The observed time lag is due to the finite distance from the sensor to the hot spot.

TCAD Simulation of Unipolar and Bipolar Devices

Personnel: Maria Politou;
Assistants: Stefan Holzer, Mauro Ciappa

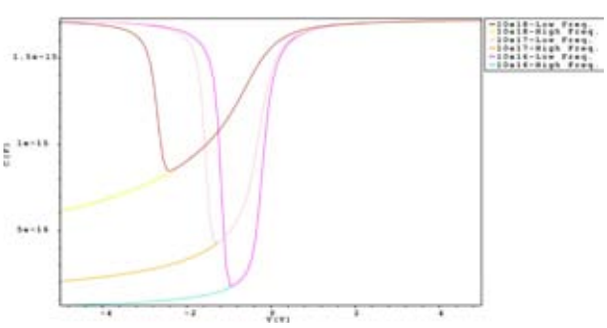
Thesis: Semester Thesis

Technology Computer Aided Design (TCAD) uses computer simulations to study, develop and optimize semiconductor devices, and their process steps. TCAD simulation tools represent the silicon wafer or the layer system of a device and solve fundamental physical equations for discretized geometries.

Simulation results are strongly dependent on the accuracy of the definition of the simulation model, on the physical models used for the different effects, as well as on the mesh strategies. Learning the interplay of all these components is of paramount relevance when using complex TCAD tools to obtain reproducible and quantitative results. In particular, the impact of the different components has to be validated both in the case of unipolar and bipolar conduction devices.

This semester project was intended as an introduction to a complex simulation tool and to deepen the knowledge and experience of semiconductor physics by comparing theoretical results with simulation obtained by using the TCAD tools.

Sentaurus Structure Editor, Sentaurus Device, Tecplot_SV and Inspect were mainly used, for the design, electrical characterization, visualization and study of the behavior of the basic semiconductor devices, like silicon resistors, diodes, Field Effect Transistors, Bipolar Junction Transistors and finally MOS Capacitors.



Quasi-static and high-frequency capacitance curves as simulated at different doping concentrations after optimizing the mesh.

PhD Theses – Abstracts

A TCAD Analysis of Long-Wavelength Vertical-Cavity Surface-Emitting Lasers

Alexandra Bäcker

This dissertation deals with the TCAD simulation and analysis of long-wavelength VCSELs. The simulations are performed with the commercial device simulator *Synopsys Sentaurus Device*. A thorough calibration of the electro-opto-thermal properties of a long-wavelength VCSEL with tunnel junction is presented. The temperature-dependence of external device characteristics, such as threshold current, thermal roll-over, and single-mode stability is investigated in detail. Special emphasis is laid on the understanding of the mode-switching behavior of the VCSEL. This thesis closes with a design optimization improving the maximum single-mode output power.

Prof. Dr. B. Witzigmann, ETH Zürich, examiner
Prof. Dr. H. Jäckel, ETH Zürich, co-examiner

Diss. ETH-Nr. 18330
ISBN 978-3-86628-258-3

Power Efficiency and the Mapping of Communication Algorithms into VLSI

Christian Benkeser

To satisfy the growing demands of today's information society, increased data rates and complex algorithms have to be supported. The key enabler for the required processing power has been the continuous, great progress in CMOS technology. However, in digital CMOS circuits implemented in recent deep sub-micron CMOS technologies power consumption has become a major bottleneck. This work explores the potential of improving the power efficiency of digital circuits with optimizations at the algorithmic and architectural level. To this end, the impact of the algorithm characteristics on architectural complexity is investigated and high-level, low-power design techniques are discussed. To demonstrate the effectiveness of the proposed methods power-efficient ASIC implementations for the major challenges of the digital baseband in 2G, 3G and 4G cellular systems have been realized, with a focus on turbo decoding and channel equalization.

Prof. Dr. Q. Huang, ETH Zürich, examiner
Prof. Dr. Y. Leblebici, EPFL, co-examiner

Diss. ETH-Nr. 18727
ISBN 978-3-86628-323-7

Resolution Enhancement Techniques for High-Speed Folding and Interpolation A/D Converters

Yihui Chen

The folding and interpolating architecture is a promising candidate for future high-speed analog-to-digital converters (ADCs). However, the achievable resolution of folding ADCs is heavily limited by the poor matching properties of differential pairs and current mirrors in CMOS technologies. To maintain reasonable offsets, fairly large transistor sizes are inevitable, which leads to low sampling rates or high power consumption. In order to enhance the resolution while maintain the speed and power consumption, two different techniques have been proposed in this work, and two prototypes have been implemented in a 0.13 µm CMOS technology with a supply voltage of only 1.2 V. The first prototype employs an open-loop auto-zeroing technique, and achieves an ENOB of 8.6-bit at 200 MS/s with a power consumption of 195 mW. The second prototype utilizes a novel digital calibration scheme, and reaches an ENOB of 9.0 bits at 250 MS/s. Its total power consumption is 230 mW.

Prof. Dr. Q. Huang, ETH Zürich, examiner
Prof. Dr. H.-A. Loeliger, ETH Zürich, co-examiner

Diss. ETH-Nr. 18520

Multi-Mode Delta-Sigma A/D Converters for Multi-Standard Wireless Receivers

Thomas Christen

Since the advent of 2G cellular systems, wireless communication has witnessed tremendous growth. At the same time, new standards are continuously introduced to satisfy the increasing demand for cheap and ubiquitous broadband wireless services. Considering however the predominance of 2G systems, a complete transition to the next generation of wireless systems is not feasible. Radio handsets with multi-standard capabilities have therefore become a pressing need. As analog circuitry is generally seen as an impediment to reconfigurability, RF receiver design has evolved by incorporating digitization closer to the receiver antenna. Multi-mode ADCs have consequently become a key component for multi-standard radios. The most promising multi-mode ADC architecture is the ΔΣ modulation which forms the subject of this thesis. The proposed multi-mode and low power concepts are vindicated with a 2-2 cascaded and a 3rd-order multi-mode ΔΣ modulator prototype implemented in 0.13µm CMOS which cover bandwidths up to 10MHz and 20MHz, respectively.

Prof. Dr. Q. Huang, ETH Zürich, examiner
Prof. Dr. H.-A. Loeliger, ETH Zürich, co-examiner

Diss. ETH-Nr. 18730
ISBN 978-3-86628-318-3

Application Specific Processor for MIMO OFDM Software-Defined Radio

Stefan Eberli

Software-defined radios (SDRs) present a promising approach to face the demands of today's fast evolving environment of wireless communication standards. Ever increasing requirements in terms of performance and flexibility call for programmable, highperformance signal processing platforms. This thesis contributes to the SDR research domain, addressing the implementation of a 2x2 MIMO-OFDM receiver on an SDR platform. Appropriate receiver algorithms are evaluated with special regard to the associated computational complexity. The use of low-complexity algorithms is imperative to spare the limited processing resources available on the SDR platform. The platform consists of two application specific processors, each tailored to the computational needs of the associated digital signal processing kernels. The first processor performs the per stream MIMOOFDM processing. The second processor handles the MIMO detection. The layout of the proposed processors in 0.18 µm CMOS technology is presented and provides reference for silicon area and power consumption.

Prof. Dr. W. Fichtner, ETH Zürich, examiner
Prof. Dr. H. Meyr, RWTH Aachen, co-examiner

Diss. ETH-Nr. 18582
ISBN 978-3-86628-285-8

MF Health Risk Assessment: RF Exposure Systems for Large-Scale Laboratory and Experimental Provocation Studies

Sven Ebert

Various biological and health effects have been suggested as resulting from exposure to radiofrequency electromagnetic fields (RF-EMF) emitted from mobile phones and other wireless communication devices. To foster significant progress in the health risk assessment of low-level RF-EMF exposure from mobile phones, the 5th Framework program of the European Union started a large international toxicological/carcinogenic project (named PERFORM). The objectives of this dissertation were the development, characterization and successful operation of optimized exposure systems for the large-scale laboratory and experimental provocation studies of the European PERFORM project. Significant contributions were achieved for all major requirements of such systems, to realize well-defined, well-controlled, well-characterized, and artifact-free exposures.

Prof. Dr. W. Fichtner, ETH Zürich, examiner
Prof. Dr. N. Kuster, IT'IS Zürich, co-examiner
Prof. Dr. P. Niederer, ETH Zürich, co-examiner

Diss. ETH-Nr. 18636
ISBN 978-3-86628-285-8

EMF Risk Assessment: Exposure Assessment and Compliance Testing in Complex Environments

Sven Kühn

This thesis aimed at the development of novel experimental and numerical methods to assess human exposure to electromagnetic fields (EMF) for safety and compliance evaluation as well as for the characterization of human exposure in epidemiological studies.
A large cross-section of mobile phones, general mobile communication devices and fixed communication installations were assessed using experimental methods. Absorption characteristics in human bodies were studied numerically. The conservativeness of current EMF safety limits was analyzed using realistic human bodies in arbitrary environments. Experimental compliance test methods for base station antennas and general mobile transmitters were developed. Dosimetric proxies and models for the estimation of induced EMF in human bodies were developed to support epidemiological studies of arbitrary wireless devices.

Prof. Dr. W. Fichtner, ETH Zürich, examiner
Prof. Dr. N. Kuster, IT'IS Zürich, co-examiner
Prof. Dr. L. Martens, Universiteit Gent, co-examiner

Diss. ETH-Nr. 18637
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VLSI Circuits for MIMO Preprocessing

Peter Jan Lüthi

The latest mobile applications and the growing number of wireless users are increasing the demand for high-throughput wireless access solutions. Multiple-input multiple-output (MIMO) technology combined with orthogonal frequency-division multiplexing (OFDM) constitute today's most promising approach to exploit the limited radio frequency resources in a highly efficient way. Unfortunately, the adoption of these technologies significantly increases the signal processing complexity, what ultimately calls for dedicated very-large scale integration (VLSI) circuits. At system-level, careful evaluation of MIMO preprocessing aspects offers great opportunities for lowering MIMO detection complexity. This work focuses on VLSI circuits for MIMO preprocessing, with emphasis on QR decomposition-based architectures, and contains considerations for joint algorithmic and architectural optimizations. Several architectures have been realized as integrated circuits, including one proving its full operational capabilities by being successfully deployed to a real-time MIMO-OFDM testbed.

Prof. Dr. W. Fichtner, ETH Zürich, examiner
Prof. Dr. H. Meyr, RWTH Aachen, co-examiner

Diss. ETH-Nr. 18777
ISBN 978-3-86628-295-8

Modelling Nano-LEDs

Sebastian Steiger

This dissertation describes two approaches to the numerical modelling of electroluminescence in nanostructured semiconductor light-emitting diodes (LEDs). The semiclassical simulator *tdkp/AQUA* aims at the unified description of transport and luminescence in three-dimensional structures with varying degrees of quantization. As examples serve an AlGaAs-based quantum wire LED and an InGaN-based nanocolumn LED. The second simulator employs the NEGF formalism for a fully quantum-mechanical description of planar nanostructures, enabling deep physical insight into scattering, carrier capture and energetic carrier distributions. A GaAs resistor and an AlGaAs-based quantum well LED are investigated.

Prof. Dr. B. Witzigmann, ETH Zürich, examiner
Prof. Dr. A. Imamoglu, ETH Zürich, co-examiner

Diss. ETH-Nr. 18399
ISBN 978-3-86628-257-5

Iterative MIMO Decoding: Algorithms and VLSI Implementation Aspects

Christoph Studer

The key requirements of modern wireless communication systems are throughput, coverage, and range. Multiple-input multiple-output (MIMO) wireless technology in combination with iterative MIMO decoding is one of the most promising methods to improve these requirements without sacrificing spectral efficiency or increasing the transmit power. This dissertation focuses on the design and optimization of algorithms for iterative MIMO decoding and presents corresponding VLSI implementations. The main contributions of this work are the development and implementation of novel low-complexity and high-performance soft-input soft-output (SISO) detection algorithms for MIMO systems based on parallel interference cancellation and on sphere decoding. In addition, implementation results for SISO decoding of convolutional, LDPC, and turbo codes are presented. The algorithms and circuits provided in this work give reference for the performance and the silicon complexity associated with iterative MIMO decoding.

Prof. Dr. W. Fichtner, ETH Zürich, examiner
Prof. Dr. E. Viterbo, Uni Calabria, co-examiner

Diss. ETH-Nr. 18512
ISBN 978-3-86628-288-5

Preserving High Resolution in Deep-Submicron CMOS Pipelined A/D Converters

Jürg Andreas Treichler

While the continuing development of new process technologies with shrinking minimum feature sizes allows digital designs to have higher integration densities and more functionality per area, analog circuits increasingly suffer from the lowering of the supply voltage.
The design of analog-to-digital converters (ADCs) is particularly affected by this problem.
This thesis focuses on achieving high resolutions in pipelined ADCs running at low supply voltages. After an introduction comprising an overview of converter architectures and a literature summary, noise and error sources in pipelined converters are analyzed.
Architectural considerations with a special focus on removing the dedicated sample-and-hold stage present in most published designs follow, and different calibration schemes for certain subcircuits are described as well.
Two chapters deal with the implementation and measurements of realized converters, together with an analysis of encountered problems.

Prof. Dr. Q. Huang, ETH Zürich, examiner
Prof. Dr. H.-A. Loeliger, ETH Zürich, co-examiner

Diss. ETH-Nr. 18631
ISBN 987-3-86628-316-9

Computational Modeling of Semiconductor Nanostructures for Optoelectronics

Ratko G. Veprek

This dissertation deals with parts of the theory and its numerical implementation of a novel simulator *tdkp/AQUA*, suitable for the unified simulation of nanostrucures for optoelectronics of any dimensionality. Here, the calculation of realistic electronic band structure, including strain and polarization effects, and the optical properties of nanostructures are covered. The presented theory is based on a continuum formulation of the physical behavior of the involved semiconductor crystal. As a central novelty, the **k·p** envelope function method for the band structure calculation is formulated absolutely spurious solution free by ensuring a mathematical consistent formulation retaining the elliptical nature of the equation. The optical properties are calculated within a density matrix formalism. Many-body effects due to Coulomb interactions between charge carriers are included on the level of the screened Hartree-Fock theory. At the end, an analysis of GaN-nanocolumn LEDs using the developed simulator is presented.

Prof. Dr. B. Witzigmann, ETH Zürich, examiner
Prof. Dr. A. di Carlo, Uni Rom, co-examiner

Diss. ETH-Nr. 18424
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Master Theses – Overview

Spring Semester 2009

Li Mu	Hardware-Efficient Matrix Decomposition Processor for MIMO Communication Systems
Roth Christoph	Design and VLSI Implementation of a Low-Power Quasi-Cyclic LDPC Decoder
Gendotti Pietro	Silicon Implementation of non-AES-Based SHA-3 Second Round Candidates
Blösch Patrick	Design of a Programmable Baseband Filter for an LTE Direct Conversion Receiver
Zgraggen Eugen	Design and Optimization of a Silicon Electro-Optic Modulator
Kaltenbacher Thomas	Embedded Systems for Reliability Monitoring
Gawlicki Piotr	Validation of the kp Method using First-Principle Function Theory

Autumn Semester 2009

Jonas Balmer	System Analysis of Digtal Baseband Receiver for Evolved EDGE
Wenger Erich	Secure Circuits for RFIDs and Smart Cards with Low Power Consumtion and Small Size
Keller Christoph	High-Order Low-Latency Audio FIR Filter
Andic Onur	Embedded Many-bit-per-Cell Dynamic Random Access Memory (DRAM) Design
Liu Xiao	High-Performance Two-Stage Amplifier Design in CMOS
Liu Dan	Linearized Phase Model for a Bang-Bang Type All-Digital Phase-Locked-Loop
La Spina Alfredo	Design of a High-Energy Electron Dosimeter

Semester Projects – Overview

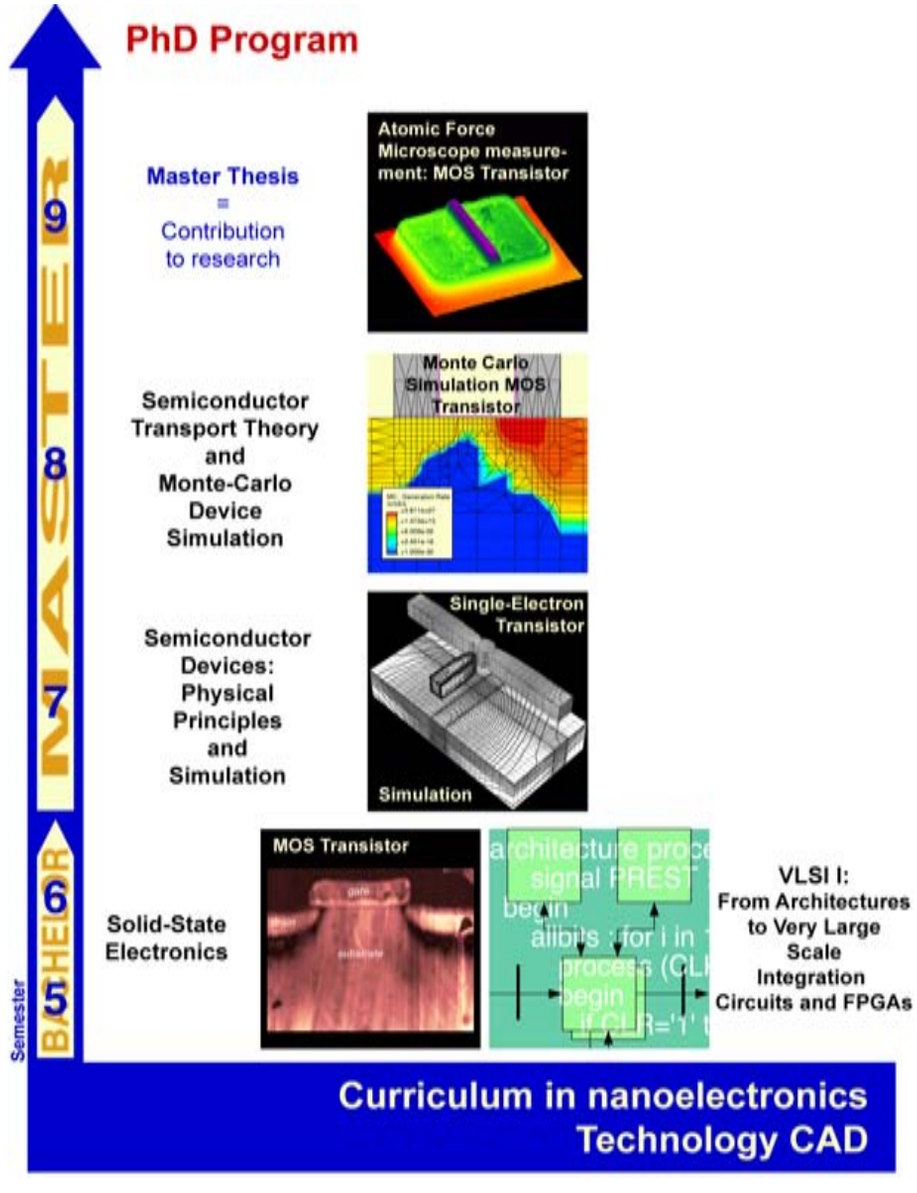
Spring Semester 2009

Müri Michael	Synchronization Parameter Estimation for Wireless MIMO OFDM Testbed
Bernet Markus	VLSI Implementation of the SHA-3 Candidates Shabal and CubeHash
Baumann Manuel	Prototype Board for Power Analysis Attack Setup
Andic Onur	Biomimetic Solar Cell Design
Politou Maria	Simulation of Bipolar and Unipolar Device Structures using Sentaurus Device
Spreng Michael	Real Space Greens Functions Solver for Nano Devices
Doll Andrin	Periodic Boundary Conditions with Nonmatching Triangulations in FEM

Autumn Semester 2009

Chai Yuning Widmer Manuel	Noise Whitening Processor Array for MIMO Communication Systems
Sporrer Benjamin Steiner Sebastian	Orthogonal Matching Pursuit for Sparse Channel Estimation
Huber Fabian	Gradient Pursuit for Sparse Channel Estimaiton
Guillet Patrice Pargaetzi Enrico Zoller Martin	Evaluation of SHA-3 Hash Function Candidates
Constantin Jeremy	Rapid Processor Design with LISA
Sele David	Touch-Screen Graphical User Interface to DSP Board
Stoop Ralph	Simulation of Nanowire Solar Cells

Education at IIS


PhD Program
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BACHELOR
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Semester
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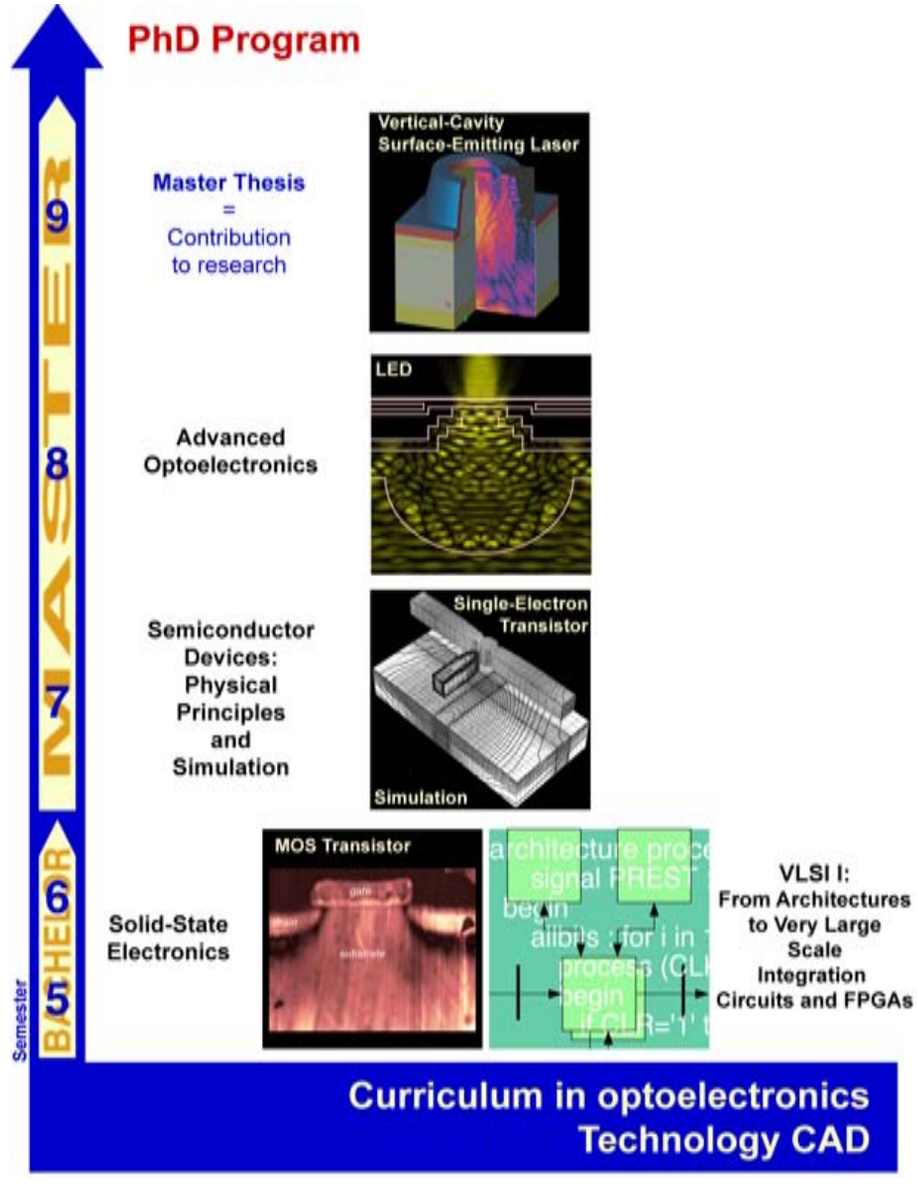
Contribution
to research
Atomic Force Microscope measure-ment: MOS Transistor
Semiconductor Transport Theory and Monte-Carlo Device Simulation
Monte Carlo Simulation MOS Transistor
Semiconductor Devices: Physical Principles and Simulation
Single-Electron Transistor
Simulation
Solid-State Electronics
MOS Transistor
VLSI I:
From Architectures to Very Large Scale Integration Circuits and FPGAs
Curriculum in nanoelectronics
Technology CAD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Contribution
to research
Vertical-Cavity Surface-Emitting Laser
Advanced Optoelectronics
LED
Semiconductor Devices: Physical Principles and Simulation
Single-Electron Transistor
Simulation
Solid-State Electronics
MOS Transistor
VLSI I:
From Architectures to Very Large Scale Integration Circuits and FPGAs
Curriculum in optoelectronics
Technology CAD

Lectures

Halbleiterbauelemente **4th Sem.**
Semiconductor Devices **EE**

A. Schenk

This lecture gives an introduction to the basics of modern semiconductor devices for micro-, opto-, and power-electronics. It bases on semiconductor physics and covers band structures, band models, dispersion relations, statistics, transport equations, macroscopic models, and the characteristics of silicon and other semiconductors. An overview on device families is presented.

The part on technologies covers the properties of materials, and introduces the steps of modern process technologies as well as packaging. To understand the basic principles of devices, ohmic and rectifying contacts, physical and electrical characteristics of pn junctions, and types of diodes are explained. The lecture continues with the bipolar transistor's function, working regions, characteristic diagrams, and its simulation. MOS devices are treated based on band diagrams, and the MOSFET behavior is deduced. Power devices, their working regions and static and dynamic behavior are followed by examples of optoelectronic devices as photo conductor, photodiode, LED, and fiber. Semiconductor measurement and characterization methods conclude the course.

Kommunikationselektronik **5th Sem.**
Communications Electronics **EE**

Q. Huang

This course provides basic design and circuit techniques for communications electronics. As a starting point, bipolar and MOS transistors are reviewed. The discussion of circuit design begins with basic amplifier topologies, impedance matching concepts, and a bit of two-port theory. Important non-ideal aspects such as non-linearity and noise are discussed. This sets the ground for more involved topics. Important building blocks of communications equipment, such as mixers and oscillators, are examined in detail. The discussions include the basic topologies, mathematical descriptions, and a thorough analysis of non-ideal behavior, from which finally guidelines for the design can be derived.

The exercises form an integral part of this course. The definitions and concepts presented in the lecture will be reinforced by small design examples, therefore providing a link between the theoretical description and real-world problems.

Solid State Electronics **5th Sem.**
Festkörperelektronik **EE**

W. Fichtner

The lecture Solid State Electronics explains the fundamental physical effects and properties for the operation of modern semiconductor devices. The focus is put on the solid state description by means of statistics, classical, and quantum physics. Device aspects play only a minor role, however, students learn the fundamentals for studying device operation in subsequent advanced lectures. In the beginning an introduction to quantum mechanics principles is given that helps understand the basic concepts from an engineering standpoint. The goal of the lecture is to get familiarized with the unique properties of semiconductors using a microscopic view, such as crystal structure, doping, energy bands, carrier dynamics and magnetic and optical properties.

VLSI I: Von Architektur zu hochintegrierter Schaltung und FPGA **6th Sem.**
VLSI I: From Architectures to Very Large Scale Integration Circuits and FPGAs **EE/CS/Phys/CSE**

N. Felber, W. Fichtner, H. Kaeslin

As becomes clear from the subsequent list of topics, the first course in this series of three is mainly concerned with system-level issues of VLSI. Terminology, overview on design methodologies and fabrication avenues, levels of abstraction used for circuit description and simulation, VLSI design flow, dedicated VLSI architectures, how to obtain an architecture for a given processing algorithm, architectural transformations for meeting throughput, area, and power requirements. Hardware Description Languages (HDL) and their underlying concepts, VHDL for simulation and synthesis, the IEEE-1164 logic system, Register Transfer Level (RTL) synthesis. Timing models, Anceau diagrams, functional verification of digital circuits and systems, building blocks of digital VLSI circuits, case studies of actual circuits, comparison with microprocessors and DSPs.

During the exercises students learn how to model digital ICs with VHDL. They write testbenches for simulation purposes and synthesize gate-level netlists for ASICs and FPGAs.

VLSI II: Entwurf von hochintegrierten Schaltungen **7th Sem.**
VLSI II: Design of Very Large Scale Integration Circuits **EE/CS/Phys/CSE**

N. Felber, W. Fichtner, H. Kaeslin

The second course begins with a thorough discussion of various technical aspects at the circuit and layout level. It then moves on to economic issues of VLSI. Topics include: limitations of functional design verification, techniques for improving controllability and observability, design for test, block isolation, scan-path techniques, partial scan and its caveats. Evaluation of various synchronous clocking disciplines, skew margins, clock distribution techniques. Asynchronous inputs, data inconsistency and metastability problems, synchronization. Cell libraries, Process-Temperature-Voltage (PTV) variations, transistor models, characteristics of CMOS inverters, complex gates. Power estimation and low-power design. Layout parasitics, transport delay, switching currents, ground bounce, controlling noise problems, power distribution, floorplanning, chip assembly. Layout design at the mask level, symbolic layout. Timing verification, physical design verification. Cost structures of microelectronics design and fabrication, avenues to low-volume fabrication, management of VLSI projects.

Exercises are concerned with physical design and sound engineering practices for avoiding timing, testability, and layout parasitics problems. Industrial CAD tools are being used for place and route, clock tree generation, chip assembly, and physical design verification. Students that elect to carry through a term project at the laboratory are offered the opportunity to complete a full IC design cycle on a circuit of their own which gets actually fabricated.

VLSI III: Test und Fabrikation von hochintegrierten Schaltungen **8th Sem.**
VLSI III: Test and Fabrication of Very Large Scale Integration Circuits **EE/CS/Phys/CSE**

N. Felber, W. Fichtner, H. Kaeslin

Whereas the preceding courses deal with design aspects of VLSI circuits, this one addresses manufacturing, testing, physical analysis, and packaging issues, such as: Effects of fabrication defects, abstraction from physical to transistor- and gate-level fault models, fault grading of large ASICs. Generation of efficient test vector sets, enhancement of testability by built-in self-test techniques. Modern IC testers: Architectures and application. Deep-submicron CMOS fabrication processes with multi metal levels and the physical analysis of their devices. Packaging problems and solutions. Technology outlook.

Exercises teach students how to use CAE/CAD software and automatic test equipment for verifying ASICs after fabrication. Students that submitted a design for manufacturing at the end of the 7th semester do so on their own circuits. Physical analysis methods with professional equipment (AFM, DLTS) complement this training.

Analog Integrated Circuits **6th Sem.**
Q. Huang **EE**

This course provides a foundation in analog integrated circuit design: After a review of bipolar and MOS devices and their small-signal equivalent circuit models, building blocks in analog circuits such as current sources, active load, current mirrors, supply independent biasing are presented. Other topics are differential amplifiers, cascade amplifiers, high gain structures, and output stages, and comparators, gain bandwidth product and stability of op-amps. Second-order effects in analog circuits such as mismatch, noise, and offset are investigated. More complex circuits such as A/D and D/A converters, analog multipliers and oscillators are analyzed. An introduction to switched-capacitor circuits from an IC designer's point of view is given.

The exercise sessions aim to reinforce the lecture material by well-guided step-by-step design tasks. Cadence design tools are used to facilitate the tasks. There is also an experimental session on op-amp measurements.

Halbleiter-Bauelemente: Physikalische Grundlagen und Simulation **7th Sem.**
Semiconductor Devices: Physical Principles and Simulation **EE/Phys**

A. Schenk

This course aims at understanding the principles behind the physics of modern electronic silicon semiconductor devices and the foundations of physical modeling of transport and its numerical simulation. During the course basic knowledge on quantum mechanics, semiconductor physics, and device physics is also provided. The main topics are: Transport models for semiconductor devices (quantum transport, Boltzmann equation, drift-diffusion model, hydrodynamic model), physical characterization of silicon (intrinsic properties, band gap narrowing, scattering processes), mobility of cold and hot carriers, recombination (SRH statistics, lifetimes for tunnel-assisted transitions), interband tunneling (Zener diode), impact ionization, metal-semiconductor contact, MIS structure, and heterojunctions.

The exercises focus on the theory and the basic understanding of special devices, such as pn-diodes, bipolar transistors, MOSFETs, and thyristors. Numerical simulations of these devices with an advanced simulation package are compared with corresponding measurements, which are also part of the exercises.

Halbleitertransporttheorie und Monte-Carlo Bauelementsimulation **8th Sem.**
Semiconductor Transport Theory and Monte-Carlo Device Simulation **EE/CSE**

F. Bufler, A. Schenk

The aim of the course is, on the one hand, to establish the link between microscopic physics and its concrete application in device simulation and, on the other hand, to introduce the numerical techniques involved. The scope encompasses therefore the basics of quantum mechanics, transport theory, and the Monte-Carlo method for the solution of the Boltzmann transport equation. The topics include second quantization, crystal symmetries, band structure calculation, phonons, Boltzmann equation, probability calculus, Monte-Carlo techniques, and device simulation.

The exercises comprise problems to illustrate the contents of the lecture, simple Monte-Carlo related programming tasks as well as the application of various professional tools for device simulation.

Elektrotechnik I **3rd Sem.**
Electrical Engineering I **MPE**

Q. Huang

This course provides the basic foundation in the specific field of electrical engineering. Starting from the basic concepts of voltage and currents, it covers the basic analyses of DC and AC networks. This includes series and parallel circuits, resistive circuits, circuits including capacitors and inductors, as well as the Kirchhoff's laws governing such circuits, and other network theorems. Transient response of RC-circuits, analysis of resonant circuits, concept of filtering, and simple filter circuits are all among the subjects covered in this course.

The understanding of the basic concepts of electrical engineering, particularly of circuit theory, shall be advanced. At the end of the course, the successful student knows the basic elements of electric circuits and the basic laws and theorems for determining voltages and currents in circuits with such elements. He/she is also familiar with basic circuit calculations.

Abbreviations:

CS	Computer Science
CSE	Computational Science and Engineering
EE	Electrical Engineering
MPE	Mechanical and Process Engineering
Phys	Physics

IC Design Projects – Overview

Projects in Progress	Type	Kind of Project
LDPC Decoder for Gigabit Ethernet	ASIC	contribution to research project
Evaluation of SHA-3 Hash Function Candidates part A	ASIC	contribution to research project
Low-Power Reconfigurable LDPC Decoder	ASIC	contribution to research project
Orthogonal Matching Pursuit for Sparse Channel Estimation	ASIC	contribution to research project
Evaluation of SHA-3 Hash Function Candidates part B	ASIC	contribution to research project
Evaluation of SHA-3 Hash Function Candidates part C	ASIC	contribution to research project
Noise Whitening Processor for MIMO Communication	ASIC	contribution to research project
Gradient Pursuit for Sparse Channel Estimation	ASIC	contribution to research project
Low-Power Embedded Microcontroller Design for Health Monitoring Applications	ASIC	contribution to research project
Matching Pursuit Implementation for Sparse Channel Implementation	ASIC	contribution to research project
Low-Power Area-Efficient Standard-Cell-based Memory	ASIC	contribution to research project
Secure Circuits for RFIDs	ASIC	contribution to research project
High-Order Low-Latency Audio FIR Filter	ASIC	contribution to research project
Highly Linear D/A Converter	ASIC	contribution to research project
LTE Receiver Base Band Section	ASIC	contribution to research project
LTE Transmitter Base Band Section	ASIC	contribution to research project
EEG Front-End	ASIC	contribution to research project
Fractional-N Synthesizer	ASIC	contribution to research project
High-Speed Folding and Interpolating A/D Converter with Digital Calibration	ASIC	contribution to research project

Completed IC Designs	Type	Result
VLSI Implementation of the Whirlpool Hash Function	ASIC	silicon fully functional
Matrix Decomposition Processor for MIMO Communication Systems	ASIC	silicon fully functional
Turbo Decoder for 3GPP LTE	ASIC	silicon fully functional
MBCJR Decoder design for 3GPP	ASIC	silicon fully functional
Low-Power Secure Circuits for RFID Tag	ASIC	silicon fully functional
Noise Estimation for MIMO-OFDM Testbed	FPGA	successfully verified
Advanced Detection on MIMO-OFDM Testbed	FPGA	successfully verified
High-Dimensional Cube Testers on the Stream Cipher Grain-128	FPGA	successfully verified
VLSI Implementation of the LLL Algorithm	ASIC	silicon fully functional
2x2 MIMO-OFDM Baseband Processing on a Reconfigurable Processor	ASIC	silicon fully functional
VLSI Implementation of SISO MMSE PIC	ASIC	silicon fully functional
Receiver for GSM/EDGE	ASIC	silicon fully functional
Receiver for GSM/EDGE/Evolved EDGE	ASIC	silicon fully functional
Multi-Mode Delta-Sigma ADC	ASIC	silicon fully functional
High-Speed Pipelined A/D Converter in Deep-Submicron CMOS Technology	ASIC	silicon fully functional

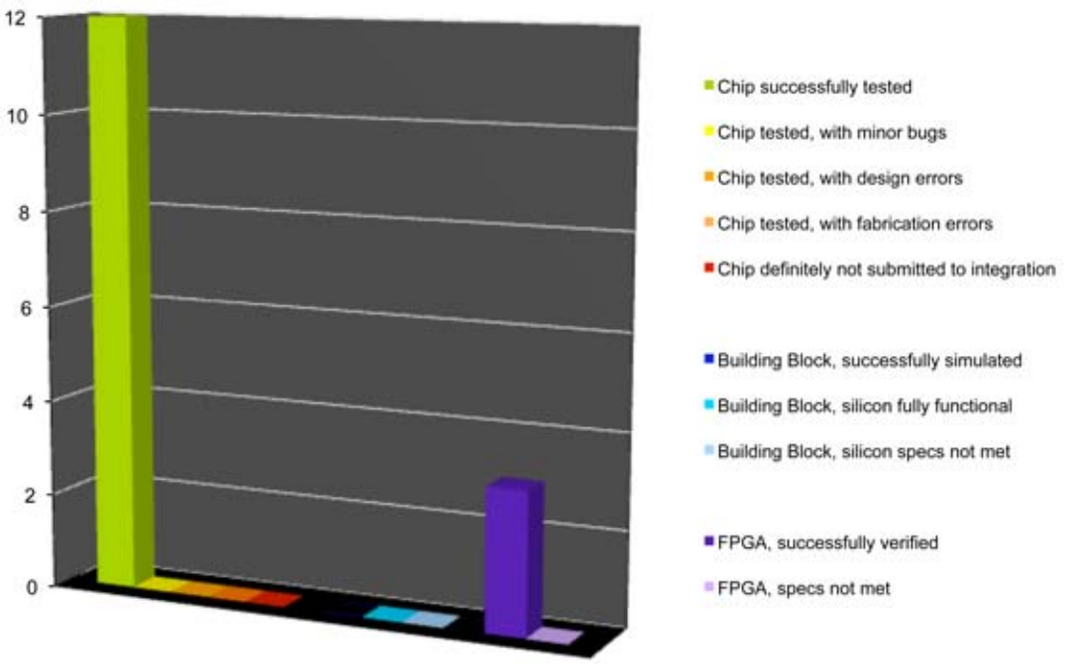
Abbreviations:

ASIC: Application-Specific Integrated Circuit

BB: Building Block (contribution to research or industrial ASIC)

FPGA: Field-Programmable Gate Array

Overview of IC Design Projects Completed in 2008



Research Projects – Overview

IC and System Design and Test

Subject: **MASCOT - Multiple Access Space-Time Coding Testbed (European IST Project)**

Partners: Laboratory for Communication Technology, ETH Zürich, Zürich (Switzerland
MASCOT Consortium
Period: January 06 – January 09
Funding, Number: European Union, IST-26905

Subject: **Quantum Cryptography Based Point-to-Point Secure Data Communication System (ESCRYPT II)**

Partners: id Quantique SA, Carouge (Switzerland)
Fachhochschule Nordwestschweiz, Windisch (Switzerland)
Period: December 08 – May 10
Funding, Number: KTI*, 9821.1 PFNM-NM
id Quantique SA, Carouge (Switzerland)

Subject: **Algorithmen und Archtekturen für drahtlose Heimnetztwerke der nächsten Generation (MIMO) (Algorithms and Architectures for Next Generation Wireless home Networks)**

Partners: Celestrius AG, Zürich (Switzerland)
Computer Engineering and Networks Laboratory, ETH Zürich, Zürich (Switzerland)
Period: March 08 – June 09
Funding, Number: KTI*, 9268.1 PFNM-NM
Celestrius AG, Zürich (Switzerland)

Signal Processing Circuits and Systems

Subject: **Circuits ans Systems for Next Generation Wireless Communications (FESS)**

Period January 09 - December 12
Funding, Number: SNF*, PP02-119057/1

Subject: **Wireless LAN Circuits Evolution (WiLANCE)**

Partners: Hasler Stiftung, Bern (Switzerland)
Period: October 09 – September 12
Funding, Number: Hasler Stiftung Bern (Switzerland), 09042

Analog and Mixed-Signal IC Design

Subject: **Advanced Data Conversion and Digital Front-End Signal Processing for Multi-Standard Radios (ADEMAR)**

Partners: ACP AG, Zürich (Switzerland)
Period: February 07 – July 09
Funding, Number: KTI*, 8514.3 NMS
ACP AG, Zürich (Switzerland)

Subject: **Advanced Multi-Mode Transceivers Beyond 3G (AMXCV3)**

Partners: Hasler Stiftung, Bern (Switzerland)
Period: February 08 – January 10
Funding, Number: Hasler, Bern (Switzerland)

Subject: **Enhanced Reconfigurable Transceivers for long Term Evolution for 3GPP and WiMax (ERT)**

Partners: ACP AG, Zürich (Switzerland)
Period: March 09 – February 11
Funding, Number: KTI*, 8514.3 NMS
ACP AG, Zürich (Switzerland)

Technology CAD

Subject: **Microscopic Investigation of Optical Properties in Quantized Semiconductors Structures (GAIN)**

Period: April 05 – January 09
Funding, Number: SNF*, 200021-107932

Subject: **Improvement of Dopant Diffusion and Activation Models in Strained Silicon by Ab Initio Simulations on the Atomic Scale (ATOMDIFF)**

Partners: Synopsys Switzerland LLC, Zürich (Switzerland)
Pilot Users: Applied Materials, Inc., Sunnyvale, CA (USA)
Fujitsu Laboratories, Atsugi (Japan)
NEC Corporation, Kanagawa (Japan)
Samsung Electronics, Yongin-City (Korea)
ST Microelectronics, Crolles (France)
Varian Semiconductor Equipment Associates, Inc., Gloucester, MA (USA)
Period: May 06 – September 09
Funding, Number: KTI*, 8349.1 NMPP NM
Synopsys Switzerland LLC, Zürich (Switzerland)

Subject: **Non Equilibrium Quantum Transport in Semiconductor Nanostructures: Bridging the Silicon based Nanostructures and Nanodevices for Long Term Nanoelectronics Applications (NANOSIL)**

Period: January 08 - December 10
Funding, Number European Union, IT-216171

Subject: **Evaluation and Comparison of Monte-Carlo Simulation Codes for Modeling of Electron Beam Lithography (EVAL-LITHO)**

Partners: Synopsys Switzerland LLC, Zürich (Switzerland)
Period: September 08 – February 09
Funding, Number: Synopsys Switzerland LLC, Zürich (Switzerland)

Subject: **Multi Physics Simulation and Modeling of Advanced CMOS Technologies (DEVICE)**

Partners: Toshiba Corporation, Minato-ku (Japan)
Period: December 08 – December 11
Funding, Number: Toshiba, Yokohama, (Japan)

Computational Optoelectronics

Subject: **Photodetectors for Next Generation Broadband Access Passive Optical Networks (PONDETECT)**

Partners: Enablence Switzerland AG, Rüschlikon (Switzerland)
Period: July 07 – June 10
Funding, Number: KTI*, 8894.1 PFNM-NM
Enablence Switzerland AG, Rüschlikon (Switzerland)

Subject: **Towards directly modulated VCSELs at 40 Gbit/s (NCCR - VCSEL)**

Partners: QP-NCCR, Lausanne (Switzerland)
Period: October 07 – June 09
Funding, Number: SNF*

Subject: **Physics and Simulation of Electro-Optical Properties in Non-Polar Nitride-Based Heterostructures (NONPOLAR)**

Period: August 08 – July 11
Funding, Number: SNF*, 20PA21-120079

Physical Characterization and Technology Development

Subject: **PORTES – Power Reliability for Traction Electronics (Alstom)**

Partners: Alstom
Period: February 07 - January 09
Funding, Number: Alstom, Levallois-Perret (France)

Subject:	**Thermal Interface Reliability**
Partners:	ECPE Engineering Center for Power Electronics GmbH, Nürnberg (Germany)
Period:	December 06 – August 09
Funding, Number:	ECPE, Nürnberg (Germany)
Subject:	**Design for Reliability (DfR) for SPT9**
Partners:	InfineonTechnologies Austria AG, Villach (Austria)
Period:	January 08 – December 10
Funding, Number:	Infineon Austria, Villach (Austria), 6000805
Subject:	**Modeling and Optimization of Electron Beam Cross-Linking Processes for Electrical Wires, Cables, and Optical Fibers (EBX-Link)**
Partners:	Huber + Suhner AG, Pfäffikon (Switzerland)
Period:	September 08 – August 11
Funding, Number:	KTI*, 9561.1 PFIW-IW Huber + Suhner, Pfäffikon (Switzerland)
Subject:	**Physics Based Simulation and Physical Characterization of MEMS (MEMS)**
Partners:	Toshiba Corporation, Yokohama (Japan)
Period:	October 08 – September 10
Funding, Number:	Toshiba, Yokohama, (Japan)

Bio Electromagnetics and Electromagnetic Compatibility

Subject:	**Forschungskooperation IT'IS – ETH Zürich (Research Cooperation IT'IS – ETH Zürich)**
Partners:	Foundation for Research on Information Technologies in Society (IT'IS), Zürich (Switzerland)
Period:	since January 00 – December 13
Funding, Number:	IT'IS, Zürich (Switzerland)

Abbreviations

KTI	Commission for Technology and Innovation (a Swiss Government Agency)
SNF	Swiss National Science Foundation

Microelectronics Design Center (DZ)

Personnel

Dr. H. Kaeslin (head, VLSI CAE), Dr. F. Gürkaynak (VLSI technology, VLSI CAE/CAD), B. Muheim (software operation, VLSI CAE/CAD), D. Schöni (PCB CAD).

New team member for PCB support

For almost 15 years, Rudolf Köppel has been teaching students and staff at our department the secrets of manufacturable PCB design and has helped them with numerous projects. As Ruedi has retired at the end of the year, we all would like to express our gratitude and wish him a good time with his family and hobbies. Ruedi's functions are now being assumed by Daniel Schöni whom we welcome as new colleague in our team. Dani has an industrial background as circuit, board, and software developer for biomedical and signal processing applications. He sees himself as an allrounder and looks forward to contribute to the most challenging projects. Dani will also carry on our regular courses on PCB design and construction in collaboration with our external consultant Dr. M. Nussberger.

New DZ homepage

The Microelectronics Design Center homepage at `http://www.dz.ee.ethz.ch/` has received a facelift and has adopted the look advocated by ETH Corporate Communications. The new webpage, which has been implemented with the assistance of the ISG group on the basis of Typo3, is easier to maintain and we expect it to be more up to date. We use new items to notify the installation of new tools or updates to existing software packages. We keep separate packages containing information on technologies that we support under: `http://www.dz.ee.ethz.ch/en/our-range/services/asic-support.html` All of our previous pages have been carried over to the new webpage as well. There is the ever popular "Microelectronics Industry in Switzerland" page which we update regularly `http://www.dz.ee.ethz.ch/en/our-range/background/industry-in-switzerland.html` and the "HDL help page" `http://www.dz.ee.ethz.ch/en/information/hdl-help.html` that contains, among other things, our proven VHDL naming conventions.

Power distribution in sub 100 nm IC designs

One of the serious challenges in today's digital ASIC design is power distribution. Every logic gate, flip-flop, and memory needs to be supplied with electricity and therefore needs a power (VDD) and a ground connection (GND or VSS). Unfortunately, part of the voltage is lost during power distribution as a consequence of Ohm's law $U = I \cdot R$. Current that flows through a resistive path causes a voltage drop that is proportional to the amount of current and the electrical resistance as determined by the length and sectional area of the metal interconnect line. In the context of VLSI design, this undesirable phenomenon is known as *IR*-drop.

The goal of each new IC technology generation has been to increase layout density by a factor of two (thanks to the extraordinary efforts of the semiconductor industry in trying to meet the imperative of Moore's Law). This has several consequences for power distribution. Since devices keep on getting smaller, the wires connecting to these components have also decreased in width. Narrower wires (of the same height) have a higher resistance which amplifies ohmic losses. In 90 nm technology, a metal rail that distributes power along a typical row of standard cells measuring 1 mm has around 170 Ω of resistance, compared to 27 Ω in 250 nm.

Another difficulty is that voltage levels have been greatly reduced over the years to prevent excessive power densities and to protect ever thinner gate oxides from dielectric breakdown. A lower supply voltage implies that more current must flow to deliver the same electrical power, which in turn inflates the *IR*-drops in the supply connections. In simple terms, the problem is that the devices at the end of a long wire do no longer see the full supply voltage, which makes them run slower. To make things worse, a lower nominal voltage increases the relative proportion of *IR*-drops. When using a 3.3 V supply, a 100 mV drop can be considered negligible, but at 1.0 V the same drop results in a 10% voltage loss and has a significant impact on timing.

IR-drops have become a serious problem for even the smallest chips manufactured in 90 nm and have incited us to find ways to lower the parasitic resistance in the supply network. Traditional power distribution schemes rely on surrounding the core area with a wide power ring. Standard cells connect to this ring using horizontal rails on lower metal layers. Extra vertical "stripes" feed in power at regular intervals and so improve resistance and current distribution.

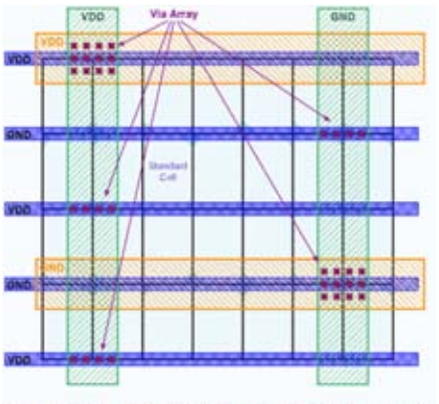


Figure 1: Detailed view of the recommended power distribution scheme.

The power grid methodology, which we have introduced with 90 nm designs is an extension of that basic scheme. The entire chip surface is covered with a dense grid of top-level metal layers carrying power and ground. Those supply grid lines exhibit a low electrical resistance as they are thicker and made fairly wide. The trade-off is that high via-stacks are required to bring power and ground to the lower layers and, ultimately, to the devices. Our experience suggests to place one routing grid on top of every third standard cell power rail as illustrated in fig.1. In standard cell rows, supply rails alternate between VDD and GND. By placing a grid line on every third rail we make sure that the horizontal grid lines also alternate between VDD and GND. Wherever possible, the grid is connected to the supply rails below using a stack of vias. The vertical and horizontal grid lines are also regularly cross-connected using thick via arrays on intersection points. Fig.2 compares the quality of the two variants.

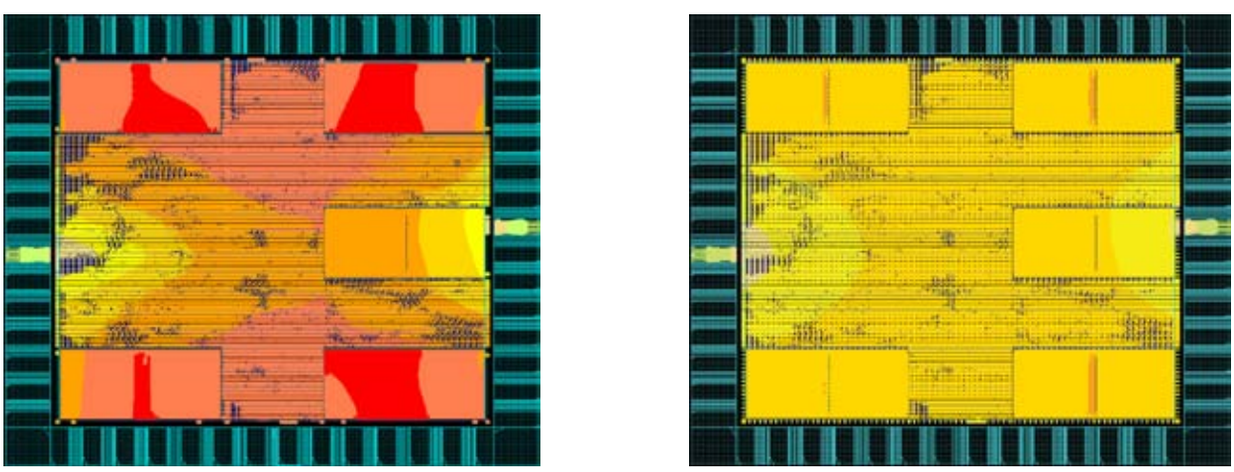


Figure 2: Result from an *IR*-drop analysis of a digital filter chip (90 nm CMOS, 1.7 mm × 1.7 mm, 660 MHz, 1.2 V). Six color grades represent estimated VDD node potential: green →99% or more, red → 95% or less. Note that a 5% drop at VDD actually corresponds to a 10% loss when VSS is affected symmetrically. The example to the left follows the traditional "rings-and-stripes" power distribution scheme whereas the one to the right implements the recommended grid-based technique.

The key to finding a good power distribution scheme is to predict the *IR*-drops in a chip with adequate precision. The well-known relationship indicates that power dissipation grows with the operating frequency, the square of the supply voltage U_{dd}, and the overall switched capacitance $\Sigma_k C_k$, all of which can be determined statically. The activity factors, in contrast, depend on what the chip does. The most accurate figures are obtained when a gate-level netlist is simulated with representative stimuli vectors and all parasitic delays to keep track of the actual switching of each circuit node individually. Unfortunately, this is a costly proposition as simulation runs take a lot of time to complete and are not practical for complex chips. On the other end of the spectrum, simpler approaches to power analysis assume a constant activity factor across an entire chip and so yield less accurate power estimations more quickly.

$$P = f_{clk} U_{dd}^2 \sum_k \frac{\alpha_k}{2} C_k$$

At the Microelectronics Design Center, we are continuously working with the latest electronic design automation tools to analyze and improve the power distribution networks of the chips designed at ETH Zurich. For details see `http://www.dz.ee.ethz.ch/en/information/how-to/power-grid.html`.

Supported fabrication processes

DZ has installed and maintains design flows for a wide range of VLSI fabrication processes and cell libraries. As any list is per force outdated by the time it gets printed, we kindly ask prospective IC designers to refer to our documentation on the Intranet available at `www.dz.ee.ethz.ch/en/information/ic-technologies.html` for up-to-date and more complete information on the resources available. Further be informed that DZ is willing to install most design kits supported by Euro practice, Mosis and other MPW vendors. Please contact DZ staff as early as possible if you feel our current offerings do not meet your needs.

Design Activities

A statistical overview of all IC design activities conducted in 2009 with software installations operated by DZ and with support by DZ staff is given in the table below along with the laboratory involved and with the target process. Only manufactured chips are listed, FPGA-based design projects and dry runs are not included in the numbers below.

IC Design		Teaching	Research	Total
Process family	Foundry			
130 nm CMOS	STM		3	3
180 nm CMOS	UMC	3		3
130 nm CMOS	UMC	2	2	4
90nm CMOS	UMC	3	1	4
Total		8	6	14

Courses Microelectronics Design Center

Cadence Methodology on Course Low-Power Digital Design

Trainer: Mikhail Alekseev, Cadence (RU)
Dates: February 16 to 18, 2009

Cadence Methodology Course on Analog and Mixed Signal Design

Trainer: Ahmed Noeman, Cadence (D)
Dates: February 25 to 27, 2009

Schaltungs- und Leiterplattenentwicklung in der Praxis

Trainer: M. Nussberger, R. Köppel
Dates: 12 half-days from March 5 to April 14, 2009

Schaltungs- und Leiterplattenentwicklung in der Praxis

Trainer: M. Nussberger, R. Köppel
Dates: 12 half-days from September 22 to December 15, 2009

Joint Research Cooperation with the IT'IS Foundation

Profile

The IT'IS Foundation was established on November 15th, 1999 through the initiative and support of the Swiss Federal Institute of Technology in Zurich (ETHZ), the global wireless communications industry, and several governmental agencies. IT'IS stands for Information Technologies in Society.

The aim of IT'IS is to create a flexible and dynamic research institution capable of addressing the research needs of society in the explosively expanding field of information technologies and the utilization of electromagnetic energies in general. Some of the areas encompassed are:

- evaluation of the safety and risks related to current and emerging information technologies
- exploration of information technologies for medical, diagnostic, and life support systems
- improvement of the accessibility of information technologies for all members of society including disabled persons.

IT'IS is committed to the advancement of science for the benefit of society at large and to maintaining strict independence from any particular interest groups. These principles are reflected in the Foundation's charter as well as the balance of the composition of its board, with distinguished personalities from science, the public sector, and the global wireless communications industry. IT'IS is a non-profit tax-exempt research organization.

Infrastructure and Cooperation

The IT'IS Foundation maintains the world's finest near-field laboratories and is situated in downtown Zurich. It includes a large semi-anechoic chamber for general near-field and dosimetric measurements. New laboratories were built, designed for accredited testing of body-mounted transmitters as well as implants.

IT'IS Foundation's closest and most important cooperative tie is with the Integrated Systems Laboratory. Close cooperation has also been established with the Laboratories of Computer Vision and Biomedical Engineering as well as other laboratories of ETH Zurich. In addition, the IT'IS team has substantial experience in multidisciplinary cooperation through a multitude of projects, resulting in an international network of over 80 academic and industry research partners in Europe, the USA, and Asia.

Current Research Focus

IT'IS Foundation's current research focus of lies in the three areas of 1) sensing and computational techniques for electromagnetic analysis, 2) health risk assessment, and 3) health support systems. In addition, IT'IS offers various services to governments and industry, including antenna engineering, device optimization for operation in EMF-hostile environments, testing of compliance, and safety white papers.

The first area, Sensing and Computational Techniques, consists of several projects, ranging from new sensor technologies and new measurement procedures for testing the compliance of wireless devices and base stations with safety limits, to extensions and improvements of FDTD for near-field applications and optics. The technologies have been integrated and commercialized in products such as DASY5, EASY4, iSAR and SEMCAD X. These products have become the standard in the wireless as well as medical device industries for R&D, testing compliance and virtual prototyping.

The second research area is Health Risk Assessment. This mainly involves the development, provision, and maintenance of exposure setups as well as the provision of detailed dosimetry for more than thirty experiments conducted in cooperation with biological and medical research groups in Switzerland, Europe, USA, China, and Japan. These include *in vitro*, *in vivo*, and human provocation studies involving various mobile communications bands as well as ELF experiments. In addition, IT'IS is conducting basic and review studies for many different agencies.

The Health Support System group, formed in 2003, is developing rapidly. Of particular mention are the projects on MR safety, MR safe implants and interventions under MR guidance, on applicators and treatment planning tools of hyperthermia and ablation, controllable nerve stimulation for neuroprothetics, optimized signal transmission over the body, and antenna designs for on-body and implanted antennas.

In addition to providing research results for governmental agencies through participation in standardization bodies and providing consultation to governments, IT'IS also provides courses to members of the public, industry, and universities.

Current research projects are being supported by public funds such as those of NIH (USA), Framework Programs (EU), EUREKA (EU), CTI (CH), SNF (CH), health agencies such as BAG (CH) and BfS (D), as well as other governmental institutions (e.g., BAKOM). Funding from industry comes from major mobile communications manufacturers, medical device companies and service providers as well as from smaller companies.

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[D2.] M. Bernet, L. Henzen, H. Kaeslin, N. Felber, W. Fichtner
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Proc. of IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Cancun, Mexico, Aug 2009

[D3.] F. Carbognani, L. Henzen
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Proc. of ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), San Francisco, CA, USA, Aug 2009

[D4.] S. Eberli
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N. Kuster
Reliability of the Radiation Dosimetry in Current Studies,
Subcommittee on Labor, Health and Human Services, and Education, and Related Agencies Hearing on The Health Effects of Cell Phone Use, Washington, DC, USA, 14 Sep 2009

N. Kuster, M. Douglas, S. Kühn, A. Christ
Concept for Demonstrating Compliance at Workplaces,
COST BM0704 Workshop, Paris, France, 4-6 Nov 2009

N. Kuster, S. Kühn, S.Y. Perov, Q. Balzano
Fast Evaluation Techniques to Demonstrate Compliance in the Near Field of Active and Passive Transmitters,
25th Progress In Electromagnetics Research Symposium (PIERS 2009 Moscow), Moscow, Russian Federation, 18-21 Aug 2009

C.H. Li, M. Capstick, N. Chavannes, N. Kuster
A Novel Design for Hyperthermia Treament at the Head and Neck Region,
Joint Meeting of The Bioelectromagnetics Society and the European BioElectromagnetics Association (BioEM), Davos, Switzerland, 14-19 Jun 2009

C.H. Li, M. Capstick, E. Neufeld, N. Chavannes, N. Kuster
Optimization of Patient Position in Hyperthermia Treatment for Head and Neck Region,
2009 IEEE International Symposium on Antennas and Propagation (APS), Charleston, Carolina, USA, 1-5 Jun 2009

Y. Li, J. Hand, A. Christ, E. Cabot, D.W. McRobbie, M. Capstick, M. Oberle, N. Kuster
Modeling Occupational Exposure to RF and Gradient Fields Associated with an Interventional Procedure in an Open 1 T MR System,
Poster Presentation at the ISMRM Seventeenth Scientific Meeting and Exhibition, Honolulu, Hawaii, USA, 18-24 Apr 2009

C.H. Li, E. Ofli, N. Chavannes, N. Kuster
The Influence of the User Hand on Mobile Phone Antenna Performance in Data Mode,
European Conference on Antennas and Propagation (EuCAP), Berlin, Germany, 23-27 Mar 2009

C.H. Li, E. Ofli, N. Chavannes, N. Kuster
SAR and Efficiency Performance of Mobile Phone Antenna with Different User Hand Positions,
2009 IEEE International Symposium on Antennas and Propagation (APS), Charleston, Carolina, USA, 1-5 Jun 2009

C.H. Li, E. Ofli, N. Chavannes, N. Kuster
Optimization of Patient Position in Hyperthermia Treatment for Head and Neck Region,
Poster Presentation at IEEE International Symposium on Antennas & Propagation and USNC/URSI National Radio Science (APSURSI 2009), Charleston, SC, USA, 1-5 Jun 2009

S. Loughran, M. Schmid, S. Regel, A. Bratic, M. Murbach, N. Kuster, P. Achermann
Effects of Pulse-Modulated RF-EMF on the Human Brain: Critical Field Parameters, Site of Interaction and Sensitivity in Early Adolescence,
NRP 57 Satellite Symposium: Non-Ionising Radiation - Health and Environment, Davos, Switzerland, 14 Jun 2009

D.W. McRobbie, M. Oberle, A. Papadaki, R. Quest, K. Hansson Mild, M. Capstick, J. Hand, N. Kuster
Occupational Exposure to Electro-Magnetic Fields in MRI: A Survey of Working Practices from 1 T-7 T,
Poster Presentation at ISMRM Seventeenth Scientific Meeting and Exhibition, Honolulu, Hawaii, USA, 18-24 Apr 2009

M. Murbach, M. Christopoulou, A. Christ, P. Crespo-Valero, M. Zefferer, S. Kühn, P. Achermann, N. Kuster
System to Study CNS Respnses of ELF Modulation and Cortex Versus Subcortical RF Exposures,
Poster Presentation at the Joint Meeting of the Bioelectromagnetics Society and the European BioElectromagnetics Association (BioEM 2009 Davos), Davos, Switzerland, 14-19 Jun 2009

M. Murbach, S. Kühn, M. Christopoulou, A. Christ, P. Achermann, N. Kuster
Evaluation of Artifacts by EEG Electrodes During RF Exposures,
Joint Meeting of the Bioelectromagnetics Society and the European BioElectromagnetics Association (BioEM 2009 Davos), Davos, Switzerland, 14-19 Jun 2009

M. Murbach, M. Mevissen, N. Kuster
Dosimetric Assessment of C. elegans Exposure in Vivo to 900 MHz Electromagnetic Fields,
Poster Presentation at the Joint Meeting of the Bioelectromagnetics Society and the European BioElectromagnetics Association (BioEM 2009 Davos), Davos, Switzerland, 14-19 Jun 2009

E. Neufeld, M. Capstick, M. Notter, G. van Rhoon, M. Oberle, N. Kuster
Hyperthermia Cancer Treatment for the Head and Neck Region: Treatment Planning and Hardware,
Poster Presentation at CTI Medtech Day, Bern, Switzerland, 1 Sep 2009

E. Neufeld, M. Christen, O. Schenk, A. Wächter, N. Kuster
Nonlinear, Temperature Based Optimization for Hyperthermia Treatment Planning Using PDE Constrained Interior Point Optimization,
25th Annual Meeting of the European Society for Hyperthermic Oncology (ESHO 2009), Verona, Italy, 4-6 Jun 2009

E. Neufeld, M. Christen, O. Schenk, A. Wächter, N. Kuster
Nonlinear, Temperature Based Optimization for Hyperthermia Treatment Planning Using PDE Constrained Interior Point Optimization,
Poster Presentation at the Joint Meeting of the Bioelectromagnetics Society and the European BioElectromagnetics Association (BioEM 2009 Davos), Davos, Switzerland, 14-19 Jun 2009

E. Neufeld, S. Kühn, N. Kuster
Measurement, Simulation and Uncertainty Assessment of Implant Heating During MRI,
Joint Meeting of the Bioelectromagnetics Society and the European BioElectromagnetics Association (BioEM 2009 Davos), Davos, Switzerland, 14-19 Jun 2009

E. Neufeld, N. Kuster
Thermal Simulation Platform for (EM Induced) Tissue Heating,
Society for Thermal Medicine 2009 Annual Meeting (STM 2009), Tucson, Arizona, USA, 3-7 Apr 2009

E. Neufeld, N. Kuster
Hyperthermia Treatment Planning and Related Topics at IT'IS,
IM2IM working group meeting of ERCIM, Paris, France, 27-29 May 2009

E. Neufeld, M. Paulides, M. Capstick, G.C. Van Rhoon, N. Kuster
Latest Advances in EM Hyperthermia Cancer Treatments,
International Conference on Electromagnetics in Advanced Applications (ICEAA 09), Torino, Italy, 14-18 Sep 2009

E. Neufeld, D. Szczerba, S. Hirsch, G. Szekely, N. Kuster
In Silicon Model of Tumor Growth and Treatment with Doxorubicin and Heat,
25th Annual Meeting of the European Society for Hyperthermic Oncology (ESHO 2009), Verona, Italy, 4-6 Jun 2009

E. Ofli, N. Kuster
Challenges in Complex Transmitter Development in View of the Increasing RF Requirements (OTA, SAR, HAC),
2009 Loughborough Antennas & Propagation Conference, Loughborough, UK, 16-17 Nov 2009

S. Perov, Q. Balzano, N. Kuster
A Scientific Approach to RF Safety Harmonization,
Joint Meeting of the Bioelectromagnetics Society and the European BioElectromagnetics Association (BioEM 2009 Davos), Davos, Switzerland, 14-19 Jun 2009

S.Y. Perov, Q. Balzano, N. Kuster
Merger of Two Different Dosimetry Rationales,
25th Progress In Electromagnetics Research Symposium (PIERS 2009 Moscow), Moscow, Russian Federation, 18-21 Aug 2009

S. Schild, N. Chavannes, N. Kuster
Challenges and Solutions for the Modeling of Linear and Nonlinear Dispersion Effects with FDTD,
International Conference on Electromagnetics in Advanced Applications (ICEAA 09), Torino, Italy, 14-18 Sep 2009

G. Schmid, A. Christ, R. Djafarzadeh, R. Überbacher, S. Cecil, M. Zefferer, N. Kuster
Whole Body Average SAR In Anatomical Child Models At Plane Wave Exposure in the 2 GHz-5.8 GHz Range,
Poster Presentation at the Joint Meeting of the Bioelectromagnetics Society and the European BioElectromagnetics Association (BioEM 2009 Davos), Davos, Switzerland, 14-19 Jun 2009

G. Vermeeren, M.C. Gosselin, S. Kühn, W. Joseph, L. Martens, N. Kuster
Influence of a Reflective Environment on the Absorption of a Human Male Exposed to Representative Base Station Antennas from 300MHz to 5GHz,
Poster Presentation at the Joint Meeting of the Bioelectromagnetics Society and the European BioElectromagnetics Association (BioEM 2009 Davos), Davos, Switzerland, 14-19 Jun 2009

Equipment for Electronic Test and Physical Characterization

Verification Systems & Logic Analyzers

Digital IC Test System HP83000 F660
660 MHz max test frequency, 10 ps edge resolution, 128 bidirectional test channels, 10 K test vector cache, 1 M test vectors, 4 device power supplies. Manufacturer: Hewlett-Packard/Verigy

Digital IC Test System HP83000 F330t
330 MHz max test frequency, 6 timing edges & 2 data per period per pin, 256 bidirectional test channels, 4 M test vectors, 4 device power supplies. Manufacturer: Hewlett-Packard/Verigy

Hewlett-Packard	HP16702A, Logic Analysis System, IEEE
Tektronix	Tektronix TLA715, Logic Analyzer
Tektronix	Tektronix TLS216, 16-Channel Logic Scope, 500MHz 2GS/s, IEEE

Spectrum & Network Analyzers

Signal Analyzer R&S FSQ 26
Frequency range: 20 Hz to 26.5 GHz, 28 MHz demod. BW, 16 Msample IQ memory, TOI +25 dBm typ., P1dB +13 dBm typ., 84 dB ACLR/3GPP with noise correction. Manufacturer: Rohde & Schwarz

Microwave Vector Network Analyzer HP8720D
Frequency range: 50 MHz to 20 GHz, dynamic range up to 105 dB, fast-sweeping synthesized source, integrated solid-state switching S-parameter test set. Manufacturer: Hewlett-Packard/Agilent

Audio Precision	Audio Precision System S1, Audio Analyzer
Rhode & Schwarz	R&S FSIQ3, Signal Analyzer, 20Hz - 3.5GHz
Rhode & Schwarz	R&S FSP, Spectrum Analyzer, 9Hz - 7GHz
Rhode & Schwarz	R&S FSEB30, Spectrum Analyzer, 20Hz - 7GHz
Agilent	Agilent 8591E, RF Spectrum Analyzer, 9kHz - 1.8GHz
Hewlett-Packard	HP89441A, Vector Signal Analyzer, DC-2650MHz
Hewlett-Packard	HP8751A, Network Analyzer, 5Hz - 500MHz, with HP87511A S-Parameter Set
Hewlett-Packard	HP8753E, Network Analyzer, 30kHz - 6GHz

Scopes

WaveMaster 808Zi SDA Oscilloscope
Bandwidth: 8 GHz, sample rate: 40 GS/s, vertical resolution 8-Bit (11 bit averaging), 4 channels, sensitivity 2mV, Manufacturer: LeCroy

Infiniium 54855 Series Oscilloscope
Bandwidth: 6 (7) GHz, sample rate: 20 GS/s, differential and single-ended, vertical resolution 8-Bit (12 bit averaging), trigger jitter 1.0 ps rms. Manufacturer: Agilent

Tektronix	TDS6804B, 4-Channel Digital Scope, 8 GHz, 20 GS/s
Tektronix	TDS784D, 4-Channel Digital Phosphor Scope, 2GHz, 4GS/s
Tektronix	TDS820, 2-Channel Digitizing Scope, 6GHz
Tektronix	TDS794D, 4-Channel Digitizing Scope, 2GHz 8GS/s, IEEE
Tektronix	TDS684A, 4-Channel Digitizing Scope, 1GHz 5GS/s, IEEE
Tektronix	TDS784, 4-Channel Digitizing Scope, 1GHz 4GS/s, IEEE (2)

Function Generators, Signal Sources

Vector Signal Generator R&S SMU200A
Frequency range: 100 kHz to 6 GHz, SSB phase noise typ. -135 dBc/Hz (f = 1 GHz, 20 kHz), ACLR typ. +70 dB for 3GPP FDD, I/Q modulator 200 MHz RF BW. Manufacturer: Rohde & Schwarz

Vector Signal Generator Agilent E8267C PSG
Frequency range: 250 kHz to 20 GHz, SSB phase noise -130 dBc/Hz (f = 1 GHz, 10 kHz), 160 MHz RF modulation bandwidth, internal baseband generator (80 MHz RFBW). Manufacturer: Agilent

Hewlett-Packard	HP33250A, Function/Arbitrary Waveform Generator, 80MHz
Hewlett-Packard	HP346A, Noise Source, 10MHz - 18GHz
Hewlett-Packard	HP346B, Noise Source, 10MHz - 18GHz
Marconi	Marconi 2042, Low-Noise Signal Generator, 10kHz - 5.4GHz
Rhode & Schwarz	R&S SML01, RF Signal Generator, 1GHz (3)
Rhode & Schwarz	R&S SML03, RF Signal Generator, 3.3GHz (3)
Rhode & Schwarz	R&S SMHU 58, Signal Generator, 100kHz - 4.320GHz
Rhode & Schwarz	R&S SMIQ6 RF Vector Signal Generator, 300kHz - 6.4GHz
Rhode & Schwarz	R&S AMIQ, 2 Channel Arbitrary Waveform Generator, 100MS/s
Stanford Research	Stanford Research DS360, Low-Noise and -Distortion Function Generator, 200kHz
Hewlett-Packard	HP80000, 10 Channel Pattern Generator 1 G Bit/s

Meters

Phase Noise Measurement Solution HP5501B
Frequency range: 50 kHz to 26.5 GHz, offset frequency range: 0.01 Hz to 100 MHz, system noise response: –180 dBc/Hz typ. (>10 kHz offset). Manufacturer: Hewlett-Packard/Agilent

Hewlett-Packard	HP8970B, Noise Figure Meter, 2GHz
Hewlett-Packard	HP4284A, LCR Meter, 20Hz-1MHz, IEEE
Rhode & Schwarz	R&S NRV D, RF Power Meter
UDT	UDT S380, 2-Channel Optometer, IEEE

Power Supplies

Heinzinger	Heinzinger LNC3000-20, Power Supply, 3kV/20mA
FUG	FUG HCN 700-12500, Power Supply, 12,5kV/50mA, IEEE
Kikusui	Kikusui PAK20-18A, Power Supply, 20V/18A (2)
Kikusui	Kikusui PAK6-60A, Power Supply, 6V/60A

Active Probes, Amplifiers & Attenuators

Agilent	Agilent 87405A, Preamplifier 22dB, 10MHz - 3GHz
Agilent	Agilent E2697A, Preamplifier Probe, 7GHz (2)
Agilent	1134A InfiniiMax 7 GHz Probe System (2)
Agilent	E2697A High Impedance Adapter (includes 500 MHz passive probe) (2)
Hewlett-Packard	HP54701A, Active Probes, DC-2.5GHz, 100kOhm (2)
Tektronix	P7380 TekConnect 8 GHz Differential Probe
Tektronix	P7260 TekConnect 6 GHz Single-ended Active Probe (2)
Tektronix	Tektronix P6015, High-Voltage Probe, 20kV
Tektronix	Tektronix P6217, FET Probe, DC-4GHz, 100kOhm (2)
Tektronix	Tektronix AM503, A6302 Current Probe, TM502A Power Rack
Tektronix	Tektronix AM503A, A6303 Current Probe, TM502A Power Rack
Tektronix	Tektronix CT1, 5mV/mA Current Transformer (2)
Tektronix	Tektronix CT2, 1mV/mA Current Transformer (2)
Chase	Chase CPA 9231 Preamplifier, 9kHz - 1GHz
MITEQ	MITEQ AMF-20-001080-20-10P RF Amplifier, 100MHz - 8GHz
Stanford Research	Stanford Research SR560, Low-Noise Preamplifier
Stanford Research	Stanford Research SR570, Low-Noise Current Preamplifier
Rhode & Schwarz	R&S, RF Step Attenuator RSH, DC-5.2GHz

Physical Characterization

Stereoscan 360 Scanning Electron Microscope
Tungsten and LaB6 cathode, 70 nm lateral resolution, secondary and backscattered electrons, absorbed current, electron channeling. Accessories: Tracor Northern Series II EDX spectrometer with thin window and Elprog EBIC amplifier. Manufacturer: Cambridge

C3230 Emission Microscope
S25 detector for the visible range. Time-resolved signal acquisition with 100 ns time resolution. Frequency-resolved signal acquisition by a set of intereference filters. Accessory: Color videoprinter Hitachi VY-300. Manufacturer: Hamamatsu

Nanoscope Dimension 3100 Scanning Probe Microscope
with Quadrex Extender. Available techniques: contact and tapping mode, lateral force, magnetic force, electric force, scanning capacitance and scanning spreading resistance microscopy. Manufacturer: Digital Instruments

FT 1020 Deep-Level Transient Spectroscopy (DLTS) Recorder
Capacitance signal 1 MHz at 5 mV with Boonton bridge. Electrical excitation, fast pulse capability down to 10 ns. Liquid nitrogen cryostat. Manufacturer: Cohausz

Balzers	Balzers SCD 40, Sputter System
Froilabo	Froilabo A, Thermo System
Zivy	Mazali A510Q1, Thermo Test Module
Cohausz	RH2010, Hall Effect Measurement System
Schlieter	Schlieter 125l, Thermo Chamber
Espec	SU241, Temperaturprüfschrank, -40°C - 150°C
Weiss Technik	Weiss 305 SB/10Ju40DU, Environmental Testing Chamber
Hughes	Hughes TVS200, Thermal Video System
IIS	ESD Transmission Line Tester IIS
Key-Tek	MiniZap ESD-Simulator and HBM-Network

Parameter Analyzers

Precision Semiconductor Parameter Analyzer 4156C
Set and control measurements and stress programs, 0.01 fA display resolution at 10 pA range, 0.2 µV resolution in differential mode, performs quasi-static CV and time-to-breakdown measurements. 2 Systems. Manufacturer: Agilent

Hewlett-Packard	HP4142B, Modular DC Source/Monitor
Tektronix	Tektronix Curve Tracer 370

Probers and Utilities

Suss	Suss PA150, Semi Automatic Prober
Suss	Suss PSM6, Submicron Prober
Temptronic	Temptronic Thermo Chuck, 0°C - 200°C
Temptronic	Temptronic TPO4000, Thermo Stream, -60°C - 140°C
Temptronic	Temptronic TPO700A, Thermo Chuck System
Alessi	Alessi LG2, Green Laser Cutting System
Hewlett-Packard	HP4085/4084, Switching Matrix/Control

Optical Microscopes

Nikon	Nikon Optiphot 66, Stereo Microscope
Carl Zeiss	Zeiss Axiophot, Microscope
Carl Zeiss	Zeiss Stemi SV8, Stereo Microscope
Leica	Leica StereoZoom S6E, Stereo Microscope

Optical Characterization Lab

Lightwave Component Analyzer 86030A
Fully vectorial S_{11}, S_{12}, S_{21}, and S_{22} characterization up to 50GHz, supports E/E, E/O, O/E and O/O measurements, full 2-port calibration, up to 90dB dynamic range. Manufacturer: Agilent

Radiometric Goniometer LD8900
Two optical heads covering 320 - 1700nm, +-72° field of view, 0.055° spatial resolution, sensitivity from 100nW to 0.1W, full 3D scan in 10s, supports any laser/LED packaging or fixture. Manufacturer: Photon Inc.

Agilent	Agilent AG 86030A, 50GHz Lightwave Component Analyzer
Ando	ANDO AQ 6317B, Optical Spectrum Analyzer, 600nm - 1750nm
Anritsu	Anritsu MS9601A, Optical Spectrum Analyzer, 1200nm - 1700nm
Bruker	Vertex 70 FT-IR Spectrometer, 780-2500nm
Coherent	Coherent 251, Spectrum Controller & Analyzer (2)
Hewlett-Packard	HP54754A, 2-Channel Differential TDR Module for HP54750A
Agilent	Agilent 4156C, Precision Semiconductor Parameter Analyzer
Hewlett-Packard	HP 8110A, Programmable Current Pulse Generator, 10V 1Hz - 150MHz
Hewlett-Packard	HP54750A Digitizing Oscilloscope with TDR Module HP54754A
Hewlett-Packard	HP8563E, Spectrum Analyzer, 27GHz
ILX Lightwave	ILX LDC-3722, Laser Diode Controller, 50mA
ILX Lightwave	ILX LDC-3742, Laser Diode Controller, 3000mA
ILX Lightwave	ILX LDC-3900, Modular Laser Diode Controller, 3000mA
ILX Lightwave	ILX Lightwave LDX 3412, 200mA Precision Laser Current Source
Laser Precision	AM-3500, Optical Power Meter
Newport	Newport 1835-C, Optical Power Meter, 100fW-300W
Cascade	Cascade 9652-URF, Wafer Probestation
Thorlabs	Thorlabs Intun TL1300-B, Tunable Laser Source, 1278nm - 1390nm
Keithley	Keithley 2601, Precision Current/Voltage Source 3A, 40V
Koheras	Koheras SuperK RED, Supercontinuum Source, 600nm - 2200nm
Advantest	Advantest Q8341, Optical Spectrum Analyzer, 350nm - 1000nm

EDA and TCAD Software

EDA Software

Design tools for the development of Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), and Printed Circuit Boards (PCBs) for education and research.

Integrated EDA Design Flow

Circuit Entry

- Emacs-VHDL Mode: VHDL coding (*D,F*)
- Cadence Virtuoso Schematic Editor: Transistor-level and Verilog, VHDL, C entry (*A,D*)
- Altium Designer - Schematic: Schematic editor (*P*)

Simulation

- Mentor Graphics Modelsim: Mixed-language (VHDL, Verilog, SystemVerilog, SystemC, ...) simulation (*D,F*)
- Cadence NC-Sim: Mixed-language (VHDL, Verilog, SystemVerilog, SystemC, ...) simulation (A,*D*)
- Synopsys Saber: Mixed-technology system simulation (*A,P*)
- Matlab: Algorithm-level behavioral simulation (*A,D,F,P*)
- Synopsys HSPICE: Transistor-level simulation (A)

Synthesis

- Synopsys Design Compiler: RTL synthesis (*D*)
- Cadence RTL Compiler: RTL synthesis (*D*)
- Synopsys Synplify Pro: RTL synthesis (*F*)

Backend Design

- Cadence SoC Encounter: Place and route, GDSII export (*D*)
- Cadence Virtuoso Layout Editor: Custom layout drawing, chip finishing (*A,D*)
- Xilinx ISE Foundation: Map, place and route, program device (*F*)
- Altium Designer - PCB: PCB placement and routing, manufacturing files (*P*)
- Altera Quartus: Place and route, program device (P)

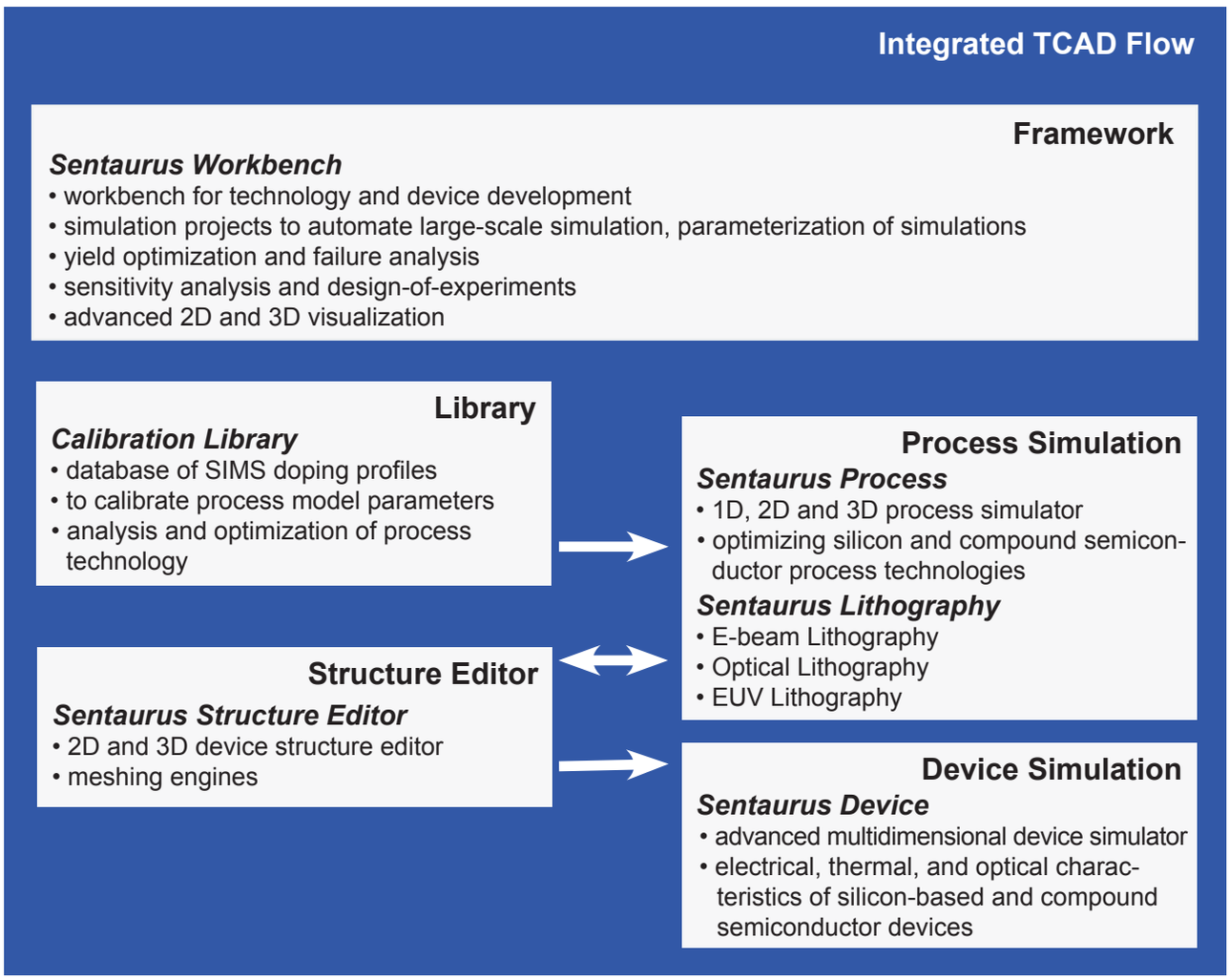
Verification and Test Generation

- Mentor Graphics Calibre: Design-rule check, layout versus schematic, parasitic extraction (*A,D*)
- Cadence Assura: Design-rule check, layout versus schematic, parasitic extraction (*A*)
- Synopsys TetraMax: Automatic test pattern generation (*D*)

Abbreviations
A: Analog ASIC
D: Digital ASIC
F: Field Programmable Gate Array (FPGA)
P: Printed Circuit Board (PCB)

TCAD Software

Technology CAD (TCAD) for technology and device development in nanoelectronics and optoelectronics.
Commercial tools of Synopsys, Inc. used in research and education.

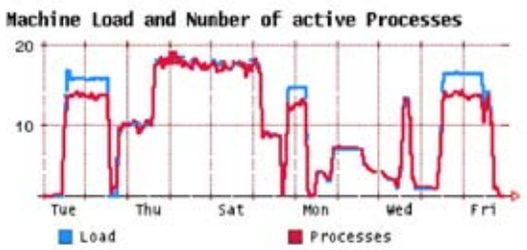


Computer Equipment

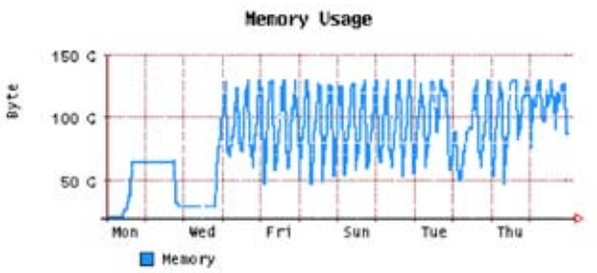
Computers are most relevant tools in teaching and research at IIS. Examples are design of integrated circuits, simulation of circuits, devices and technologies for nanoelectronics, optoelectronics and microsystems, development of application software, and information transfer.

Besides optimal reliability and uncompromising performance, homogeneity of the computing environment and user friendliness are also important. To meet these goals, the computing environment uses the operating system Unix (Linux, Solaris, Mac OS X), networking with NFS V3 and V4 and CIFS (samba), the X-Window System, and the programming languages C++, and Fortran 90/95. Besides the Unix machines in the scientific and technical area, Macintosh computers are widely applied for administration and presentation tasks. A Windows 2003 (x64) terminal server for mainly office applications is also provided. Several Windows PCs are installed for controlling measurement equipment, for lab classes, and for other special applications.

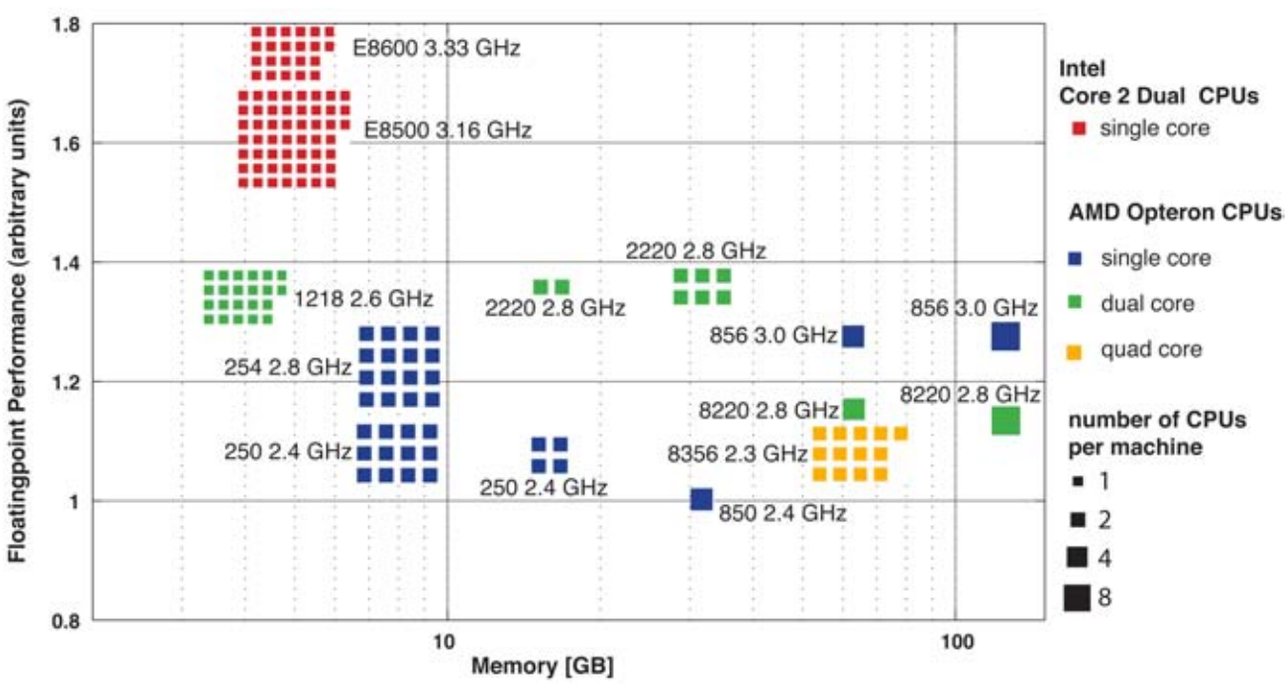
Since the teaching and research activities span many areas, computer systems of various vendors (file servers and linux PCs, mostly from Sun Microsytems) are utilized. They range from file servers to standard workstations, compute servers, and workstations with specialized dedicated hardware. The file systems of all computers are assembled via NFS into what appears to the user as a single file system. The networking of IIS computers and external computers is based on switched Gigabit Ethernet which is maintained by the network group of ETH. Important applications in the technical area are EDA (Modelsim, Synopsys, Cadence, Protel, Mentor Graphics), TCAD (Synopsys), scientific tools (Matlab, Mathematica) as well as publishing and office applications like MS Office and Adobe Creative Suite on Apple Mac computers.



Load and number of active processes of an AMD Opteron server (8 Dual Core CPUs, 128 GB memory) used for physics-based simulations. ('Load' = number of processes in running queue)



Memory usage of an AMD Opteron server (8 CPU cores, 128 GB memory): total physical memory allocation of all processes.

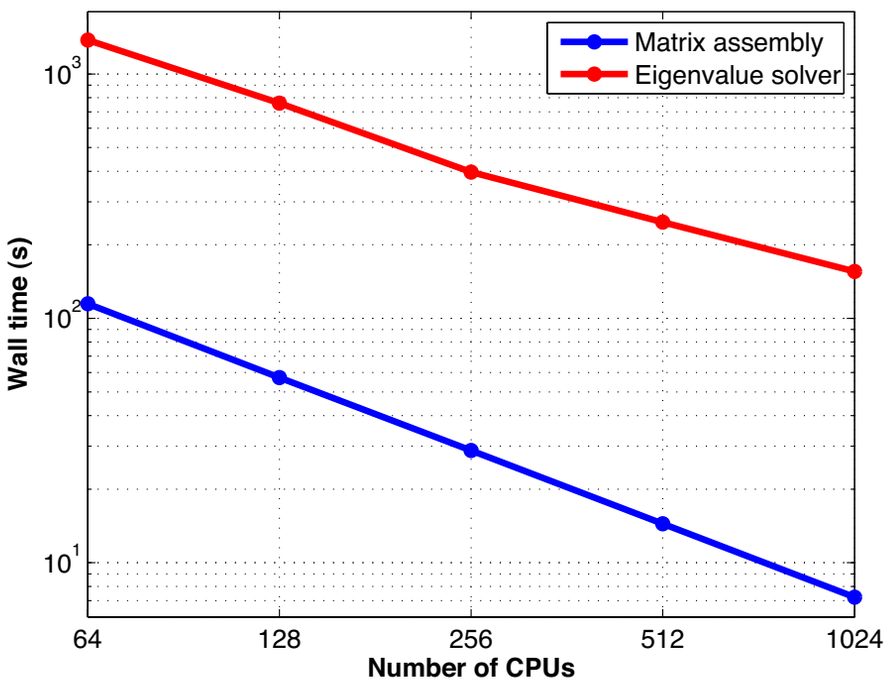


Representative figures of performance of compute servers at the Integrated Systems Laboratory: Relative floating-point performance of one CPU and memory size (Gigabytes) based on a VASP (Vienna Ab Initio Simulation Package) benchmark. The number of machines per architecture is represented by multiple symbols.

The computing equipment of IIS counts four Unix servers, 100 Linux/Solaris workstations, 26 Apple Mac computers, 33 Windows PCs and furthermore 57 powerful shared-memory AMD Opteron based Linux compute servers with 2 - 8 CPUs (2 - 16 cores) in a cluster for physical simulations. The detailed configuration of computers at the Integrated Systems Laboratory, the Department of Information Technology and Electrical Engineering (D-ITET), and the high-power and parallel computing facilities of CSCS (The Swiss Center for Scientific Computing in Manno/Ticino) is shown on page 146.

Quantum mechanical and Monte Carlo simulation of nanoelectronic device operation:

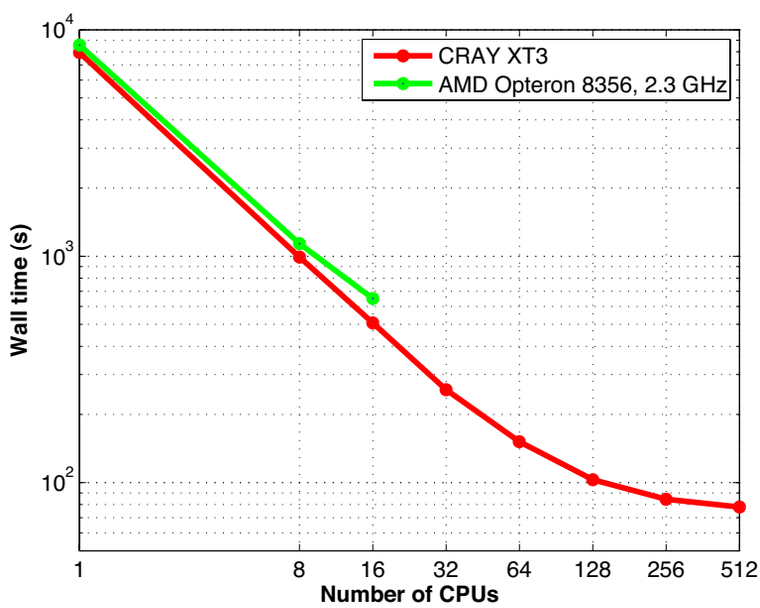
The Monte Carlo code and the quantum transport simulators have been successfully used on the machines in Manno. The figure shows a benchmark on the Cray XT5 for the assembly and solution of a large eigenvalue problem (~30,000 x30,000, full matrix) typically appearing in numerical simulations of nanodevices (e.g. in bandstructure calculations).



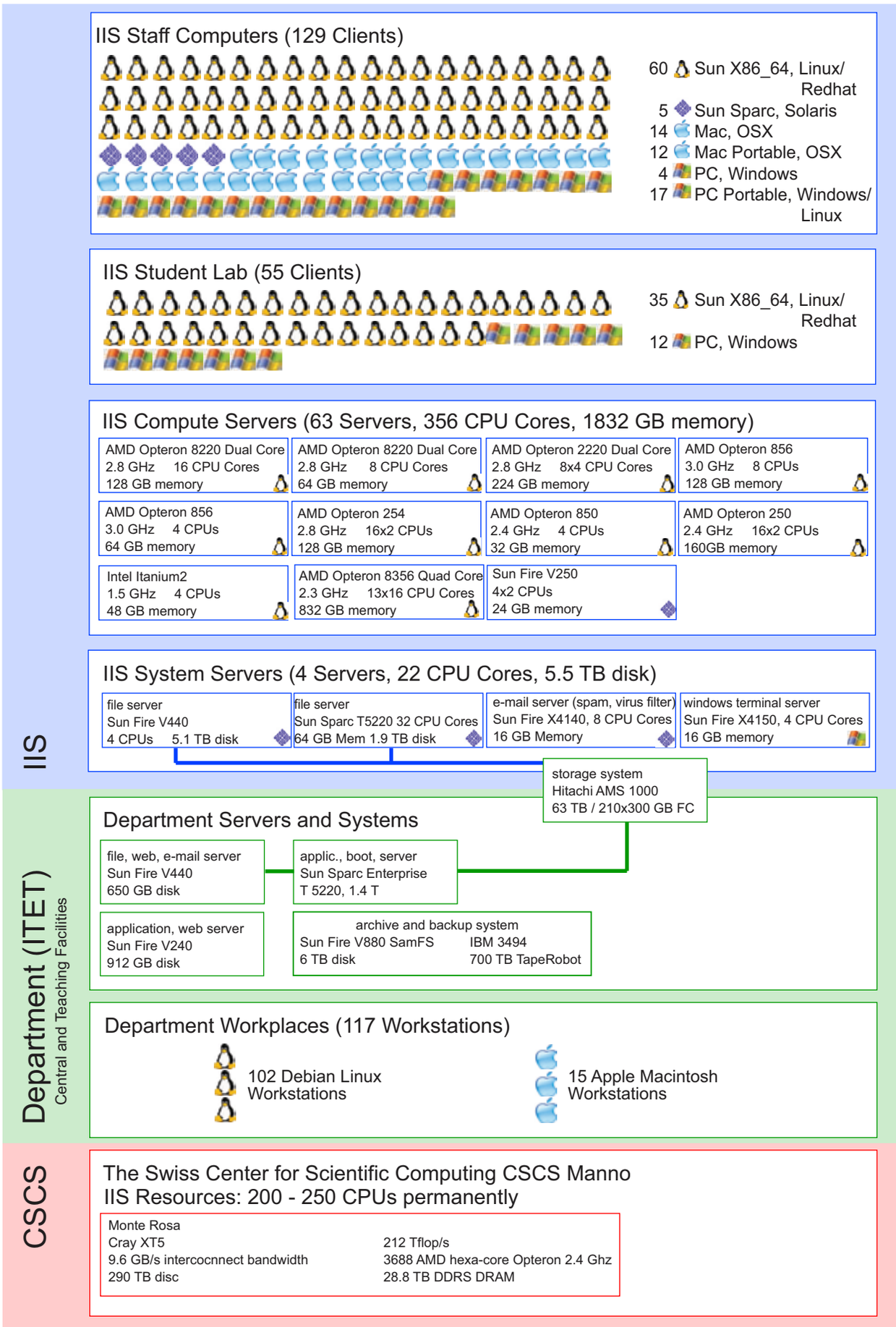
Scaling of diagonalization and assembly times for a typical matrix (~30,000x30,000) on the Cray XT5

Ab initio molecular dynamics simulation of semiconductor processing physics:

Different types of VASP calculations require different numbers of CPUs and have different memory requirements. We have performed extensive benchmarks for typical simulation types. The figure shows the results from the principal benchmark on the Cray XT3 system at CSCS (the predecessor of the XT5 system). The selected benchmark simulation contains 214 silicon atoms and one phosphorus atom. This is a typical system size used for static calculations. On the new Cray XT5 similar results are achieved.



VASP scaling for typical system with 215 atoms on the Cray XT3


IIS
IIS Staff Computers (129 Clients)
60 Sun X86_64, Linux/ Redhat
5 Sun Sparc, Solaris
14 Mac, OSX
12 Mac Portable, OSX
4 PC, Windows
17 PC Portable, Windows/ Linux
IIS Student Lab (55 Clients)
35 Sun X86_64, Linux/ Redhat
12 PC, Windows
IIS Compute Servers (63 Servers, 356 CPU Cores, 1832 GB memory)
AMD Opteron 8220 Dual Core 2.8 GHz 16 CPU Cores 128 GB memory
AMD Opteron 8220 Dual Core 2.8 GHz 8 CPU Cores 64 GB memory
AMD Opteron 2220 Dual Core 2.8 GHz 8x4 CPU Cores 224 GB memory
AMD Opteron 856 3.0 GHz 8 CPUs 128 GB memory
AMD Opteron 856 3.0 GHz 4 CPUs 64 GB memory
AMD Opteron 254 2.8 GHz 16x2 CPUs 128 GB memory
AMD Opteron 850 2.4 GHz 4 CPUs 32 GB memory
AMD Opteron 250 2.4 GHz 16x2 CPUs 160GB memory
Intel Itanium2 1.5 GHz 4 CPUs 48 GB memory
AMD Opteron 8356 Quad Core 2.3 GHz 13x16 CPU Cores 832 GB memory
Sun Fire V250 4x2 CPUs 24 GB memory
IIS System Servers (4 Servers, 22 CPU Cores, 5.5 TB disk)
file server Sun Fire V440 4 CPUs 5.1 TB disk
file server Sun Sparc T5220 32 CPU Cores 64 GB Mem 1.9 TB disk
e-mail server (spam, virus filter) Sun Fire X4140, 8 CPU Cores 16 GB Memory
windows terminal server Sun Fire X4150, 4 CPU Cores 16 GB memory
storage system Hitachi AMS 1000 63 TB / 210x300 GB FC
Department (ITET)
Central and Teaching Facilities
Department Servers and Systems
file, web, e-mail server Sun Fire V440 650 GB disk
applic., boot, server Sun Sparc Enterprise T 5220, 1.4 T
application, web server Sun Fire V240 912 GB disk
archive and backup system
Sun Fire V880 SamFS 6 TB disk
IBM 3494 700 TB TapeRobot
Department Workplaces (117 Workstations)
102 Debian Linux Workstations
15 Apple Macintosh Workstations
CSCS
The Swiss Center for Scientific Computing CSCS Manno
IIS Resources: 200 - 250 CPUs permanently
Monte Rosa
Cray XT5
9.6 GB/s intercocnnect bandwidth
290 TB disc
212 Tflop/s
3688 AMD hexa-core Opteron 2.4 Ghz
28.8 TB DDRS DRAM