ETH zürich

Master / Semester Thesis

Array-level atomistic simulations of resistive memory devices

The Big Picture

Non-volatile memory devices such as Valence-Change Memory (VCM) are potential computing primitives for emerging Neuromorphic architectures. Each device consists of a metal-oxide-metal stack (Fig 1-left), across which an applied voltage results in the generation/diffusion of oxygen vacancies, leading to changes in conductance. When used as memory cells, they are arranged in the form of crossbar arrays where the bit/word lines are pattered above and below a thin film of the oxide (Fig 1-right). Further development of VCM technology would benefit from a detailed physical understanding of how these devices operate at the atomic scale, and how the generated heat and potential gradients can couple across devices in an array.

Description

We have developed a multi-scale model to simulate the operation of single VCM devices, using *ab initio* material parameters extracted from Density Functional Theory (DFT) and a Kinetic Monte Carlo model for atomic movements (Fig 2) which includes graph-based field solvers for potential and temperature gradients. The code developed has since been accelerated to treat larger structures while remaining at an atomistic resolution. We are now interested in doing array-level simulations, treating the bit- and word-lines as boundary conditions at different locations of the oxide. Your project would involve creating atomistic array structures, computing different biasing conditions, with appropriate modifications/new additions to the code, and participating in writing publications or conference papers resulting from this study. If interested, please feel free to contact us to learn more!

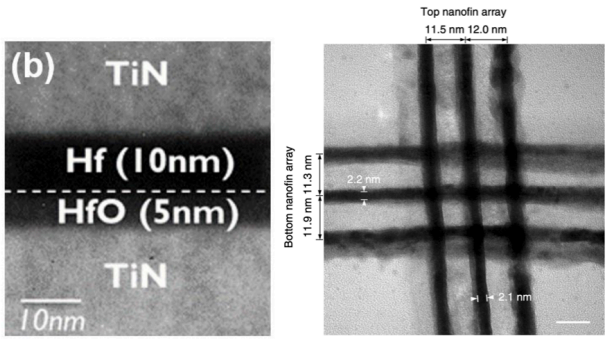

Fig 1: Experimental demonstrations of Hafnium Oxide-based valence change memory devices and arrays from the literature.

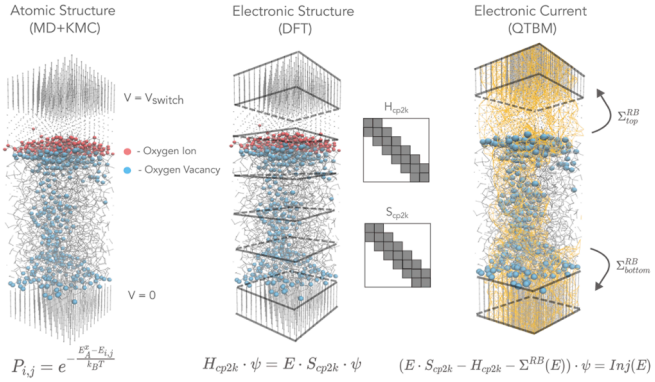

Fig 2: Overview of the atomistic modelling framework developed to simulate the operation of individual valence change memory devices.

Prerequisites

- (Required) An interest in studying the physics of modern nano-electronic and nano-ionic devices
- (Required) Coding experience in C++, or experience with a different language and strong interest in learning C++
- (Optional) Experience accelerating scientific code with CUDA
- (Optional) Knowledge of the operating principles of resistive memory
- (Optional) Experience with atomistic simulation methods such as Molecular Dynamics and Kinetic Monte Carlo

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