Fermi Level Pinning in GaAsSb Schottky Barriers

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1 Abstract

The Millimeter Wave Electronics Laboratory of the ETH investigates Heterojunction Bipolar Transistors and Uni Traveling Carrier diodes for high speed applications. A key element of these devices are metal-semiconductor contacts to the ternary alloy GaAsSb. The work to be undertaken in this master thesis, is to fashion Schottky barrier diodes on GaAsSb and electrically characterize them.

2 Project Description

2.1 Introduction

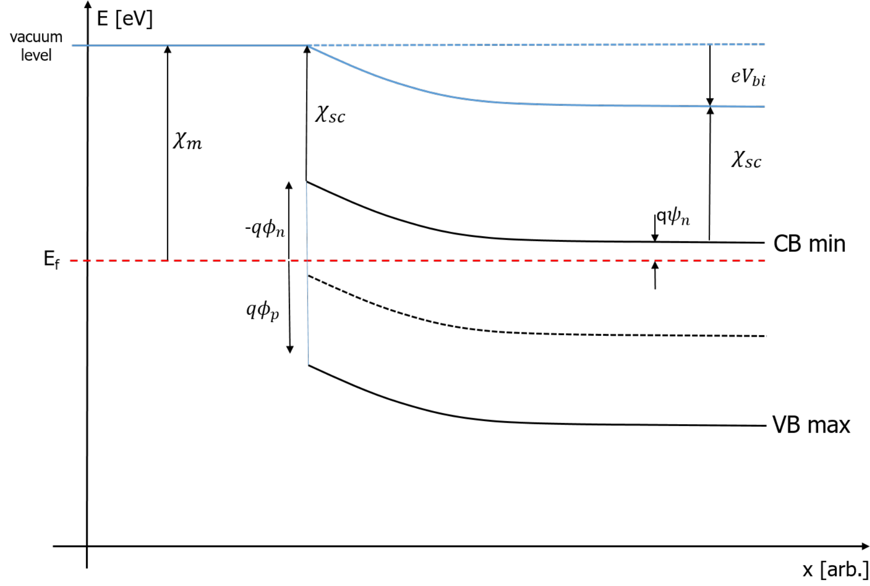
The type - II InP-GaAsSb heterojunction builds the basis for high speed transistors and optoelectronics[1]. One of the key aspects in creating faster and more efficient devices is the metallic contact to the ternary material. However:
"The fundamental physical mechanisms determining the barrier to electron and hole flow at the metal-semiconductor interface in a practical Schottky diode are not well understood. The formation of a practical Schottky diode consists of depositing a metal film onto a real semiconductor surface, a surface which is not ideal but contaminated by a few monolayers of adsorbed foreign atoms or covered by a thin layer of native oxide. In the case of GaAs and some III-V semiconductors, the Fermi level E_f^s at the interface is found to be pinned as a result of surface states and thus almost independent of the metal work function." [2]
In terms of the GaAsSb material system, it is known that

- On InAs, the Fermi level pins at or above the conduction band
- On GaAs, the Fermi level pins near midgap
- On GaSb, it pins near the valence band (0.2 eV above)

Hence it is expected that the Fermi level pinning drifts with alloy composition. There has been no direct measurements of the electrical barrier at the metal-semiconductor contact with GaAsSb or GaInAsSb, though it has a key impact on devices such as HBTs and Photodiodes. It is therefore the aim of this thesis to produce and characterize metal-semiconductor contacts on GaAsSb to gain insight and hopefully improve upon the ohmic contacts in HBTs and UTCs investigated by the MWE ETH.

2.2 Measurements & Information to be gained

Schottky barriers have been treated for example by Crowell and Sze [3] revealing a complex interplay of physical processes, the details of which are omitted as this point.
Both n & p doped samples are to be investigated. The arguments presented here are for n type material (electron Schottky barriers). It is assumed that the arguments hold for p type GaAsSb (hole Schottky barriers).



Equilibrium band diagram of an ideal Schottky barrier

DC IV measurements Fitting the IV characteristic to the diode equation yields values for the barrier ϕ_n and ideality factor η of the metal-semiconductor junction. According to thermal-emission diffusion theory, the diode current is given by [4]

$$J = A^{**}T^2 \exp\left(-\frac{q\phi_{Bn}}{k_B T}\right)\left[\exp\left(\frac{qV_F}{\eta k_B T}\right) - 1\right] \tag{1}$$

where the pre-factor A^{**} is the reduced effective Richardson constant. If tunneling is to be accounted for, it is commonly expressed by the Tsu-Esaki [5] equation:

$$J_{tunn} = \frac{q4\pi m_{teff}}{h^3} \int_{-\infty}^{\infty} T(E)\left[f_m(E) + f_{sc}(E)\right] dE \tag{2}$$

where the tunneling probability $T(E)$ has to be model or fitted.

Activation Energy measurements Rearranging the diode equation reveals the temperature dependence of the diode [6]

$$ln\left(\frac{I_F}{T^2}\right) = ln(AA^{**}) - \frac{q\left(\phi_{Bn} - V_F\right)}{k_B T} \tag{3}$$

Thus measuring a series of IV curves for different temperature, produces an Arrhenius plot (AJ_o/T^2 vs $1000/T$) from which the barrier height ϕ_{Bn} and electrically active area AA^{**} can be extracted.

DC CV measurements Based on the expression for the capacitance of an ideal Schottky diode [6]

$$\frac{1}{C^2} = \frac{2\left(V_{bi} - V - V_{th}\right)}{qN_d\epsilon_o\epsilon_{sc}} \tag{4}$$

the build in potential of the junction V_{bi} can be extracted from capacitance vs voltage measurements, which leads to a connection between Fermi level in the semiconductor and the barrier height [4]

$$q\phi_{Bn} = qV_{bi} + \frac{1}{2}E_g - k_b T ln\left(\frac{N_D}{n_i}\right) \tag{5}$$

refer to the figure for details. The intrinsic carrier concentration is connected to the bandgap via

$$n_i = \sqrt{N_c N_v}\exp\left(-\frac{E_g}{2k_B T}\right) \tag{6}$$

the bandgap terms cancel and one is left with

$$q\phi_{Bn} = qV_{bi} - k_B T ln\left(\frac{N_D}{\sqrt{N_c N_v}}\right) \tag{7}$$

Thus knowing both the doping and the built in potential produces a value for the barrier height. The exact doping can be extracted as [7]

$$N_D = -\frac{2}{q\epsilon_o\epsilon_{sc}}\left[\frac{d}{dV}\frac{1}{C^2}\right]^{-1} \tag{8}$$

Transient Measurements There is a wide variety of time resolved measurements that can be performed on Schottky diodes (e.g. [8] or [9]), which give insight into the transient behavior of the junction and the semiconductor. Should it proof possible within the given time frame and worthwhile, time resolved measurements could be made part of the thesis.

2.3 Processing

Low doped, n & p type GaAsSb on InP is grown by MOCVD and provided. Using five lithography steps the diodes are to be produced:

- Metal 1 - Schottky Contact
- Mesa Etch
- Metal 2 - Ohmic Contact
- Metal 3 - Interconnects & Air Bridges (two lithography steps involved)

To achieve this the following clean room skills are necessary

- lithography - MA6, DUV
- metal evaporation - Plassys II
- wet chemistry - resists and developers (AZ5214E, AZ1518, PMMA50k, MIF726, MIBK)
- wet chemistry - InP & GaAsSb Etch (H_3PO_4,H_2O_2,HCl)
- wet chemistry - metal lift off (DMSO, Acetone, IPA)
- possibly ICP - dry etch GaAsSb

A key step to establish before full process runs, is to determine whether GaAsSb can be wet-etched selectively with respect to a thin 2nm InP etch stop. Should that not be the case, an alternative dry etch method has to be found.

3 Organisation and Working packages

TODO with Ronja

References

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