ETH zürich

Master Project

Millimeter Wave Electronics Laboratory, D-ITET

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Investigation of direct Ohmic contact for GaInAs/GaAsSb/AlInAs/InP based mm-Wave MOSFET

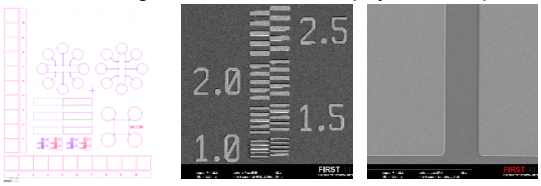
Vision

The III-V n-MOSFETs fabricated in millimetre wave Laboratory (MWE) at ETH Zürich exhibit great potential in designing THz RF electronics (low-noise receiver's sub-blocks) with exceptionally low noise figure and high speed (reaching to 700 GHz). More importantly, the ultra-steep subthreshold slope (SS_{min}) over several orders of magnitude of output current in these transistors paves the way to power-efficient digital circuits. Up to now, the upcoming research is leaning towards the development of III-V CMOS based on high-speed p-MOSFET with the lowest possible SS_{min}. To push our p-MOSFET toward breaking-edge performance, a reliable process for ohmic contact in source and drain is essential. Source and drain Ohmic contact resistances contribute to more than 90% (70%) to all parasitic resistances in III-V p-(n-)MOSFET; any effort on reducing will be beneficial.

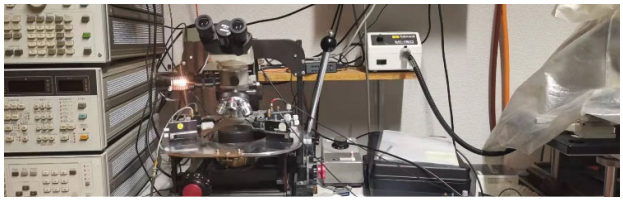
Contact resistance is defined as the resistance associated with current transfer through semiconductor layers, from ohmic metal down to the channel. To achieve lower contact resistances, one possible way is to directly contact conductive channel with ohmic metal by etching appropriate semiconductor layers and deposit metallization directly on GaAsSb and/or GaInAs channel.

Thesis Description

The investigation of achieving direct Ohmic contacts relies on processing InP-based wafers with custom-designed epitaxial layers. Knowledge of semiconductor physics and processing



TLM layout (left) and SEM image of TLM (middle&right)



DC prober in MWE Lab

techniques together with van-der-Pauw measurements techniques of the manufactured TLM structures be gained. The goal of this project is to obtain new and improved ohmic contact geometry in the field, and to offer well-functioning ohmic contact for future III-V n-MOS and p-MOS design.

You will

- Obtain competitive theoretical and practical experience working on ohmic contact formation for the world-leading low-noise transistors.
- Learn practical knowledge about processing compound semiconductor devices in the cleanroom together with general processing/characterization techniques, including dry/wet chemistry etching, photolithography, atomic layer deposition (ALD), SEM, and ebeam metal deposition.
- sssParticipate academic writing and presentations.

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