ETH zürich

Master Thesis

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Characterization and Small-Signal Modelling of an Ultra-Low Noise InP High Electron Mobility Transistor (HEMT) Technology

Project Description

The goal of this master thesis is to develop a scalable small-signal model for a state-of-the-art InP High Electron Mobility Transistor (HEMT) technology in collaboration with Diramics. The circuit model shall predict the small-signal and noise behavior for a range of transistor sizes at room and cryogenic temperatures. A scalable model will allow for a better understanding of the technology and enables an easier selection of the optimum device size for a certain application.

InP HEMTs are of great interest for high-gain and low-noise applications both at room and cryogenic temperatures. Precise circuit models are critical to obtain the ultimate performance and keep the number of amplifier design iterations low. Existing extraction methods for small-signal model elements based on single device sizes often lead to multiple or unphysical solutions. The extraction of a scalable model simultaneously based on several device types on the other hand will make the extraction process more reliable and immune against the problem of ambiguous and unphysical solutions.

For this reason, this master project will focus on extending the existing small signal model extraction routine and investigate the behavior of each single small signal model element as a function of the device size (number of gate finger and gate finger width). The work will include RF and noise measurements of a series of InP HEMTs at room and cryogenic temperatures, small signal model extractions as well as a several circuit and EM simulations.

Thesis Description

1. **Introduction**
   - Understand the existing small signal model and its parameter extraction.
   - Get to know the circuit simulator.
2. **Main part**
   - Measure S-parameters and noise of a series of HEMTs with different number of gate fingers and gate finger widths.
   - Do the small signal extraction for all measured transistor types.
   - Investigate the behavior of each small signal element as a function of the device size and find suitable scaling rules for each element.
   - Implement a small-signal model using these scaling rules and do a verification using additional transistor sizes.
3. **Outlook**
   - What are the limitations of the new model? Do you have ideas for improvements?

You will

- Obtain competitive experience working on the world-leading-level low-noise transistors.
- Run circuit and EM-simulations in PathWave Advanced Design System and PathWave EM Design
- Learn about high frequency and noise measurements, device modeling…