Optimization of the field-plate geometry for GaN-based HEMTs

Semester project, ETH Zürich, D-ITET, MWE laboratory (Prof. Bolognesi)
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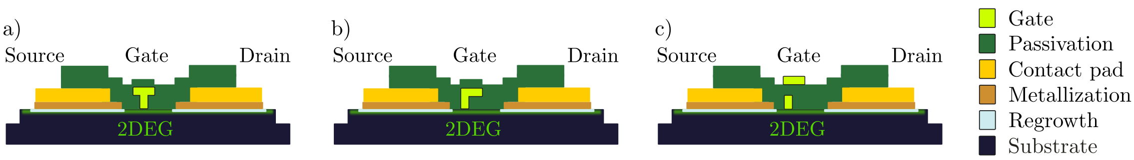
Studies:	Master in Electrical Engineering and Information Technology
Project:	Semester project: 250 - 300 hours, 8 credit points (description here)
Office location:	ETH Hönggerberg
Office requirements:	Computer to carry out simulations
Starting date:	15.10.2015 (alternative: 22.10.2015)

Contents

1 Project Description

In this semester project a Gallium Nitride (GaN) based High-Electron Mobility Transistor (HEMT) will be optimized for high breakdown voltages: three basic field-plate geometries are simulated and compared to experimental results. Finally, based on the experimentally verified model, a new, optimized field-plate design will be proposed by the student.

A field-plate is used to reshape the electrical field distribution and reduces its peak value at the drain-side of the gate: This minimizes the risk of a break-down at the drain side and hinders high field trapping of electrons. A well designed field plate maximizes the off-state breakdown voltage BV_{off} without considerable decrease in the current gain cutoff frequency f_{T}. For GaN-based HEMT transistors the product $f_{\text{T}} \times BV_{\text{off}}$ is roughly ~ 5 THz $\times$ V. Here, we are aiming for $BV_{\text{off}} > 100V$ (i. e. $f_{\text{T}} \approx 50$ GHz).



The figure shows the simplified cross section of three basic field-plate geometries a), b) and c). They were chosen as a starting point for the project and are currently fabricated in the MWE-laboratory. Device type a) has a symmetric field plate and is expected to show higher breakdown voltages than a device geometry without any field plate. Device type b) shapes the field more towards the drain-side and is expected to outperform a) used in e.g. [2]. In c) the field plate is also oriented towards the drain and is connected to the gate-foot at the end point of the gate. Compared to b) an additional passivation layer is used between the field-plate and the gate-foot [3].

Experimentally, this semester project offers the student to gain experience in the characterization and measurements of high-power transistors. Theoretically, the electrical field in the gate region will be simulated for the three different field-plate geometries and will be compared to the measured break-down voltages. Once the developed model can predict the behavior of the three starting field-plate geometries it will be used to improve future devices. For example, one promising, but fabrication-wise more challenging route is a slant field plate device as described in [4].

The optimized field-plate design developed in this Semester thesis can be used to start a Master thesis project, which involves the fabrication of the optimized field plate design in the FIRST-cleanroom.

References

[1] R. Pengelly, S. Wood, J. Milligan, S. Sheppard, and W. Pribble, Microwave Theory and Techniques, IEEE Transactions on **60**, 1764–1783 (2012).

[2] Q. Fareed, A. Tarakji, J. Dion, M. Islam, V. Adivarahan, and A. Khan, physica status solidi (c) **8**, 2454–2456 (2011).

[3] V. Palankovski, S. Vitanov, and R. Quay, in *Compound Semiconductor Integrated Circuit Symposium, 2006. CSIC 2006. IEEE* (2006) pp. 107–110.

[4] K. Kobayashi, S. Hatakeyama, T. Yoshida, Y. Yabe, D. Piedra, T. Palacios, T. Otsuji, and T. Suemitsu, Applied Physics Express **7**, 096501 (2014).

2 Organisation and Working packages

- Preparation of a written report and presentation

- ☐ **Introduction:**
  - ☐ Choice of the simulator
  - ☐ Definition of source, gate, drain contacts: Simulation of IV-curves to verify the influence of the gate-bias on the source-drain current
- ☐ **Main part:**
  - ☐ Identification of critical electrical field points depending on the bias point (when does the transistor break down?)
  - ☐ How do the different field-plate configurations mend the critical field points?
  - ☐ Prediction of break-down voltages based on the electrical field simulations
  - ☐ Comparison with experimental results
- ☐ **Outlook:** Optimized design- and fabrication-proposal