ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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Three-Phase PFC Rectifier and AC-AC Converter Systems

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Outline

60 Min
- Introduction to Three-Phase PFC Rectifier Systems
- Passive and Hybrid Rectifier Systems

15 Min

50 Min
- Unidir. Phase-Modular PFC Rectifier Systems
- Unidir. Boost-Type Two- and Three-Level Active PFC Rectifier Syst.

15 Min

45 Min
- Unidir. Buck-Type PFC Rectifier Systems
- Summary of Unidir. Rectifier Systems

15 Min

40 Min
- Bidirectional PFC Rectifier Systems
- Extension to AC/DC/AC and AC/AC Converter Systems
- Conclusions / Questions / Discussion

- Multi-Domain Simulator Based Design (GECKO) GeckoCIRCUITS

Part 1

Three-Phase PFC Rectifier Systems

Outline

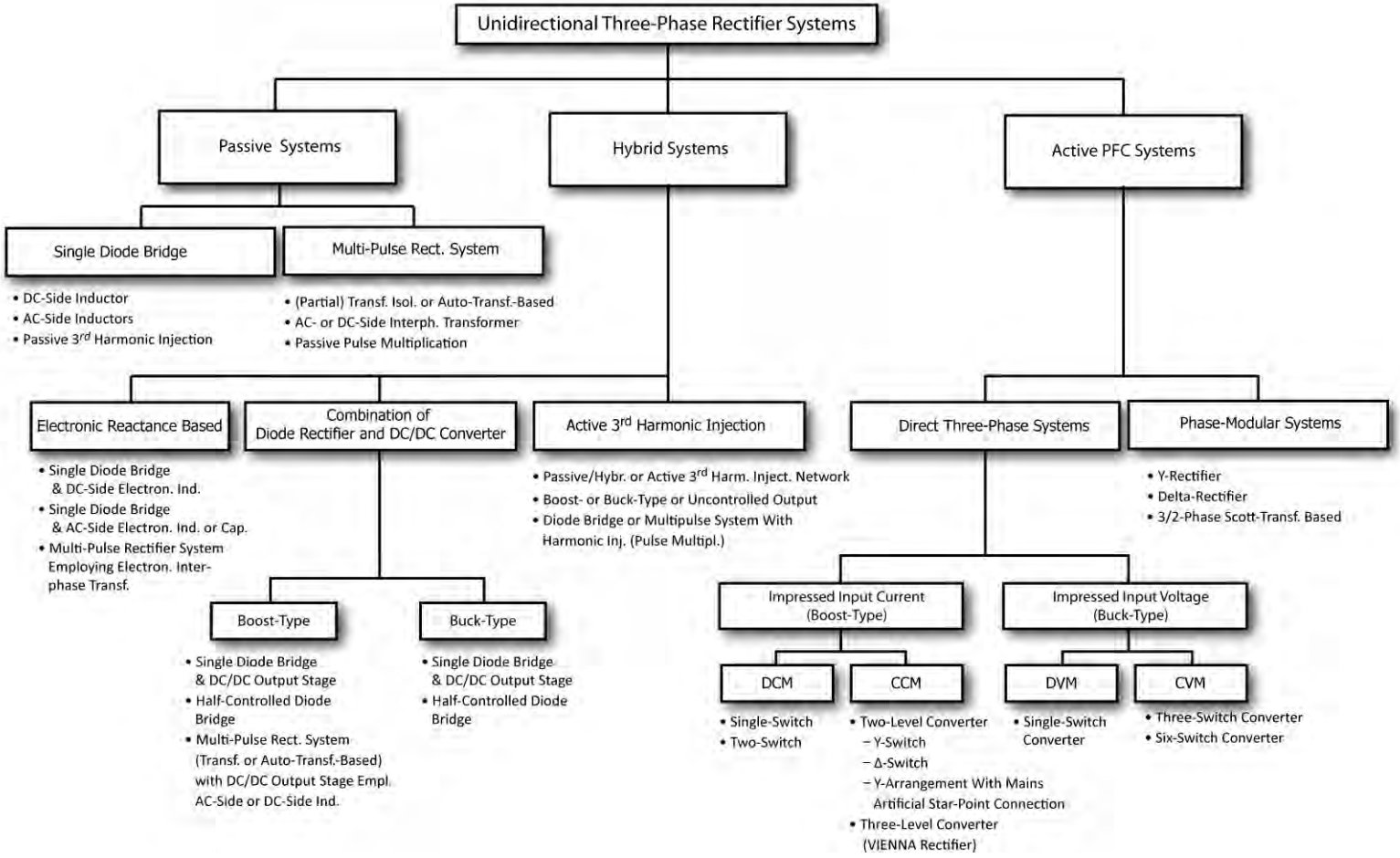
Unidirectional Rectifier Systems

- Passive Systems
- Hybrid Systems
- Active PFC Systems
- Comparative Evaluation

Bidirectional Rectifier Systems

- Two-Level Converters
- Three-Level Converters

▶ Classification of Unidirectional Rectifier Systems



▶ Classification of Unidirectional Rectifier Systems

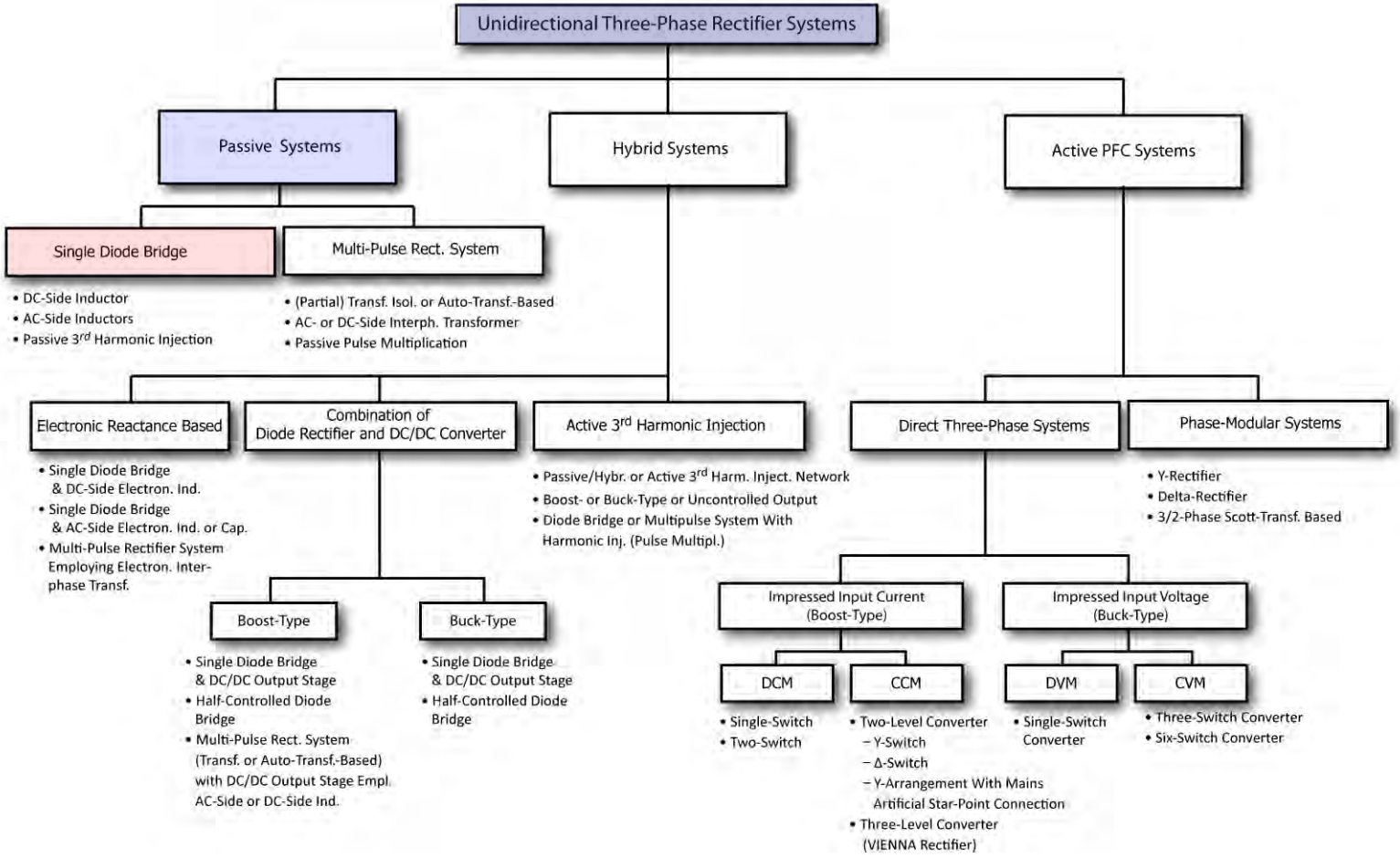
■ Definitions and Characteristics

- **Passive Rectifier Systems**
  - Line Commutated Diode Bridge/Thyristor Bridge - Full/Half Controlled
  - Low Frequency Output Capacitor for DC Voltage Smoothing
  - Only Low Frequency Passive Components Employed for Current Shaping, No Active Current Control
  - No Active Output Voltage Control
- **Hybrid Rectifier Systems**
  - Low Frequency and Switching Frequency Passive Components and/or
  - Mains Commutation (Diode/Thyristor Bridge - Full/Half Controlled) and/or Forced Commutation
  - Partly Only Current Shaping/Control and/or Only Output Voltage Control
  - Partly Featuring Purely Sinusoidal Mains Current
- **Active Rectifier Systems**
  - Controlled Output Voltage
  - Controlled (Sinusoidal) Input Current
  - Only Forced Commutations / Switching Frequ. Passive Components

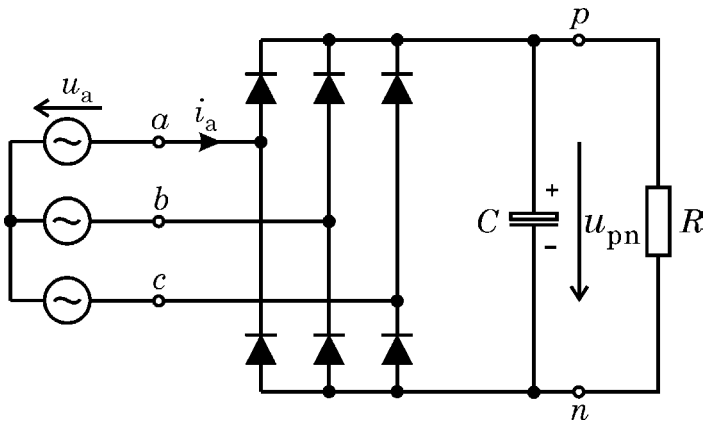
■ **Phase-Modular Systems**
- Phase Rectifier Modules of Identical Structure
- Phase Modules connected in Star or in Delta
- Formation of Three Independent Controlled DC Output Voltages

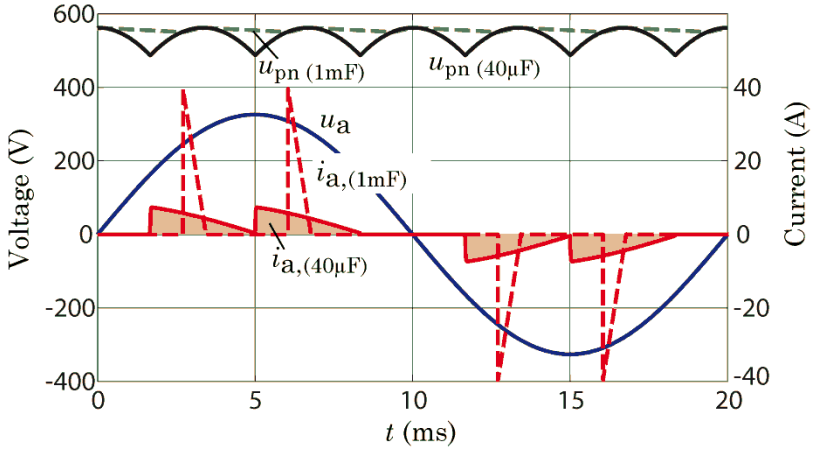
■ **Direct Three-Phase Syst.**
- Only One Common Output Voltage for All Phases
- Symmetrical Structure of the Phase Legs
- Phase (and/or Bridge-)Legs Connected either in Star or Delta

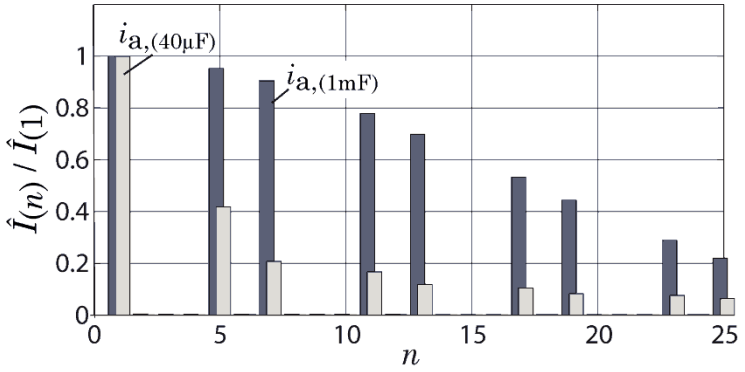
▶ Classification of Unidirectional Rectifier Systems



▶ Diode Bridge Rectifier with Capacitive Smoothing

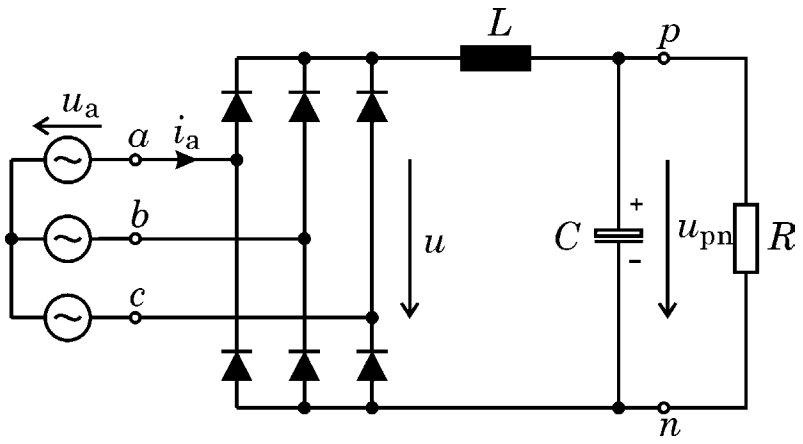


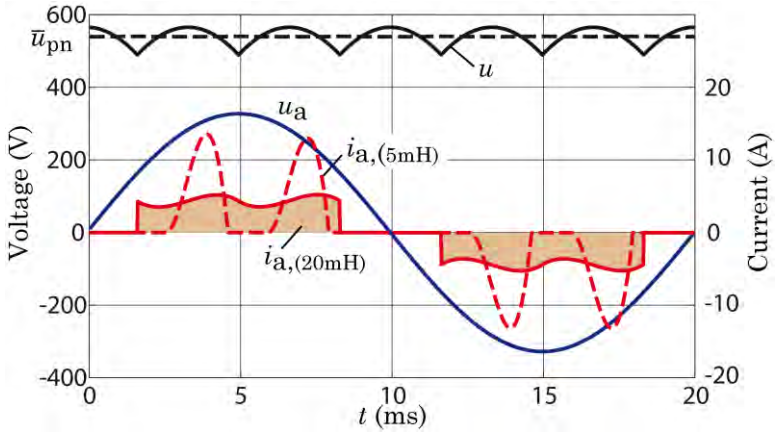




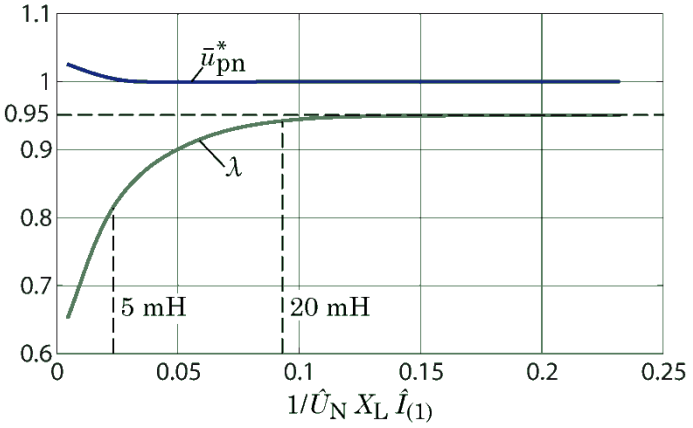
U_{LL} = 3 x 400 V
f_N = 50 Hz
P_{out} = 2.5 kW (R=125 Ω)
C = 1 mF; 40 µF
X_c/R = 0.025; 0.636

▶ Diode Bridge Rectifier / DC-Side Inductor and Output Capacitor



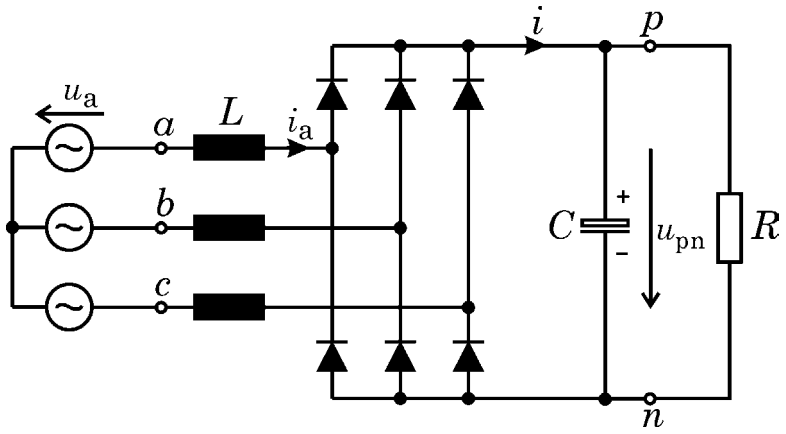


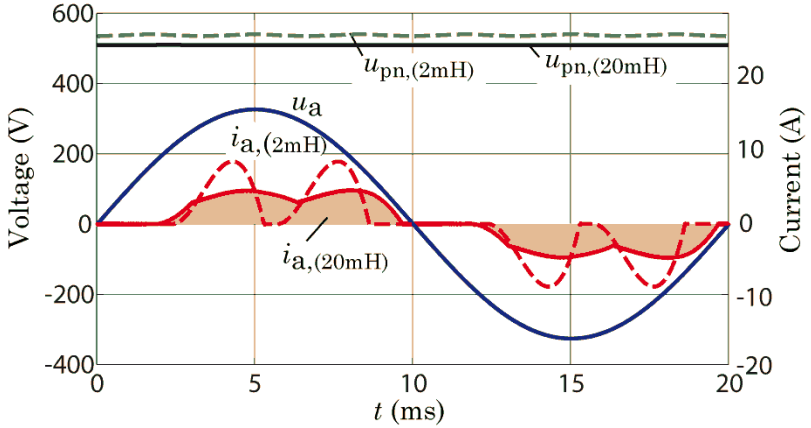
$$\bar{u}^*_{pn} = \frac{\bar{u}_{pn}}{\frac{\pi}{3}\hat{U}_{N,LL}}$$



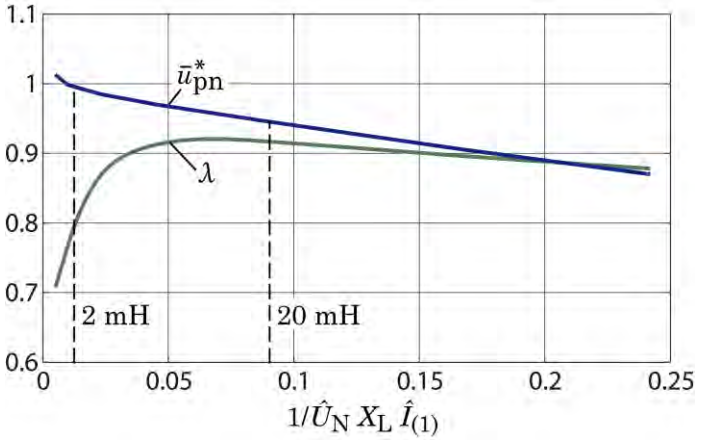
U_{LL} = 3 x 400 V
f_N = 50 Hz
P_{out} = 2.5 kW (R=125 Ω)
C = 1 mF
L = 5 mH; 20 mH

▶ Diode Bridge Rectifier / AC-Side Inductor and Output Capacitor



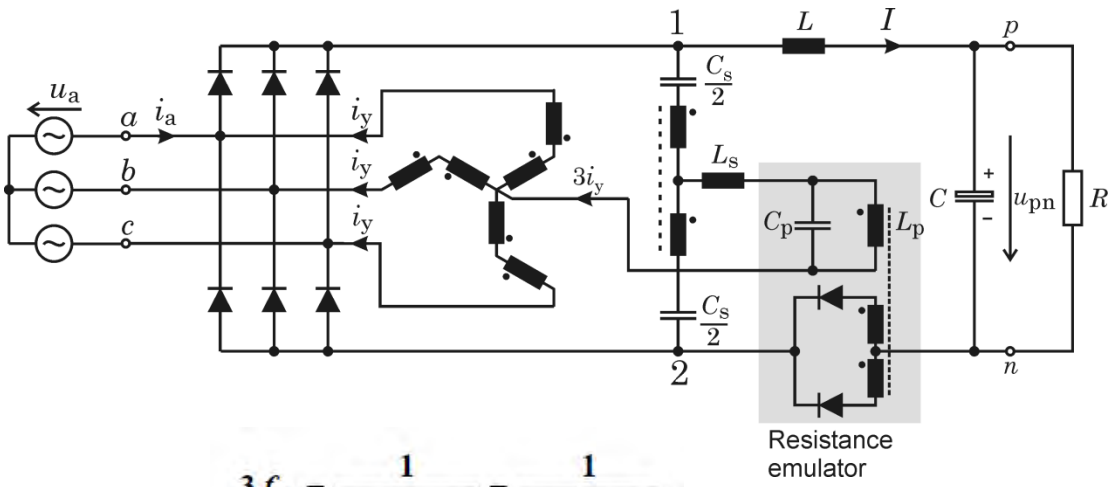


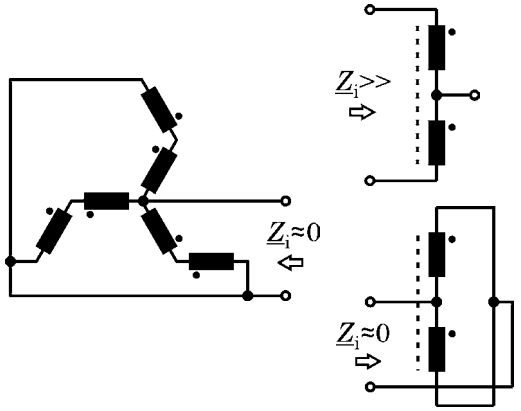
$$\bar{u}_{pn}^{*} = \frac{\bar{u}_{pn}}{\frac{\pi}{3}\hat{U}_{N,LL}}$$



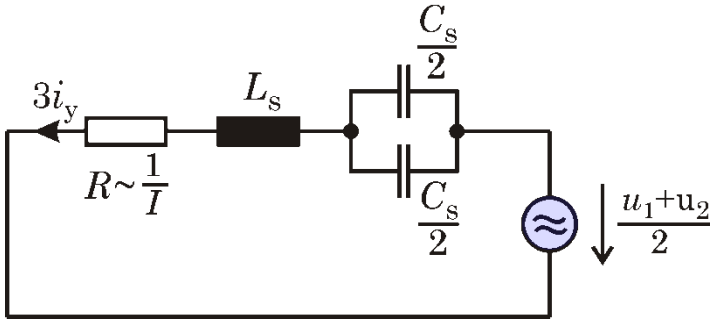
U_{LL} = 3 x 400 V
f_N = 50 Hz
P_{out} = 2.5 kW (R=125 Ω)
C = 1 mF
L = 2 mH; 20 mH

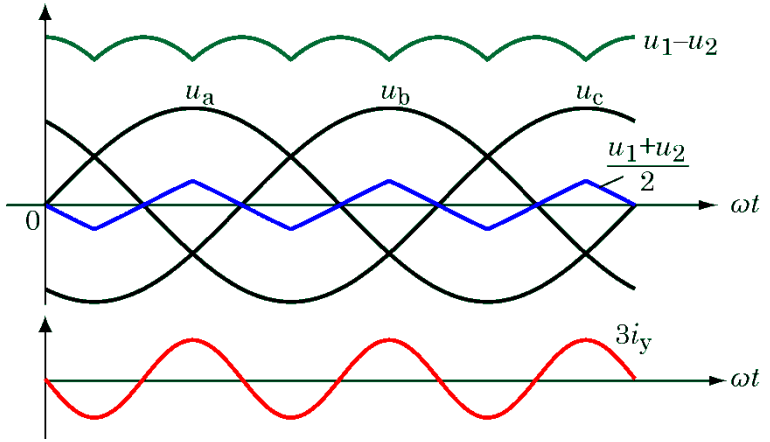
▶ Passive 3rd Harmonic Injection



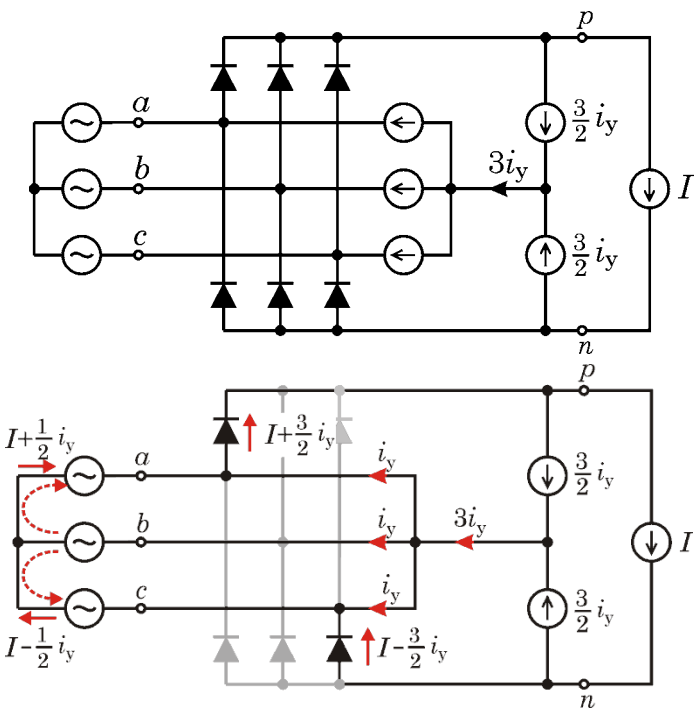


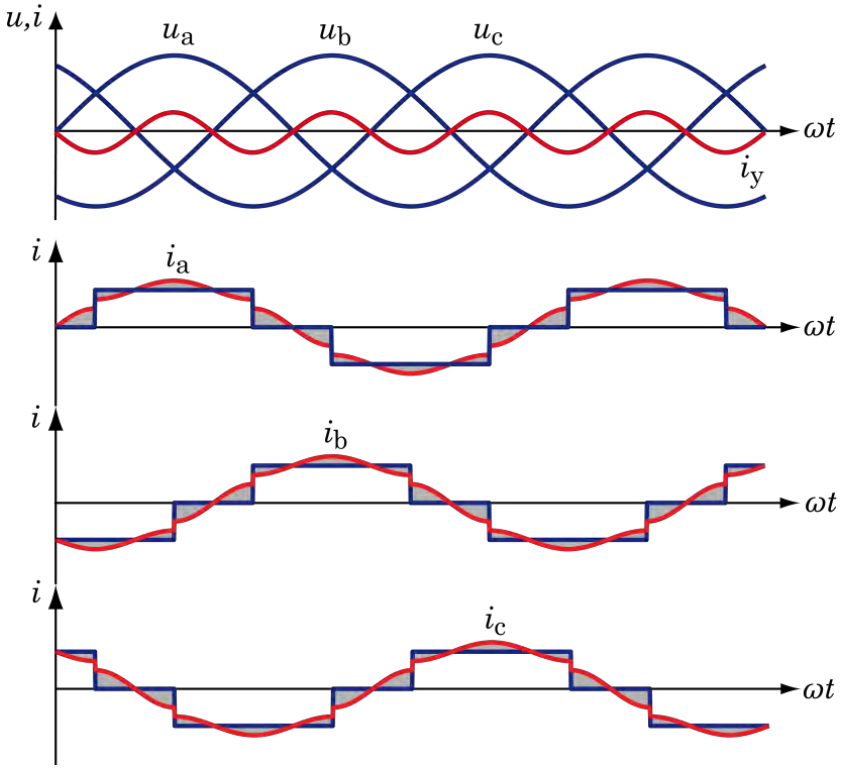
$$3f_N = \frac{1}{2\pi\sqrt{L_S C_S}} = \frac{1}{2\pi\sqrt{L_p C_p}}$$





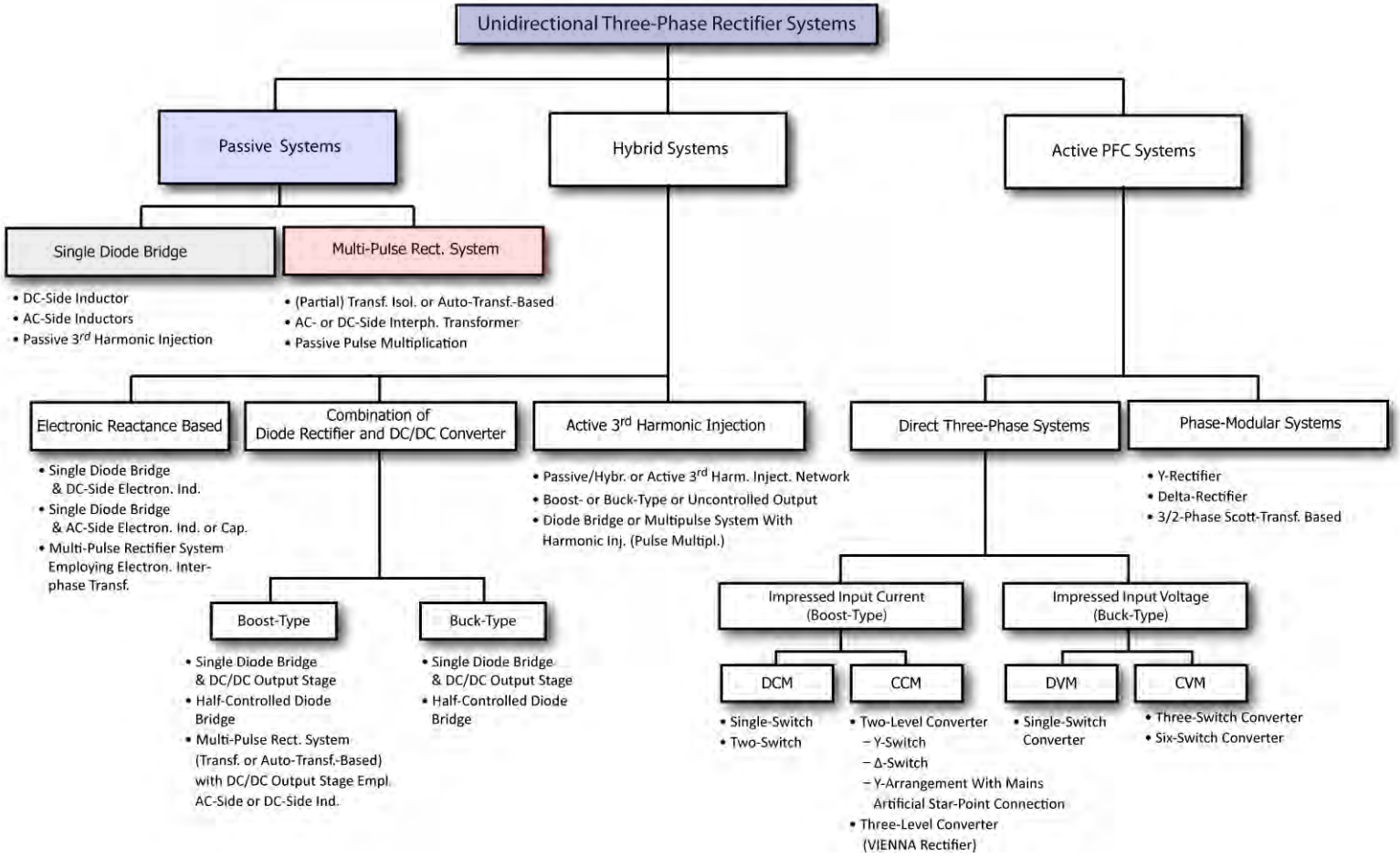
▶ Passive 3rd Harmonic Injection





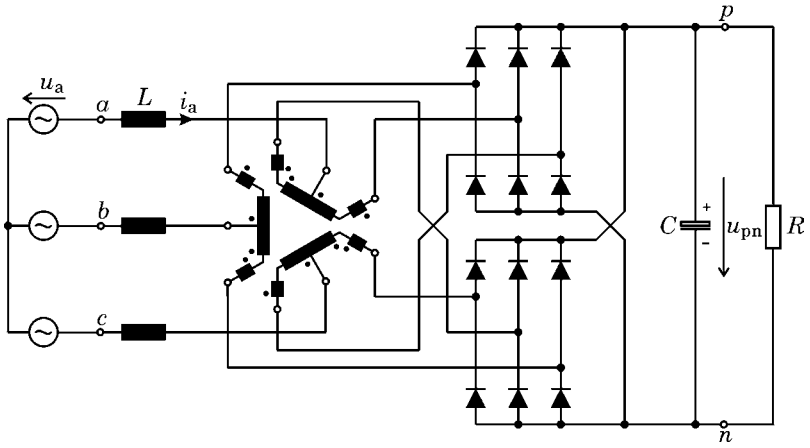
- Minimum THD of Phase Current for $i_y = 1/2\ I$
- $THD_{min} = 5\ \%$

▶ Classification of Unidirectional Rectifier Systems

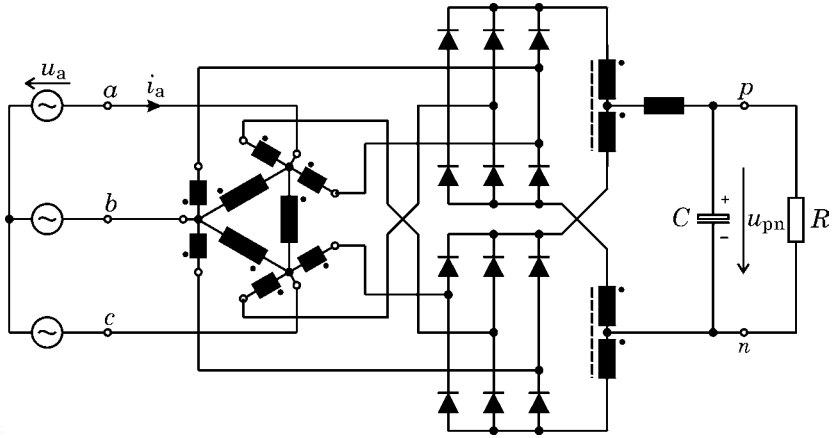


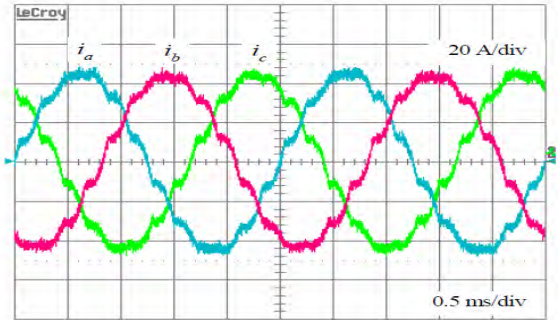
▶ Auto-Transformer-Based-12-Pulse Rectifier Systems

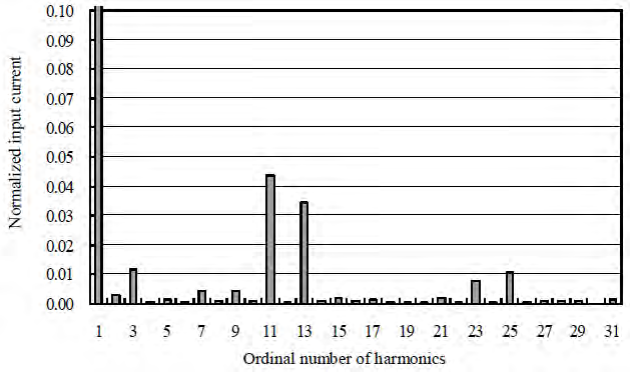
■ AC-Side Interphase Transf. (Impr. DC Voltage)



■ DC-Side Interphase Transf. (Impr. DC Current)

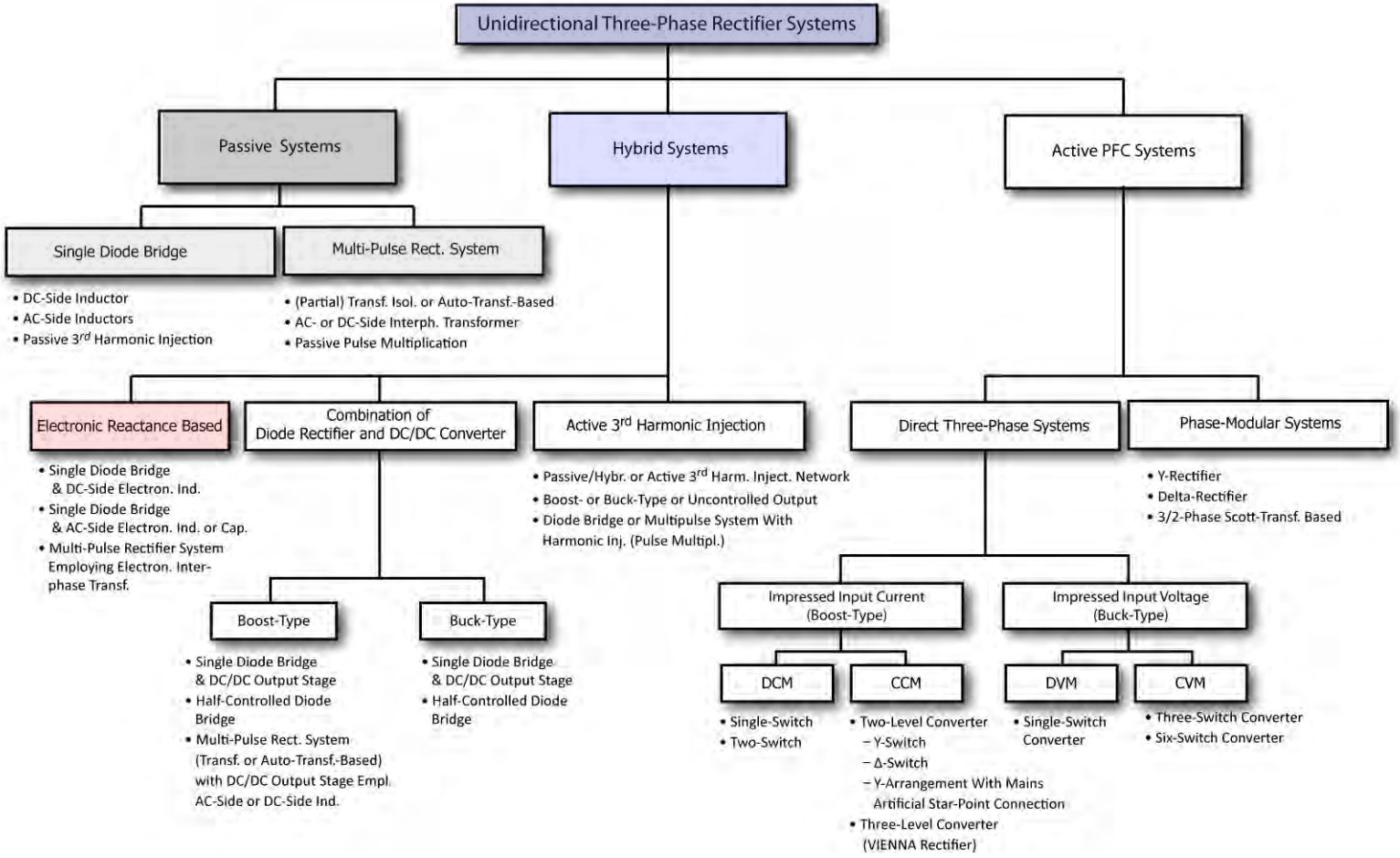




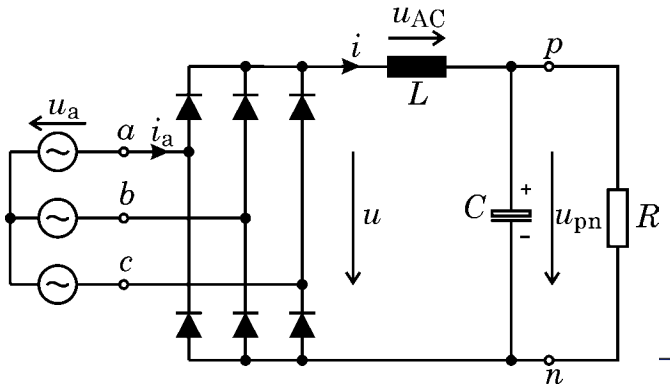


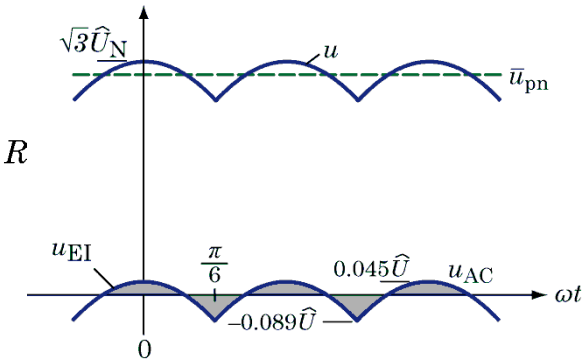
DC-Side Interphase Transformer can be omitted in Case of Full Transformer Isolation of Both Diode Bridges

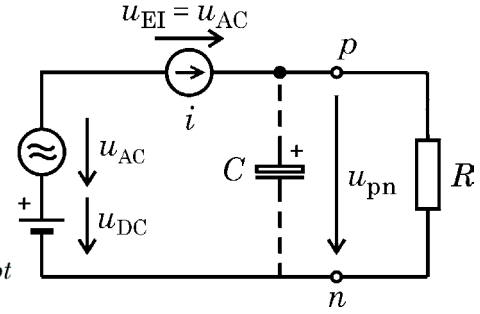
▶ Classification of Unidirectional Rectifier Systems



▶ Diode Bridge and DC-Side Electronic Inductor (EI)

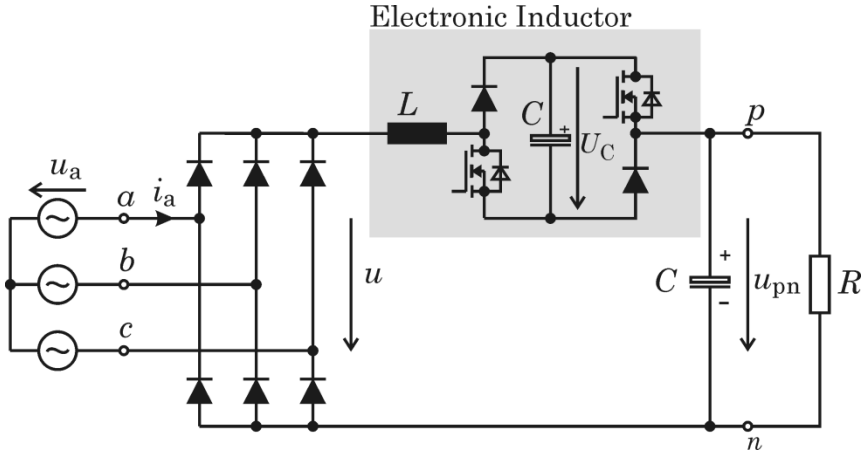






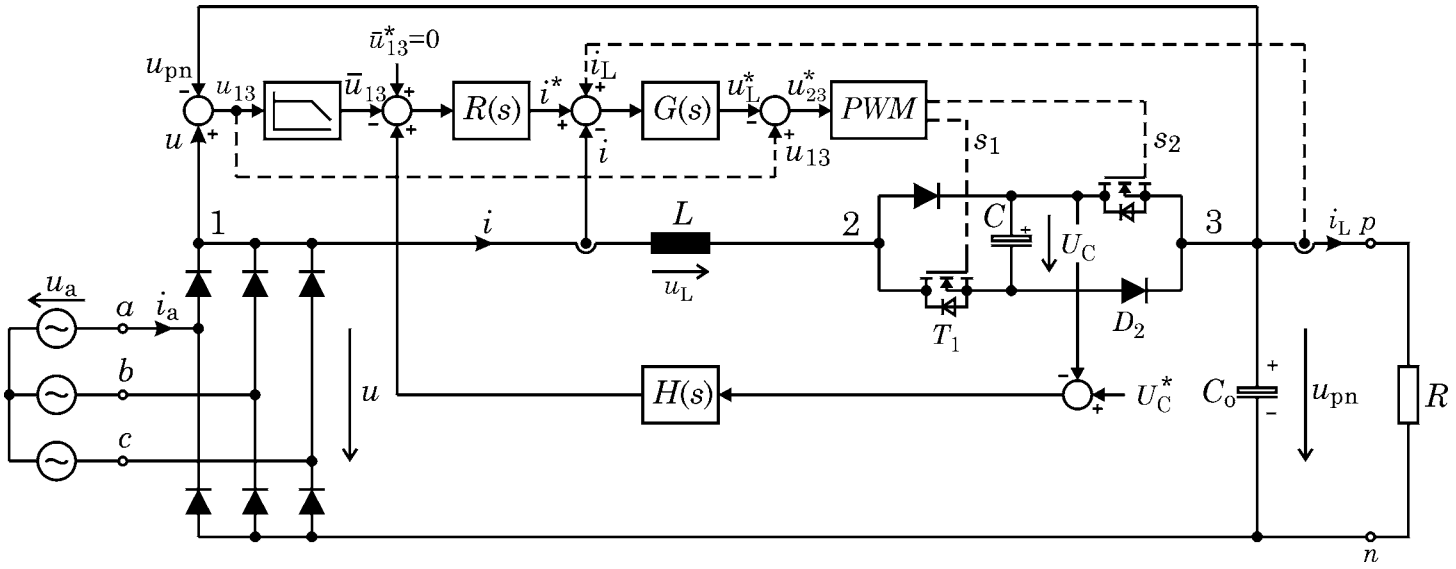
+ Only Fract. of Output Power Processed
+ High Efficiency and Power Density

– Not Output Voltage Control
– EMI Filtering Required



▶ Diode Bridge and DC-Side Electronic Inductor (EI)

■ Control Structure



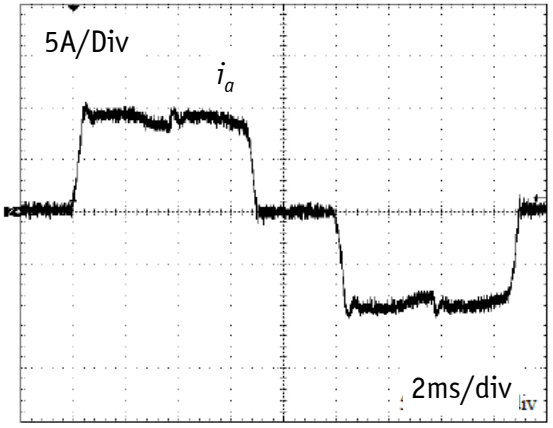
- Current Control could Theoretically Emulate Infinite Inductance Value but Damping (Parallel Ohmic Component) has to be Provided for Preventing Oscillations

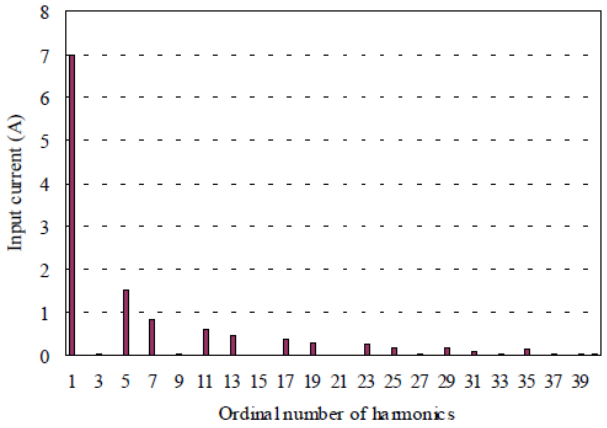
▶ Diode Bridge and DC-Side Electronic Inductor (EI)

■ Experimental Results

U_{LL} = 3 x 400 V
P_o = 5 kW
f_s = 70 kHz
C = 4 x 330 µF /100 V

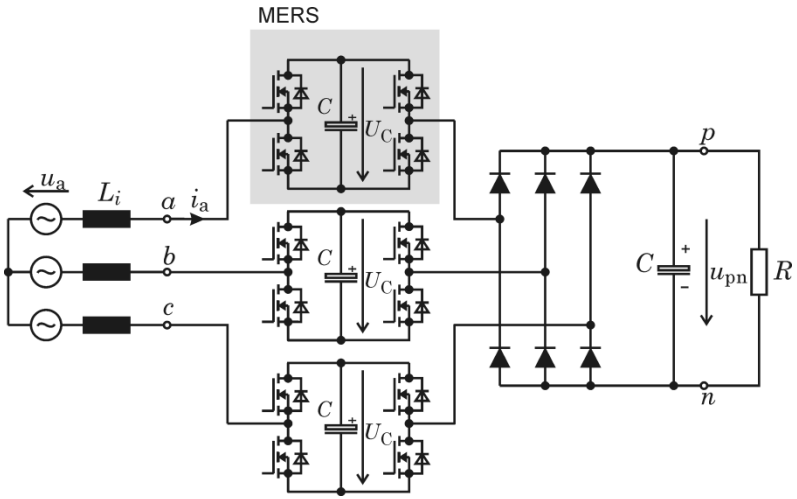
η = 98.3 %
λ = 0.955
THD = 28.4 %

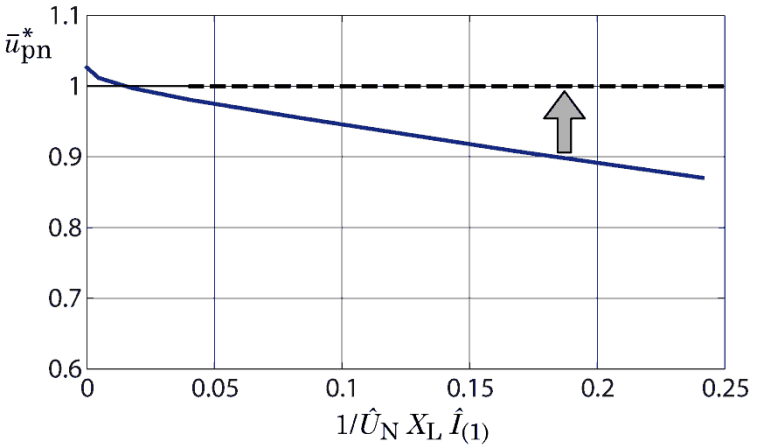




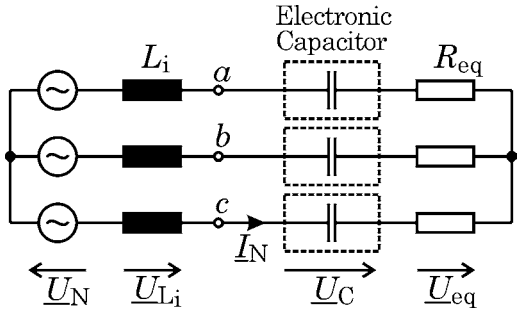
▶ Diode Bridge and DC-Side EI or Electronic Capacitor

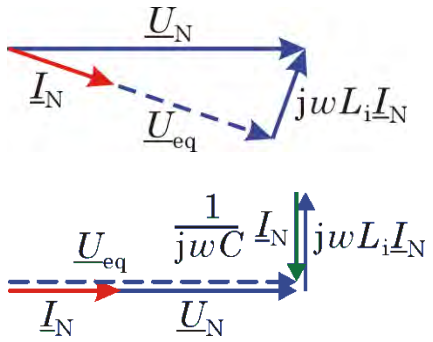
■ MERS Concept (Magnetic Energy Recovery Switch)



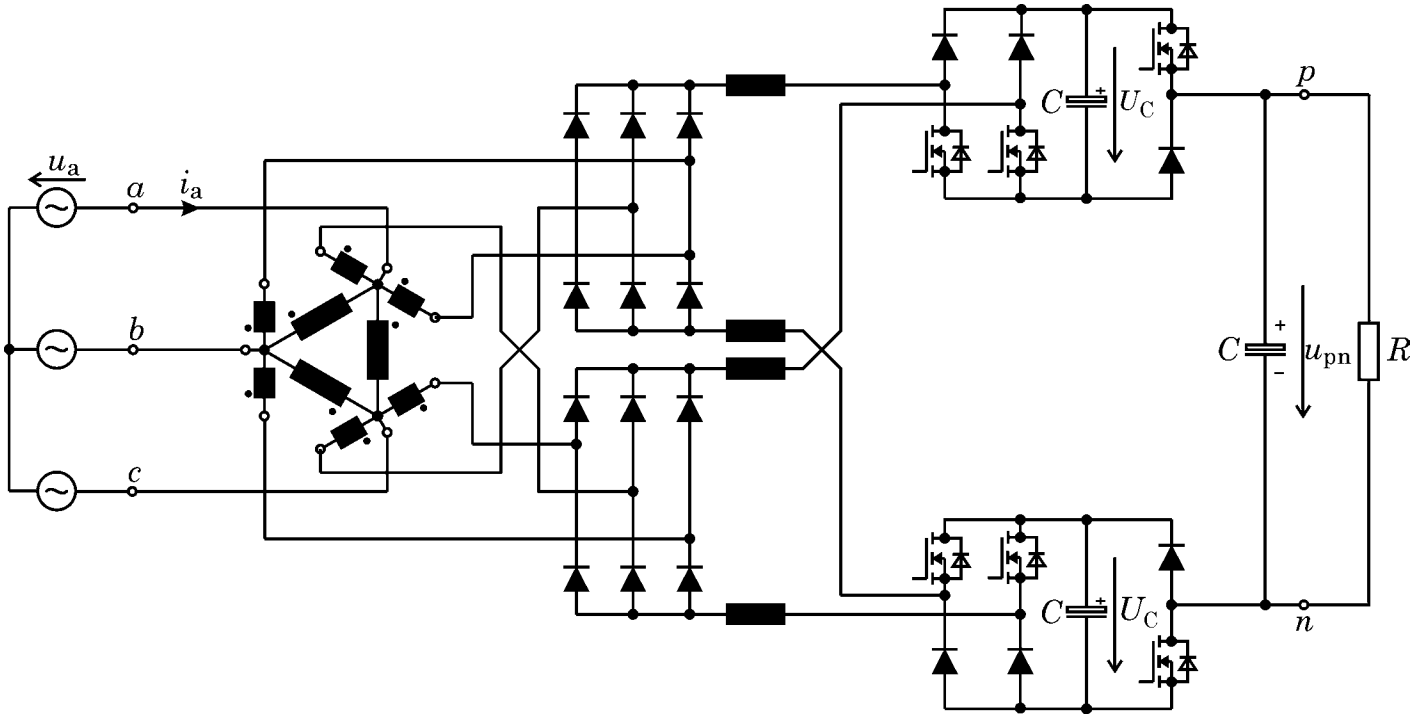


Fundamental Frequency Equivalent Circuit



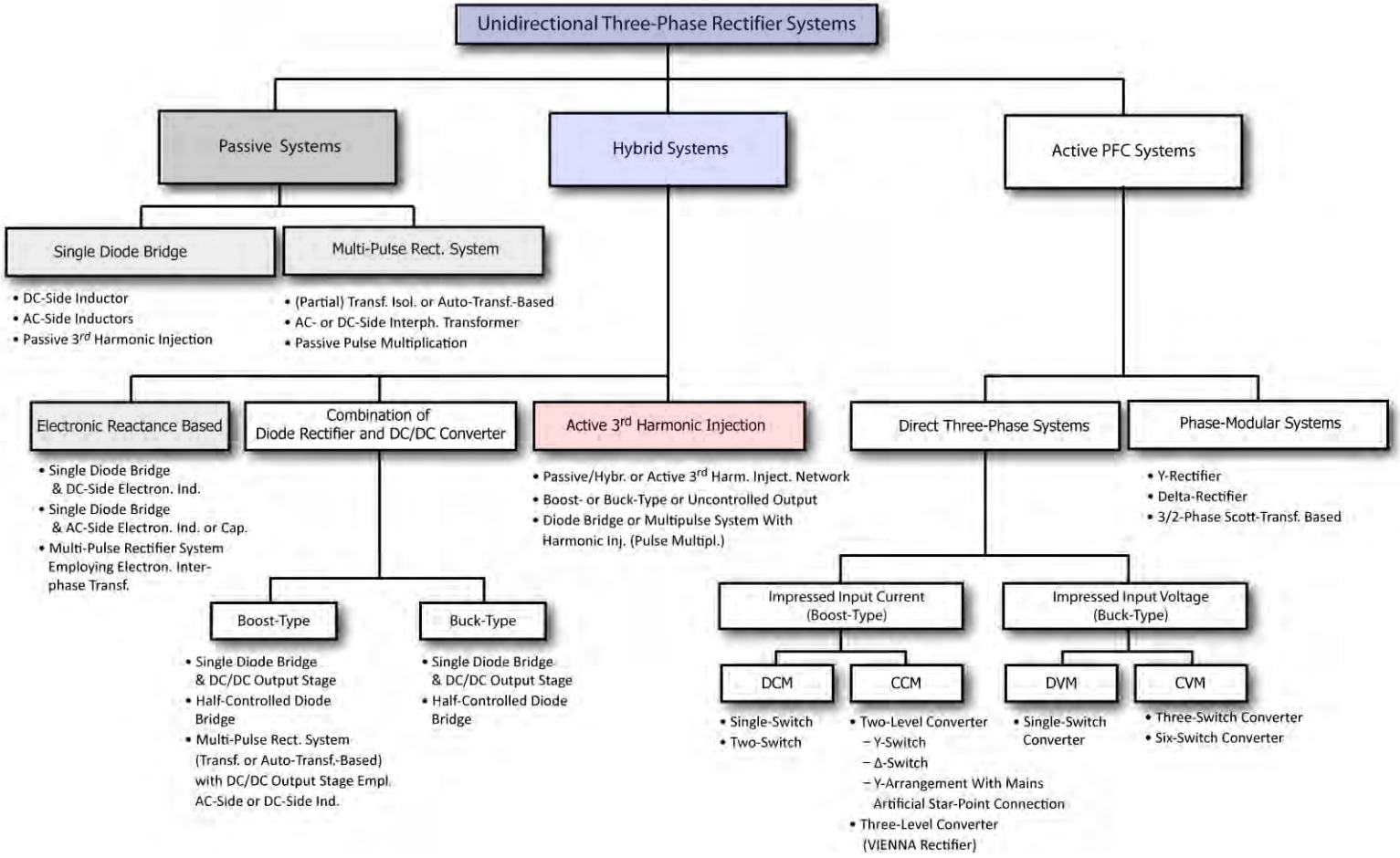


▶ 12-Pulse Rectifier Employing Electr. Interphase Transformer (EIT)

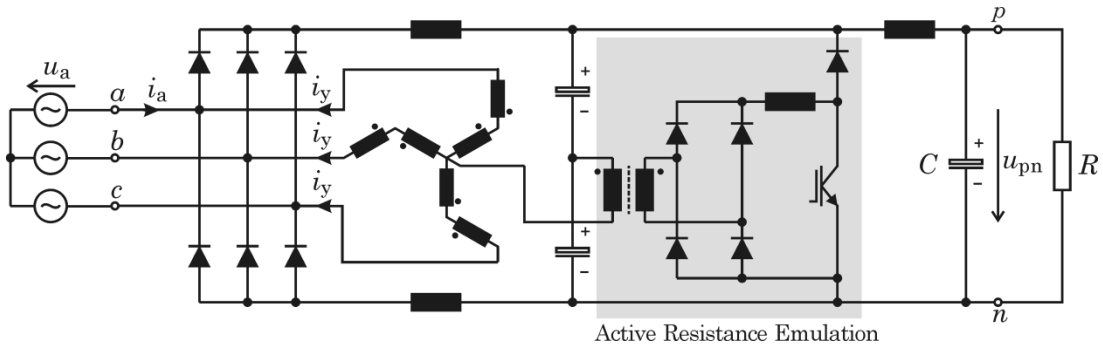


- Switching Frequency DC-Side Inductors
- Proper Control of the EIT Allows to Achieve *Purely Sinusoidal* Mains Current !

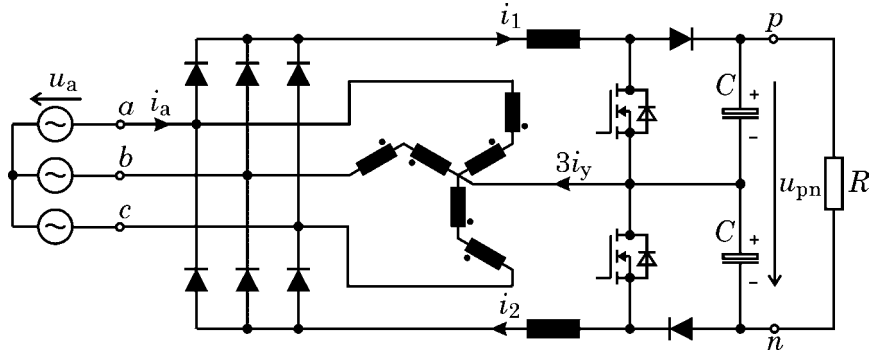
▶ Classification of Unidirectional Rectifier Systems



▶ Active 3rd Harmonic Injection into All Phases



- *No Output Voltage Control*
- Mains Current Close to Sinusoidal Shape



e.g.: $i_1 = I + 3/2\ i_y$
$i_2 = I - 3/2\ i_y$

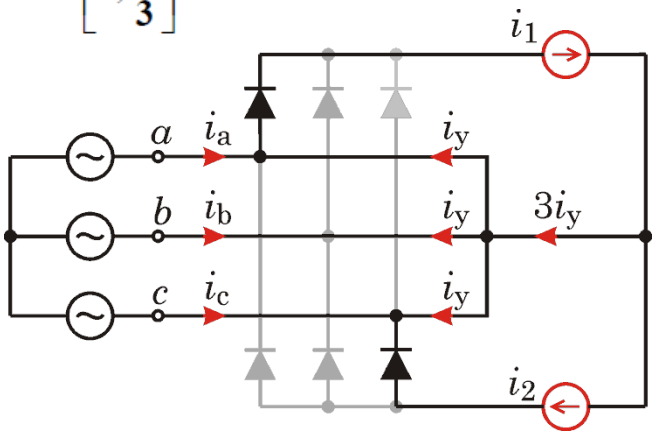
CCL: $3i_y = i_1 - i_2$

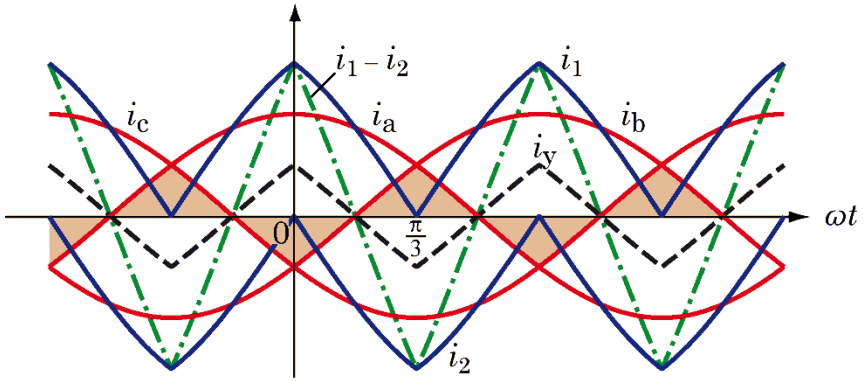
Minnesota Rectifier

- Controlled Output Voltage
- Purely Sinusoidal Shape of Mains Current

▶ Active 3rd Harmonic Injection into All Phases

$$\omega t \in \left[0, \frac{\pi}{3}\right]$$





$$i_a = \hat{I}\cos(\omega t)$$

$$i_b = \hat{I}\cos\left(\omega t - \frac{2\pi}{3}\right)$$

$$i_c = \hat{I}\cos\left(\omega t + \frac{2\pi}{3}\right)$$

$$i_y = -i_b$$

$$i_1 = i_a + i_y$$

$$i_2 = -(i_c + i_y)$$

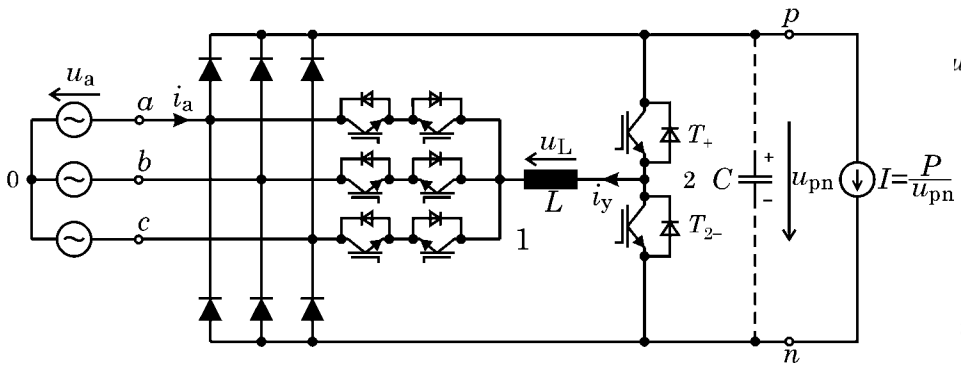
$$i_a + i_b + i_c = 0$$

$$i_1 - i_2 = i_a + i_y + i_c + i_y = -i_b + 2i_y = 3i_y$$

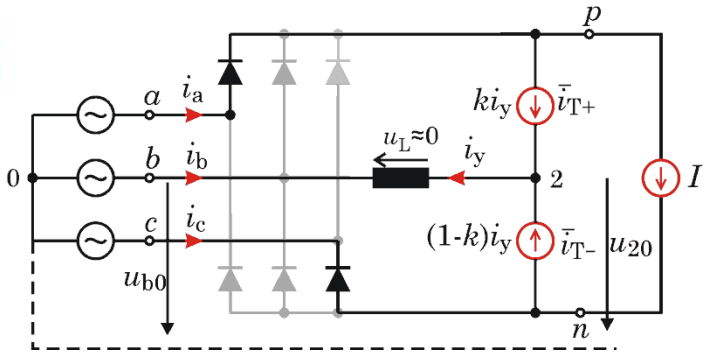
- Current Control Implemention with Boost-Type DC/DC Converter (*Minnesota Rectifier*) or with Buck-Type Topology

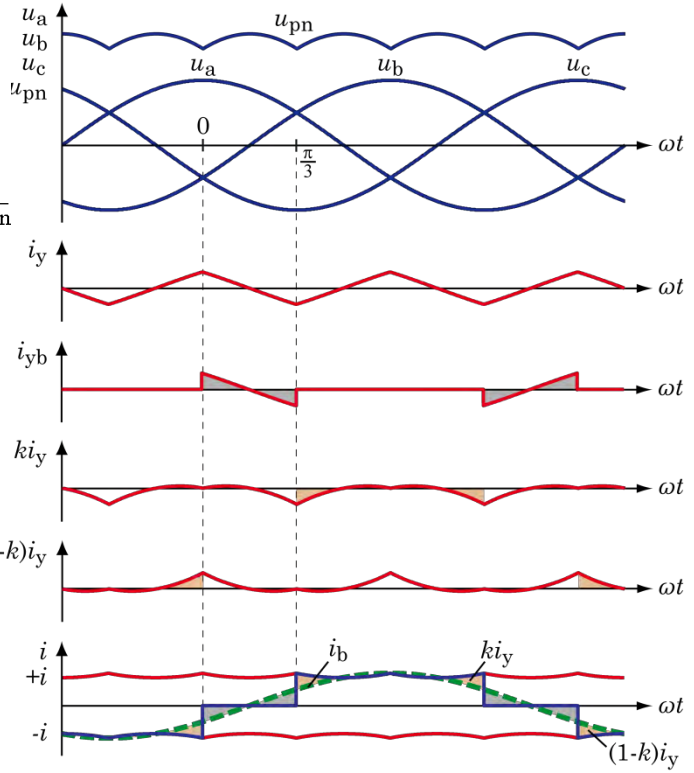
▶ Active 3rd Harmonic Inj. Only into One Phase (I)

+ Purely Sinusoidal Mains Current (Only for Const. Power Load)
+ Low Current Stress on Active Semicond. / High Efficiency
+ Low Complexity
- *No Output Voltage Control*



$\omega t \in \left[0, \frac{\pi}{3}\right]$





- T_+, T_- Could be Replaced by Passive Network

■ Proof of Sinusoidal Mains Current Shape for $\omega t \in \left[0, \frac{\pi}{3}\right]$

$$i_a = G \cdot u_{a0}$$

$$i_b = G \cdot u_{b0}$$

$$i_c = G \cdot u_{c0}$$

- Current to be Inj. Into Phase *b*: $i_y = -i_b$

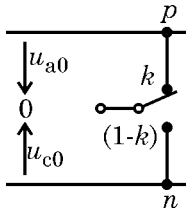
- Local Avg. Ind. Voltage / Bridge Leg (T_+, T_-) Output Voltage: $\bar{u}_L \approx 0$ and/or $\bar{u}_{20} = u_{b0}$

- Bridge Leg Voltage Formation:

$$\bar{u}_{20} = u_{b0} = k \cdot u_{a0} + (1-k) u_{c0}$$

$$u_{b0} = k \cdot u_{ac} + u_{c0}$$

$$k = \frac{u_{bc}}{u_{ac}}$$



- Bridge Leg Current Formation: $\bar{i}_{T_+} = k \cdot i_y = -k \cdot G \cdot u_{b0} = -G \cdot u_{b0} \frac{u_{bc}}{u_{ac}}$

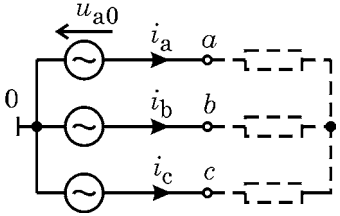
- Constant Power Load Current:

$$i = \frac{P}{u_{ac}} = \frac{u_{ac} \cdot i_a + u_{bc} \cdot i_b}{u_{ac}}$$

$$= G \frac{u_a \cdot u_{ac} + u_b \cdot u_{bc}}{u_{ac}} = G\left(u_{a0} + u_{b0} \frac{u_{bc}}{u_{ac}}\right)$$

Condition:

$$i_a + i_b + i_c = 0$$



■ Sinusoidal Mains Current:

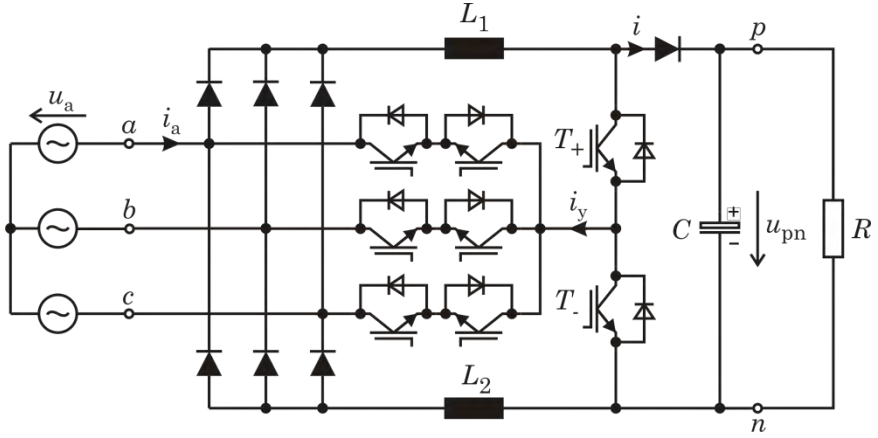
$$i + \bar{i}_{T_+} = G \cdot u_{a0} = i_a$$

▶ Active 3rd Harmonic Inj. Only into One Phase (II)

■ Boost-Type Topology

+ Controlled Output Voltage
+ Purely Sinusoidal Mains Current

- Power Semiconductors Stressed with Line-to-Line and/or Full Output Voltage



■ Proof of Sinusoidal Mains Current Shape for $\omega t \in \left[0, \frac{\pi}{3}\right]$ (1)

- 4 Different Switching States:

T_+ on, T_- off	k_1
T_+ off, T_- on	k_2
T_+ off, T_- off	k_2
T_+ on, T_- on	$k_3 = (1 - k_1 - k_2)$

3 Different States Regarding the Current Paths with Relative On-Times k_1, k_2, and k_3

Proof of Sinusoidal Mains Current Shape for $\omega t \in \left[0, \frac{\pi}{3}\right]$ (2)

- Current to be Injected into *b*: $i_y^* = -i_b^*$

$$i_a^* = G \cdot u_{a0}$$
$$i_b^* = G \cdot u_{b0}$$
$$i_c^* = G \cdot u_{c0}$$

- Inductor Voltages: $\bar{u}_{L,1}^* \approx 0 \qquad \bar{u}_{L,2}^* \approx 0$

- Bridge Leg (T_+, T_-): Voltage Form.:

$$k_1 u_{ab} + k_2 \left(u_{ab} - U_{pn}\right) + \left(1 - k_1 - k_2\right) u_{ab} \overset{!}{=} 0$$

$$k_2 = \frac{u_{ab}}{U_{pn}}$$

$$k_1 \left(u_{bc} - U_{pn}\right) + k_2 u_{bc} + \left(1 - k_1 - k_2\right) u_{bc} \overset{!}{=} 0$$

$$k_1 = \frac{u_{bc}}{U_{pn}}$$

- Constant Power, Load Current:

$$\bar{i} = \frac{P}{U_{pn}} = \frac{u_{ab} i_a - u_{bc} i_c}{U_{pn}} = -k_1 i_c + k_2 i_a$$

- Current Formation in T_+:

$$\bar{i}_{T+} = k_1 i_y^* + \left(1 - k_1 - k_2\right) i_a^*$$

Condition: $i_a^* + i_b^* + i_c^* = 0$

- Sinusoidal Mains Current:

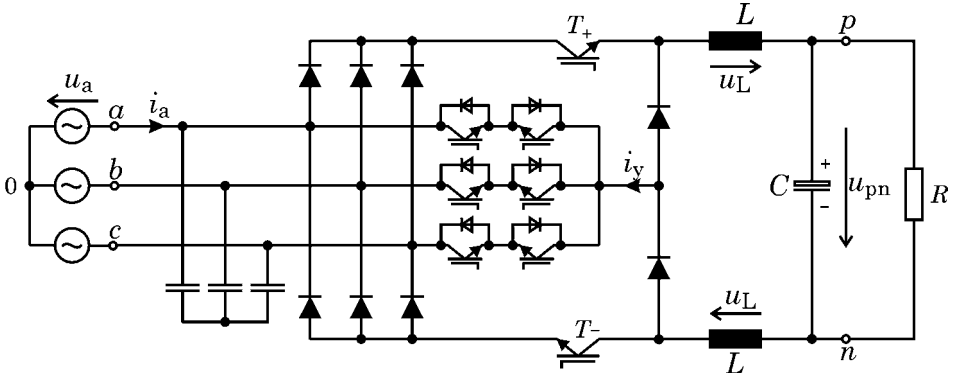
$$\bar{i}_{T+} + \bar{i}^* = i_a^*$$

▶ Active 3rd Harmonic Inj. Only into One Phase (III)

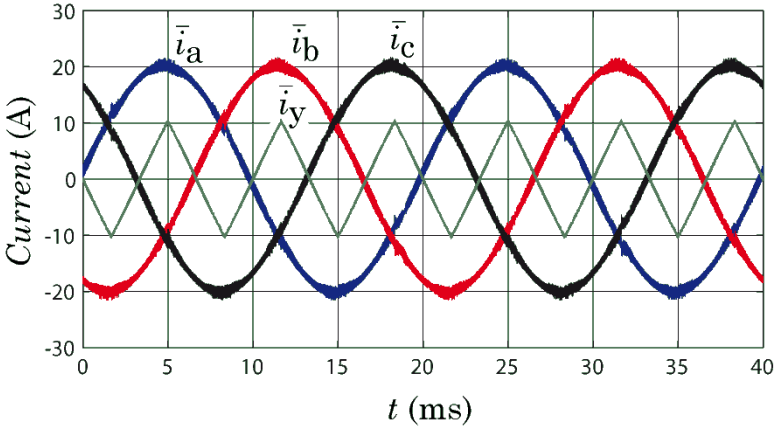
■ Buck-Type Topology

+ Controlled Output Voltage
+ Purely Sinusoidal Mains Current
+ Low Current Stress on the Inj. Current Distribution Power Transistors / High Eff.
+ Low Control Complexity

- Higher Number of Active Power Semiconductors than Active Buck-Type PWM Rect. (but Only T_+, T_- Operated with Switching Frequency)



$U_{N,LL}$= 400V_{rms}
U_{pn}= 400V_{DC}
P=10kW



- Patent Pending
- Switches Distributing the Injected Current could be Replaced by Passive Network

■ Proof of Sinusoidal Mains Current Shape for $\omega t \in \left[0, \frac{\pi}{3}\right]$

- Current to be Inj. into Phase *b*: $i_y = -i_b$

- Current Formation:

$$k_1 I = i_a \quad k_2 I = -i_c$$

$$i_y = -(1-k_1)I + (1-k_2)I = -i_b$$

$$i_a + i_b + i_c = 0$$

Duty Cycles: $T_+ \} k_1$, $T_- \} k_2$

$$i_a = G \cdot u_{a0}$$
$$i_b = G \cdot u_{b0}$$
$$i_c = G \cdot u_{c0}$$

- Local Avg. Ind. Voltage : $\bar{u}_L \approx 0$

- Voltage Formation:

$$k_1 u_a + (1-k_1)u_b - (k_2 u_c + (1-k_2)u_b) = u_{pn}$$

$$k_1 u_{ab} - k_2 u_{cb} = u_{pn}$$

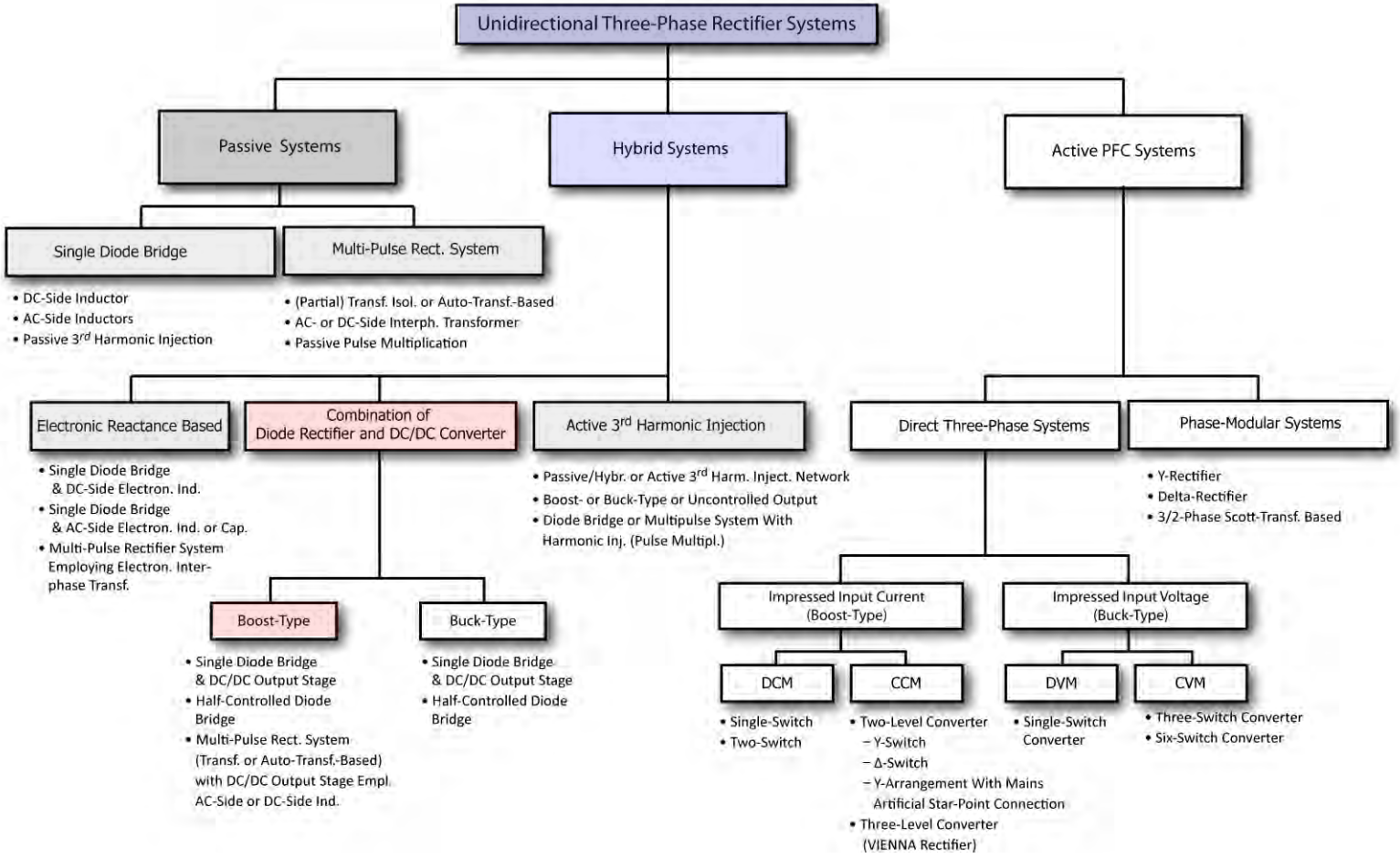
$$i_a u_{ab} + i_c u_{cb} = u_{pn} I$$

$$i_a u_{ab} + i_c u_{cb} = P \text{ = const.}$$

$$k_1 I = i_a$$
$$k_2 I = -i_c$$

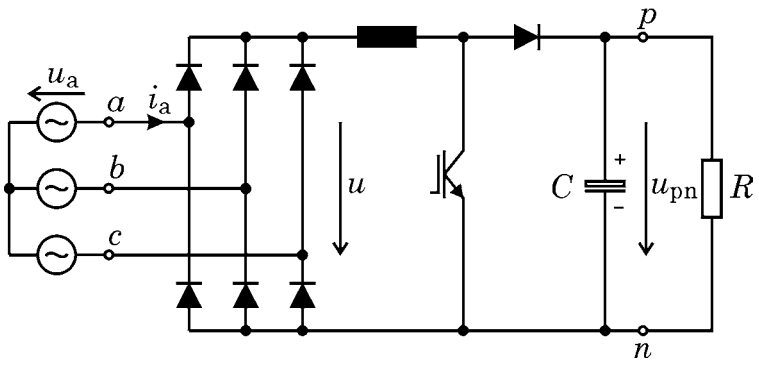
I = const. → u_{pn} = const.

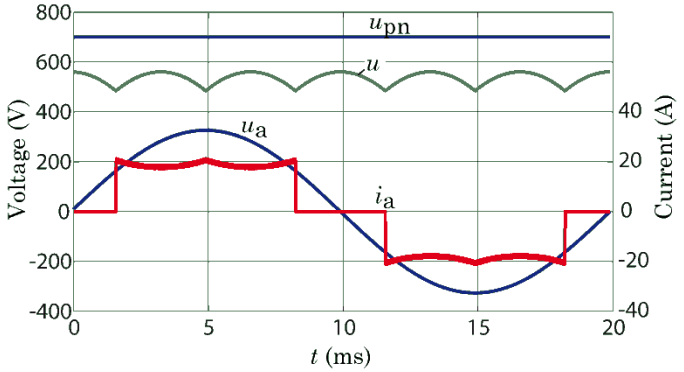
▶ Classification of Unidirectional Rectifier Systems

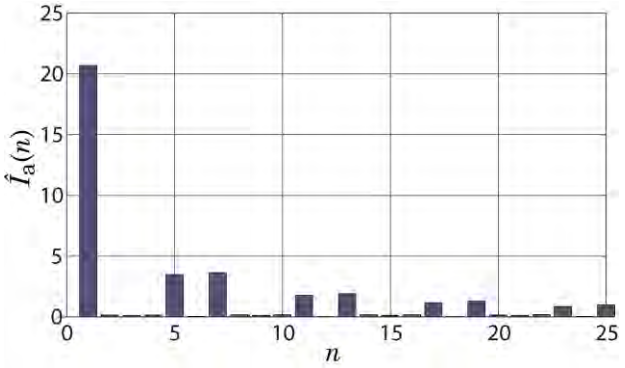


▶ Diode Bridge Combined with DC/DC Boost Converter

U_{LL} = 3 x 400 V (f_N = 50 Hz)
P_{out} = 10 kW
λ = 0.952
THD= 32 %

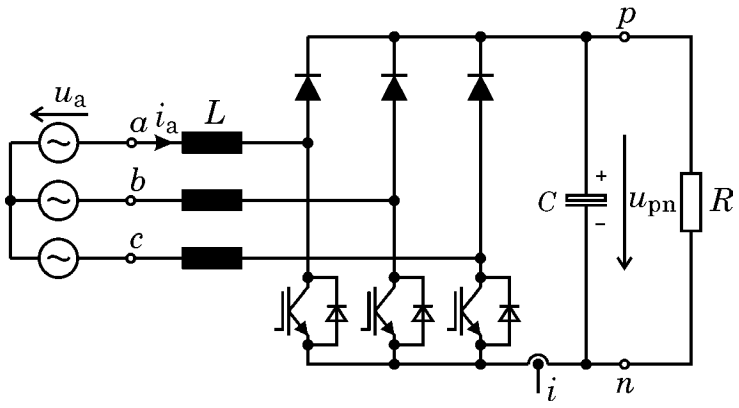


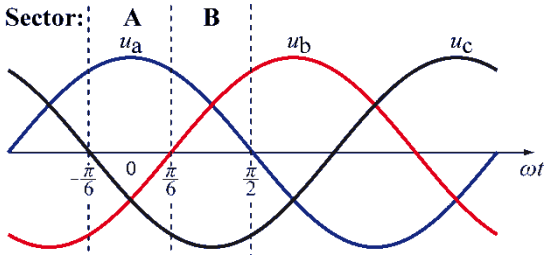




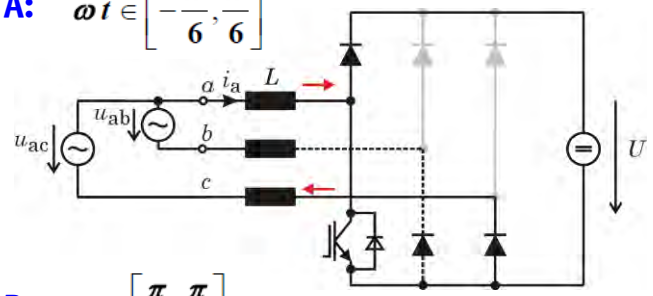
■ Other Diode Bridge Output Current Impressing DC/DC Converter Topologies (e.g. SEPIC, Cuk) result in Same Mains Current Shape

▶ Half-Controlled Rectifier Bridge Boost Converter

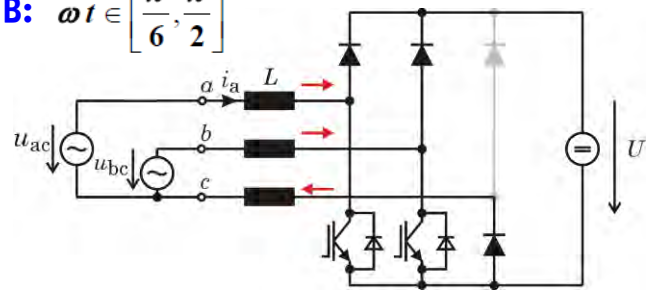




Sector A: $\omega t \in \left[-\frac{\pi}{6}, \frac{\pi}{6}\right]$



Sector B: $\omega t \in \left[\frac{\pi}{6}, \frac{\pi}{2}\right]$



- Sinusoidal Current Control Only in Sectors with 2 Positive Phase Voltages, e.g. in Sector B
- In other Sectors, Only One Phase Current could be Shaped, e.g. in Sector A

\+ Controlled Output Voltage ($U > \sqrt{6}\,\hat{U}$)
\+ Low Complexity (e.g. Single Curr. Sensor)
\+ Low Conduction Losses

– Block Shaped Mains Current

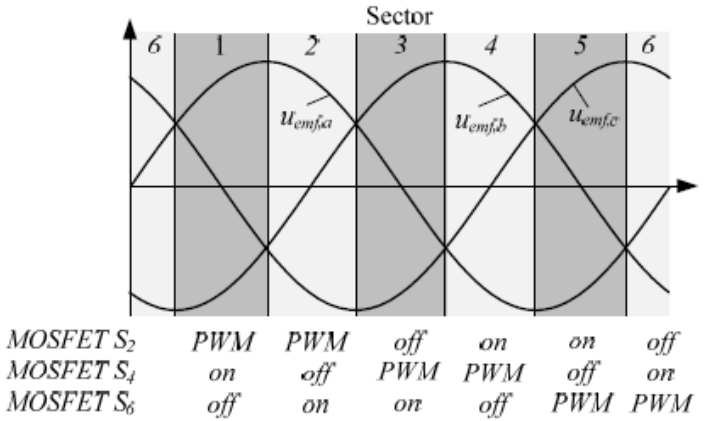
▶ Half-Controlled Rectifier Bridge Boost-Type Converter

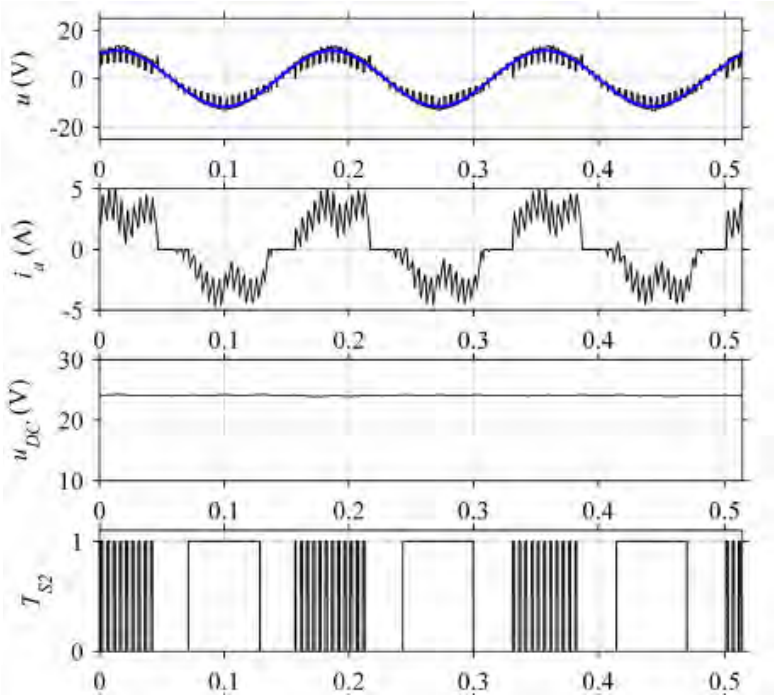
■ Current Control Concepts

Option 1: All Switches Simultaneously Controlled with Same Duty-Cycle (Synchr. Modulation)

Option 2: Only Phase with most Positive Voltage is Modulated, Switch of Phase with most Neg. Voltage is Cont. Turned on for Lowering Conduction Losses in Case of Switch Implementation with MOSFETs. Middle Phase Switch is OFF; Results in Block Shaped Mains Current

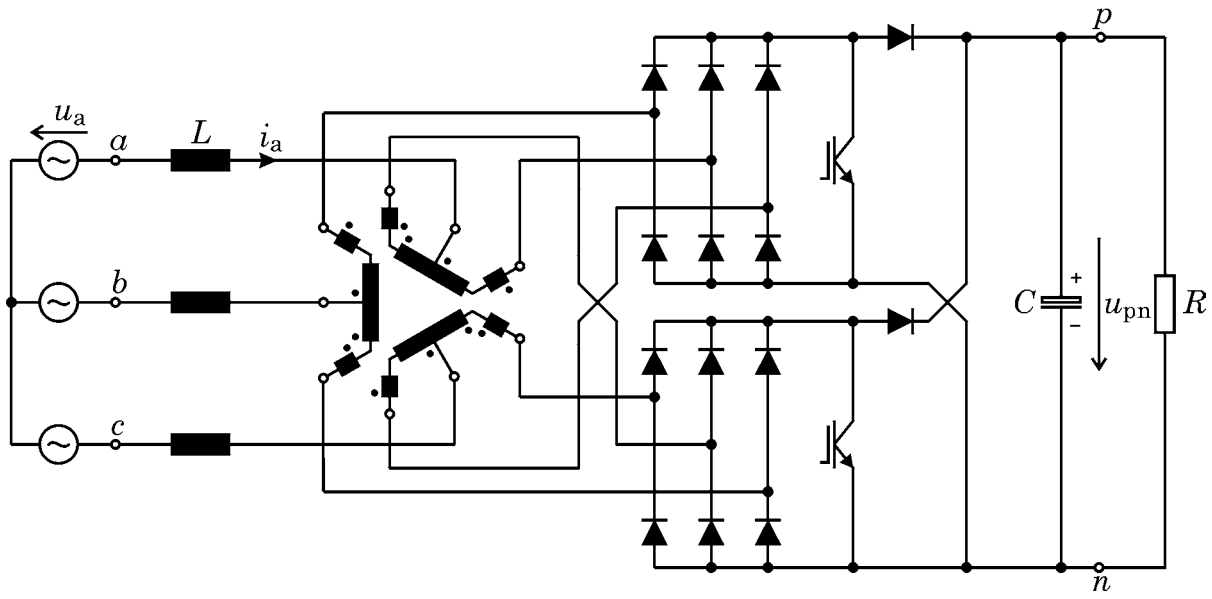
Control Acc. to Option 2





▶ Boost-Type Auto-Transf.-Based 12-Pulse Hybrid Rectifier

■ Impressed Diode Bridge Output Voltages



+ Output Voltage Controlled
+ Sinusoidal Mains Current Shaping Possible

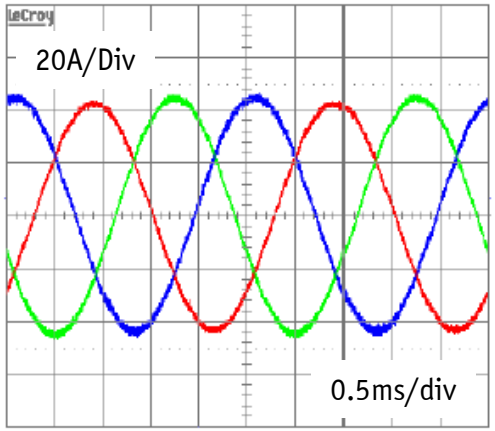
- Active Converter Stage Processes Full Output Power
- Low Frequency Magnetics Employed

▶ Boost-Type Auto-Transf.-Based 12-Pulse Hybrid Rectifier

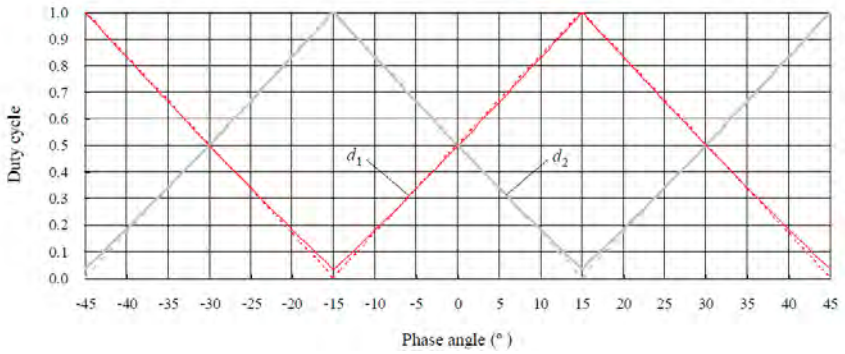
■ Experimental Results (Impressed Diode Bridge Output Voltages)

U_{LL} = 3 x 115 V (400 Hz)
P_o = 10 kW
U_o = 520 V
f_s = 60 kHz
THD_i = 3.1%

Input Currents

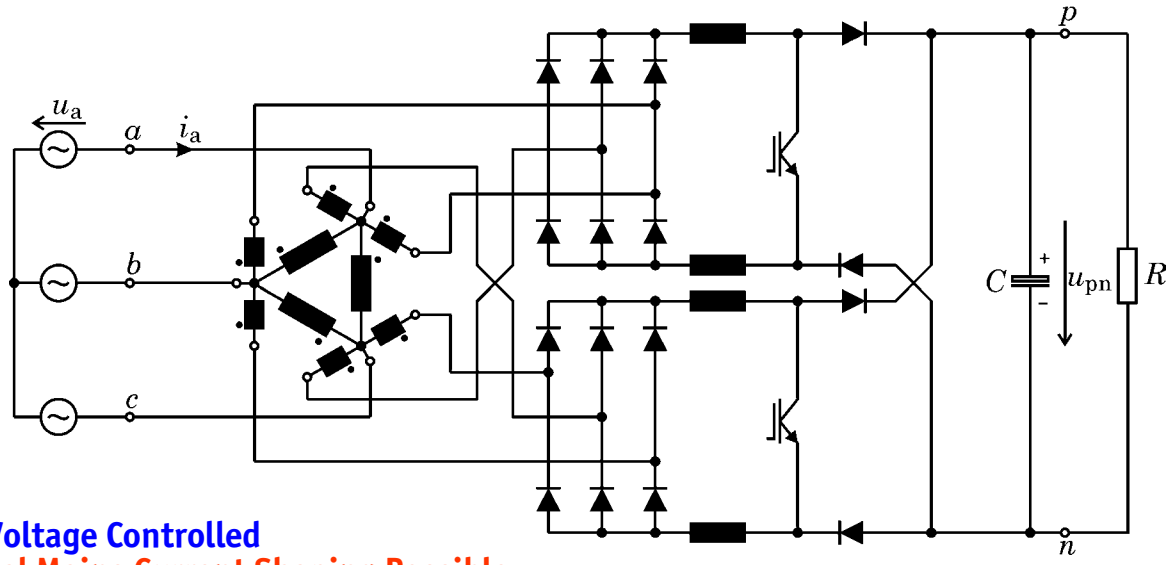


Duty Cycle Variation



▶ Boost-Type Auto-Transf.-Based 12-Pulse Hybrid Rectifier

■ Impressed Diode Bridge Output Currents

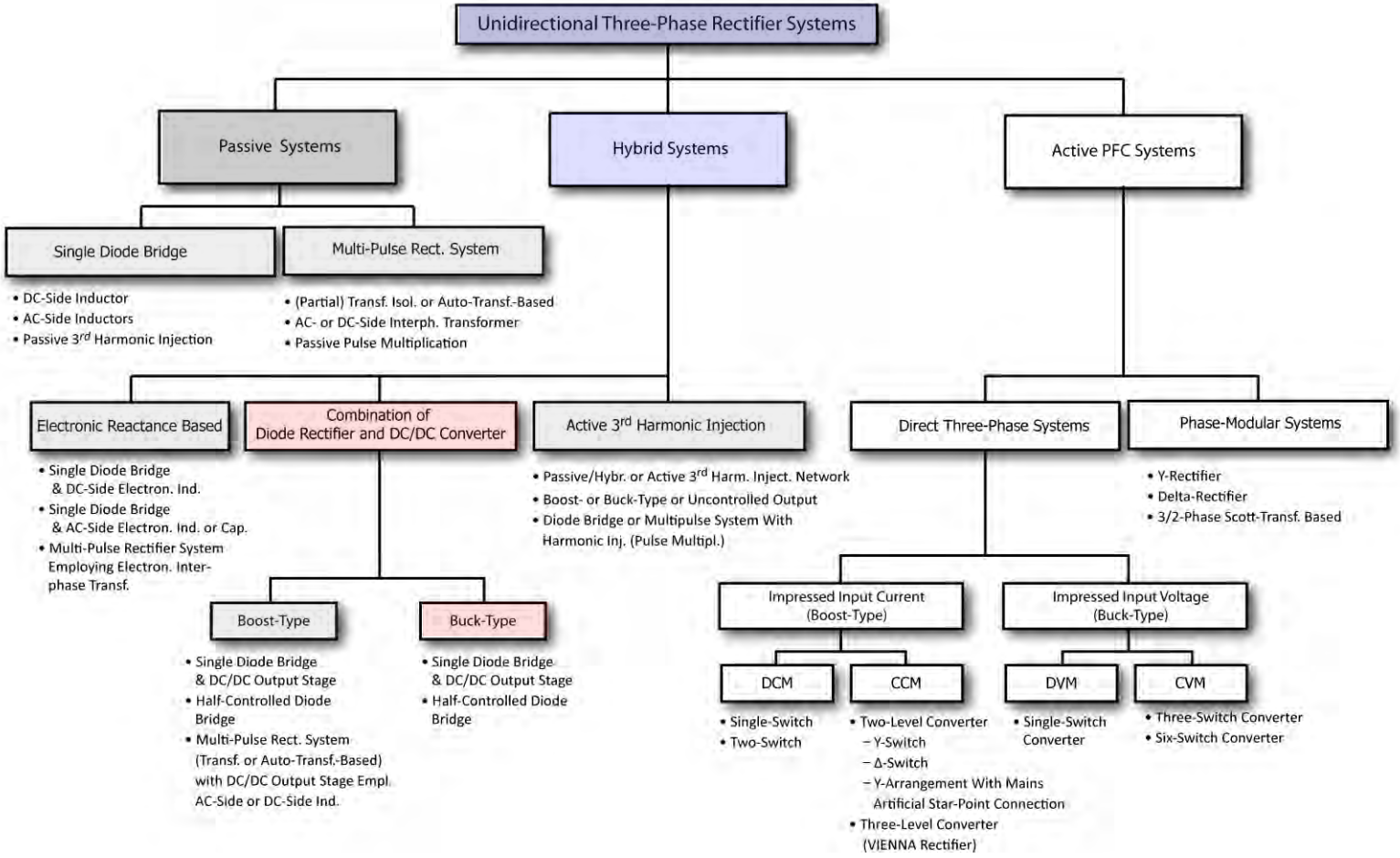


+ Output Voltage Controlled
+ Sinusoidal Mains Current Shaping Possible

- Active Converter Stage Processes Full Output Power
- Low Frequency Magnetics Employed

▶ Wide Varity of Further Topologies for Pulse Multiplication (e.g. 12p → 36p) which Process Only Part of Output Power but don´t Provide Output Voltage Control

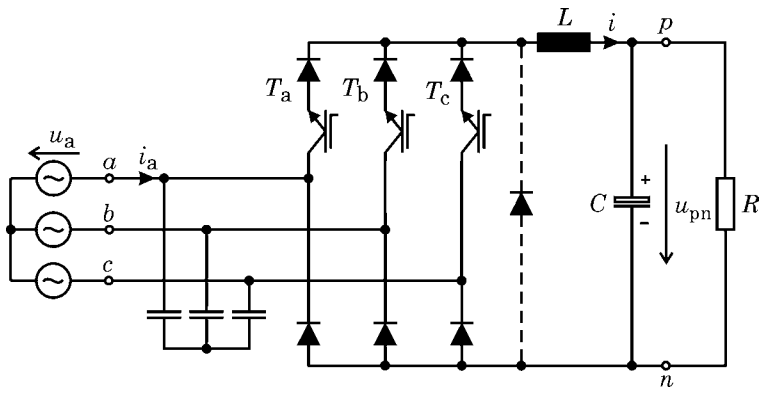
▶ Classification of Unidirectional Rectifier Systems



▶ Half-Controlled Rectifier Bridge Buck-Type Converter

+ Controlled Output Voltage
+ Low Complexity
+ Low Conduction Losses

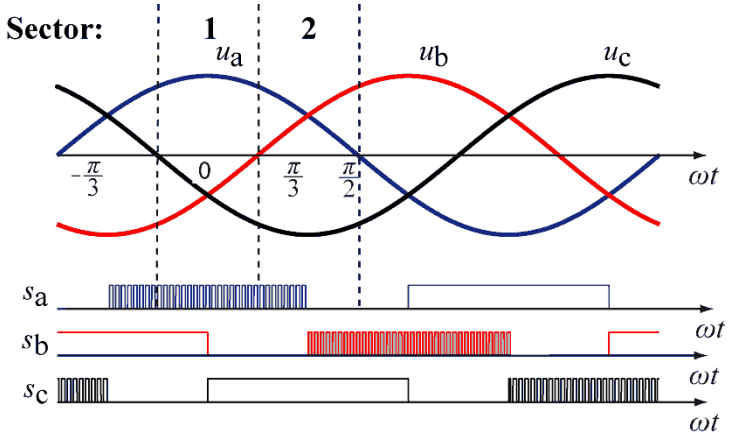
− Block Shaped Mains Current



- Topology Limits Input Current Shaping to Intervals with Positive Phase Voltage

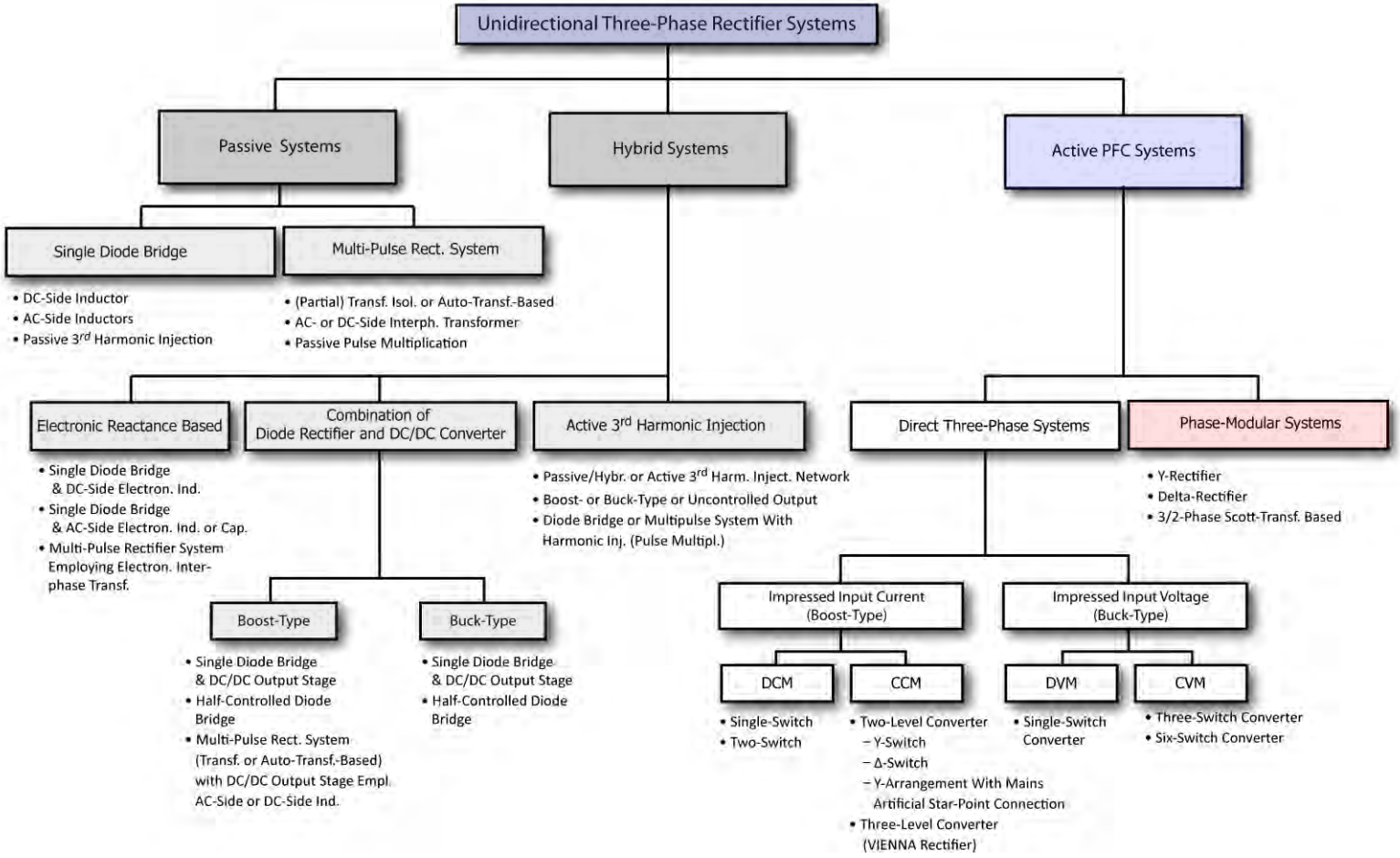
  Sector 1: Only i_a could be Controlled
  Sector 2: i_a and i_b could be Controlled

- Low Complexity Control: Only Current of Phase with most Positive Voltage Controlled; Switch of Phase with most Neg. Voltage Turned On Cont. for Providing a Free-Wheeling Path



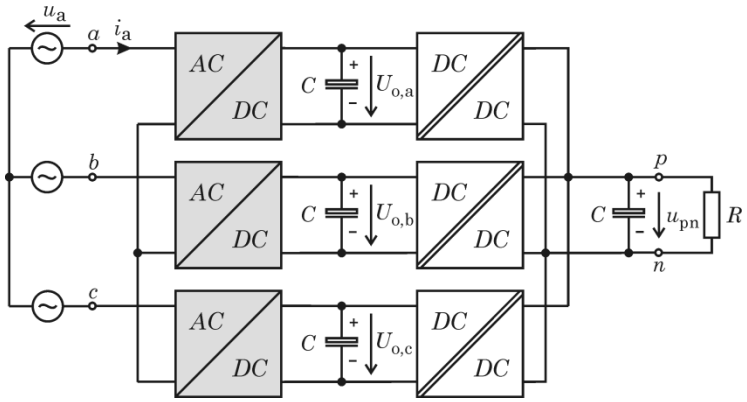
Coffee Break !

▶ Classification of Unidirectional Rectifier Systems

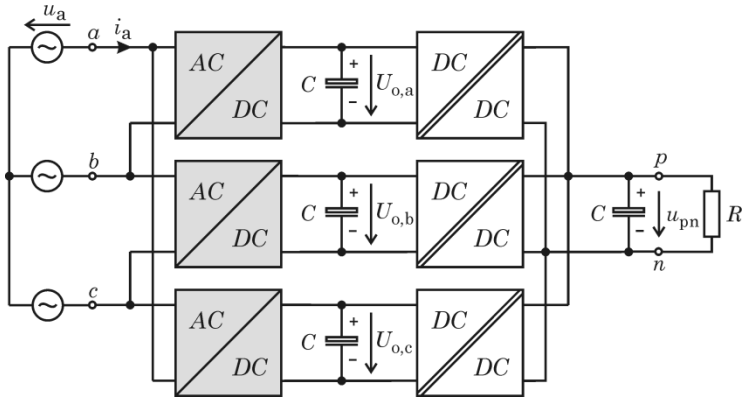


▶ Phase-Modular Rectifier Topologies

■ Y-Rectifier

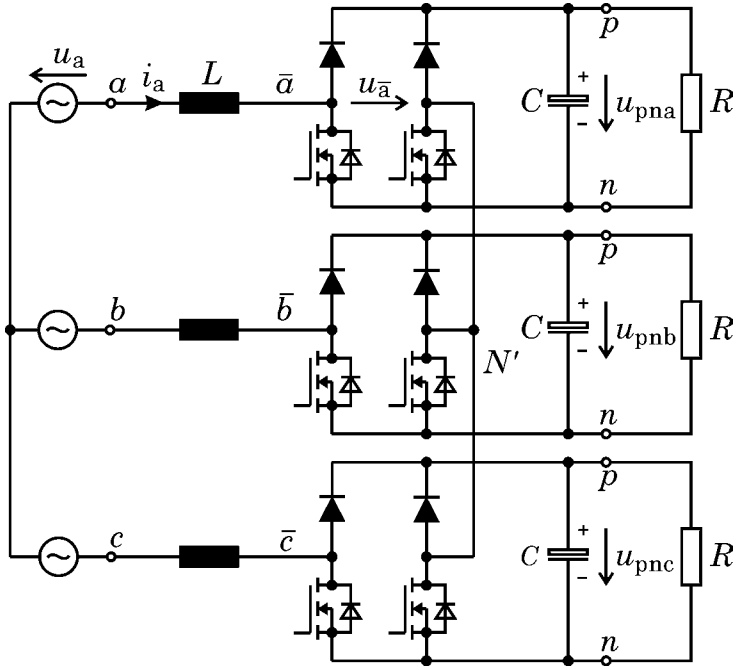


■ Δ-Rectifier

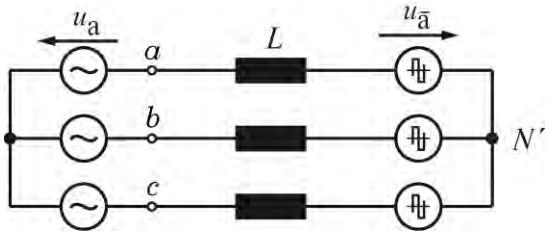


- **Individual DC Output Voltages of the Phase Units**
- **Isolated DC/DC Converter Stages Required for Forming Single DC Output**

▶ Y-Rectifier



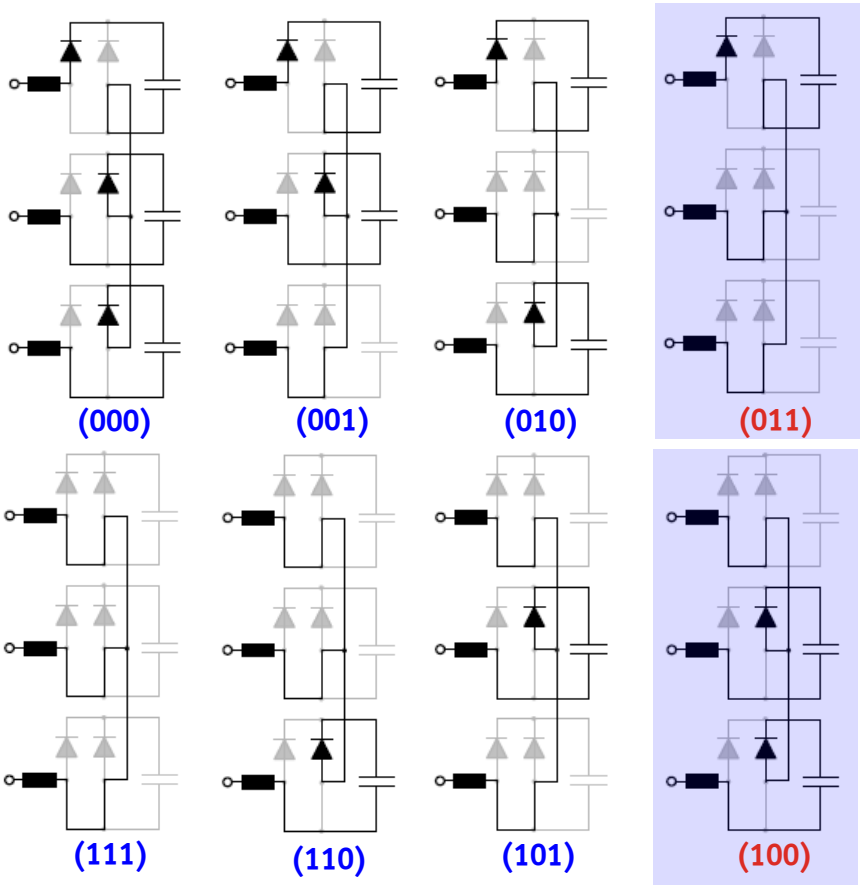
AC-Side Equivalent Circuit



- **Basic AC-Side Behavior Analogous to Direct Three-Phase Three-Level Rectifier Systems**

▶ Y-Rectifier

■ Cond. States for $i_a>0$, $i_b<0$, $i_c<0$ in Dep. on Transistor Switching States (S_a S_b S_c)

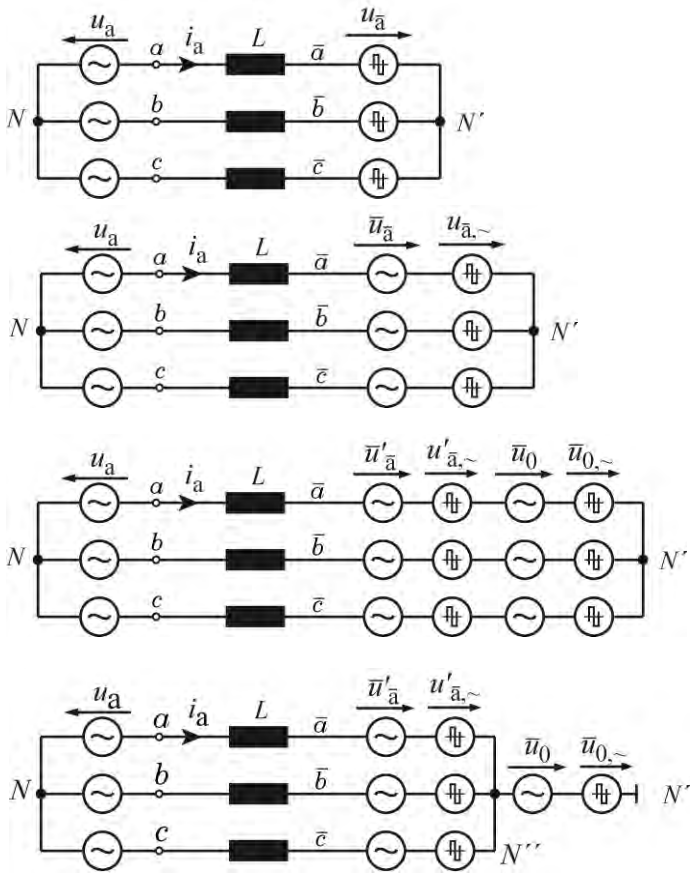


Switching States (011) and (100)

- Redundant Concerning Formation of $u_{\bar{a}\bar{b}}$, $u_{\bar{b}\bar{c}}$, $u_{\bar{c}\bar{a}}$
- Inverse Concerning Charging of C_a and C_c (and C_b)

▶ Y-Rectifier

■ Equivalent Circuit and Voltage Formation



$$u_{\bar{a}} = \bar{u}_{\bar{a}} + u_{\bar{a},\sim}$$
$$u_{\bar{b}} = \bar{u}_{\bar{b}} + u_{\bar{b},\sim}$$
$$u_{\bar{c}} = \bar{u}_{\bar{c}} + u_{\bar{c},\sim}$$

$$u_{\bar{a}} = u'_{\bar{a}} + u_0 \qquad u'_{\bar{a}} + u'_{\bar{b}} + u'_{\bar{c}} \overset{!}{=} 0$$
$$u_{\bar{b}} = u'_{\bar{b}} + u_0$$
$$u_{\bar{c}} = u'_{\bar{c}} + u_0$$

$$\Rightarrow \quad u_0 = \frac{1}{3}\left(u_{\bar{a}} + u_{\bar{b}} + u_{\bar{c}}\right)$$

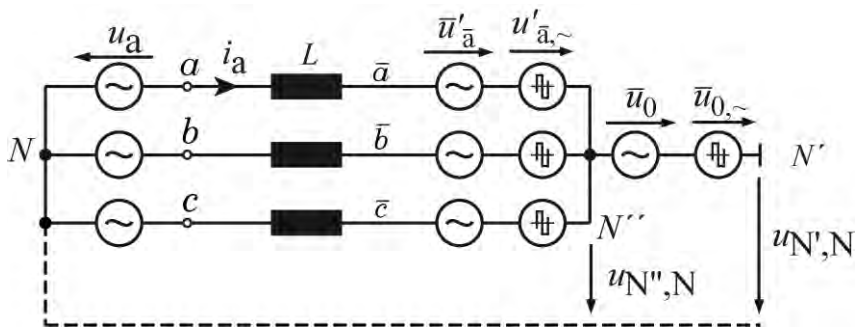
$$\Rightarrow \quad \bar{u}_{\bar{a}} = \bar{u}'_{\bar{a}} + \bar{u}_0$$
$$u_{\bar{a},\sim} = u'_{\bar{a},\sim} + u_{0,\sim}$$

(shown at the Example of Phase a)

▶ Y-Rectifier

■ Equivalent Circuit and Voltage Formation

$$u_a + u_b + u_c = 0$$



$$u_a = L\frac{di_a}{dt} + \underline{u}'_{\bar{a}} + u'_{\bar{a},\sim} + u_{N'',N}$$

$$u_b = L\frac{di_b}{dt} + \underline{u}'_{\bar{b}} + u'_{\bar{b},\sim} + u_{N'',N}$$

$$u_c = L\frac{di_c}{dt} + \underline{u}'_{\bar{c}} + u'_{\bar{c},\sim} + u_{N'',N}$$

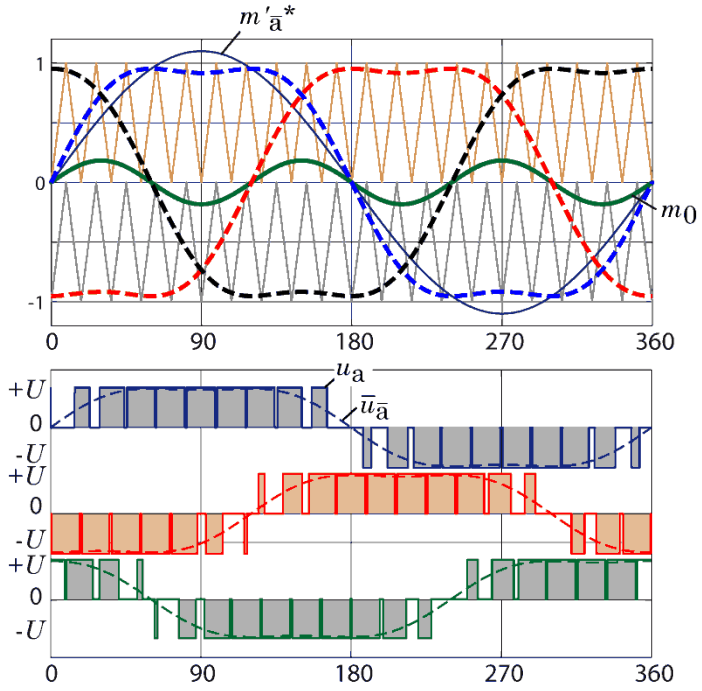
$$0 = 0 + 0 + 0 + 3u_{N'',N}$$

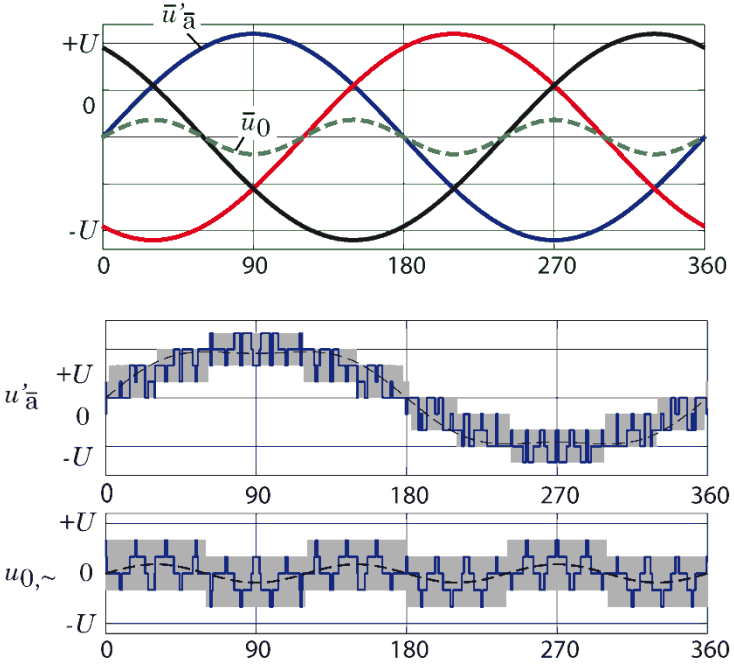
$$\Rightarrow \quad u_{N'',N} = 0$$

- Voltage of the Star Point *N´* Defined by u_0 (CM-Voltage)

▶ Y-Rectifier

■ Modulation and Voltage Formation





$$m'_{\bar{a}} = \frac{\bar{u}'_{\bar{a}}}{U}$$

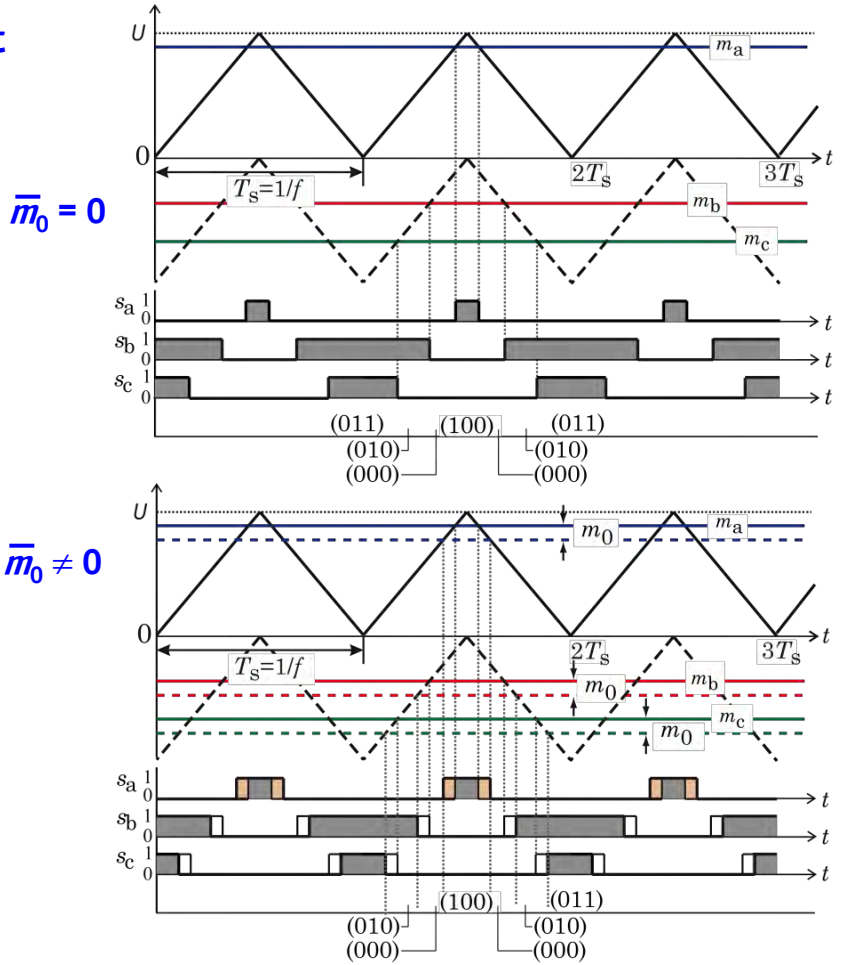
$$m_0 = \frac{\bar{u}_0}{U}$$

$$u_{0,\sim} = u_{NN',\sim}$$

- Addition of m_0 Increases Modulation Range from $\hat{U}_a = U$ to $\hat{U}_a = 2/\sqrt{3}U$
- Potential of Star Point N' Changes with LF ($\bar{u}_0$) and Switching Frequency ($u_{0,\sim}$)

▶ Y-Rectifier

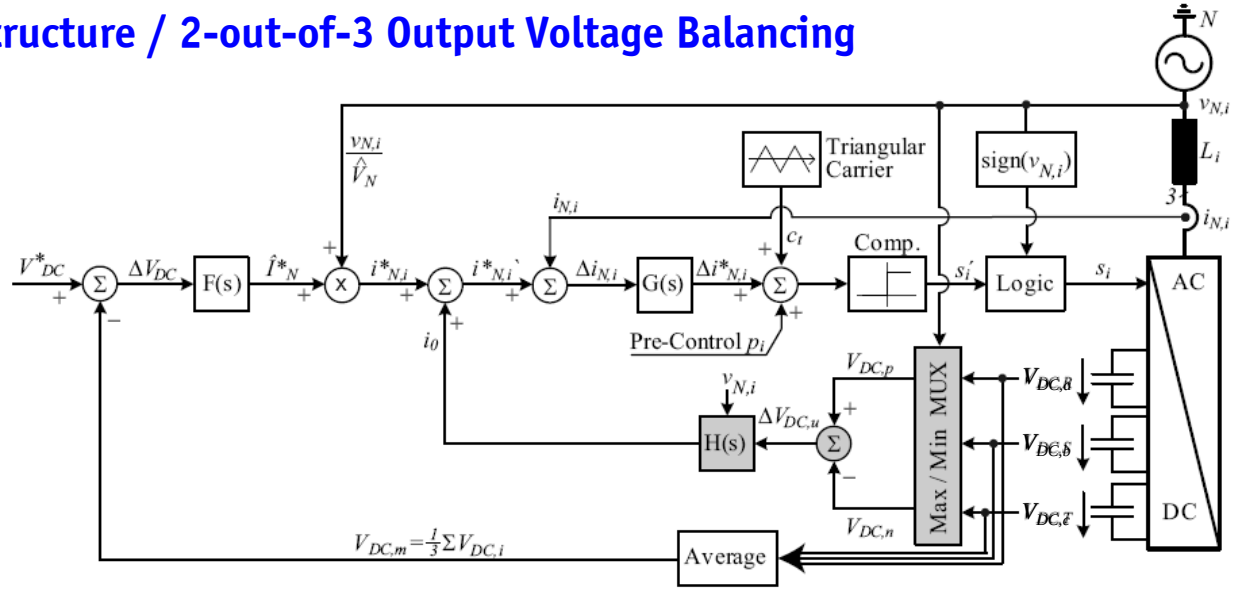
- **Balancing of Phase-Module DC-Output Voltages by DC Component of u_0 ($\overline{m}_0$)**



- **$\overline{m}_0$ Only Changes the On-Time of Redundant Switching Stages, e.g. (100) and (011)**
- **No Influence on the AC-Side Current Formation– Allows Balancing of the Module Output Voltages Independent of Input Current Shaping**

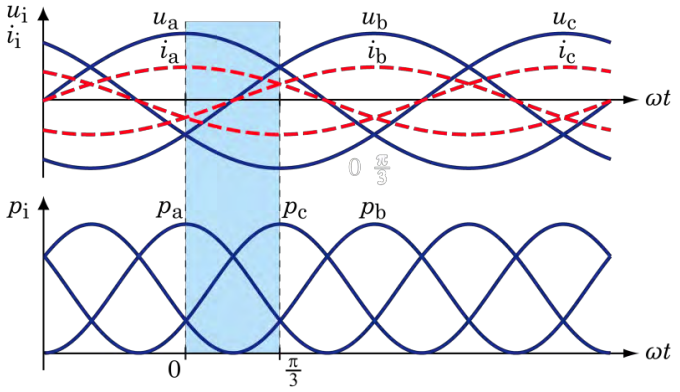
▶ Y-Rectifier

■ Control Structure / 2-out-of-3 Output Voltage Balancing



E.g.: $\omega t \in \left[0, \frac{\pi}{3}\right]$

$$\max(u_a, u_b, u_c) = u_a$$
$$\min(u_a, u_b, u_c) = u_c$$



- Output Voltage Balancing Considers Only Output Cap. Voltage of Phase with Max. Voltage (e.g. Phase *a*) and Phase with Min. Voltage (e.q. Phase *b*).

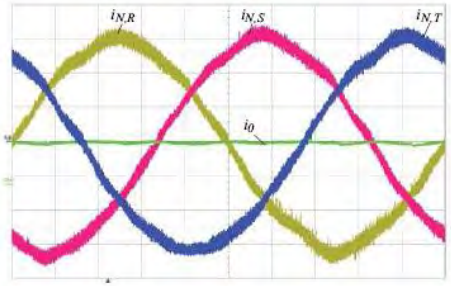
▶ Y-Rectifier

■ Experimental Verification of Output Voltage Balancing

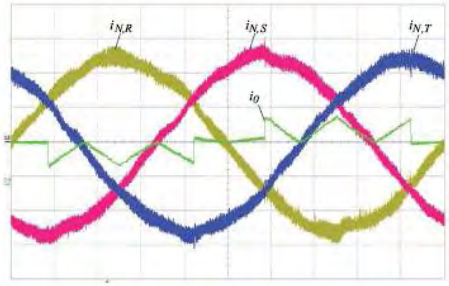
- Symm. Loading $P_a = P_b = P_c = 1000$ W
- Asymm. Loadng $P_a = 730$ W, $P_b = P_c = 1000$ W

$U_N = 3 \times 230$ V (50 Hz)
$P_o = 3 \times 1$ kW
$U_o = 400$ V
$f_s = 58$ kHz
$L = 2.8$ mH (on AC-side)
$C = 660$ µF

Symm. Loading

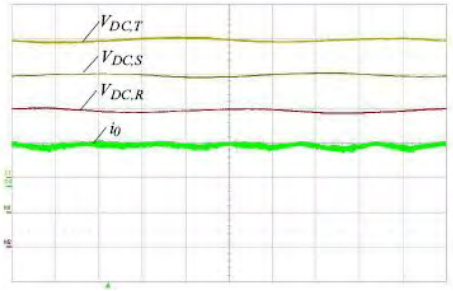


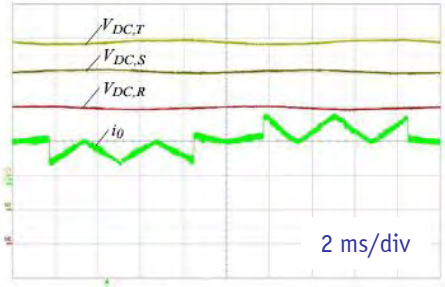
Asymm. Loading



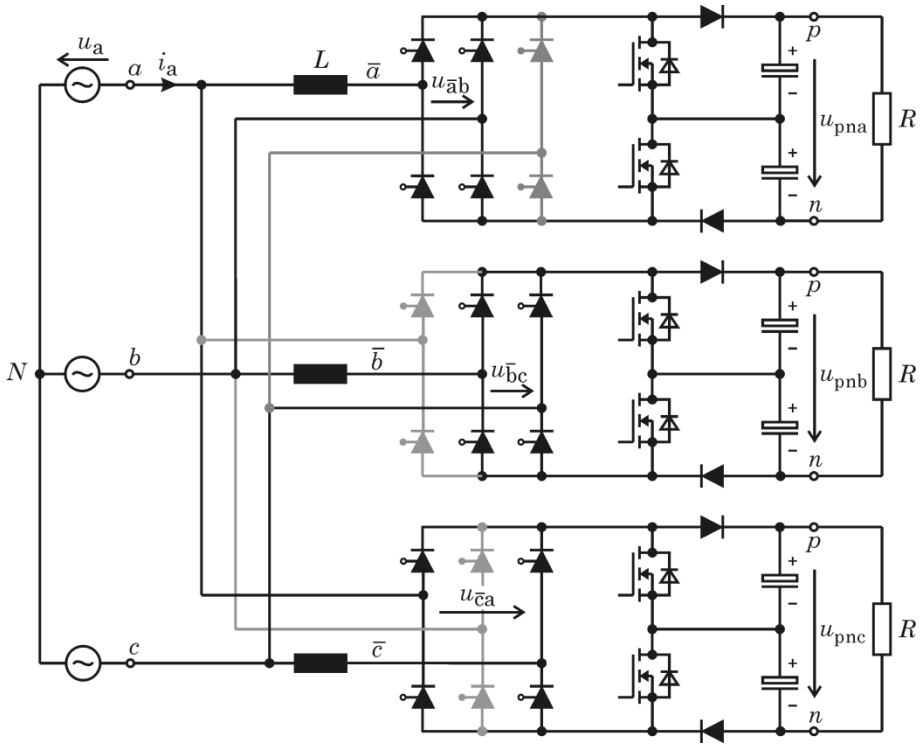
Input Phase Currents, Control Signal i_0, Output Voltages

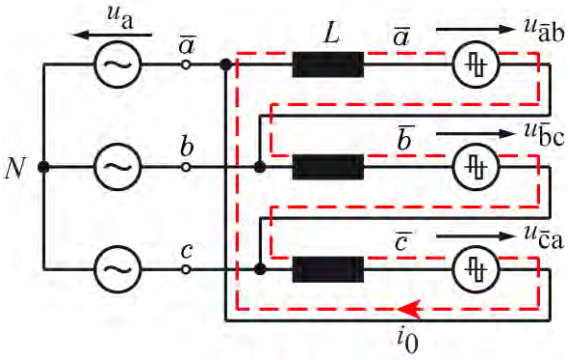
$i_{N,i}$: 1 A/div
$V_{DC,i}$: 100 V/div





▶ Δ-Rectifier

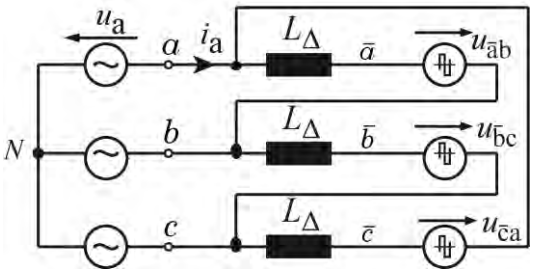




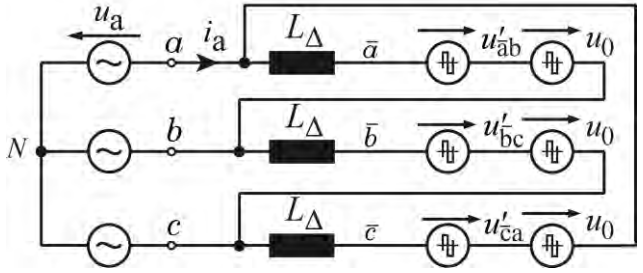
- **Connection of Each Module to All Phases / Rated Power also Available for Phase Loss !**

▶ Δ-Rectifier

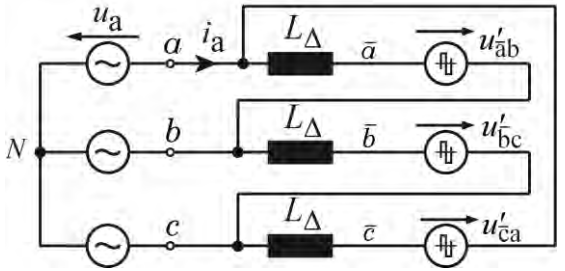
■ Derivation of Equivalent Circuit / Circulating Current Component i_0



$$u_{\bar{a}b} = u'_{\bar{a}b} + u_0$$
$$u_{\bar{b}c} = u'_{\bar{b}c} + u_0$$
$$u_{\bar{c}a} = u'_{\bar{c}a} + u_0$$

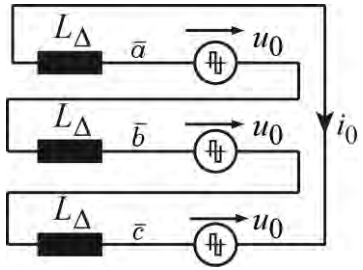


Def.: $u'_{\bar{a}b} + u'_{\bar{b}c} + u'_{\bar{c}a} = 0$



- Mains Phase Current Formed by $u'_{\bar{a}b}$, $u'_{\bar{b}c}$, $u'_{\bar{c}a}$ and u_a, u_b, u_c
- Circulating Current i_0 Formed by u_0

$$u_0 = \frac{1}{3}\left(u_{\bar{a}b} + u_{\bar{b}c} + u_{\bar{c}a}\right)$$



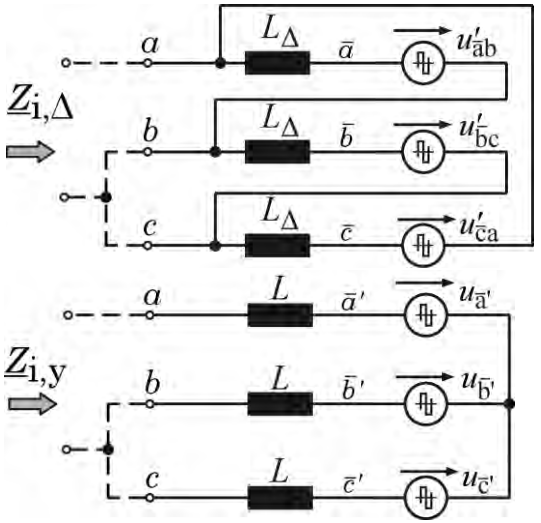
- u_0 and/or i_0, which does not Appear in i_a, i_b and i_c, can be Maximized by Proper Synchron. of Module PWM Carrier Signals; Accordingly, Switching Frequency Components of $u'_{\bar{a}b}$, $u'_{\bar{b}c}$ and $u'_{\bar{c}a}$ are Minimized

▶ Δ-Rectifier

■ Y-Equivalent Circuit Describing Mains Current Formation

- **Equiv. Conc. No-Load Voltage at Terminals *a*, *b*, *c* (No Circ. Current i_0, i.e. No Voltage Drop across L_Δ**

$$u_{ab} = u'_{\bar{a}b} = u_{\bar{a}'} - u_{\bar{b}'}$$
$$u_{bc} = u_{\bar{b}c} = u_{\bar{b}'} - u_{\bar{c}'}$$



- **Equiv. Y-Voltage Syst. should not Contain Zero Sequ. Comp.**

$$u_{\bar{a}'} + u_{\bar{b}'} + u_{\bar{c}'} \overset{!}{=} 0 \quad \Rightarrow \quad u'_{\bar{b}c} = u_{\bar{b}'} - (-u_{\bar{a}'} - u_{\bar{b}'})$$
$$u'_{\bar{b}c} = 2u_{\bar{b}'} + u_{\bar{a}'}$$

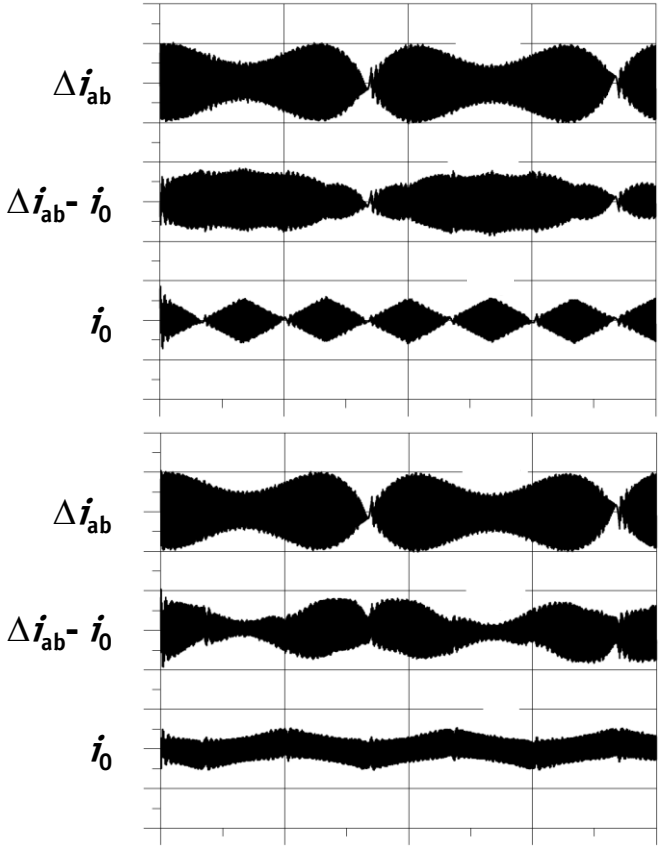
$$u_{\bar{a}'} = \frac{1}{3}(u'_{\bar{a}b} - u'_{\bar{c}a})$$
$$u_{\bar{b}'} = \frac{1}{3}(u'_{\bar{b}c} - u'_{\bar{a}b})$$
$$u_{\bar{c}'} = \frac{1}{3}(u'_{\bar{c}a} - u'_{\bar{b}c})$$

- **Equiv. Concerning Input Impedance between any Terminals**

$$\underline{Z}_{i,\Delta} = \underline{Z}_{i,y} \quad \Rightarrow \quad L_\Delta // L_\Delta = \frac{1}{2}L_\Delta = L_Y + L_Y // L_Y = \frac{3}{2}L_Y \qquad L_Y = \frac{1}{3}L_\Delta$$

▶ Δ-Rectifier

■ Circulating Current Max. / Minimization of Mains Current Ripple



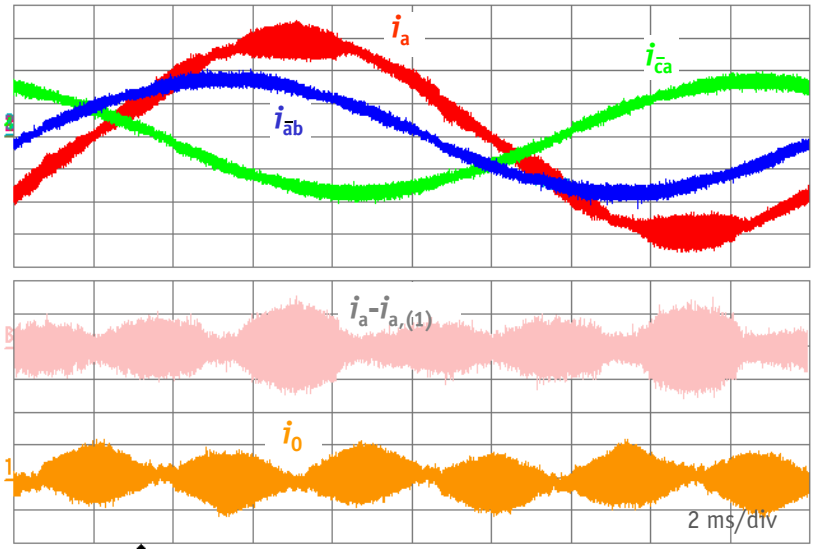
U_{LL} = 3 x 480 V (50 Hz)
P_o = 5 kW
U_o = 800 V
f_s = 25 kHz
L = 2.1 mH (on AC-Side)

- For Proper Phase Shift of Module PWM Carrier Signals a Share of the Line-to-Line Current Ripple can be Confined into the Delta Connection.

▶ Δ-Rectifier

■ Experimental Results

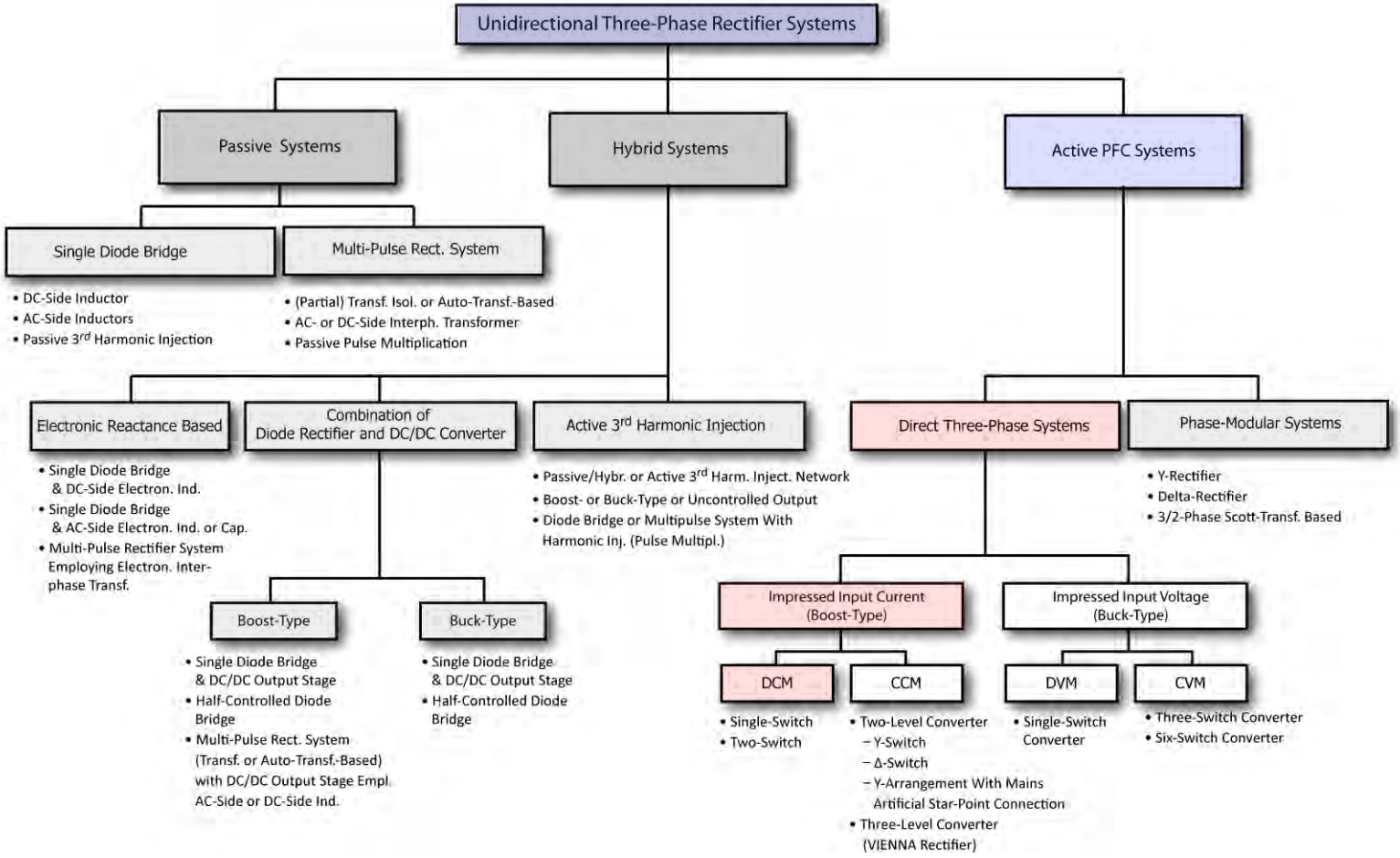
U_{LL} = 3 x 480 V (50 Hz)
P_o = 5 kW
U_o = 800 V
f_s = 25 kHz
L = 2.1 mH (on AC-Side)



i_a, $i_{\bar{a}b}$, $i_{\bar{c}a}$: 5 A/div; i_a-$i_{a,(1)}$, i_0: 2 A/div

- Formation of Input Phase Current $i_a = i_{\bar{a}b} - i_{\bar{c}a}$
- Circulating Zero Sequence Current i_0

▶ Classification of Unidirectional Rectifier Systems

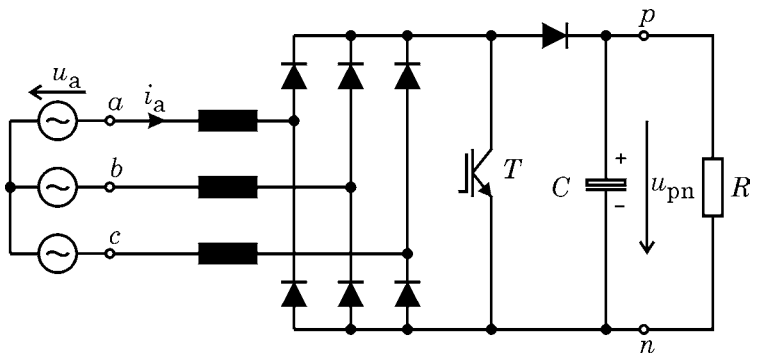


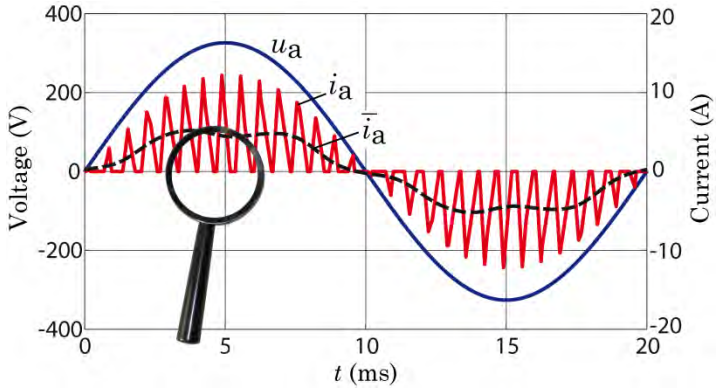
▶ Single-Switch + Boost-Type DCM Converter Topology

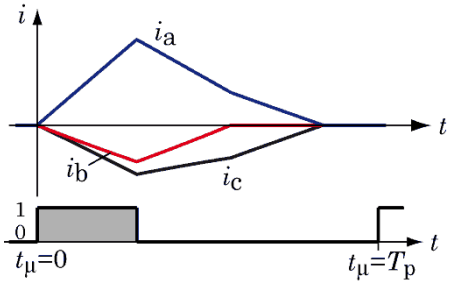
+ Low Complexity / Single Switch
+ No PWM, Constant Duty Cycle Operation
+ No Current Measurement

− High Peak Current Stress
− Low Frequ. Distortion of Mains Currents / Dep. on $U_{pn}/\hat{U}$
− High EMI Filtering Effort

U_{LL} = 3 x 400 V (50Hz)
P_o = 2.5 kW
U_o = 800 V
THD_i = 13.7 %

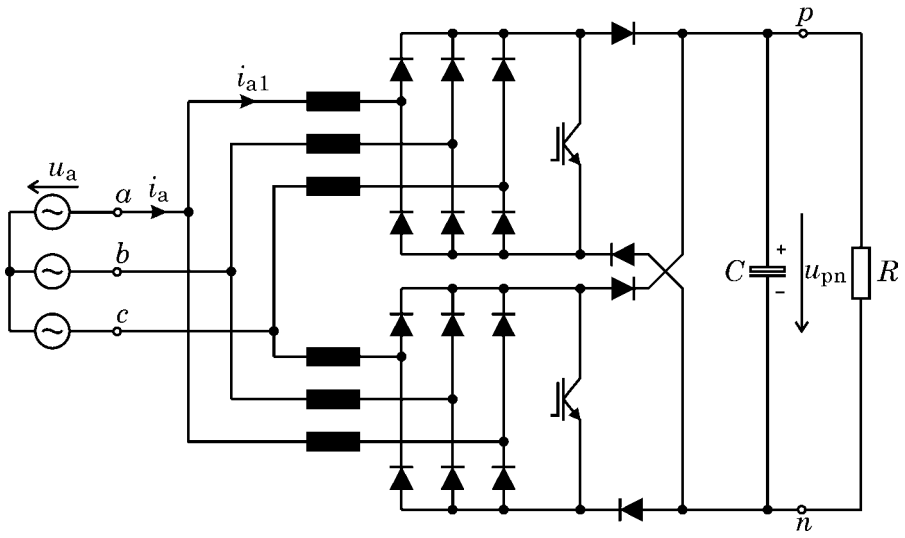


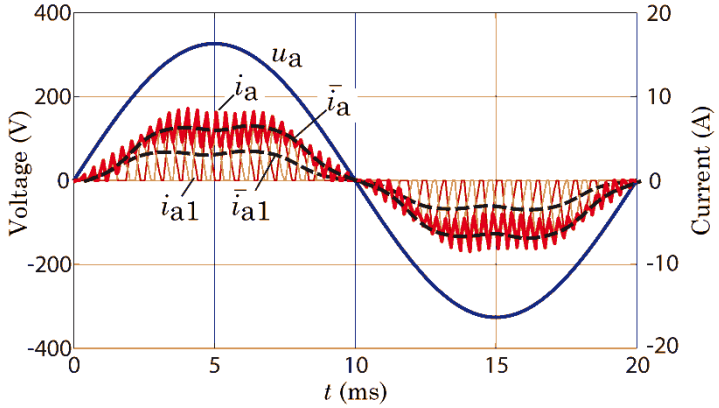




- Improvement of Mains Current Shape by 6th Harmonic Duty Cycle Modulation or Boundary Mode Operation
- Reduction of EMI Filtering Effort by Interleaving

▶ Two Interleaved Single-Switch Boost-Type DCM Converter Stages

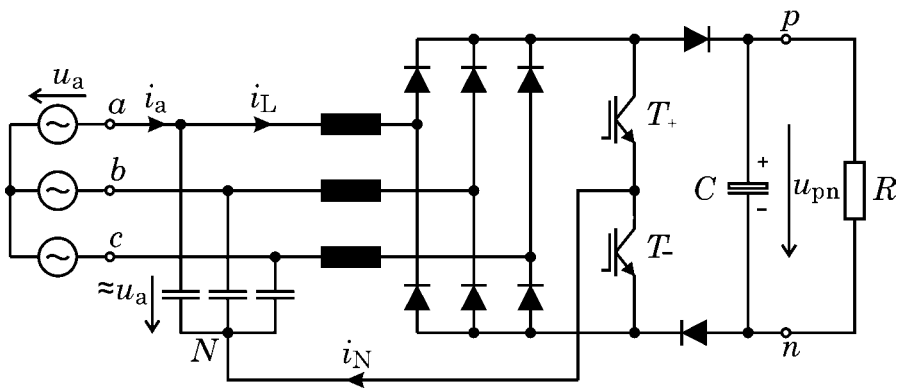




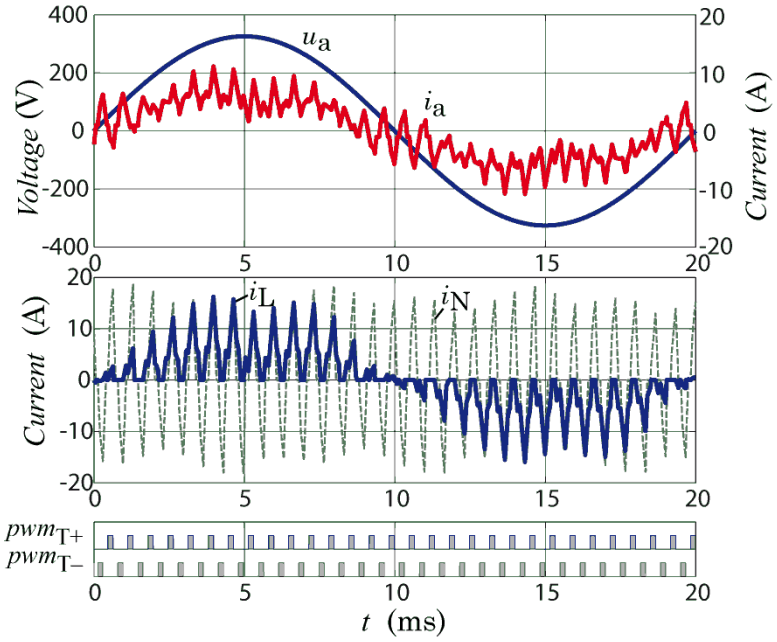
+ Interleaving Reduces Switching Frequency Input Current Ripple
+ For Low Power Only One Unit Could be Operated – Higher Efficiency

– Low Frequency Mains Current Distortion Still Remaining
– Relatively High Implementation Effort

▶ Two-Switch Boost-Type DCM Converter Topology



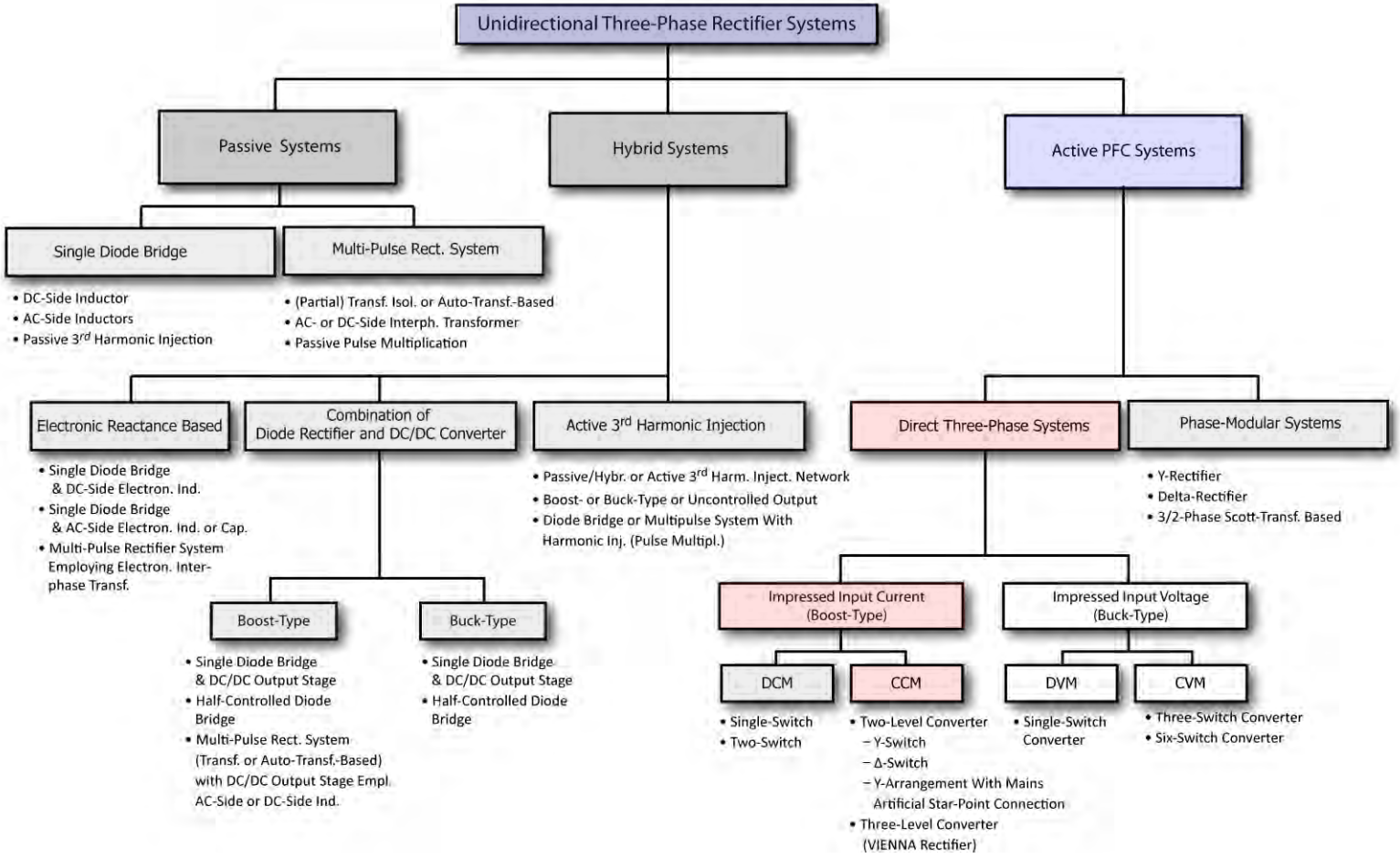
U_{LL} = 3 x 400 V
P_o = 2.5 kW
U_o = 700 V
THD_i = 9 %



+ Slightly Lower THD_I for same $U_{pn}/\hat{U}_N$ Component as Single-Switch DCM Converter
− Large Switching Frequency CM Output Voltage Comp.
− High Input Capacitor Current Stress

- Artificial Capacitive Neutral Point *N*
- Decoupling of the Phases
- Pros and Cons. as for Single-Switch Converter
- T_+ and T_- Could also be Gated Simultaneously

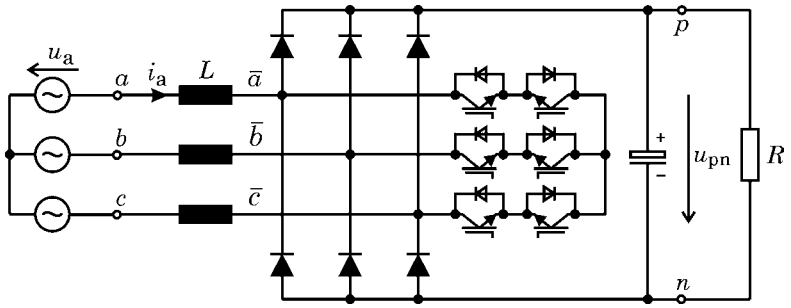
▶ Classification of Unidirectional Rectifier Systems

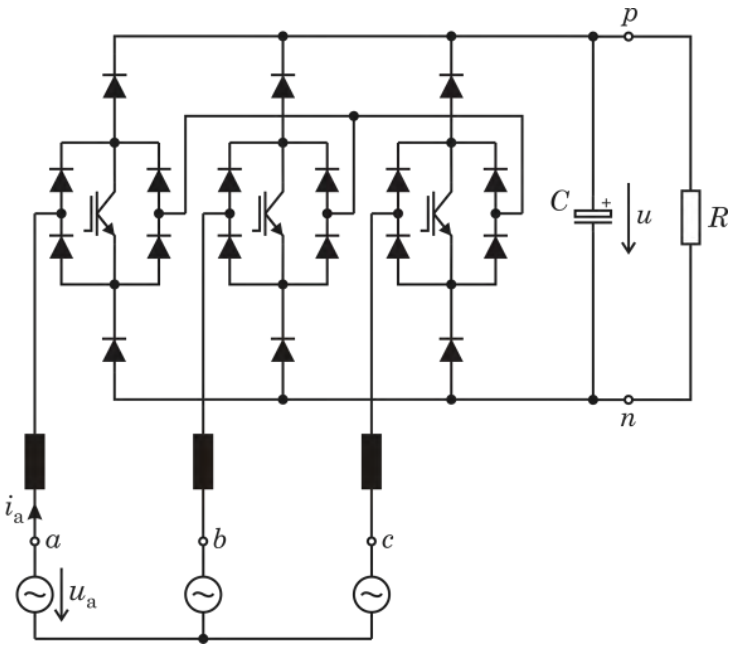


Two-Level CCM Boost-Type PFC Rectifier Systems

- *Y-Switch Rectifier*
- *Δ-Switch Rectifier*

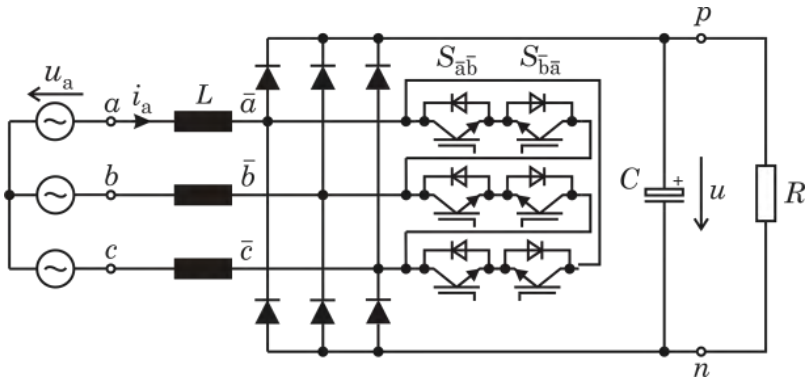
▶ Y-Switch Rectifier

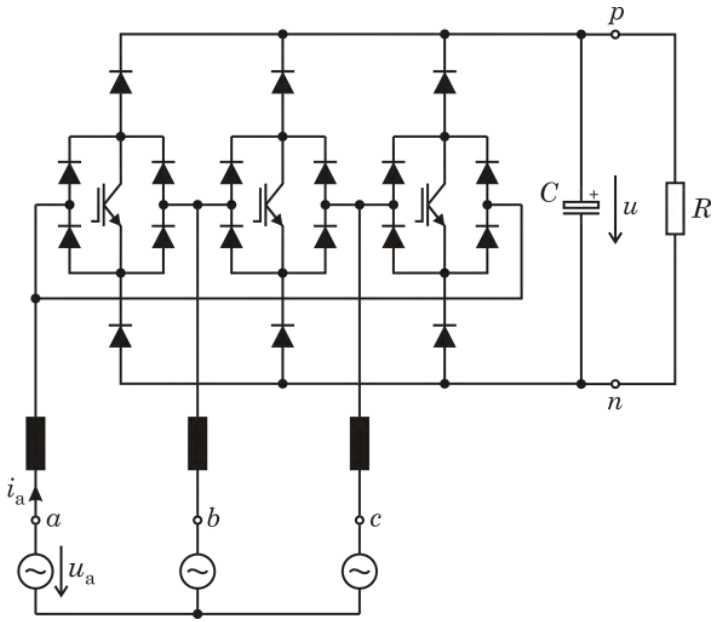




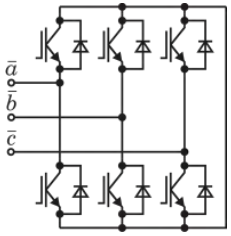
- **Proper Control of Power Transistors Allows Formation of PWM Voltages at $\bar{a}$, $\bar{b}$, $\bar{c}$ and/or Impression of Sinusoidal Mains Current**

▶ Δ-Switch Rectifier





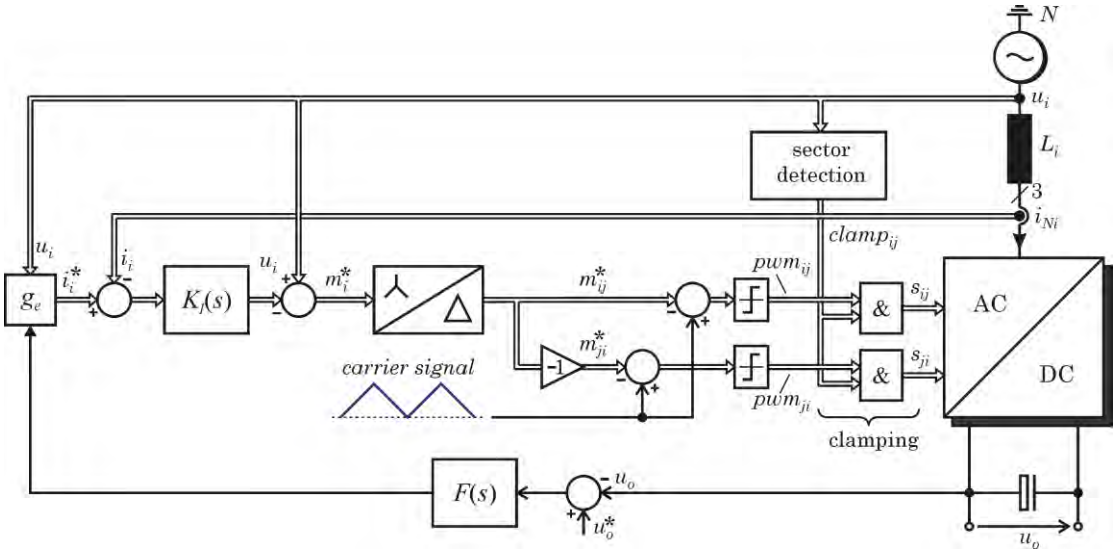
- **Δ-Switch Rectifier Features Lower Conduction Losses Compared to Y-Switch System**
- **Active Switch Could be Implemented with Six-Switch Power Module**

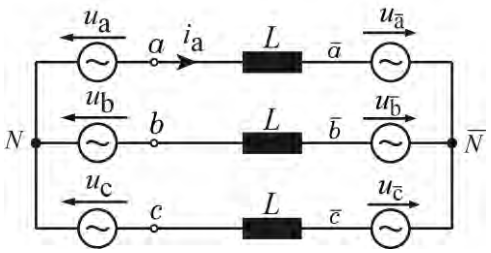


▶ Δ-Switch Rectifier

■ Equivalent Circuit / Mains Current Control

- Reference Voltages, i.e. the Output of the Phase Current Controllers Need to be Transformed into Δ-Quantities





$$\underline{u}_{\bar{a}\bar{b}} = \underline{u}_{\bar{a}} - \underline{u}_{\bar{b}}$$

$$\underline{u}_{\bar{b}\bar{c}} = \underline{u}_{\bar{b}} - \underline{u}_{\bar{c}}$$

$$\underline{u}_{\bar{c}\bar{a}} = \underline{u}_{\bar{c}} - \underline{u}_{\bar{a}}$$

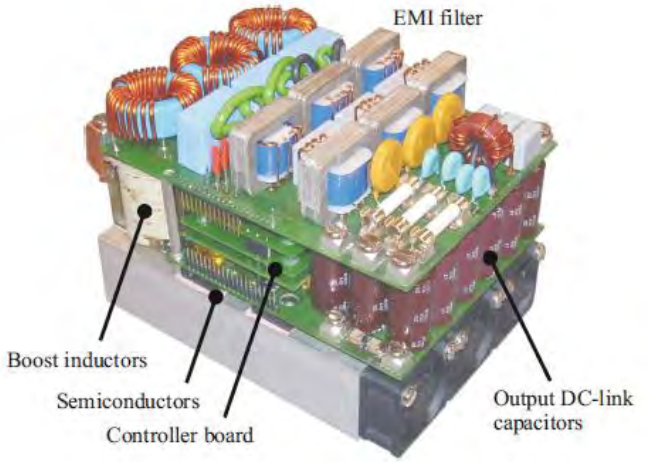
- Mains Currents Controlled in Phase with Mains Voltages u_a, u_b, u_c
- Voltage Formation at *a*, *b*, *c* is Determined by Switching State of $S_{\bar{a}\bar{b}\bar{a}}$, $S_{\bar{b}\bar{c}\bar{b}}$, $S_{\bar{c}\bar{a}\bar{c}}$ and AND Input Current Direction/Magnitude
- Always Only Switches Corresponding to Highest and Lowest Line-to-Line Voltage are Pulsed
- Switch of Middle Phase Turned Off Continuously

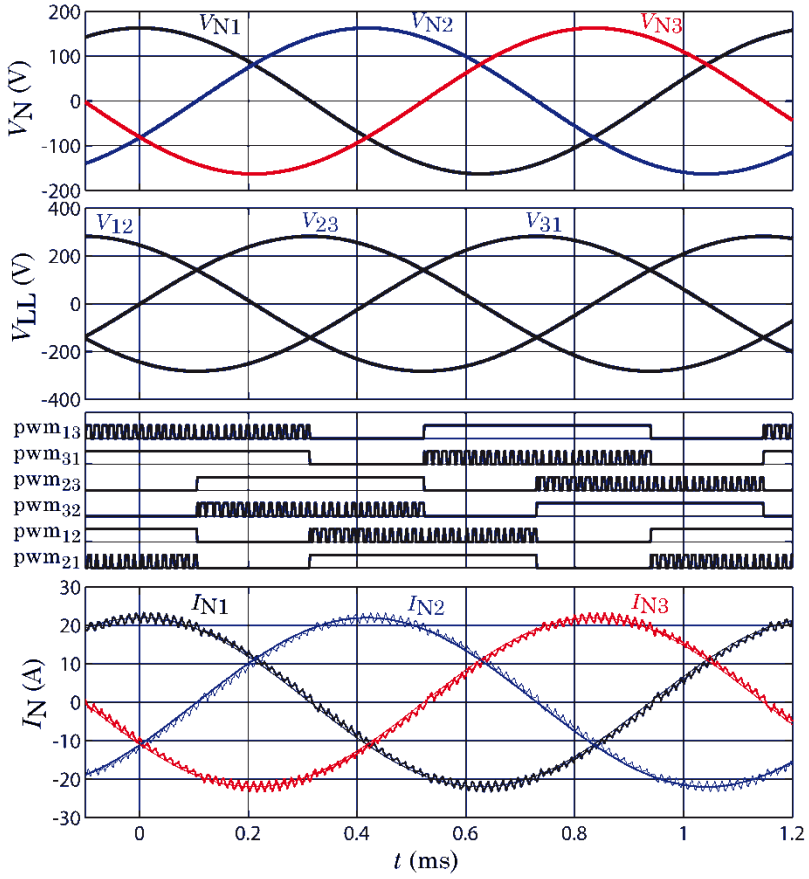
▶ Δ-Switch Rectifier

■ Modulation

U_{LL} = 115 V (400Hz)
P_o = 5 kW
U_o = 400 V
f_S = 72 kHz

Power Density: 2.35 kW/dm³



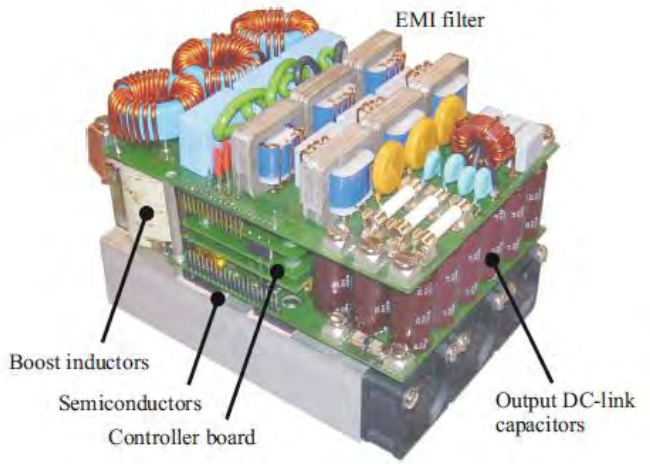


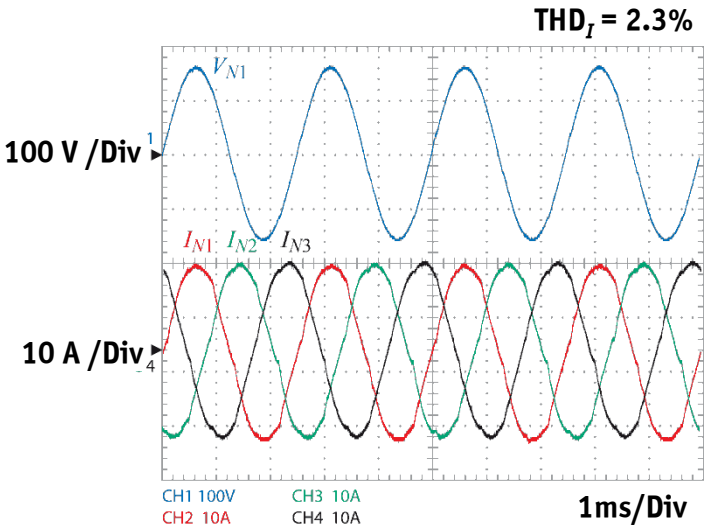
▶ Δ-Switch Rectifier

■ Experimental Analysis

U_{LL} = 115 V (400Hz)
P_o = 5 kW
U_o = 400 V
f_S = 72 kHz

Power Density: 2.35 kW/dm^3

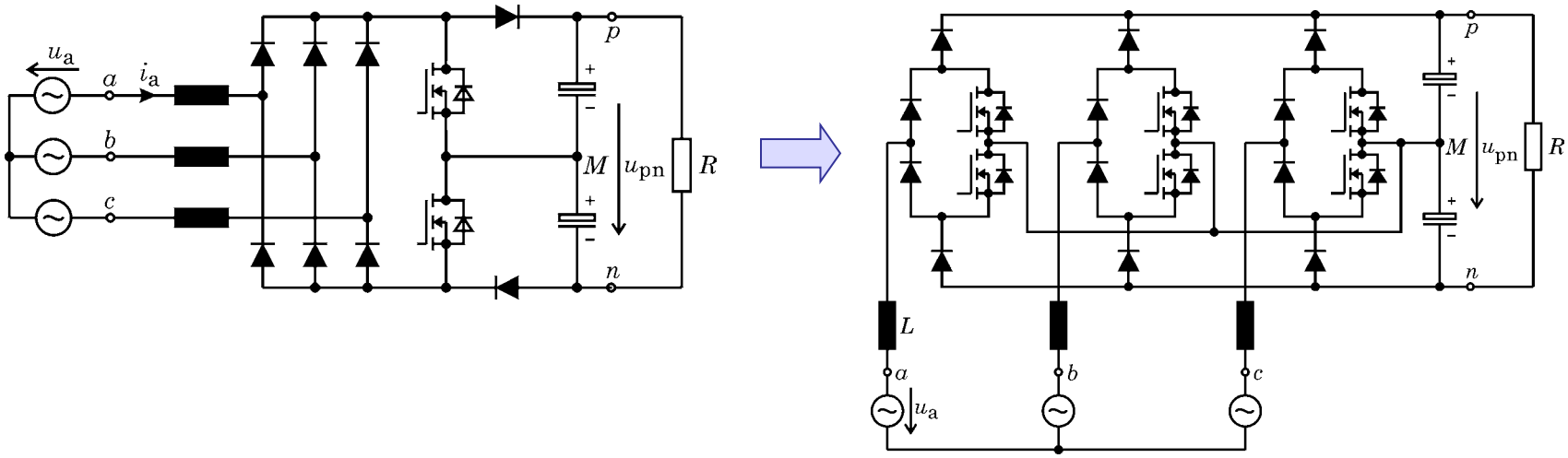




Three-Level Boost-Type CCM PFC Rectifier System

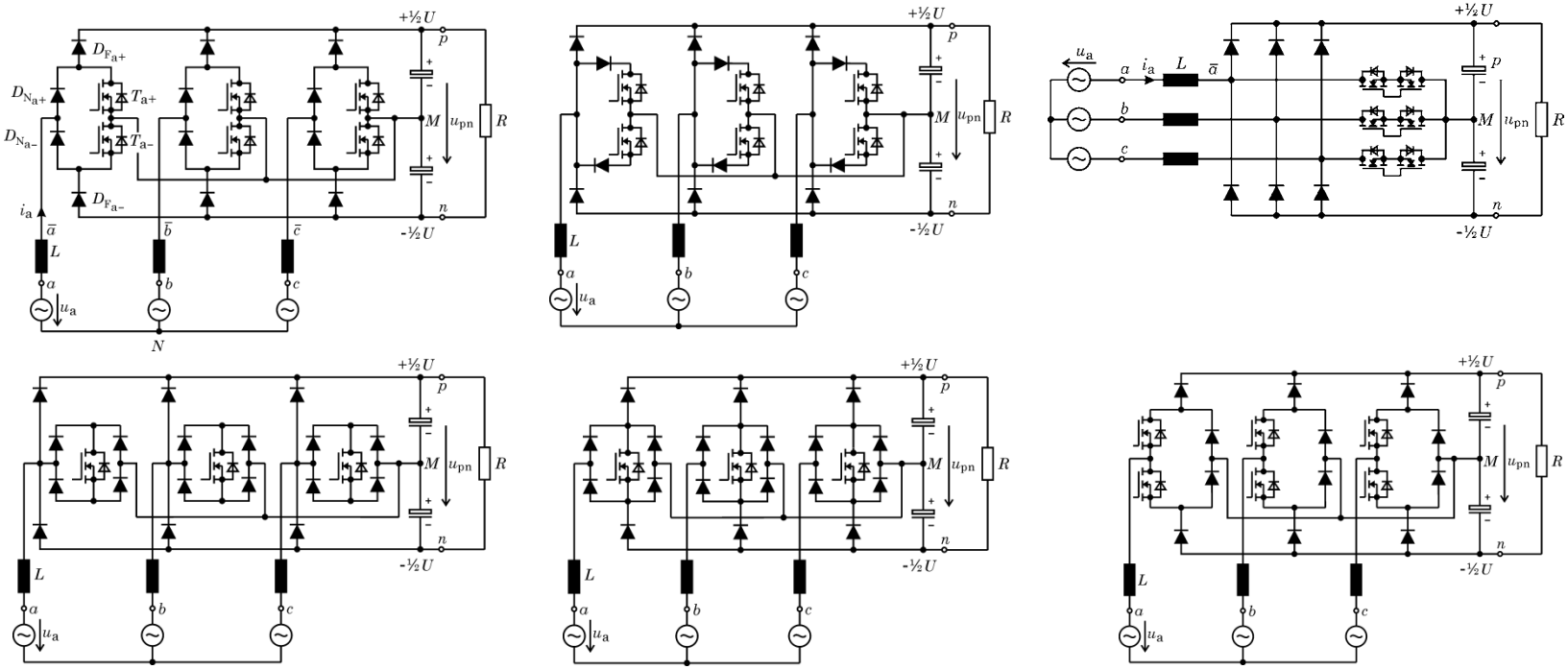
- *Derivation of Circuit Topologies*

▶ Derivation of Three-Level Rectifier Topologies (1)



- **Sinusoidal Mains Current Shaping Requires Independent Controllability of the Voltage Formation of the Phases**

▶ Derivation of Three-Level Rectifier Topologies (2)



- **Three-Level Characteristics**

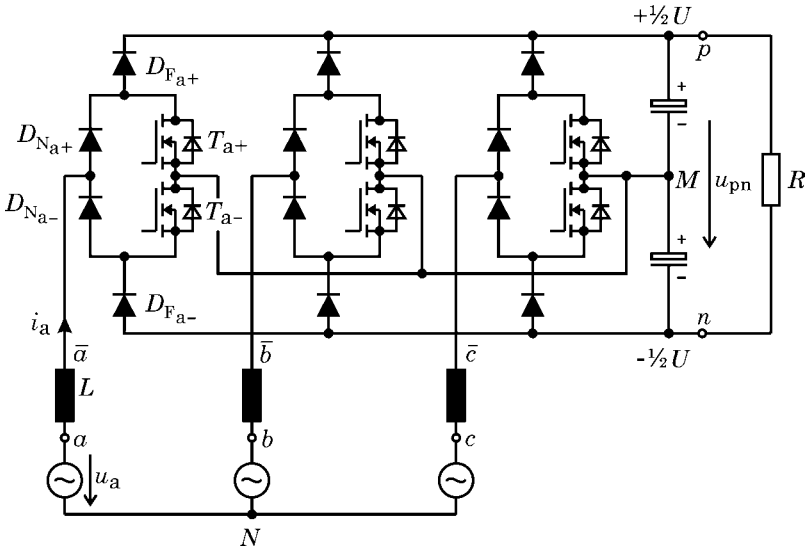
+ Low Input Inductance Requ.
+ Low Switching Losses,
+ Low EMI

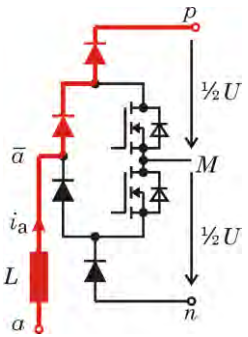
– Higher Circuit Complexity
– Control of Output Voltage Center Point Required

Three-Level PFC Rectifier Analysis

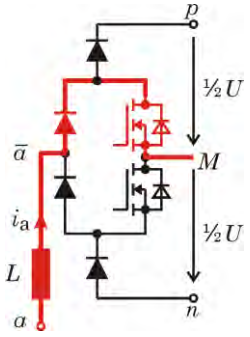
- *Input Voltage Formation*
- *Modulation / Sinusoidal Input Current Shaping*
- *Output Center Point Formation*
- *Control*
- *Design Considerations*
- *EMI Filtering*
- *Digital Control*
- *Experimental Analysis*

▶ Input Voltage Formation

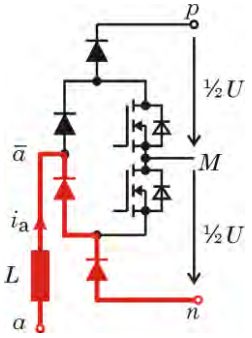




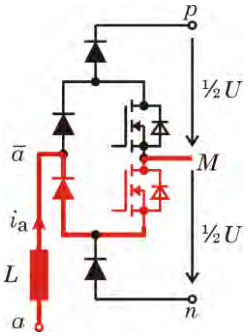
$s_a = 0$
T_{a+}, T_{a-}: OFF
$u_{\bar{a}M} = +½U$



$s_a = 1$
T_{a+}, T_{a-}: ON
$u_{\bar{a}M} = 0$



$s_a = 0$
T_{a+}, T_{a-}: OFF
$u_{\bar{a}M} = -½U$



$s_a = 1$
T_{a+}, T_{a-}: ON
$u_{\bar{a}M} = 0$

- **Voltage Formation**

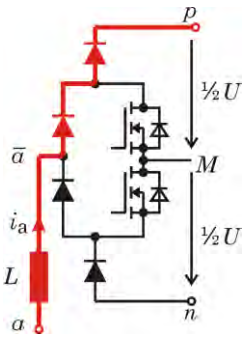
$$u_{\bar{a}M} = (1 - s_a)\,\mathrm{sign}(i_a)\,\frac{U}{2}$$

is Determined by Phase Switching State AND Direction of Phase Current

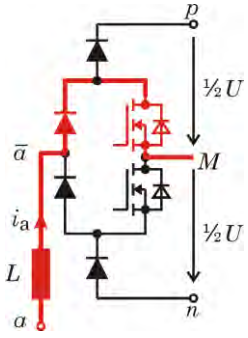
▶ Semiconductor Blocking Voltage Stress

■ Blocking Voltage Definition

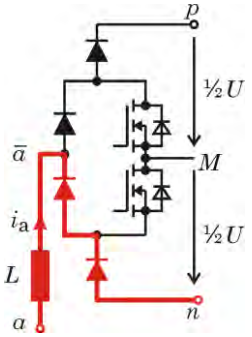
- D_{F+}: Limited to U_+ via Parasitic Diode of T_{a+}
- D_{N+}: Not Dir. Def. by Circuit Structure
- D_{N-}: Not Dir. Def. by Circuit Structure
- D_{F-}: Limited to U_- via Paras. Diode of T_{a-}
- T_{a+}: Limited to U_+ via D_{F+}
- T_{a-}: Limited to U_- via D_{F-}



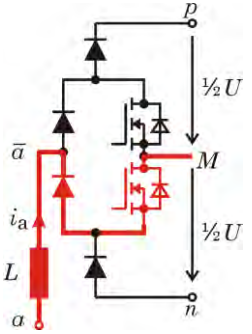
$s_a = 0$
T_{a+}, T_{a-}: OFF
$u_{\bar{a}M} = +½U$



$s_a = 1$
T_{a+}, T_{a-}: ON
$u_{\bar{a}M} = 0$

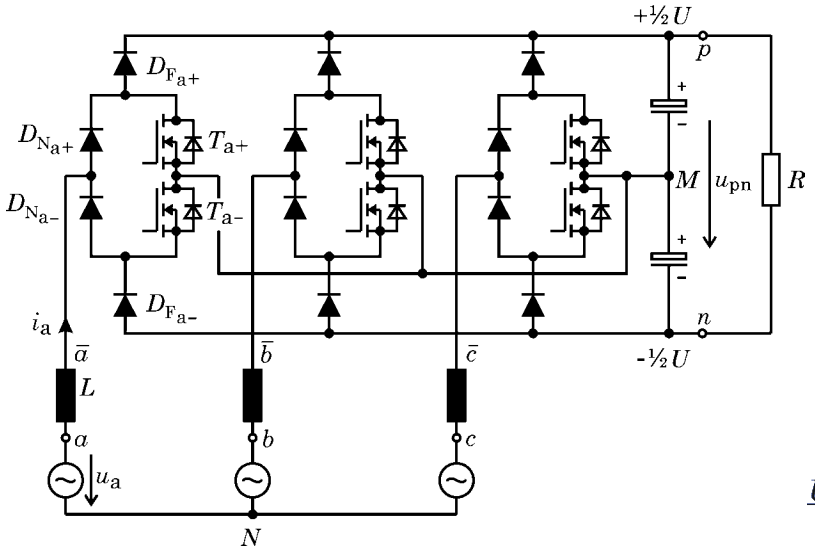


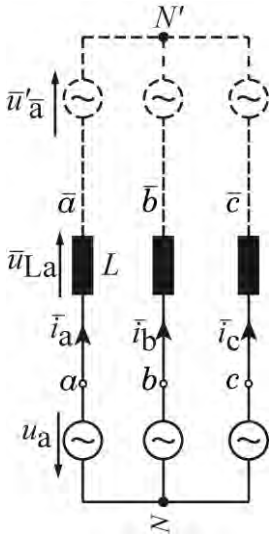
$s_a = 0$
T_{a+}, T_{a-}: OFF
$u_{\bar{a}M} = -½U$

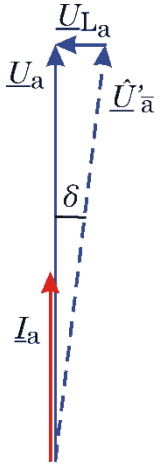


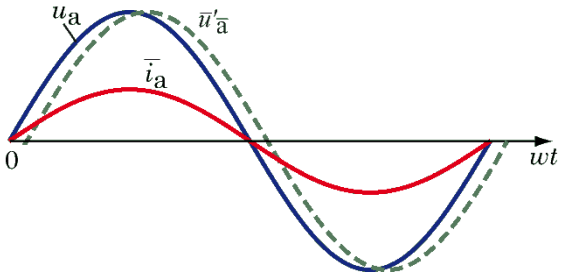
$s_a = 1$
T_{a+}, T_{a-}: ON
$u_{\bar{a}M} = 0$

▶ Impression of Input Current Fund. (Ohmic Fund. Mains Behavior)









δ = 0,1°... 0,3° (50/60 Hz)
δ = 1°... 3° (360 Hz ... 800 Hz)

- Difference of Mains Voltage (e.g. u_a) and Mains Frequency Comp. of Voltage Formed at Rectifier Bridge Input (e.g. $\bar{u}'_{\bar{a}}$) Impresses Mains Current (e.g. i_a)

▶ PWM / Formation of $\bar{u}_a$, $\bar{u}_b$, $\bar{u}_c$ / AC-Side Equiv. Circuit (1)

- **Def. of Modulation Index:**

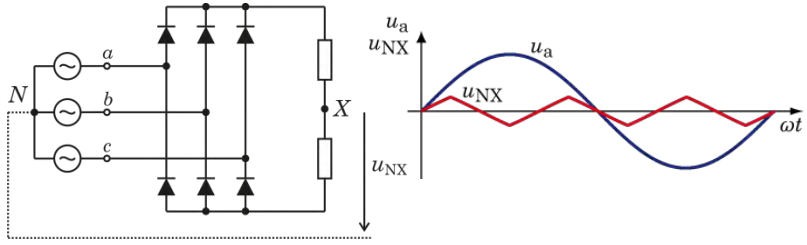
$$M = \frac{\hat{U}_{\bar{a}}}{\frac{1}{2}U} \qquad \left(0 \ldots \frac{2}{\sqrt{3}}\right)$$

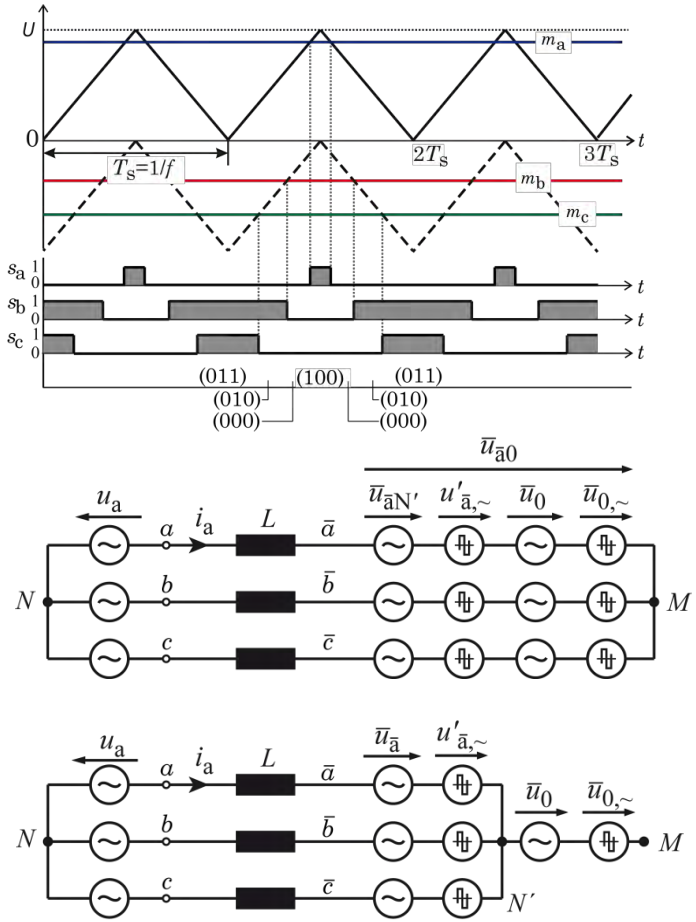
- **Zero-Sequence Signal to Achieve Ext. Mod. Range**

$$u_{\bar{a}0} = u'_{\bar{a}} + u_0$$
$$u_{\bar{b}0} = u'_{\bar{b}} + u_0$$
$$u_{\bar{c}0} = u'_{\bar{c}} + u_0$$

$$u'_{\bar{a}} + u'_{\bar{b}} + u'_{\bar{c}} = 0$$
$$u_0 = \frac{1}{3}\left(u_{\bar{a}0} + u_{\bar{b}0} + u_{\bar{c}0}\right)$$

- **Generation of u_0, *i.e.* 3rd Harmonic Signal**





▶ PWM / Formation of $\bar{u}_a$, $\bar{u}_b$, $\bar{u}_c$ / AC-Side Equiv. Circuit (2)

$\bar{u}'_a, \bar{u}'_b, \bar{u}'_c$ — Impression of Mains Current Fundamental in Combination with u_a, u_b, u_c

$$u'_{\bar{a}} = u_{\bar{a}N'} = \bar{u}'_{\bar{a}} + u_{\bar{a}\sim}$$
$$u'_{\bar{b}} = u_{\bar{b}N'} = \bar{u}'_{\bar{b}} + u_{\bar{b}\sim}$$
$$u'_{\bar{c}} = u_{\bar{c}N'} = \bar{u}'_{\bar{c}} + u_{\bar{c}\sim}$$

$\bar{u}'_{a\sim}, \bar{u}'_{b\sim}, \bar{u}'_{c\sim}$ — Causing the Switching Frequ. Ripple of the Mains Currents and/or DM Filtering Requirement

Note: $u_{NN'} = 0$

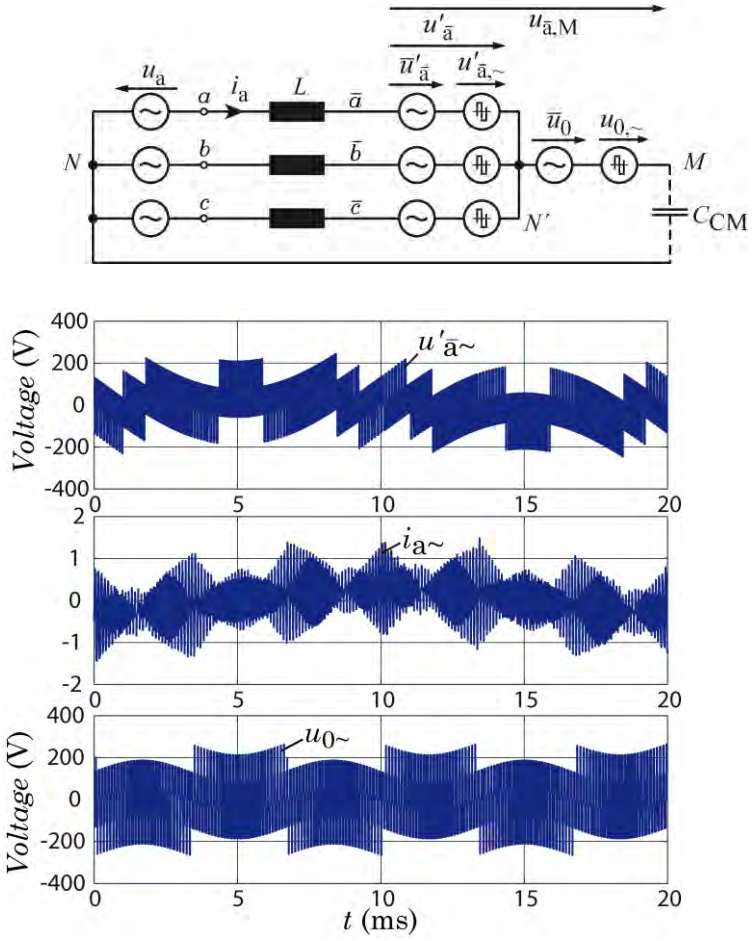
$$u_{\bar{a}0} = u'_{\bar{a}} + u_0$$
$$u_{\bar{b}0} = u'_{\bar{b}} + u_0$$
$$u_{\bar{c}0} = u'_{\bar{c}} + u_0$$

$\bar{u}_0$ — Low Frequency Zero Sequence Component for Extending the Modulation Range from $M = 0 \ldots 1$ (Sinusoidal Modulation) to $M = 0 \ldots \frac{2}{\sqrt{3}}$

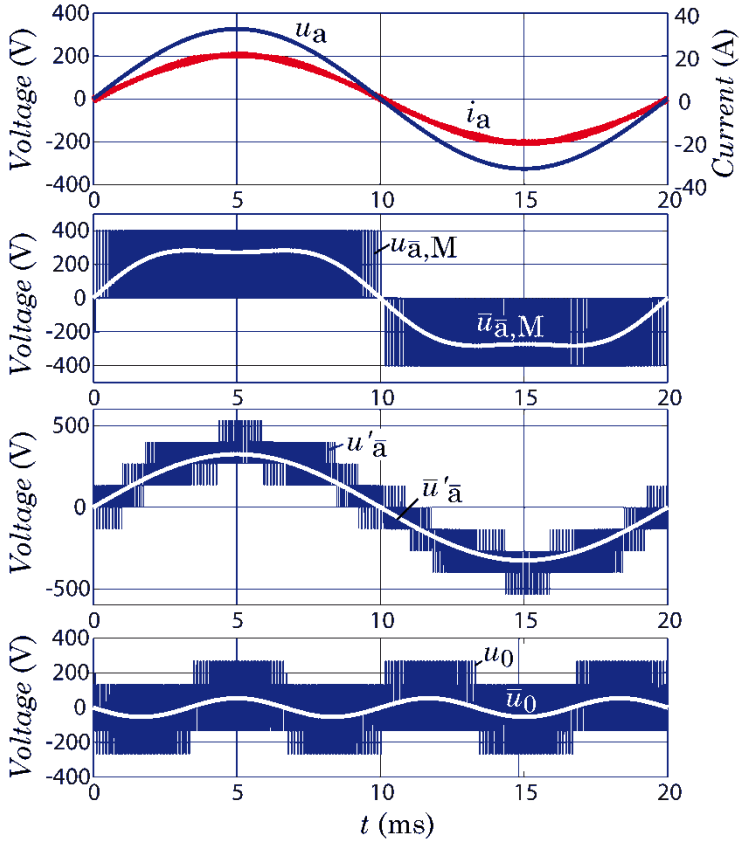
$$u_0 = \bar{u}_0 + u_{0\sim}$$

$u_{0\sim}$ — Switching Frequency CM Voltage Fluctuation of the Output → Resulting in CM Current and/or CM Filtering Requirement

▶ Time Behavior of the Components of Voltages $u_{\bar{a}}$, $u_{\bar{b}}$, $u_{\bar{c}}$



$$i_a = \bar{i}_a + i_{a\sim}$$



▶ Local Average Value of Center Point Current

- **Derivation of Low-Frequency Component $\bar{i}_M$ of Center Point Current Assuming a 3rd Harmonic Component of u_0 as Employed for Increasing the Modulation Range)**

Assumption: $i_a > 0, i_b < 0, i_c < 0$

$$m_a = m'_a + m_0 = M_1 \cdot \cos(\omega t) + M_3 \cdot \cos(3\omega t)$$

$$m_b = m'_b + m_0 = M_1 \cdot \cos\left(\omega t - \frac{2\pi}{3}\right) + M_3 \cdot \cos(3\omega t)$$

$$m_c = m'_c + m_0 = M_1 \cdot \cos\left(\omega t + \frac{2\pi}{3}\right) + M_3 \cdot \cos(3\omega t)$$

$$M_1 = \frac{\hat{U}}{\frac{1}{2}U} \qquad M_3 = \frac{\hat{U}_0}{\frac{1}{2}U}$$

$\alpha_a = 1 - m_a$ (relative on-time of T_{a+})

$\alpha_b = 1 - m_b$ (relative on-time of T_{b+})

$\alpha_c = 1 - m_c$ (relative on-time of T_{c+})

$$\bar{i}_M = \alpha_a \cdot i_a + \alpha_b \cdot i_b + \alpha_c \cdot i_c$$
$$= (1 - m_a) \cdot i_a + (1 - m_b) \cdot i_b + (1 - m_c) \cdot i_c$$

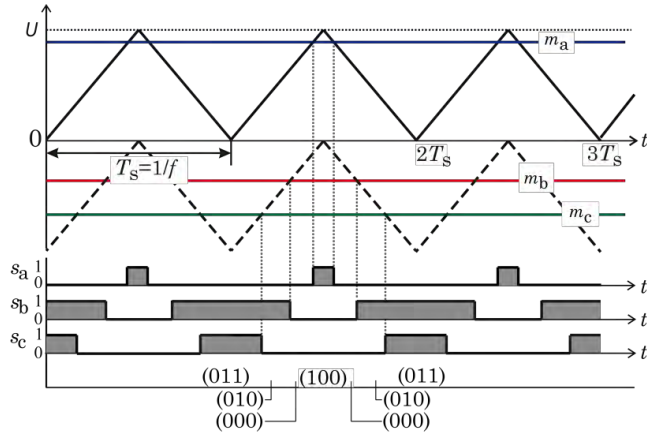
RMS of $\bar{i}_M$ minimal for $\frac{M_3}{M_1} \approx \frac{1}{4}$

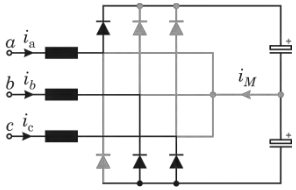
- **m_0, i.e. PWM incl. 3rd Harm., Reduces $\bar{i}_M$ and Extends the Modulation Range**

▶ Cond. States within a Pulse Period / Center Point Current Formation

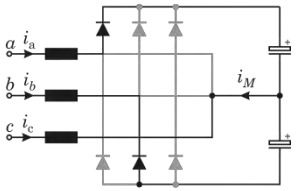
- Consider e.g. $i_a > 0, i_b < 0, i_c < 0$

- Switching States (100), (011) are Forming Identical Voltages u'_a, u'_b, u'_c but Inverse Centre Point Currents i_M
- Control of i_M by Changing the Partitioning of Total On-Times of (100) and (011)

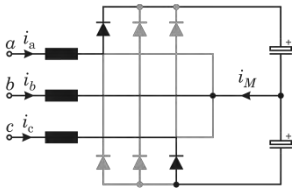




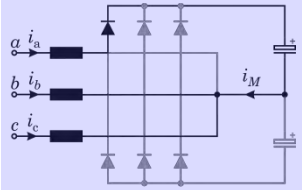
(000), $i_M = 0$



(001), $i_M = i_a$

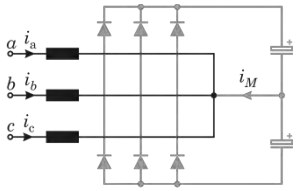


(010), $i_M = -i_b$

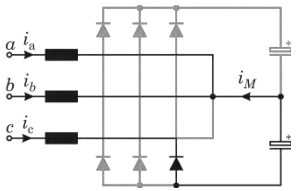


(011), $i_M = i_a$

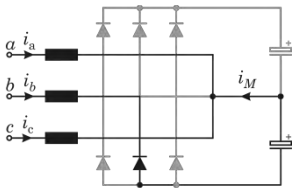
- Corresponding Switching States and Resulting Currents Paths



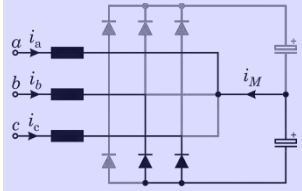
(111), $i_M = 0$



(110), $i_M = i_c$



(101), $i_M = i_b$

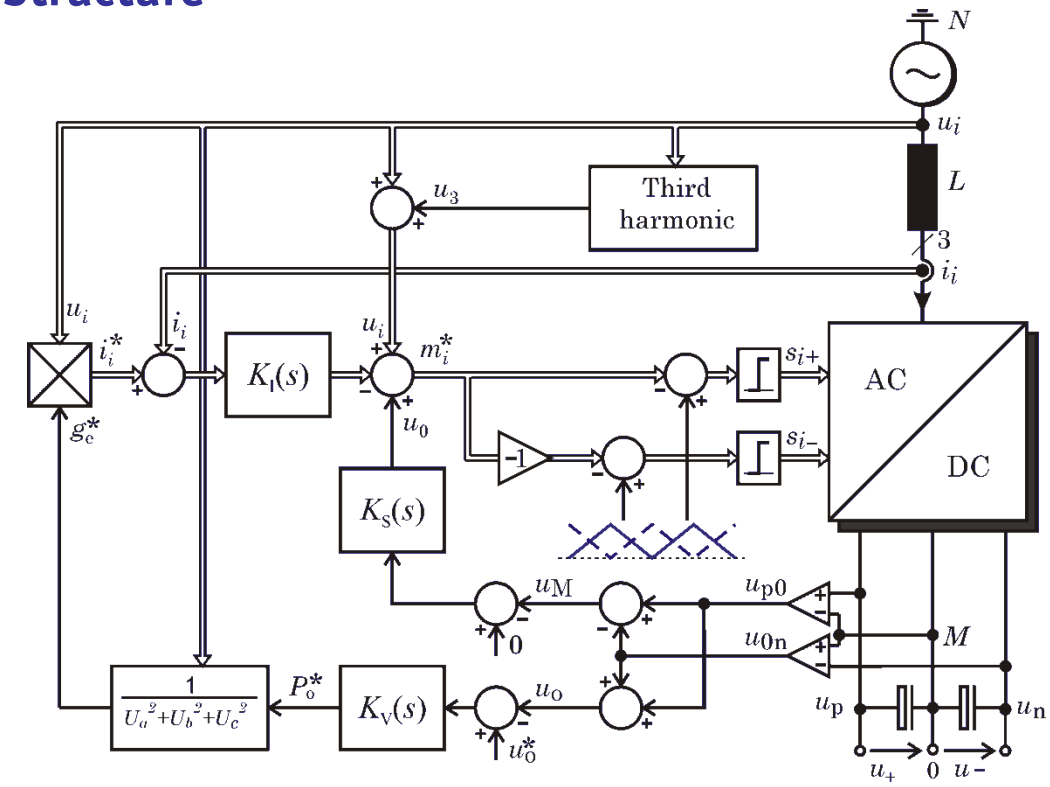


(100), $i_M = -i_a$

System Control

- *Control Structure*
- *Balancing of the Partial Output Voltages*

▶ Control Structure

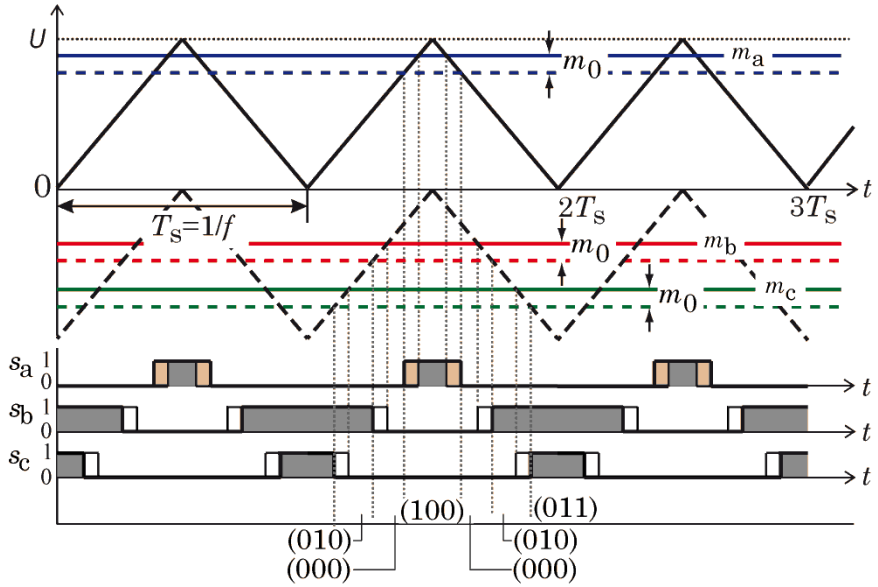


- Output Voltage Control
- Mains Phase Current Control
- Control of Output Center Point Potential (Balancing of U_+, U_-)

- Control of i_a, i_b, i_c Relies on $u_{\overline{a}}$, $u_{\overline{b}}$, $u_{\overline{c}}$
- Control of u_M Relies on $\overline{u}_0$ (DC Component)
- No Cross Coupling of both Control Loops

▶ Control of Potential u_M of Output Voltage Center Point

- **Assumption: $i_a > 0$, $i_b < 0$, $i_c < 0$**



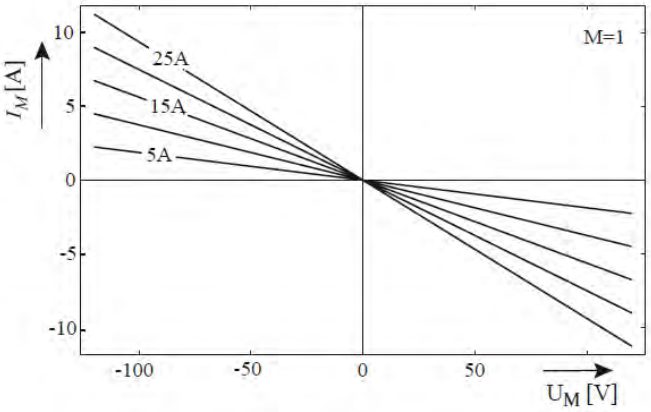
- **Control via DC Component of u_0, i.e. by Adding m_0 to the Phase Modulation Signals i.e. by Inversely Changing the Rel. On-Times of (100) and (011), $\delta_{(100)}$ and $\delta_{(011)}$, without taking Influence on the Total On-Time $\delta_{(100)} + \delta_{(011)}$.**

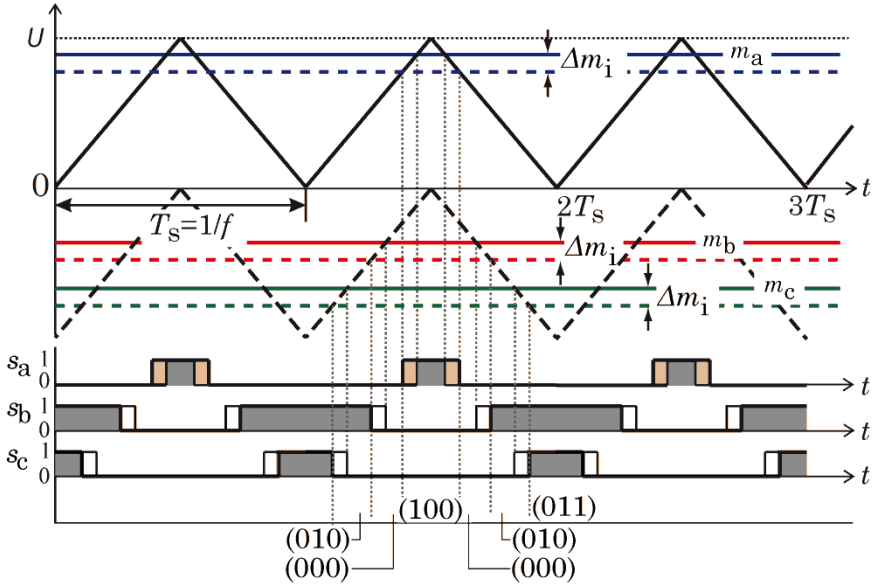
▶ Control of Output Voltage Center Point Potential u_M

- **Assumption:**

$$U_+ = \frac{1}{2}U + \Delta U$$

$$U_- = \frac{1}{2}U - \Delta U$$

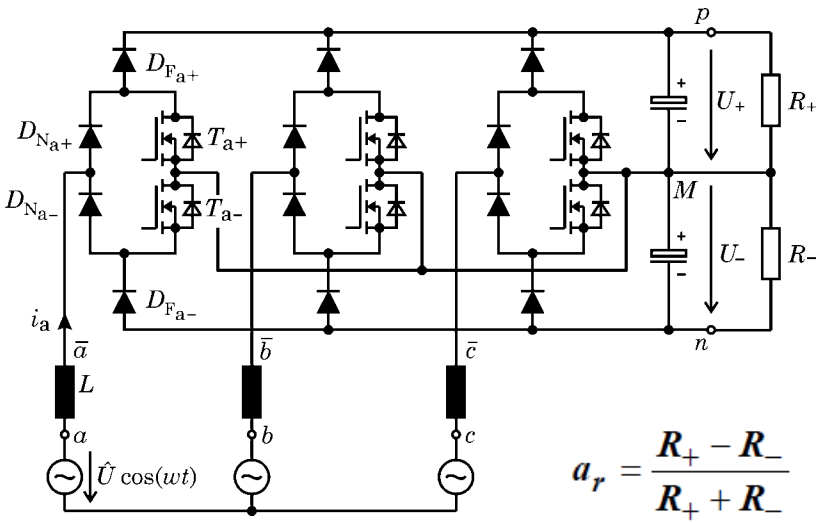




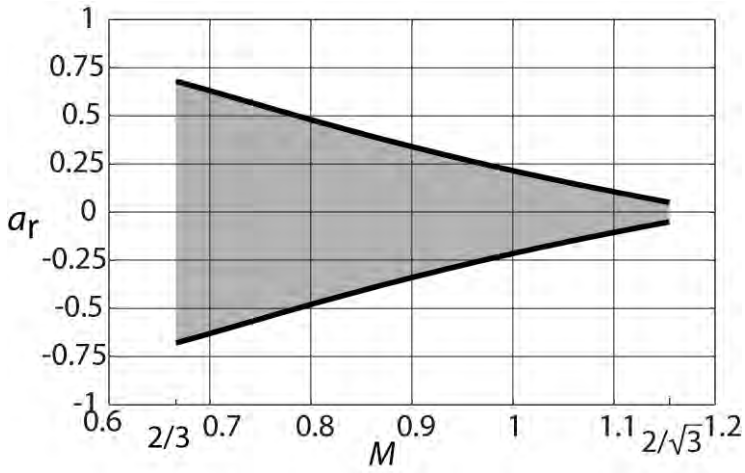
- **Output Voltage Unbalance Results in Increasing On-Time of T_{a+} and Decreasing Off-Times of T_{b-} and T_{c-} so that the Voltages $\overline{u}'_{\overline{a}}$, $\overline{u}'_{\overline{b}}$, $\overline{u}'_{\overline{c}}$ are Formed as in the Symmetric Case ($\Delta U = 0$) and/or the Mains Phase Currents Remain at Sinusoidal Shape**

- **Resulting $\bar{i}_M$ Reduces ΔU, i.e. Self Stability Guaranteed** ✓

▶ Admissible Unbalance of Loading of U_+ and U_-



$$a_r = \frac{R_+ - R_-}{R_+ + R_-}$$



- System Tolerates Load Unbalance Dependent on the Voltage Transfer Ratio $(U_+ + U_-)/\hat{U}$ and/or the Value of The Modulation Index M

Design Guidelines

- *Current Stress on the Components*
- *Transistor Selection*
- *Output Pre-Charging at Start-up*

▶ Current Stress on Power Semiconductors

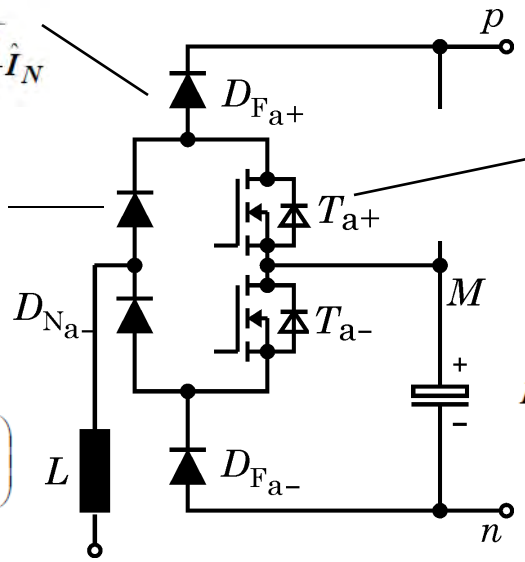
■ 6-Switch Circuit Topology

$$I_{DF,avg} = \frac{M}{4}\hat{I}_N$$

$$I_{DF,rms} = \sqrt{\frac{2M}{3\pi}}\hat{I}_N$$

$$I_{DN,avg} = \frac{1}{\pi}\hat{I}_N$$

$$I_{DN,rms} = \frac{1}{2}\hat{I}_N$$



$$I_{T,avg} = \left(\frac{1}{\pi} - \frac{M}{4}\right)\hat{I}_N$$

$$I_{T,rms} = \sqrt{\frac{1}{4} - \frac{2M}{3\pi}}\hat{I}_N$$

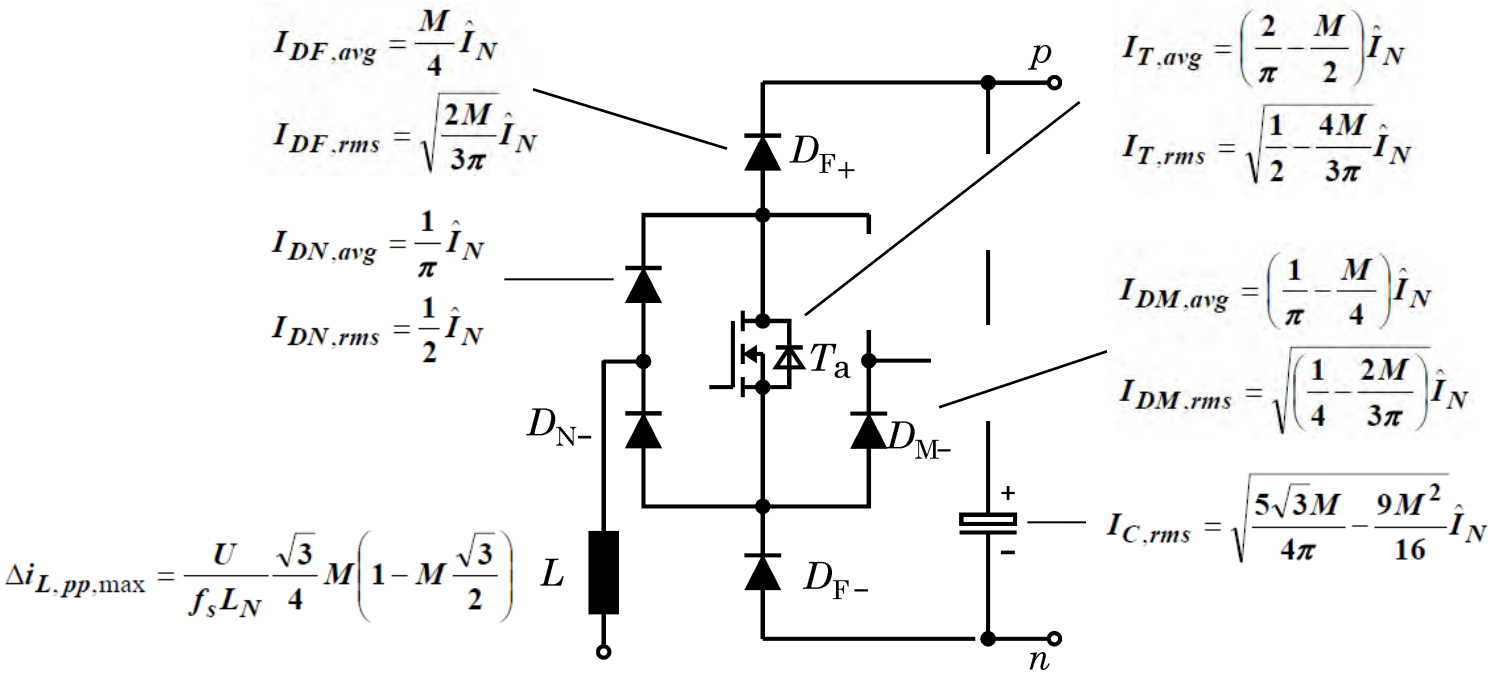
$$I_{C,rms} = \sqrt{\frac{5\sqrt{3}M}{4\pi} - \frac{9M^2}{16}}\hat{I}_N$$

$$\Delta i_{L,pp,\max} = \frac{U}{f_s L_N}\frac{\sqrt{3}}{4}M\left(1 - M\frac{\sqrt{3}}{2}\right)$$

- Output Voltage > $\sqrt{3}\,\hat{U}_{max}$ (typ. 1.2 $\sqrt{3}\,\hat{U}_{max}$); $\hat{U}_{max}$: Ampl. of Max. Mains Phase Voltage
- Required Blocking Capability of All Semiconductors: ½ U

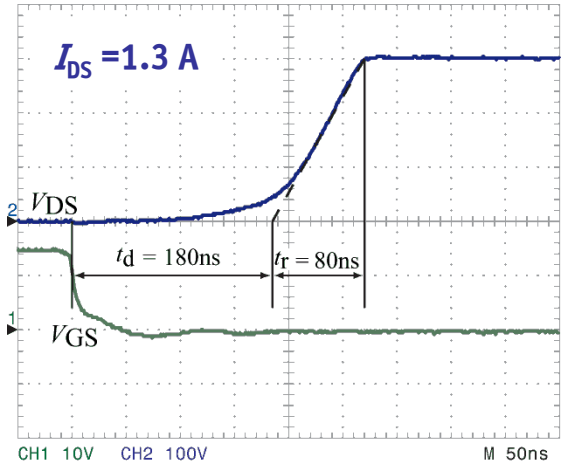
▶ Current Stress on Power Semiconductors

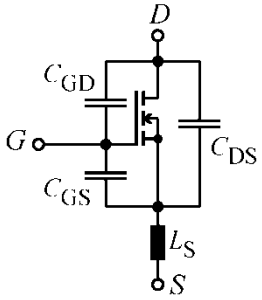
■ 3-Switch Circuit Topology

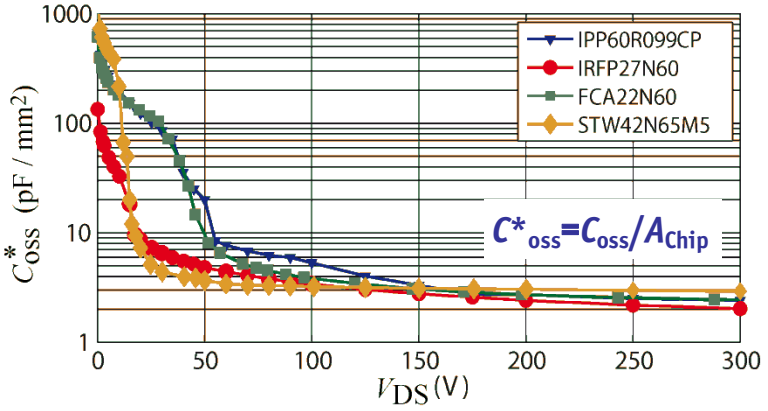


- Output Voltage > $\sqrt{3}\,\hat{U}_{max}$ (typ. 1.2 $\sqrt{3}\,\hat{U}_{max}$); $\hat{U}_{max}$: Ampl. of Max. Mains Phase Voltage
- Required Blocking Capability of All Semiconductors: ½ U

▶ Nonlin. C_{oss} of Superjunct. MOSFETs Causes Input Curr. Distortion

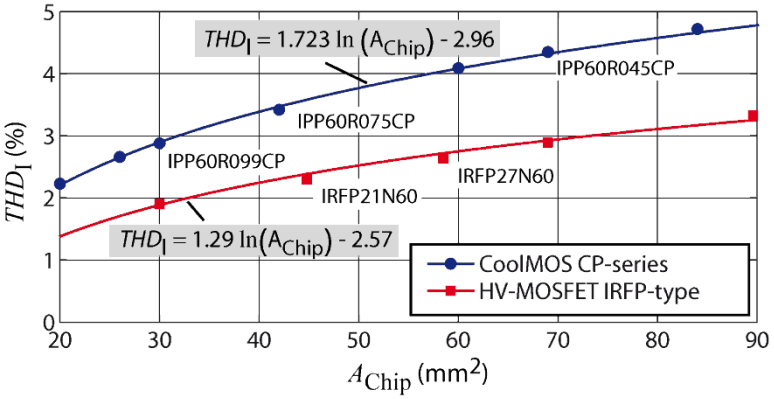






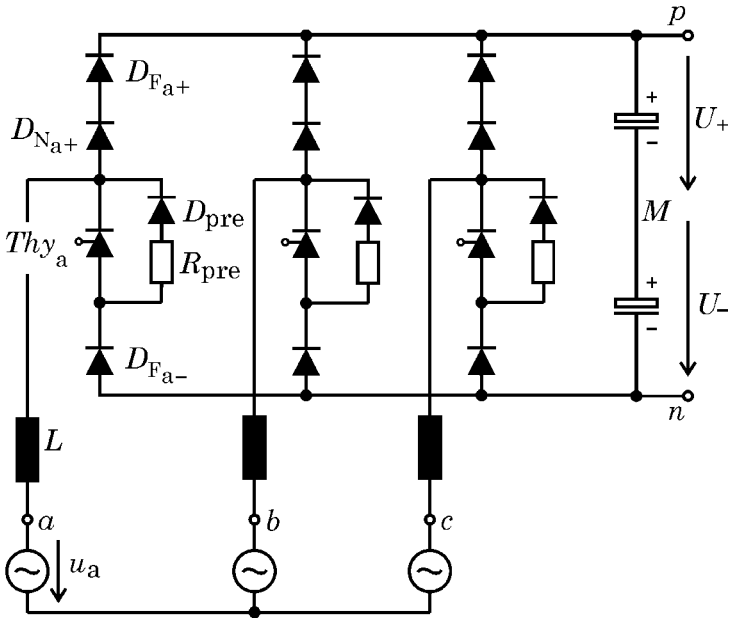
- Nonlinear Output Capacitance C_{oss} of MOSFET (CoolMOS) has to be Charged at Turn-off
- Large Turn-Off Delay for Low Currents (e.g. Delay of CoolMOS IPP60R099 (@ IDS = 1.3 A): 11% of Switching Cycle @ fs = 500 kHz
- Results in PWM Volt. and/or Input Curr. Distortion

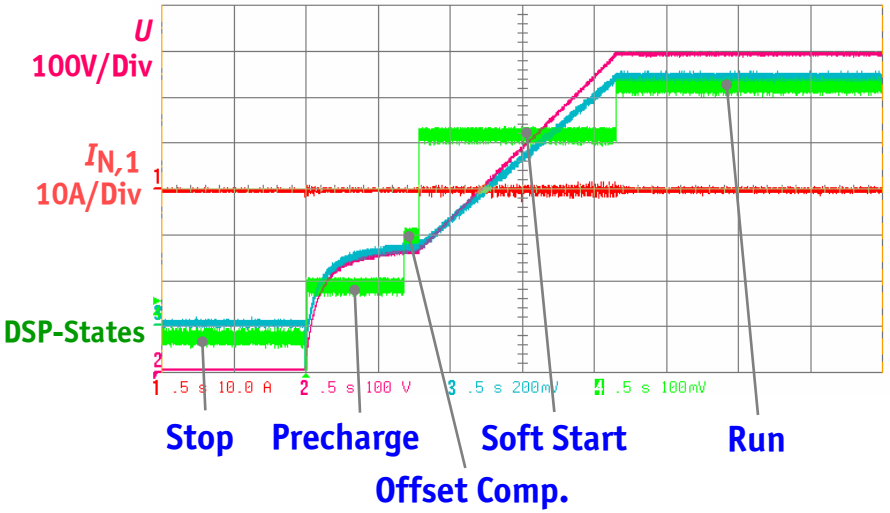
U_{LL} = 3 x 400 V (50 Hz), f_s = 1 MHz, P_O = 10 kW



▶ Pre-Charging of Output Capacitors / Start-Up Sequence

- Lower Mains Diode D_{N-} is Replaced by Thyristor
- Inrush Current is Limited by R_{pre}
- Switches are not Gated During Start-Up
- Start-up Sequence is Required





Digital Control Issues

- *Implementation Using a DSP vs. Using an FPGA*
- *Sampling Strategy*
- *Controller Requirements*

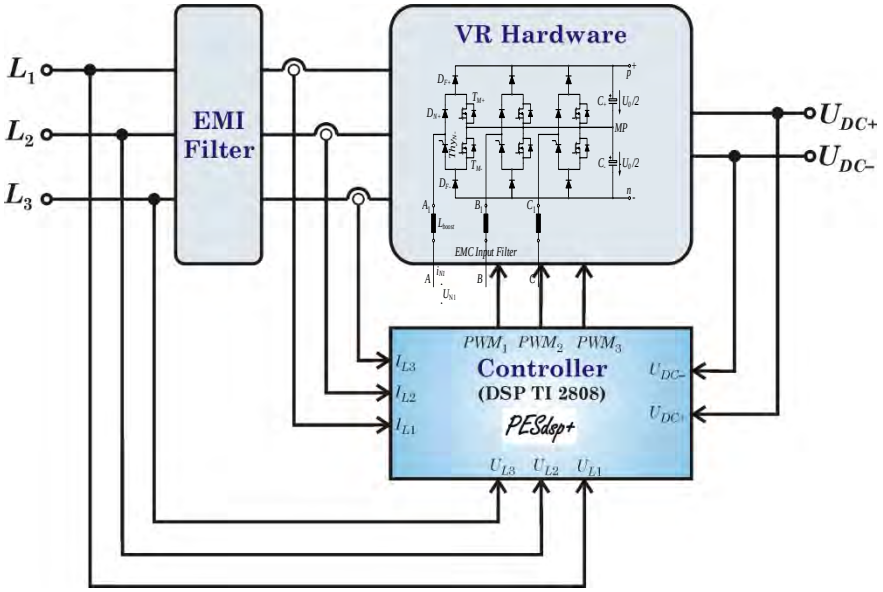
▶ Software Tasks

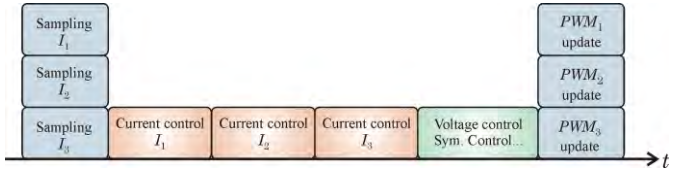
- Calculation of Controller Outputs
  - Current Controller
  - Voltage Controller
  - Balancing of Output Voltages
- Startup – Sequence
- Observe Error Conditions
  - Over-Voltage at the Output
  - Over-Current
  - Over-Temperature
  - Output Voltage Unbalance

▶ Digital Control Employing a Single DSP

+ Using ADC's of DSP
+ PWM Modules of DSP for PWM Gen.

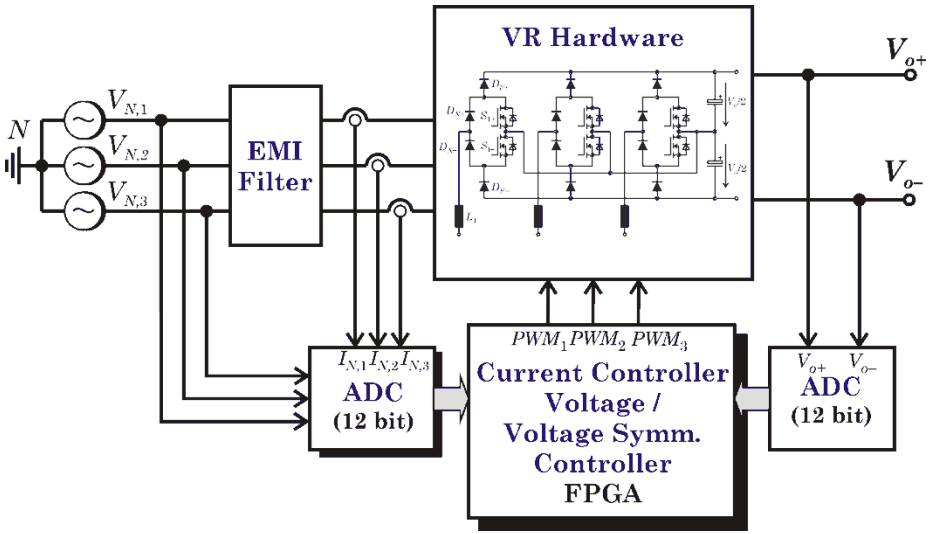
– Sequential Calculation
– Limited Calculation Capability

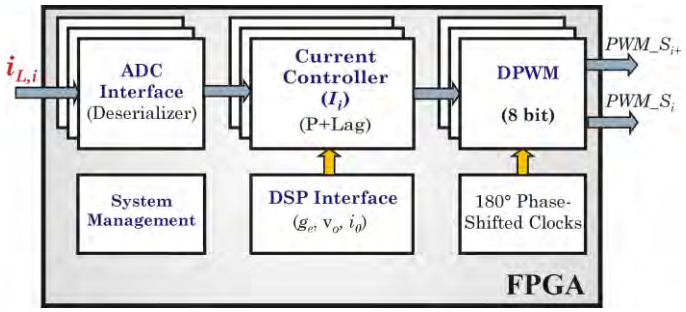


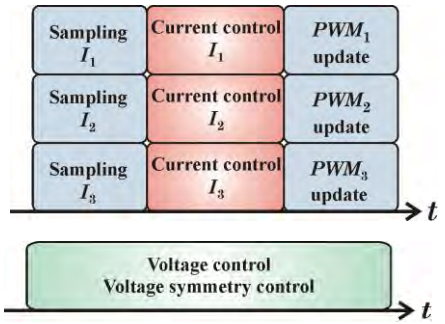


▶ Parallelization of Controller Calculation Required

▶ Implementation Using a Single FPGA

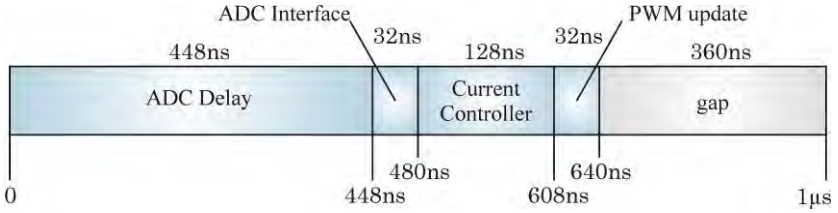






- External ADCs Required
- Calculation Capability Nearly Unlimited

- Example Timing VR1000 (f_s = 1 MHz):



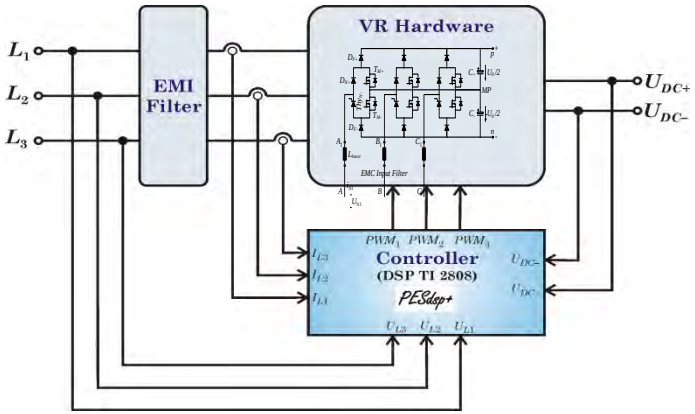
▶ Implementation Using an FPGA vs. a Single DSP

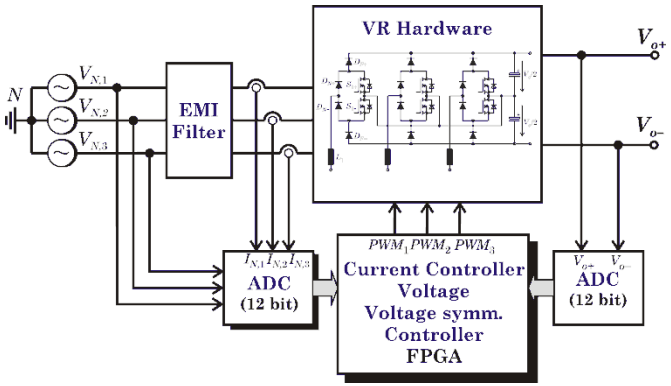
• Single DSP Implementation

+ No External ADCs Required
+ Easy Debugging
+ Implementation using C
− Limited Calculation Capability
− Glue Logic can Not be Included

• FPGA-Based Implementation

+ Calc. Capability Nearly Unlimited
+ Glue Logic can be Included
− External ADCs Required
− Debugging Not Easily Possible



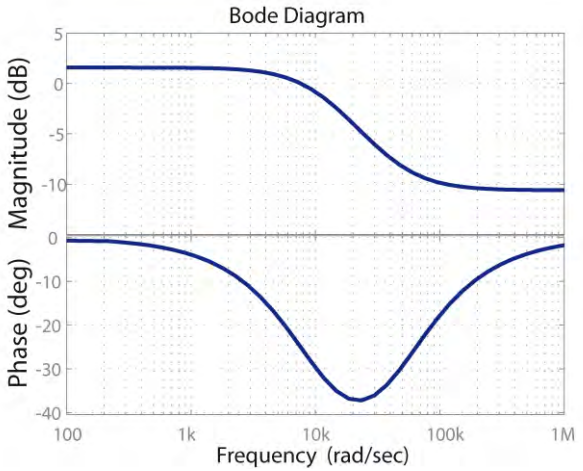


▶ Sampling Strategy / Current Controller

■ Current Controller

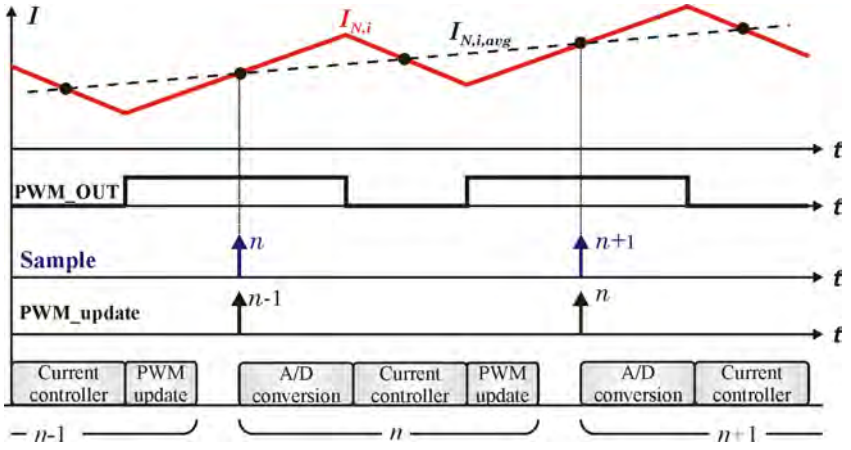
- PI-Type Controller Shows Problems With Integral Part at Current Zero Crossing
- P-Type Controller + Input Voltage Feed Forward Shows Good Results and can be Extended to P+Lag Controller (Improves Performance)

$$K(s) = K_P \frac{1 + sT_D}{1 + sT_1}$$



■ Sampling Strategy

- Sampling at the Pulse Period Midpoint (Symmetric) PWM, Direct Sampling of Fundamental
- Single Update or Double Update Possible
- Current Control of All Three Phases has to be Done in 1 Cycle



▶ Output Voltage Controller / Balancing of Partial Output Voltages

■ Output Voltage Controller

- Generates Conductance g_e for Ref. Value of Current Controller
- Design for No Steady State Deviation
- Needs to be Able to Handle Loss of a Mains Phase (Bandwidth << 2fN)
- Should show Good Dynamical Behavior at Load-Steps

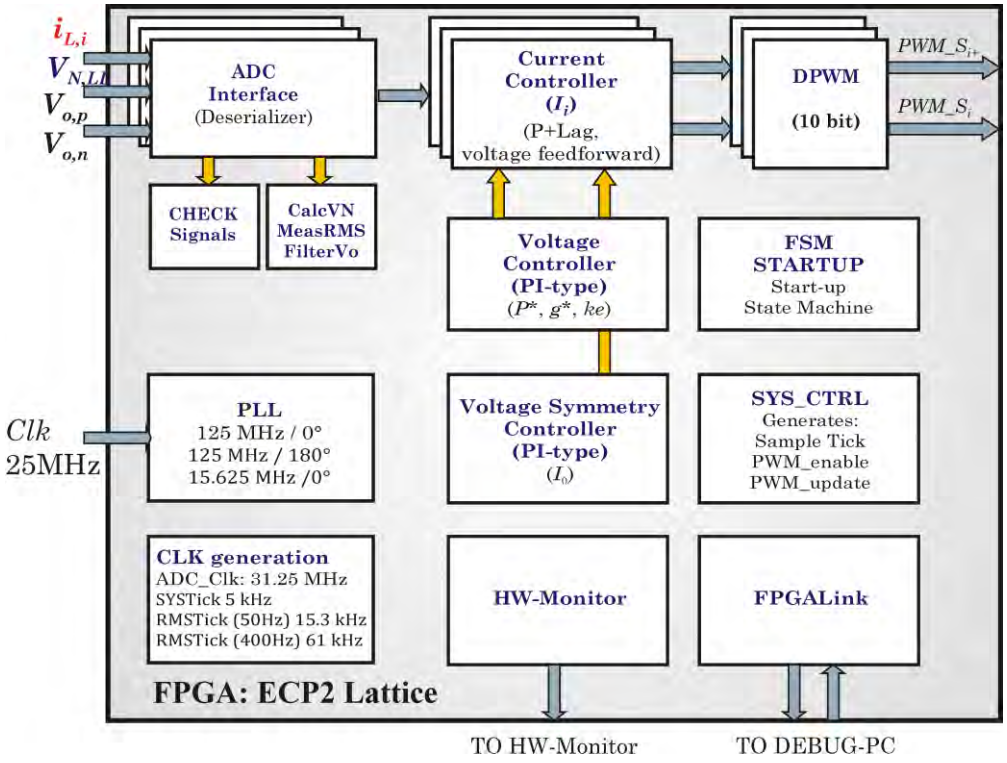
PI-Type – Controller is a Good Choice

■ Balancing of the Output Voltages

- Generates Controller Output u_0 ($\bar{m}_0$)
- Design for No Steady State Deviation
- Bandwidth has to be Set Lower than Three Times Mains Frequency f_N (Bandwidth << $3f_N$)
- Should Show Lowest Dynamic of all Control Loops

PI-Type – Controller is a Good Choice

▶ Example of Implementation Using an FPGA (VR250)



EMI Filtering

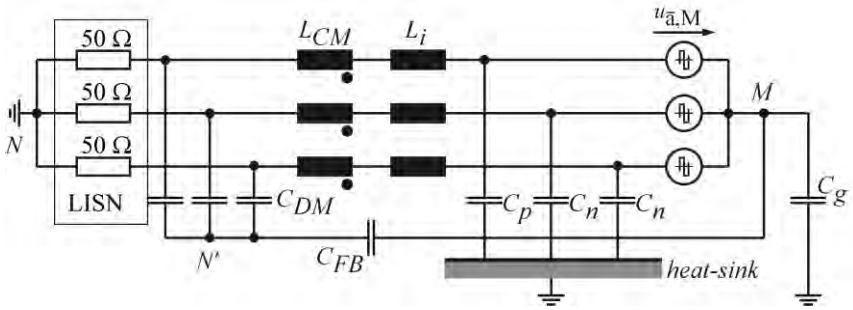
- *DM Filtering*
- *CM Filtering*

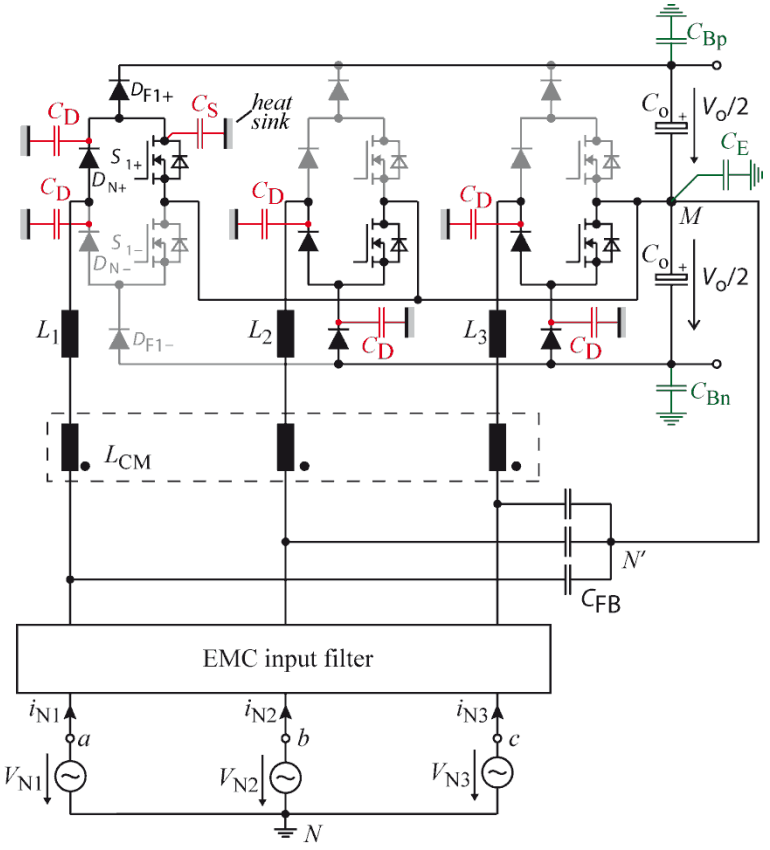
▶ EMI Filtering Concept

- DM and CM Filter Stages
- Connection of Output Voltage Midpoint *M* to Artificial Mains Star-Point *N′*

→ No High-Frequency CM-Voltage at *M*
→ Capacitance of C_{FB} Not Limited by Safety Standards

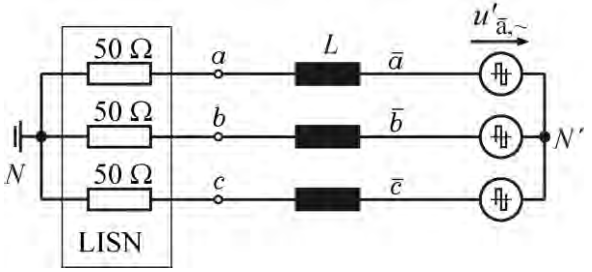
- Parasitic Capacitances have to be Considered for CM-Filter Design



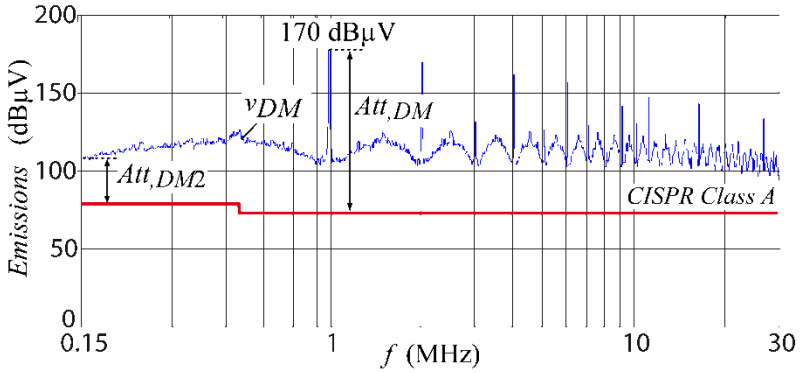


▶ DM Filter Design

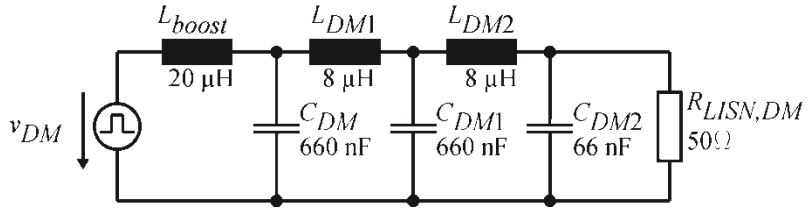
- **DM Equivalent Circuit**



- **Required DM Attenuation, e.g. for fs = 1 MHz (VR1000)**

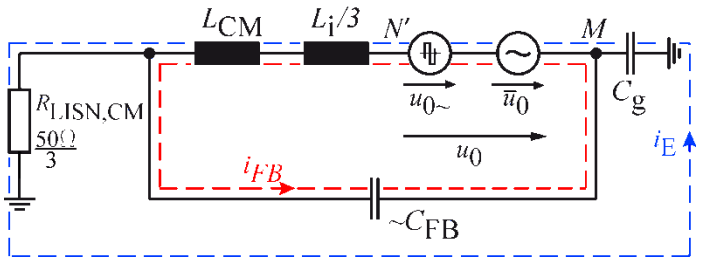


- **DM Filter Structure**



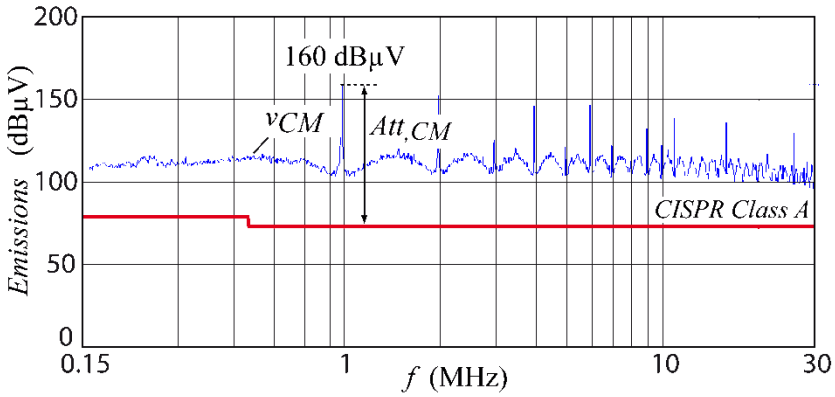
▶ CM Filter Design

- **CM Equivalent Circuit**



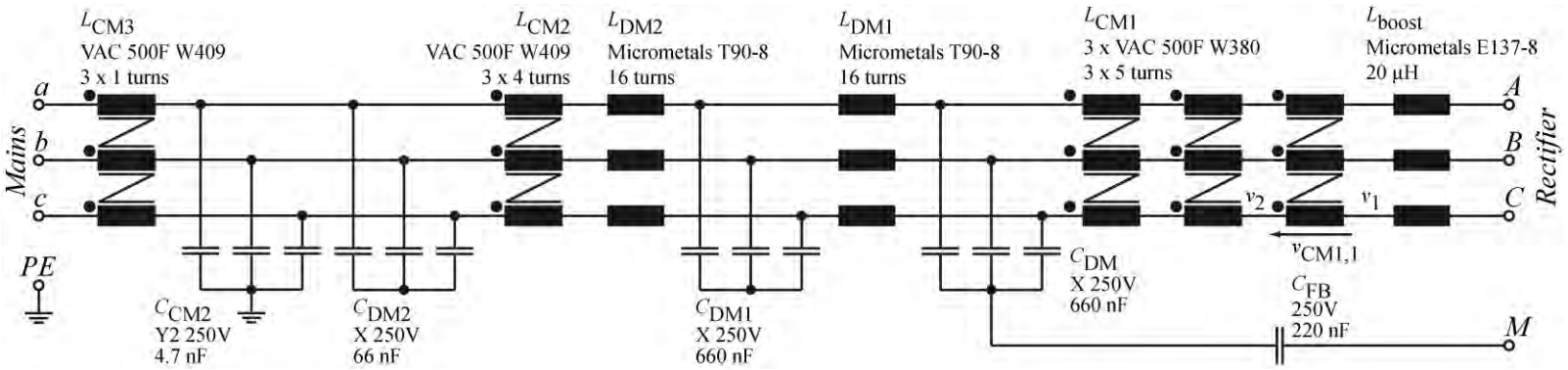
C_{FB} = 220 nF

- **Required CM Attenuation**



▶ EMI Filter Structure for VR1000 Rectifier System

- 3 Stage DM Filter
- 2 Filter Stages for CM Filter



- 3 x CM Inductors in Series to Implement Proposed Filter Concept
- Additional CM Filter Stage Required Due to Parasitic Capacitances

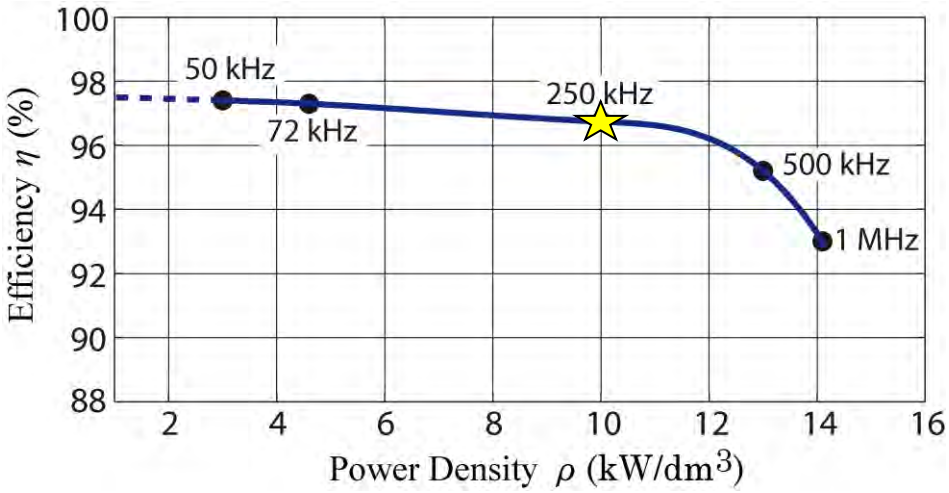
Experimental Analysis

- *Power Density / Efficiency Pareto Limit*
- *Experimental Analysis – VR250*

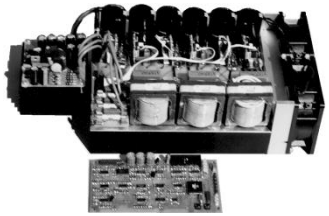
▶ Experimental Analysis

■ Generation 1 – 4 of VIENNA Rectifier Systems

- Switching Frequency of f_S = 250 kHz Offers Good Compromise Concerning Power Density / Weight per Unit Power, Efficiency and Input Current Quality THD_i



f_S = 50 kHz
ρ = 3 kW/dm³



f_S = 72 kHz
ρ = 4.6 kW/dm³

f_S = 250 kHz
ρ = 10 kW/dm³
(164 W/in³)
Weight = 3.4 kg

f_S = 1 MHz
ρ = 14.1 kW/dm³
Weight = 1.1 kg

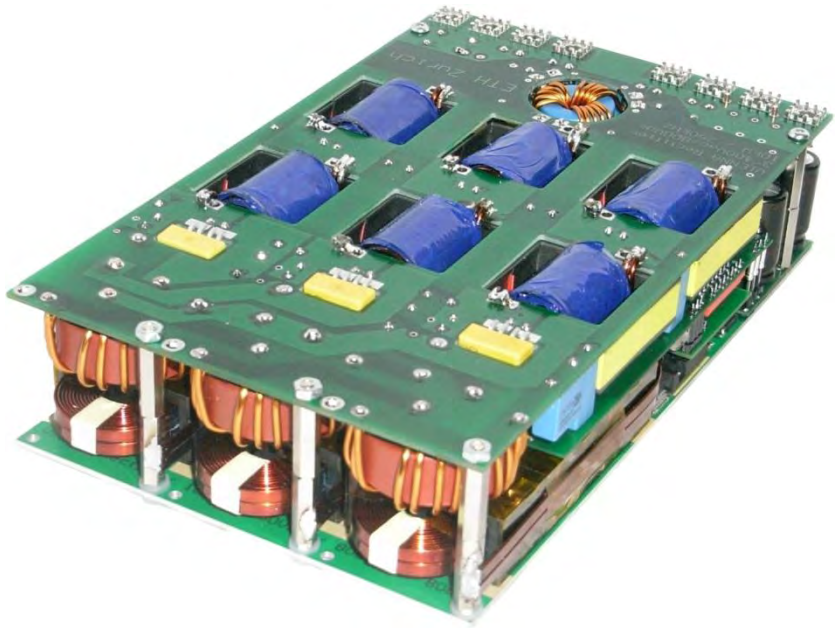
▶ Demonstrator – VR250 (1)

- **Specifications**

  U_{LL} = 3 x 400 V
  f_N = 50 Hz ... 60 Hz or 360 Hz ... 800 Hz
  P_o = 10 kW
  U_o = 2 x 400 V
  f_s = 250 kHz

- **Characteristics**

  η = 96.8 %
  THD_i = 1.6 % @ 800 Hz
  10 kW/dm3
  3.3 kg (≈3 kW/kg)



Dimensions: 195 x 120 x 42.7 mm^3

▶ Demonstrator – VR250 (2)

- **Specifications**

  U_{LL} = 3 x 400 V
  f_N = 50 Hz ... 60 Hz or 360 Hz ... 800 Hz
  P_o = 10 kW
  U_o = 2 x 400 V
  f_s = 250 kHz

- **Characteristics**

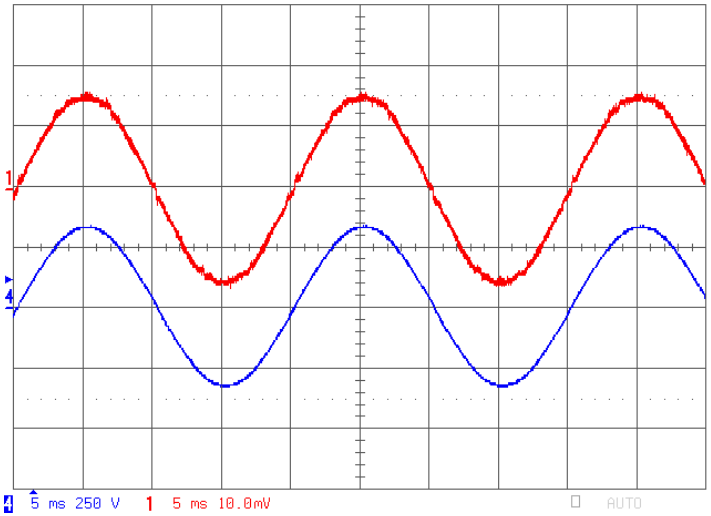
  η = 96.8 %
  THD_i = 1.6 % @ 800 Hz
  10 kW/dm3
  3.3 kg (≈3 kW/kg)

Dimensions: 195 x 120 x 42.7 mm^3

▶ Mains Behavior @ f_N = 50 Hz

P_O = 4kW
U_N = 230V
f_N = 50Hz
U_O = 800V
THD_i = 1.1%

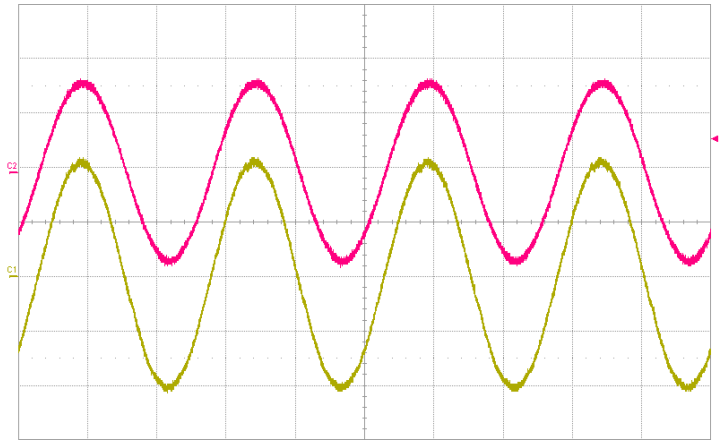
5A/Div
200V/Div
5ms/Div



▶ Mains Behavior @ f_N = 400Hz / 800Hz

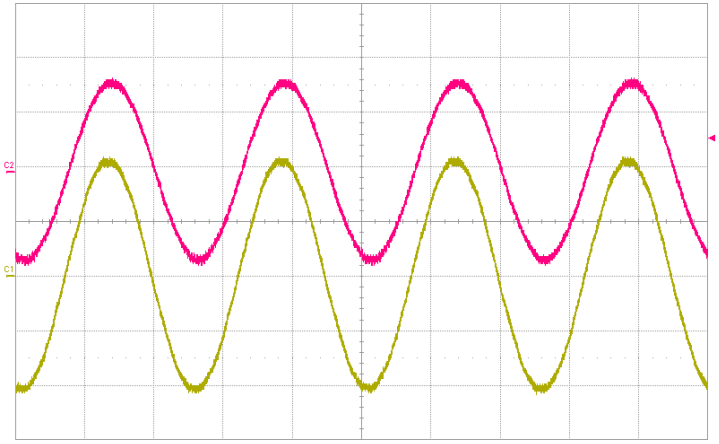
P_O = 10kW
U_N = 230V
f_N = 400Hz
U_O = 800V
THD_i = 1.4%

10A/Div
200V/Div
1ms/Div



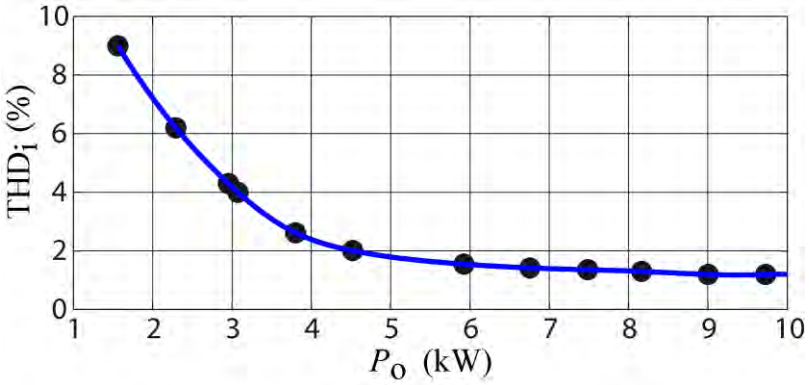
P_O = 10kW
U_N = 230V
f_N = 800Hz
U_O = 800V
THD_i = 1.6%

10A/Div
200V/Div
0.5ms/Div

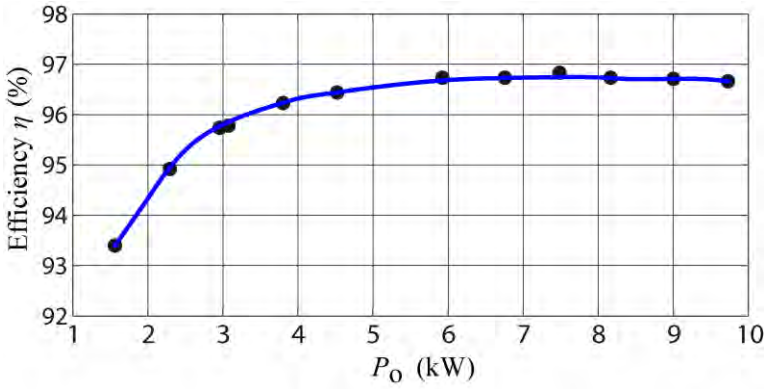


▶ Demonstrator Performance (VR250)

- **Input Current Quality @ f_N = 800 Hz**

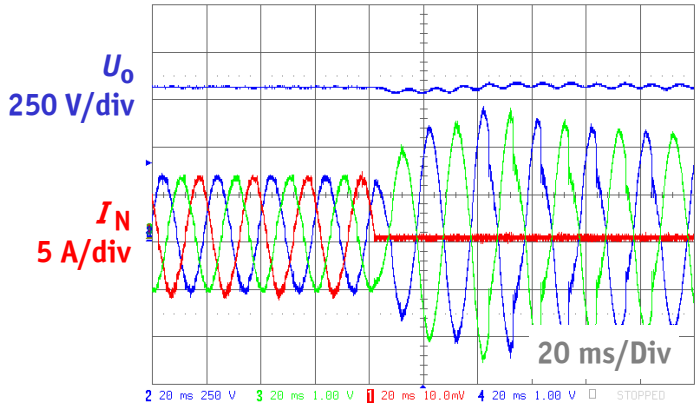


- **Efficiency @ f_N = 800 Hz**

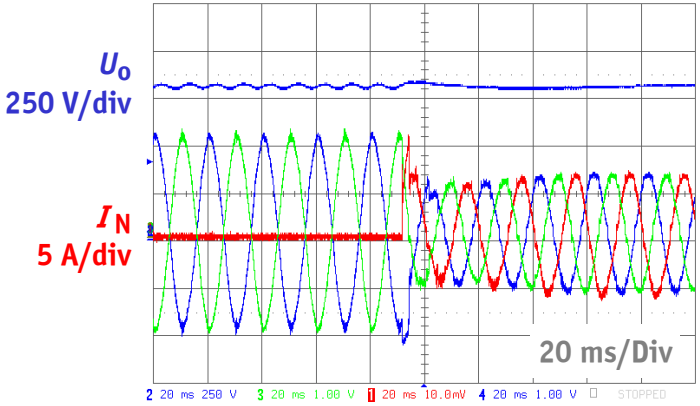


▶ Demonstrator (VR250) Control Behavior

- **Mains Phase Loss**

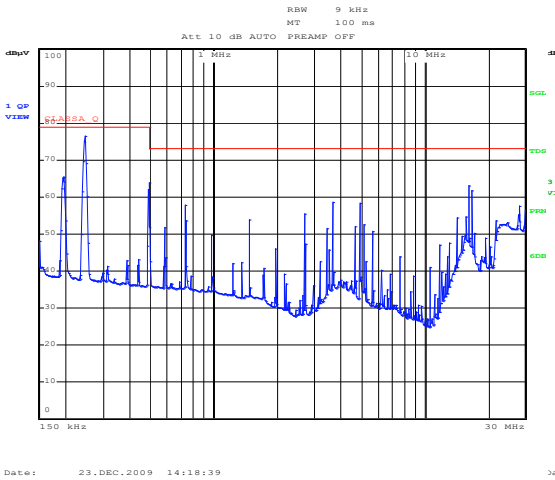


- **Mains Phase Return**

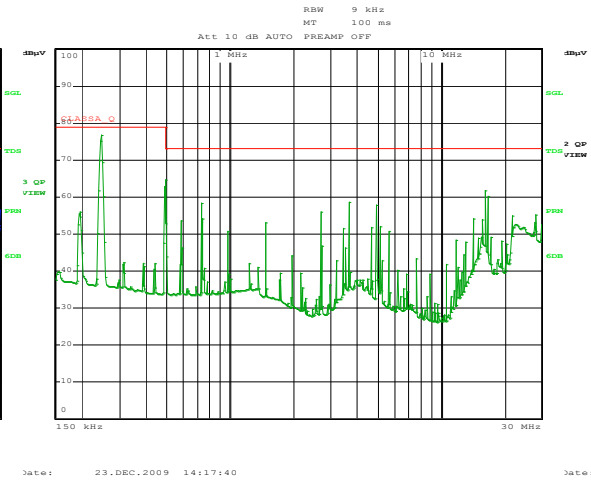


▶ Demonstrator (VR250) EMI Analysis

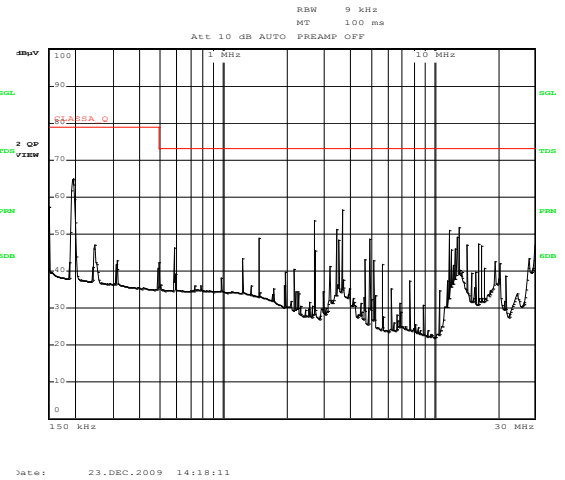
- **Total Emissions**



- **DM Emissions**

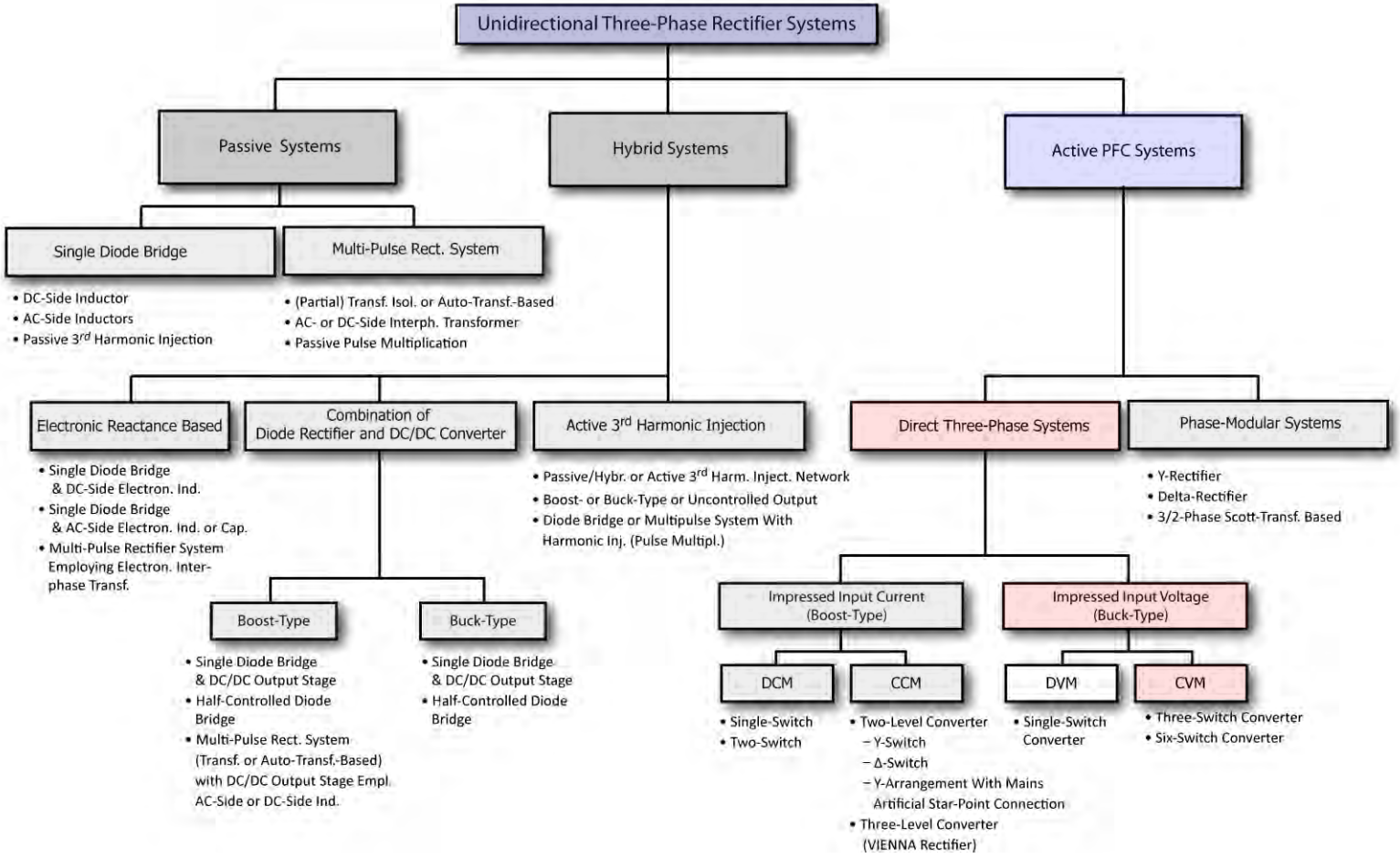


- **CM Emissions**



Coffee Break !

▶ Classification of Unidirectional Rectifier Systems

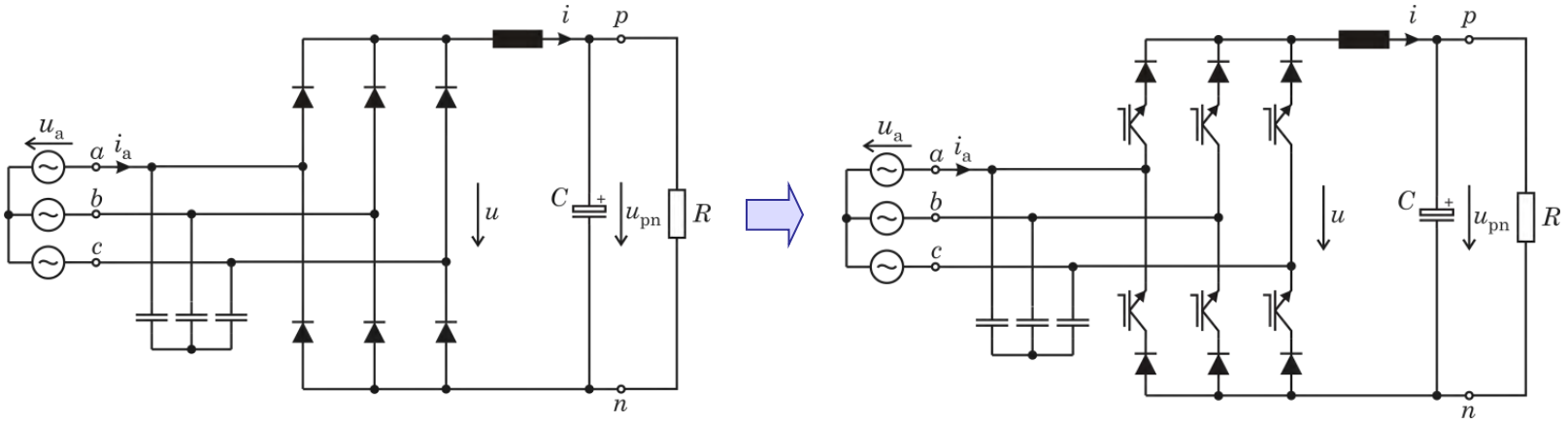


Buck-Type CVM PFC Rectifier System

- *Derivation of Circuit Topologies*

▶ Derivation of the Circuit Topology (1)

■ Insertion of Switches in Series to the Diodes



+ DC Current Distribution to Phases *a*, *b*, *c* can be Controlled
+ Control of Output Voltage $0 \le u \le \frac{3}{2}\hat{U}$

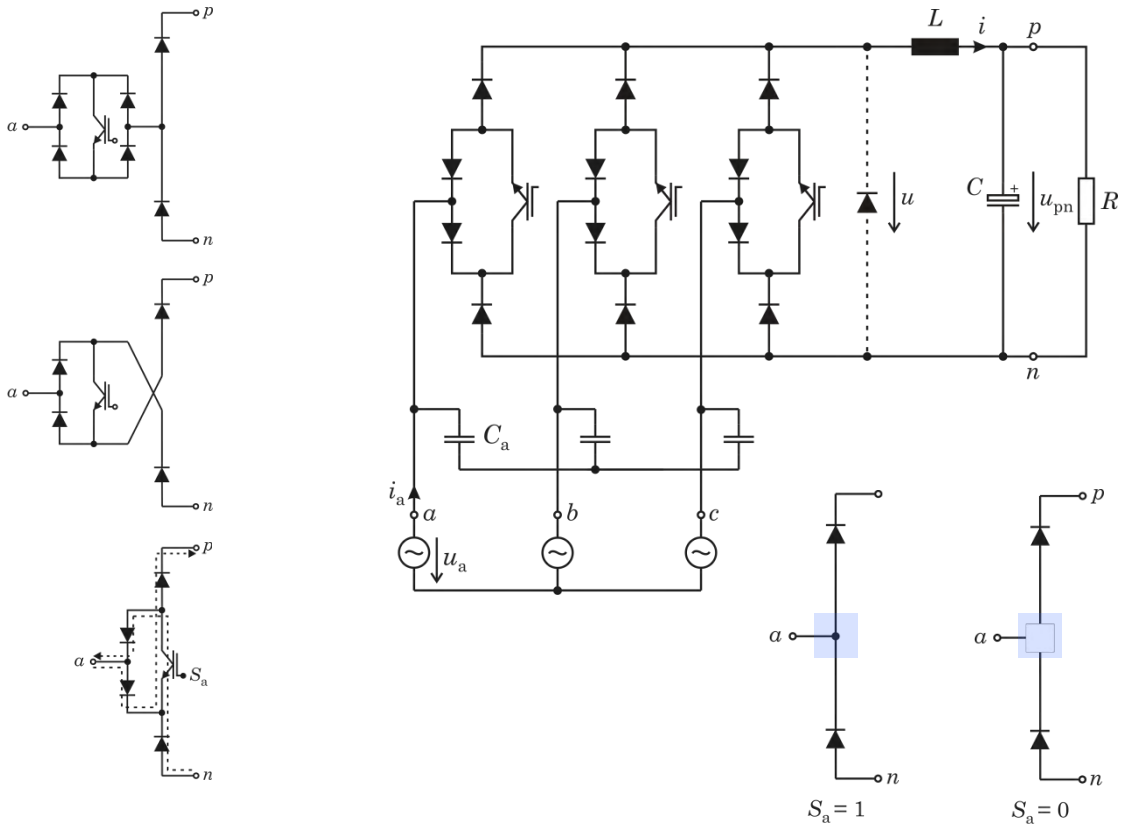
– Pulsating Input Currents / EMI Filtering Requ.
– Relatively High Conduction Losses

Derivation of the Circuit Topology (2)

(1)

(2)

(3)

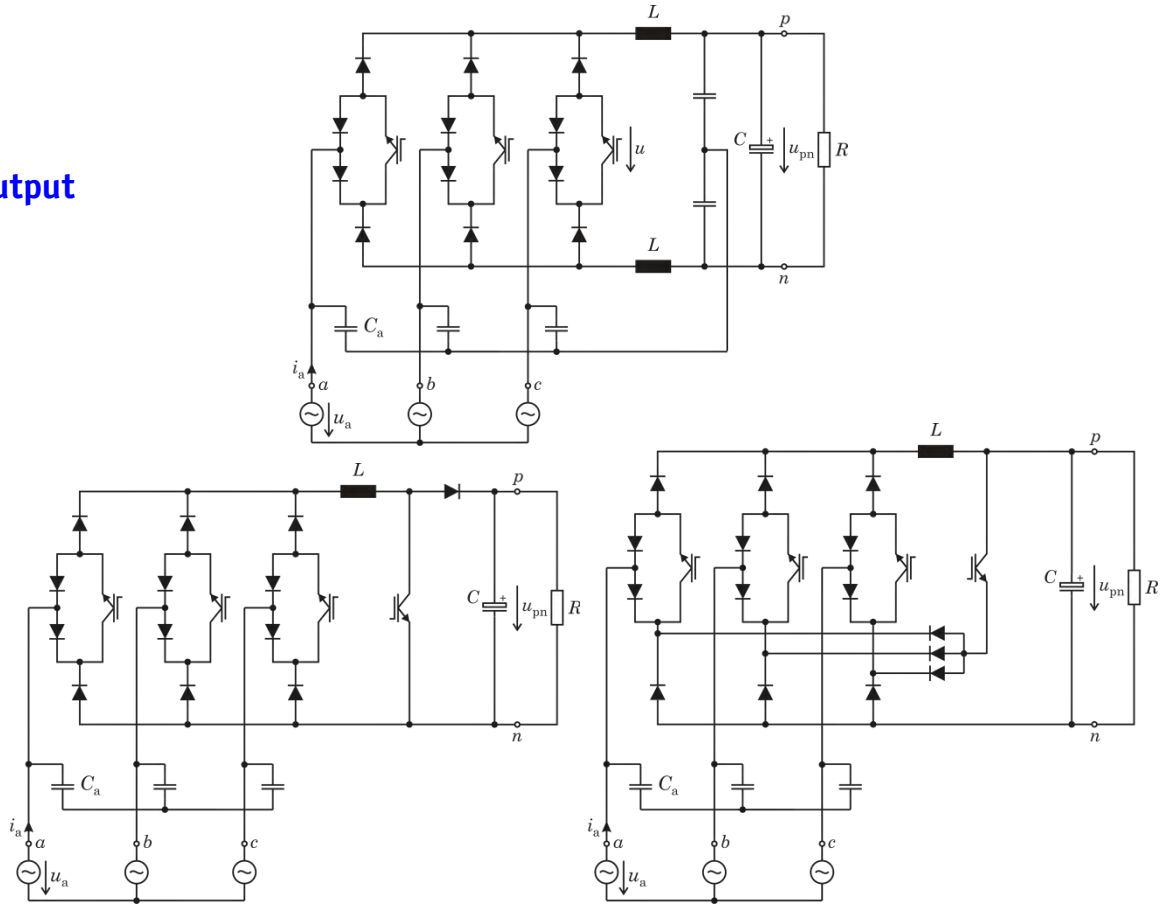


- **Insertion of 4Q-Switches on the AC-Side in Order to Enable Control of the DC Current Distribution to Phases *a*, *b*, *c***

Derivation of the Circuit Topology (3)

Circuit Extensions

- Internal Filtering of CM Output Voltage Component
- Integration of Boost-Type Output Stage
- Wide Output Voltage Range, i.e. also $U > \frac{3}{2}\hat{U}$
- Sinusoidal Mains Current also in Case of Phase Loss



- Circuit Extensions Shown for 3-Switch Topology, but is also Applicable to 6-Switch Topology

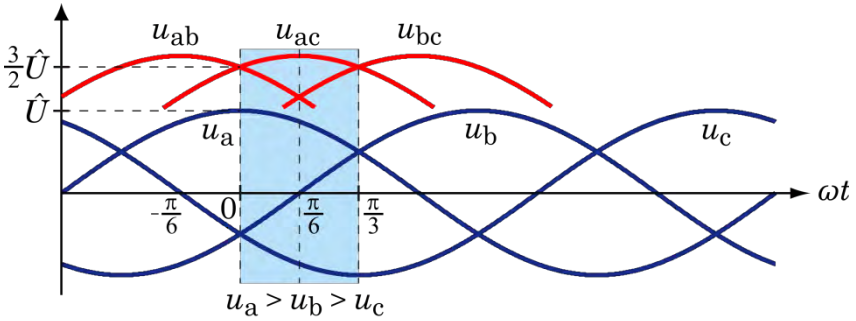
Buck-Type PFC Rectifier Analysis

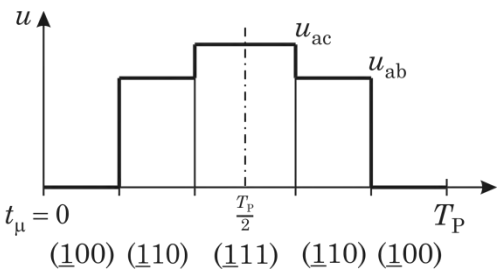
- *Modulation*
- *Input Current Formation*
- *Output Voltage Formation*
- *Experimental Analysis*

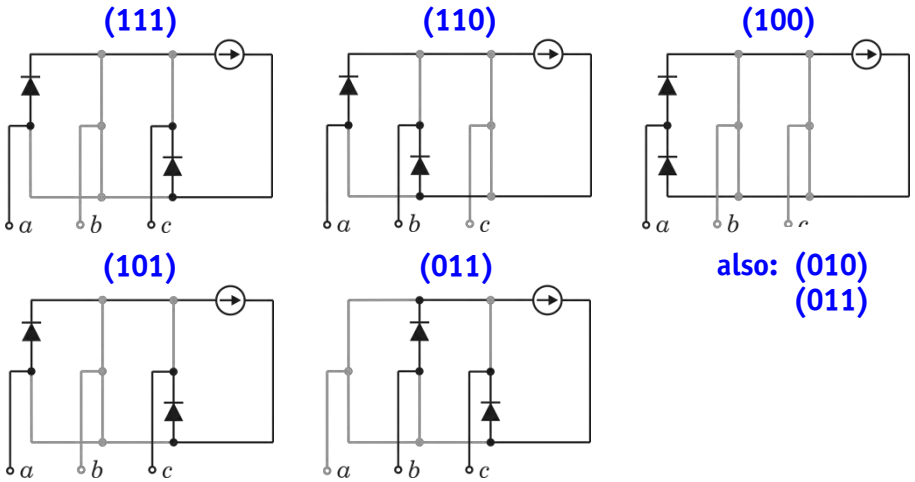
Modulation Scheme

- Consider 60°-Wide Segment of the Mains Period; Suitable Switching States Denominated by (s_a, s_b, s_c)

- Clamping to Phase with Highest Absolute Voltage Value, i.e.
  - Phase *a* for $\omega t \in \left(-\frac{\pi}{6}, +\frac{\pi}{6}\right)$,
  - Phase *c* for $\omega t \in \left(+\frac{\pi}{6}, +\frac{\pi}{2}\right)$ etc.
  - Assumption: $\omega t \in \left(0, +\frac{\pi}{6}\right)$





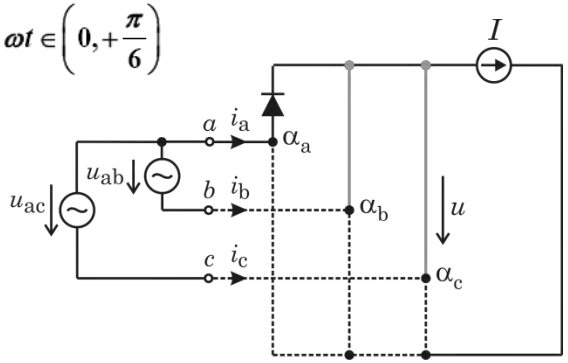


also: (010)
(011)

- Clamping and "Staircase-Shaped" Link Voltage in Order to Minimize the Switching Losses

▶ Input Current and Output Voltage Formation (1)

- **Assumption:** $\omega t \in \left(0, +\frac{\pi}{6}\right)$



- **Ohmic Mains Behavior:**

$$i_a = G^* u_a = (\alpha_b + \alpha_c) \cdot I$$

$$i_b = G^* u_b = -\alpha_b \cdot I$$

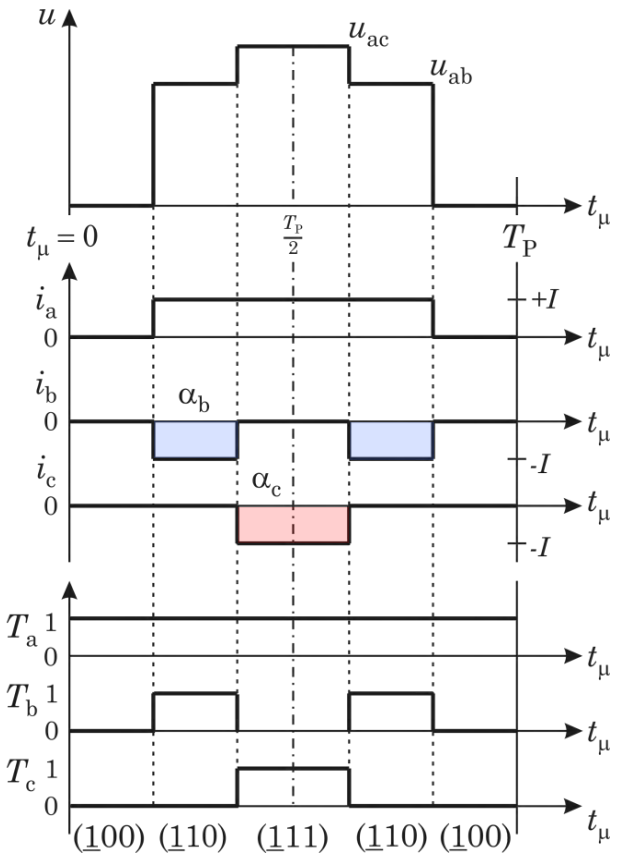
$$i_c = G^* u_c = -\alpha_c \cdot I$$

- **Example:**

$$\alpha_b + \alpha_c = \frac{G^* u_a}{I} = \frac{G^* \hat{U}}{I} \cdot \cos(\omega t) = M \cdot \cos(\omega t)$$

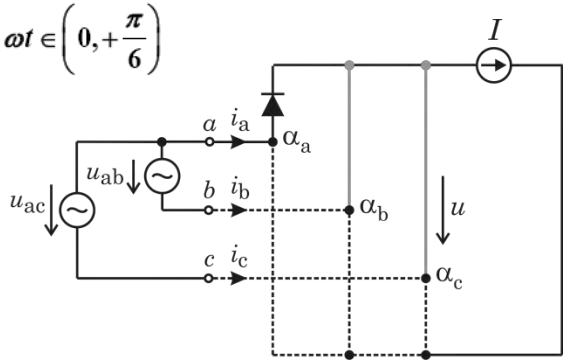
$$\alpha_b = -\frac{G^* u_b}{I} = M \cdot \cos\left(\omega t - \frac{2\pi}{3}\right)$$

$$M \in (0 \ldots 1), I \geq \hat{I}^* \qquad \alpha_c = -\frac{G^* u_c}{I} = M \cdot \cos\left(\omega t + \frac{2\pi}{3}\right)$$



▶ Input Current and Output Voltage Formation (2)

- **Assumption:** $\omega t \in \left(0, +\frac{\pi}{6}\right)$



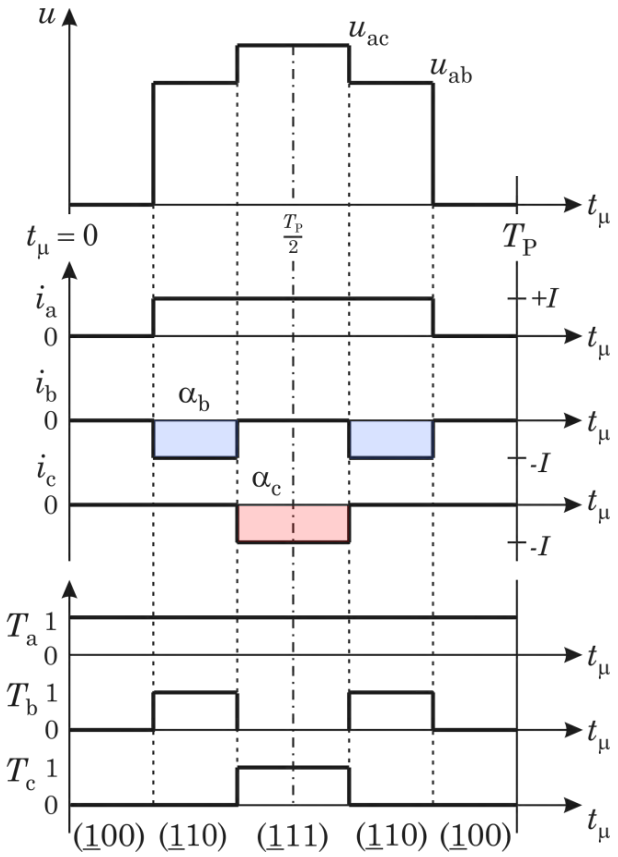
- **Output Voltage Formation:**

$$\overline{u} = u_{ab} \cdot \alpha_b + u_{ac} \cdot \alpha_c$$

$$P_{\text{link}} = P_{\text{input}}$$

$$\overline{u} \cdot I = \frac{3}{2} \cdot \hat{U} \cdot \hat{I}^*$$

$$\overline{u} = \frac{3}{2} \cdot \hat{U} \cdot \frac{\hat{I}^*}{I} = \frac{3}{2} \cdot \hat{U} \cdot M$$



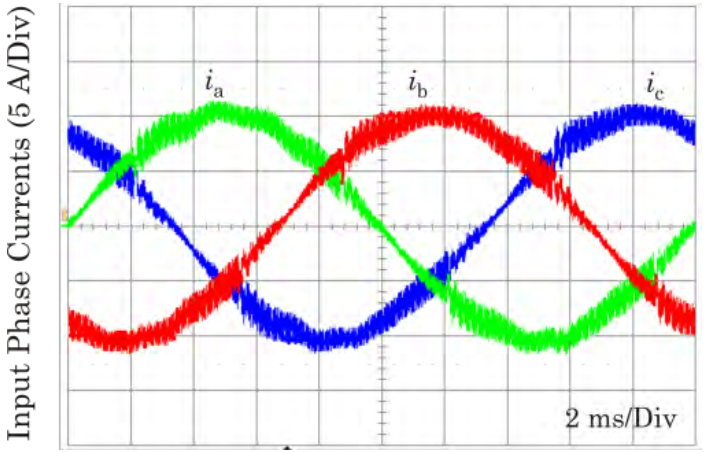
- **Output Voltage is Formed by Segments of the Input Line-to-Line Voltages**
- **Output Voltage Shows Const. Local Average Value**

▶ Experimental Results

■ Ultra-Efficient Demonstrator System

U_{LL} = 3 x 400 V (50 Hz)
P_o = 5 kW
U_o = 400 V
f_s = 18 kHz
L = 2 x 0.65 mH

η = 98.8% (Calorimetric Measurement)

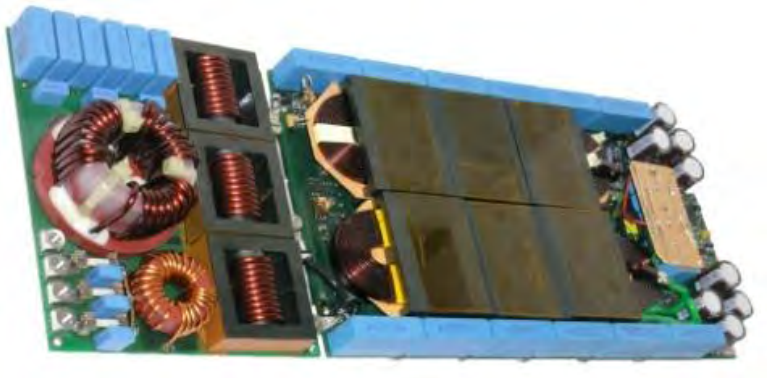


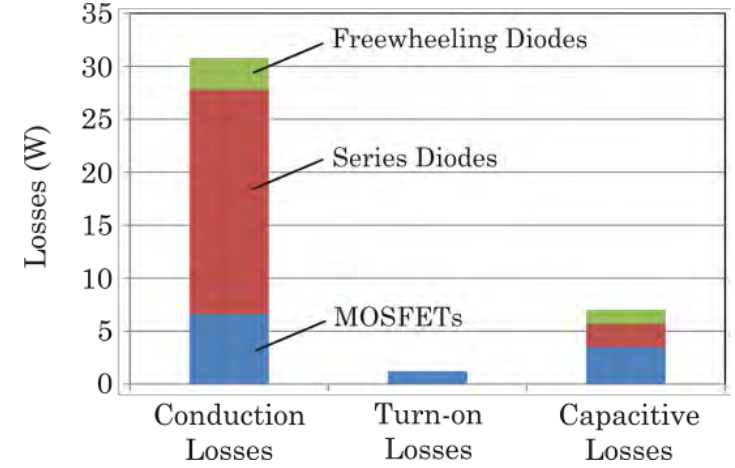
Experimental Results

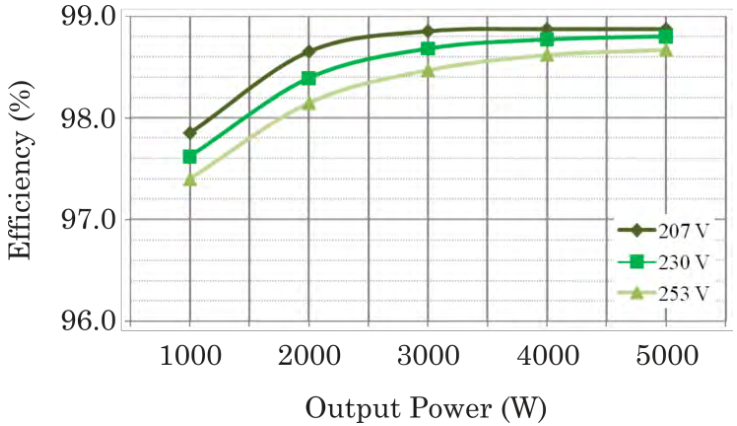
Ultra-Efficient Demonstrator System

U_{LL} = 3 x 400 V (50 Hz)
P_o = 5 kW
U_o = 400 V
f_s = 18 kHz
L = 2 x 0.65 mH

η = 98.8% (Calorimetric Measurement)







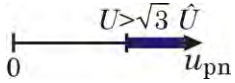
Summary of Unidirectional PFC Rectifier Systems

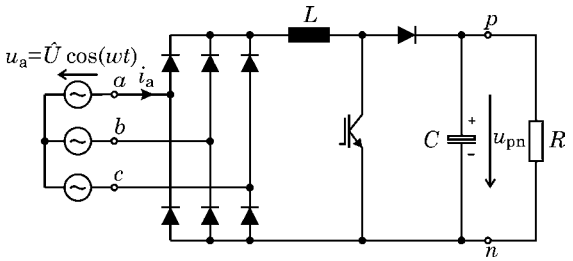
- *Block Shaped Input Current Systems*
- *Sinusoidal Input Current Systems*

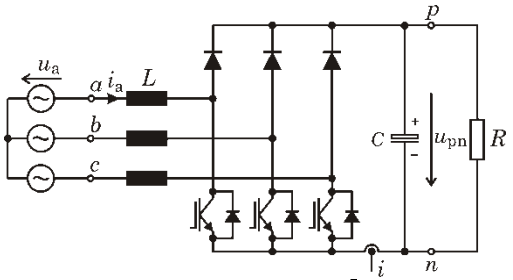
▶ Block Shaped Input Current Rectifier Systems

+ Controlled Output Voltage
+ Low Complexity
+ High Semicond. Utilization
+ Total Power Factor $\lambda \approx 0.95$
− $THD_I \approx 30\%$

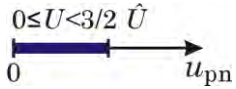
Boost-Type

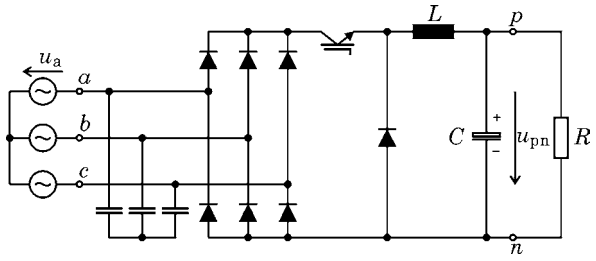


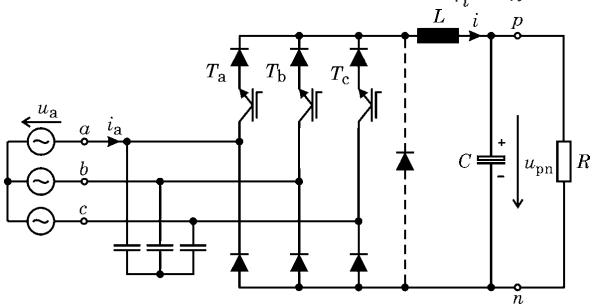




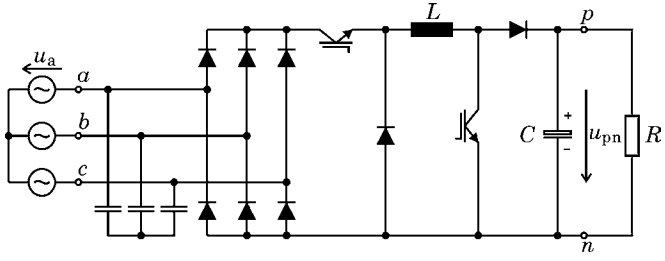
Buck-Type

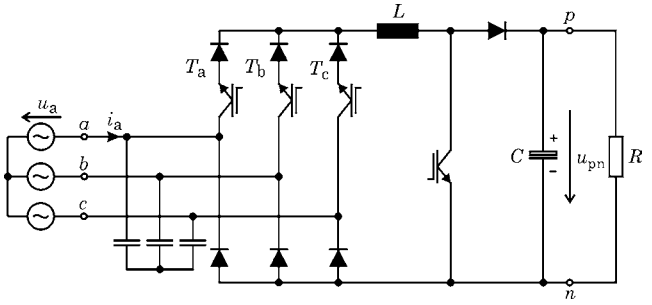






Buck+Boost-Type

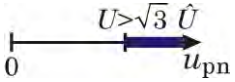


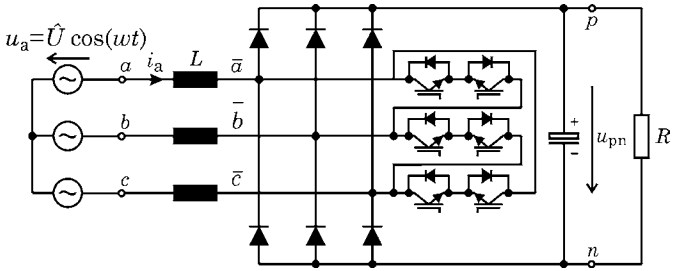


▶ Sinusoidal Input Current Rectifier Systems (1)

+ Controlled Output Voltage
+ Relatively Low Control Complexity
+ Tolerates Mains Phase Loss
- 2-Level Characteristic
- Power Semiconductors Stressed with Full Output Voltage

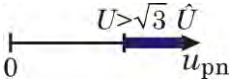
Boost-Type

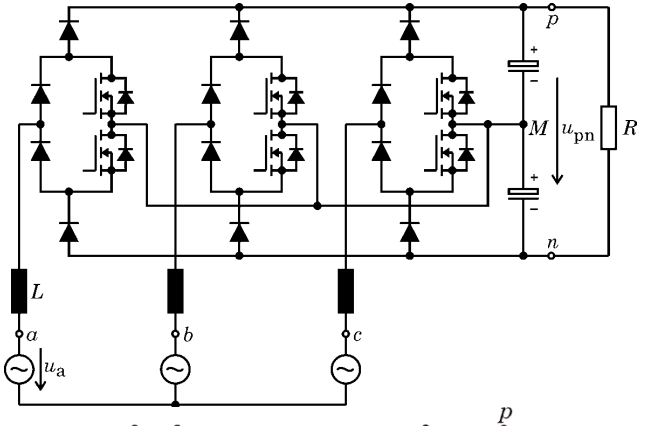




+ Controlled Output Voltage
+ 3-Level Characteristic
+ Tolerates Mains Phase Loss
+ Power Semicond. Stressed with Half Output Voltage
- Higher Control Complexity

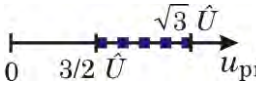
Boost-Type

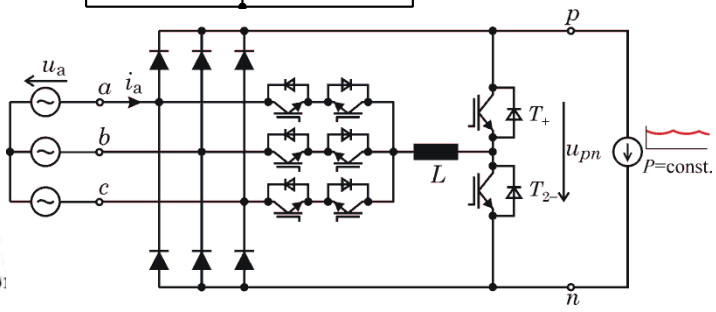




+ Low Current Stress on Power Semicond.
+ In Principal No DC-Link Cap. Required
+ Control Shows Low Complexity
- Sinusoidal Mains Current Only for Const. Power Load
- Power Semicond. Stressed with Full Output Voltage
- Does Not Tolerate Loss of a Mains Phase

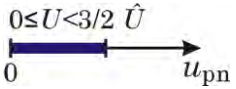
Unregulated Output

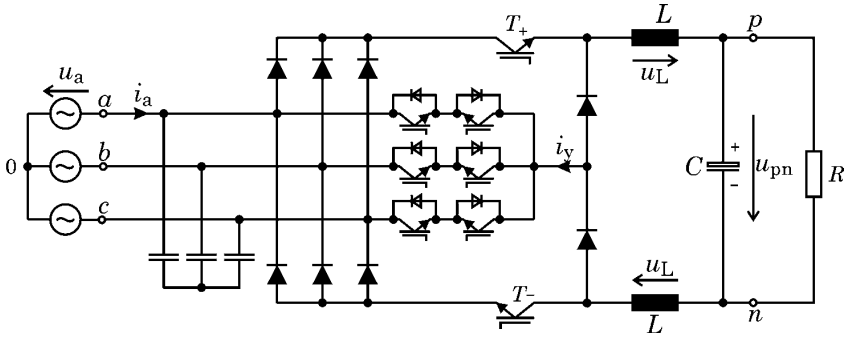




▶ Sinusoidal Input Current Rectifier Systems (2)

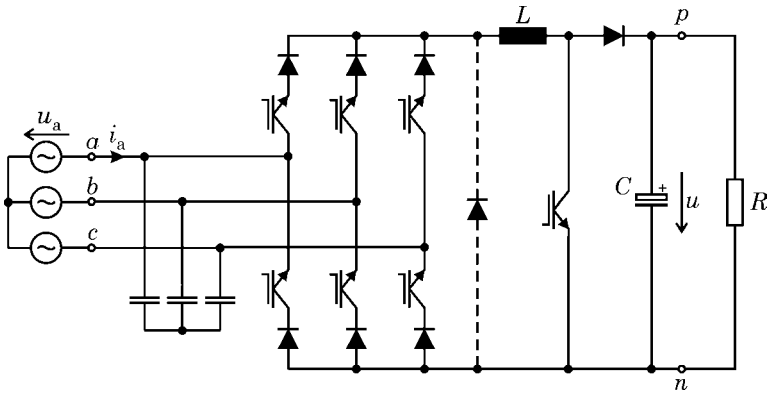
Buck-Type





+ Allows to Generate Low Output Voltages
+ Short Circuit Current Limiting Capability
– Power Semicond. Stressed with LL-Voltages
– AC-Side Filter Capacitors / Fundamental Reactive Power Consumption

Buck+Boost-Type



+ See Buck-Type Converter
+ Wide Output Voltage Range
+ Tolerates Mains Phase Loss, i.e. Sinusoidal Mains Current also for 2-Phase Operation
– See Buck-Type Converter (6-Switch Version of Buck Stage Enables Compensation of AC-Side Filter Cap. Reactive Power)

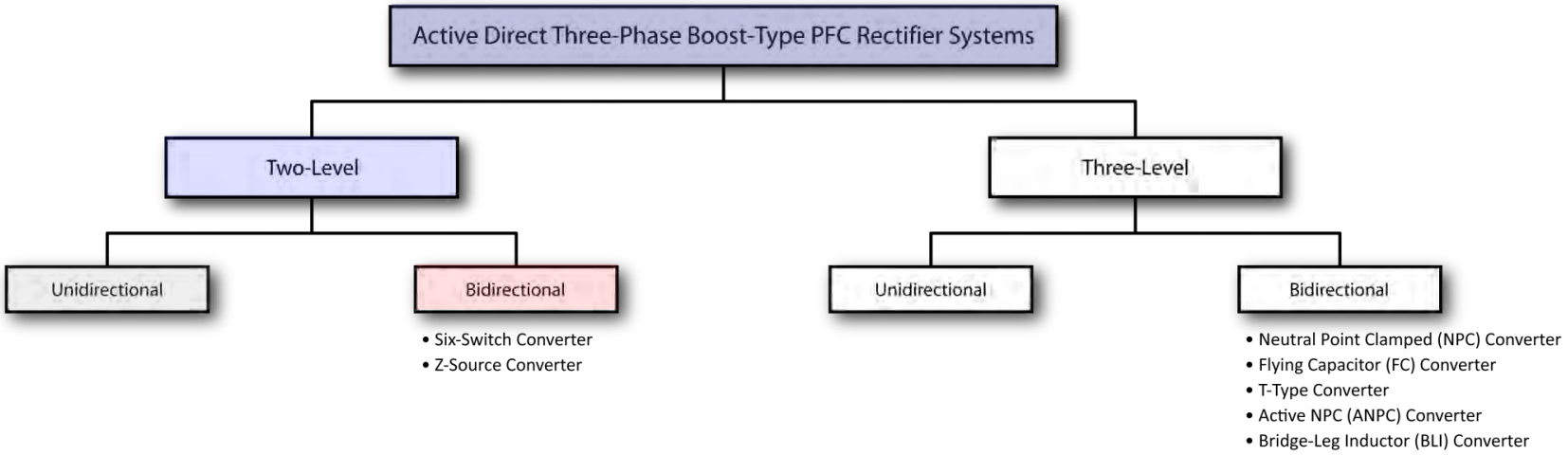
Coffee Break !

Bidirectional PFC Rectifier Systems

- *Boost-Type Topologies*
- *Buck-Type Topologies*

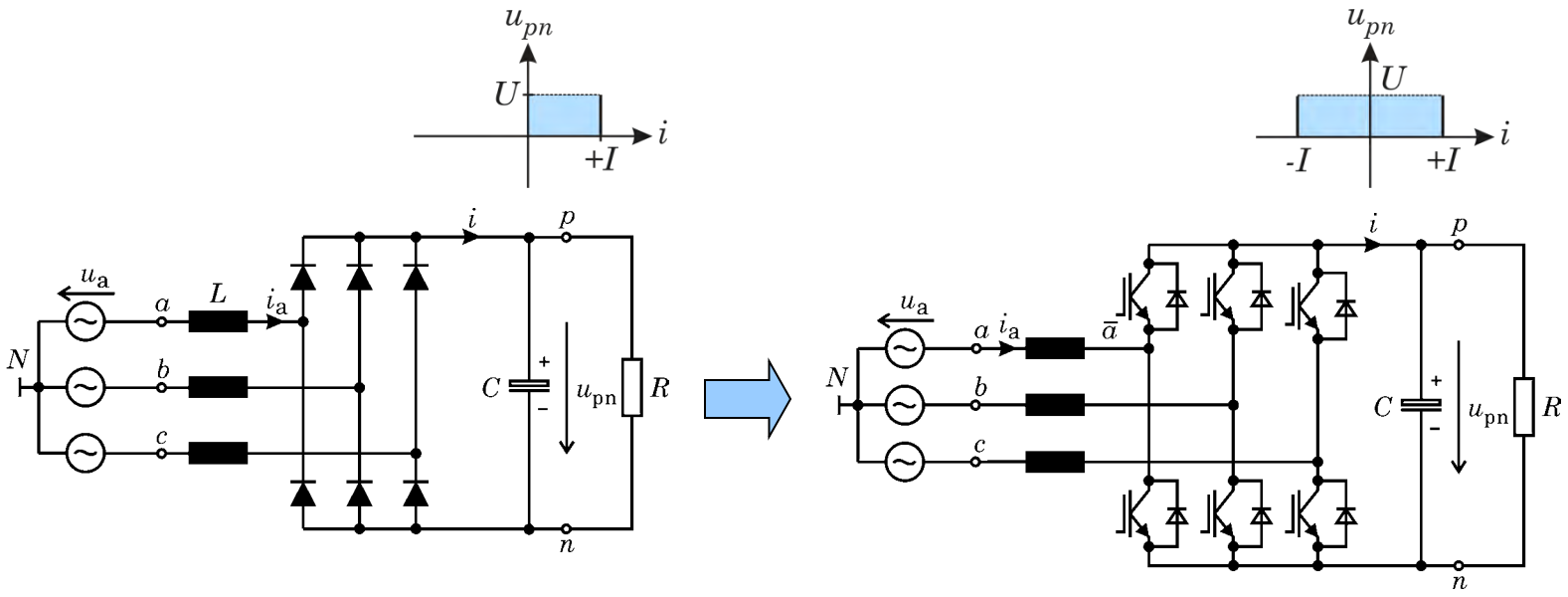
Boost-Type Topologies

▶ Classification of Bidirectional Boost-Type Rectifier Systems

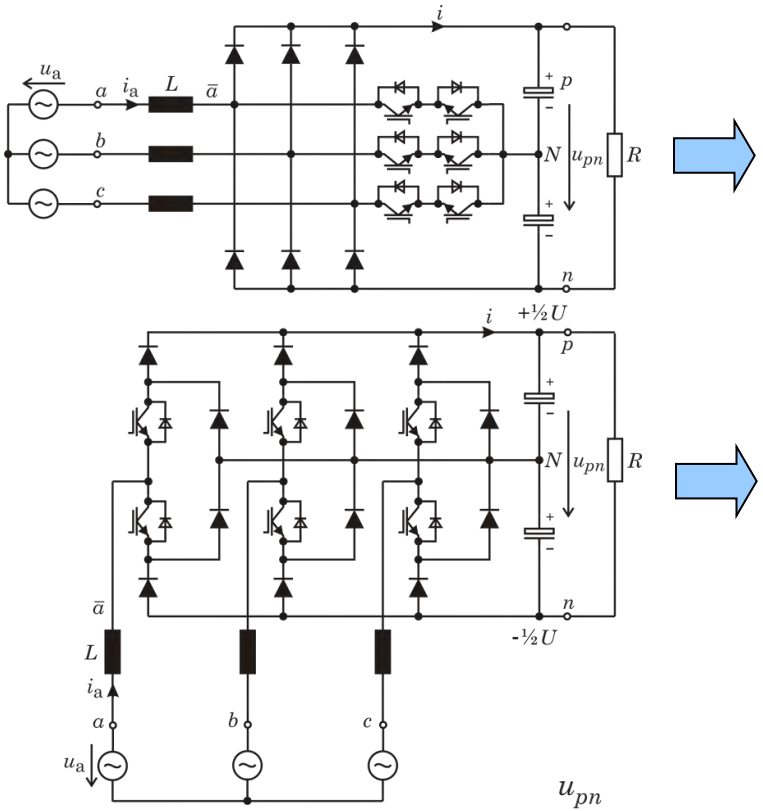


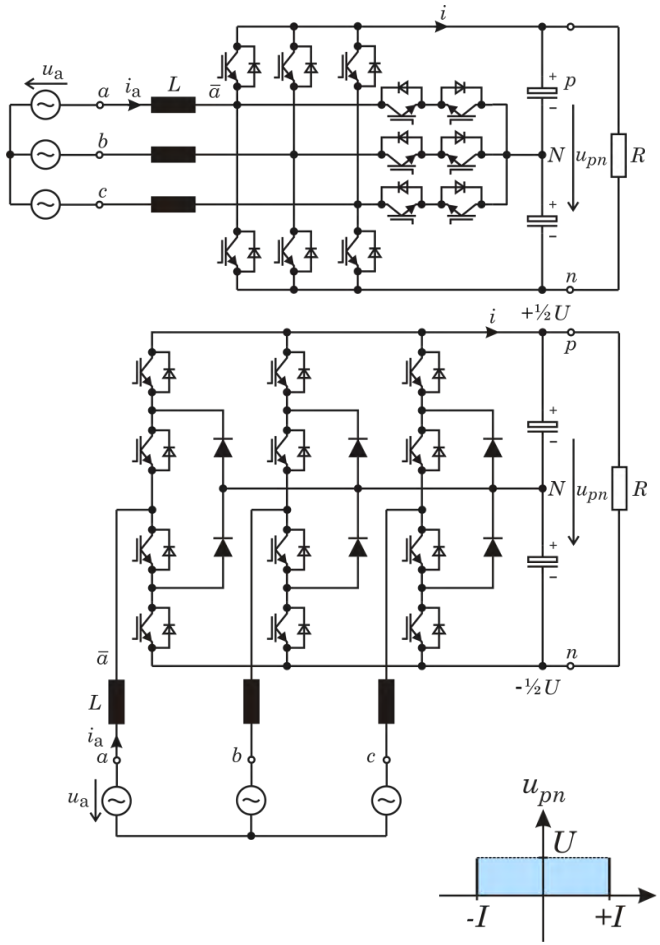
Derivation of Two-Level Boost-Type Topologies

- **Output Operating Range**

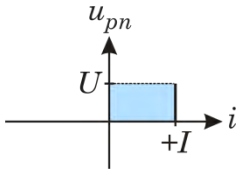


Derivation of Three-Level Boost-Type Topologies

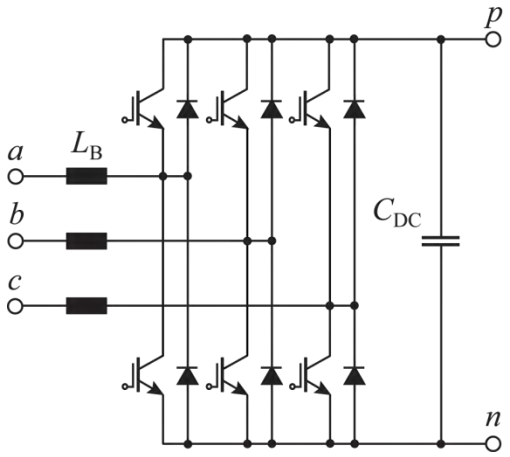


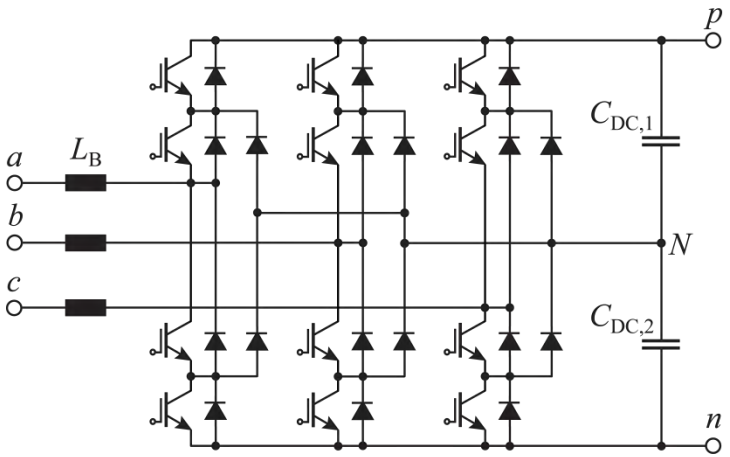


- **Output Operating Range**



▶ Comparison of Two-Level/Three-Level NPC Boost-Type Rectifier Systems





- Two-Level Converter Systems

+ State-of-the-Art Topology for LV Appl.
+ Simple, Robust, and Well-Known
+ Power Modules and Auxiliary Components Available from Several Manufacturers

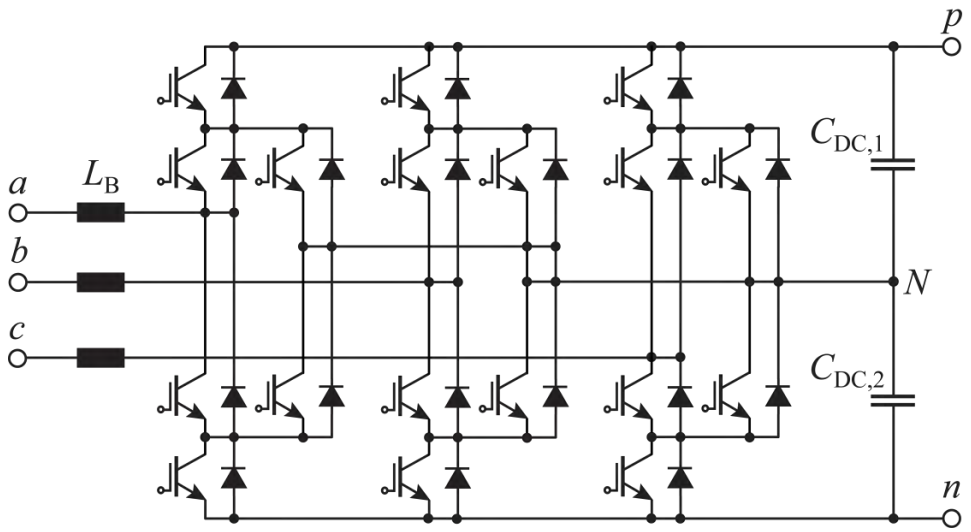
- Limited Maximum Switching Frequency
- Large Volume of Input Inductors

- Two-Level → Three-Level Converter Systems

+ Reduction of Device Blocking Voltage Stress
+ Lower Switching Losses
+ Reduction of Passive Component Volume

– Higher Conduction Losses
– Increased Complexity and Implementation Effort

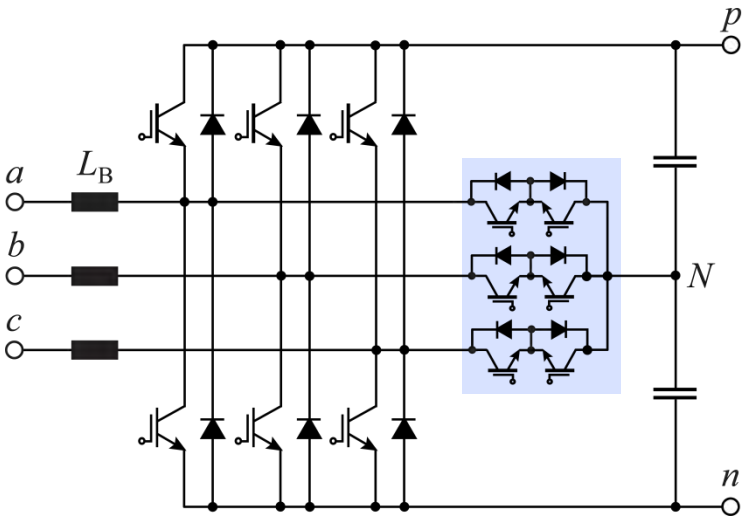
▶ Active Neutral Point Clamped (ANPC) Three-Level Boost-Type System



+ Active Distribution of the Switching Losses Possible
+ Better Utilization of the Installed Switching Power Devices

– Higher Implementation Effort Compared to NPC Topology

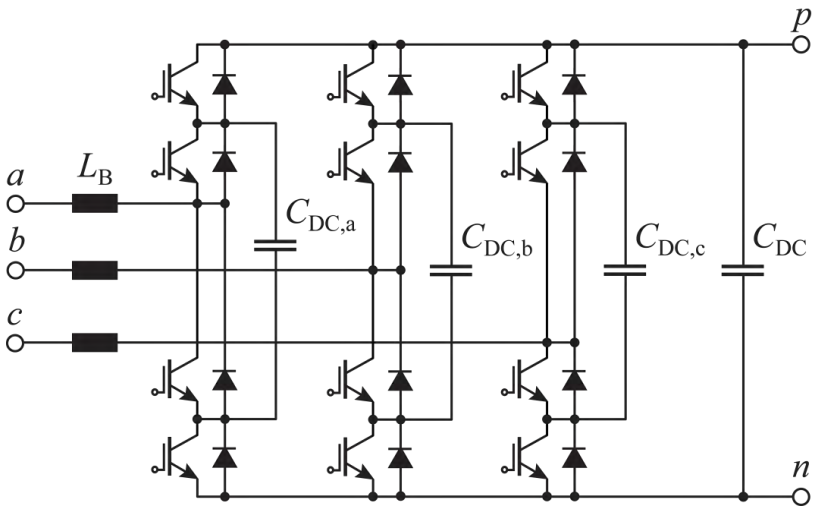
T-Type Three-Level Boost-Type Rectifier System



+ Semiconductor Losses for Low Switching Frequencies Lower than for NPC Topologies
+ Can be Implemented with Standard Six-Pack Module

– Requires Switches for 2 Different Blocking Voltage Levels

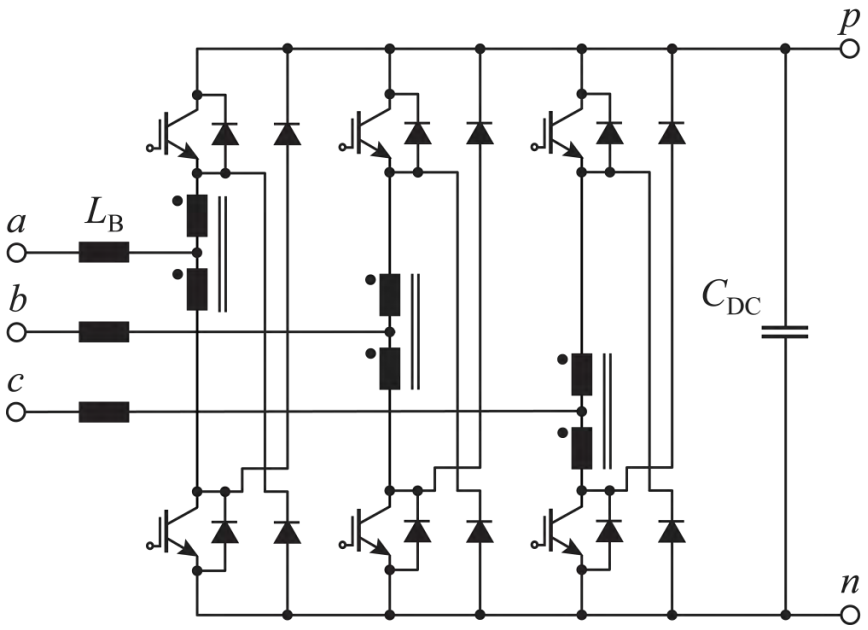
▶ Three-Level Flying Capacitor (FC) Boost-Type Rectifier System



+ Lower Number of Components (per Voltage Level)
+ For Three-Level Topology only Two Output Terminals

– Volume of Flying Capacitors
– No Standard Industrial Topology

▶ Three-Level Bridge-Leg Inductor (BLI) Boost-Type Rectifier System



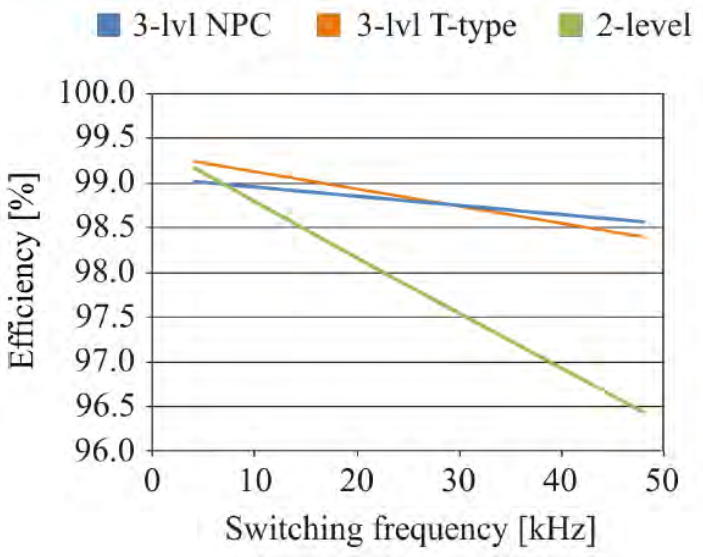
+ Lower Number of Components (per Voltage Level)
+ For Three-Level Topology only Two Output Terminals

– Additional Volume due to Coupled Inductors
– Semiconductor Blocking Voltage Equal to DC Link Voltage

▶ Pros and Cons of Three-Level vs. Two-Level Boost-Type Rectifier Systems

+ Losses are Distributed over Many Semicond. Devices; More Even Loading of the Chips → Potential for Chip Area Optimization for Pure Rectifier Operation
+ High Efficiency at High Switching Frequency
+ Lower Volume of Passive Components

− More Semiconductors
− More Gate Drive Units
− Increased Complexity
− Capacitor Voltage Balancing Required
− Increased Cost



Consideration for 10kVA/400V_{AC} Rectifier Operation; Min. Chip Area, $T_{j,max}$= 125°C

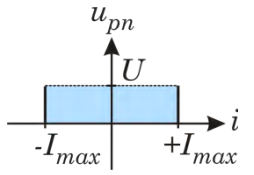
● Moderate Increase of the Component Count with the T-Type Topology

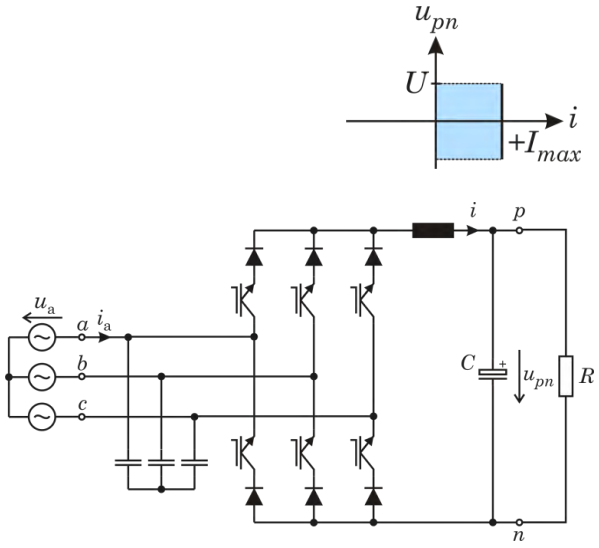
▶ Multi-Level Topologies are Commonly Used for Medium Voltage Applications but Gain Steadily in Importance also for Low-Voltage Renewable Energy Applications

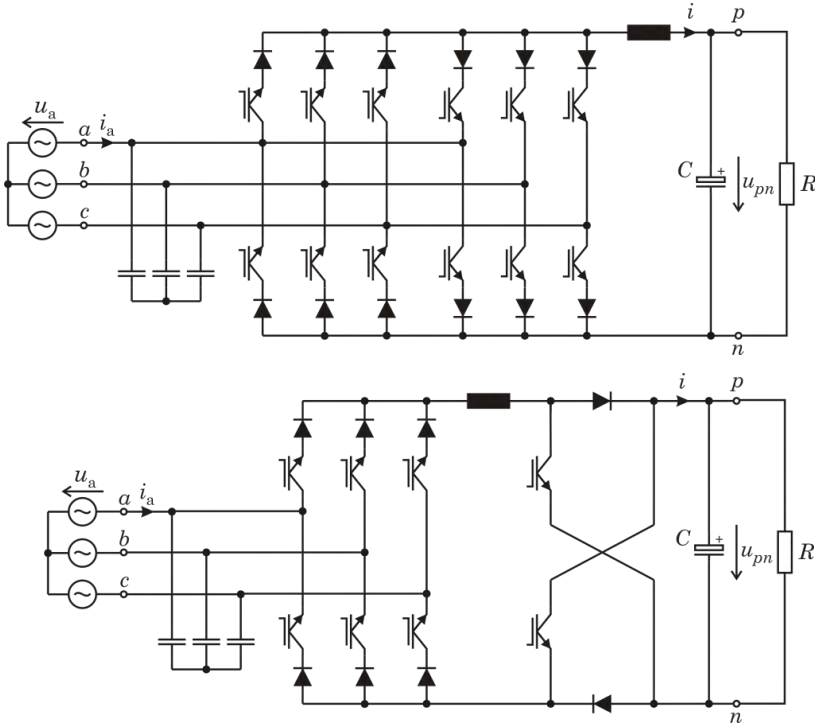
Buck-Type Topologies

Derivation of Unipolar Output Bidirectional Buck-Type Topologies

- **Output Operating Range**

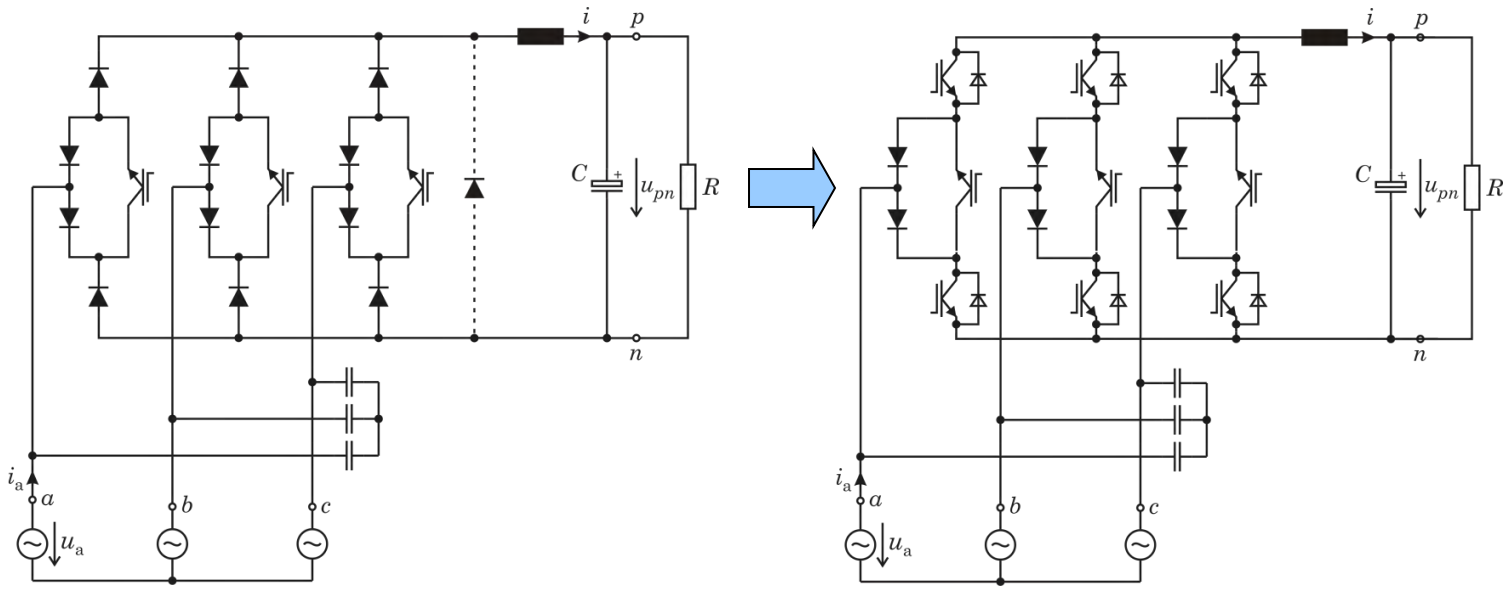




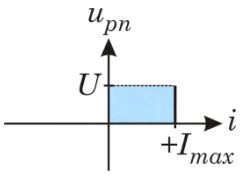


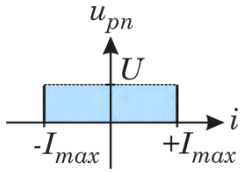
- System also Features Boost-Type Operation

▶ Derivation of Unipolar Output Bidirectional Buck-Type Topologies

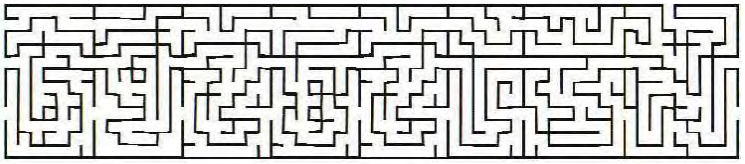


- **Output Operating Range**





End of Part 1



Passive Rectifier Systems

[1.1] **P. Pejovic ,** *"A Novel Low-Harmonic Three-Phase Rectifier,"* IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol.49, no.7, pp.955-965, Jul 2002.

[1.2] **P. Pejovic, P. Bozovic, D. Shmilovitz,** *"Low-Harmonic, Three-Phase Rectifier That Applies Current Injection and a Passive Resistance Emulator,"* IEEE Power Electronics Letters , vol.3, no.3, pp. 96- 100, Sept. 2005.

[1.3] **P. Pejovic, Z. Janda,** *"Optimal Current Programming in Three-Phase High-Power-Factor Rectifier Based on Two Boost Converters,"* IEEE Transactions on Power Electronics, vol.13, no.6, pp.1152-1163, Nov 1998.

[1.4] **S. Kim, P. Enjeti, P. Packebush, and I. Pitel,** *"A New Approach to Improve Power Factor and Reduce Harmonics in a Three Phase Diode Rectifier Type Utility Interface,"* Record of the IEEE Industry Applications Society Annual Meeting, Pt. II, pp. 993-1000, 1993.

[1.5] **P. Pejovic Z. Janda,** *"Low Harmonic Three-Phase Rectifiers Applying Current Injection,"* Proc. of the Internat. Conf. on Power Electronics and Motion Control, Prague, 1998.

[1.6] **P. Pejovic and Z. Janda,** *"A Novel Harmonic-Free Three-Phase Diode Bridge Rectifier Applying Current Injection,"* Proc. of the 14th IEEE Appl. Power Electron. Conf. APEC´99, Dallas, USA, March 14-18, Vol. 1, pp. 241-247, 1999.

[1.7] **P. Pejovic, and Z. Janda,** *"An Improved Current Injection Network for Three-Phase High-Power-Factor Rectifiers that Apply Third Harmonic Current Injection,"* Letter to the Editor, IEEE Transactions on Industrial Electronics, Vol. 47, No. 2, pp. 497-499, 2000.

[1.8] **T. Sakkos and V. Sarv,** *"New Unity Power Factor Diode Rectifiers Using Ripple-Power Re-Rectification,"* in. Proc. of the 8th Internat. Conf. on Power Electron. and Variable Speed Drives, London, Sept. 18-19, pp. 378-381, 2000.

[1.9] **T. Sakkos, V. Sarv, and J. Soojärv,** *"Optimun Diode-Switched Active Filters for Power Factor Correction of Single- and Three-Phase Diode Recifiers with Capacitive Smoothing,"* in Proc. of the 7th European Conf. on Power Electron. and Appl., Trondheim, Norway, Vol. 2, pp. 870-875, 1997.

Hybrid Rectifier Systems (Electronic Reactance Based)

[2.1] **H. Ertl, J.W. Kolar, and F.C. Zach,** *"A Constant Output Current Three-Phase Diode Bridge Employing a Novel Electronic Smoothing Inductor,"* Proc. of the 40th Internat. Conf. on Power Conversion, Nuremberg, June 22-24, pp. 645–651 (1999).

[2.2] **K. Mino, M.L. Heldwein, and J.W. Kolar,** *"Ultra Compact Three-Phase Rectifier With Electronic Smoothing Inductor,"* Proc. of the 20th Annual IEEE Appl. Power Electron. Conf. and Exp. (APEC 2005), Vol.1, pp. 522-528 (2005).

[2.3] **R. Shimada, J.A. Wiik, T. Isobe, T. Takaku, N. Iwamuro, Y. Uchida, M. Molinas, T.M. Undeland,** *"A New AC Current Switch Called MERS with Low On-State Voltage IGBTs (1.54 V) for Renewable Energy and Power Saving Applications,"* Proc. of the 20th Internat. Symp. on Power Semicond. Devices and IC's, (ISPSD '08), pp.4-11, (2008).

[2.4] **T. Takaku, G. Homma, T. Isober, S. Igarashi, Y. Uchida, R. Shimada**, "Improved Wind Power Conversion System Using Magnetic Energy Recovery Switch (MERS)," Proc. of the Industry Appl. Conf. 2005. 40th IAS Annual Meeting, Vol.3, pp. 2007- 2012 (2005).

[2.5] **J.A. Wiik, F.D. Widjaya, T. Isobe, T. Kitahara, R. Shimada,** *"Series Connected Power Flow Control using Magnetic Energy Recovery Switch (MERS),"* Proc. of the Power Conv. Conf. - Nagoya, 2007 (PCC '07), pp.983-990 (2007).

[2.6] **J.A. Wiik, F.D. Wijaya, R. Shimada,** *"Characteristics of the Magnetic Energy Recovery Switch (MERS) as a Series FACTS Controller,"* IEEE Transactions on Power Delivery, vol.24, no.2, pp.828-836, (2009).

Hybrid Rectifier Systems (Active 3rd Harmonic Injection) (1)

[2.7] **H. Ertl, J.W. Kolar, and F.C. Zach,** *"A Constant Output Current Three-Phase Diode Bridge Employing a Novel Electronic Smoothing Inductor,"* Proc. of the 40th Internat. Conf. on Power Conversion, Nuremberg, June 22-24, pp. 645–651 (1999).

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Coffee Break !

Part 2

Three-Phase AC-AC PWM Converter Systems

Outline

Basics of AC/DC/AC Converter Systems

- Voltage DC-Link (V-BBC)
- Current DC-Link (I-BBC)

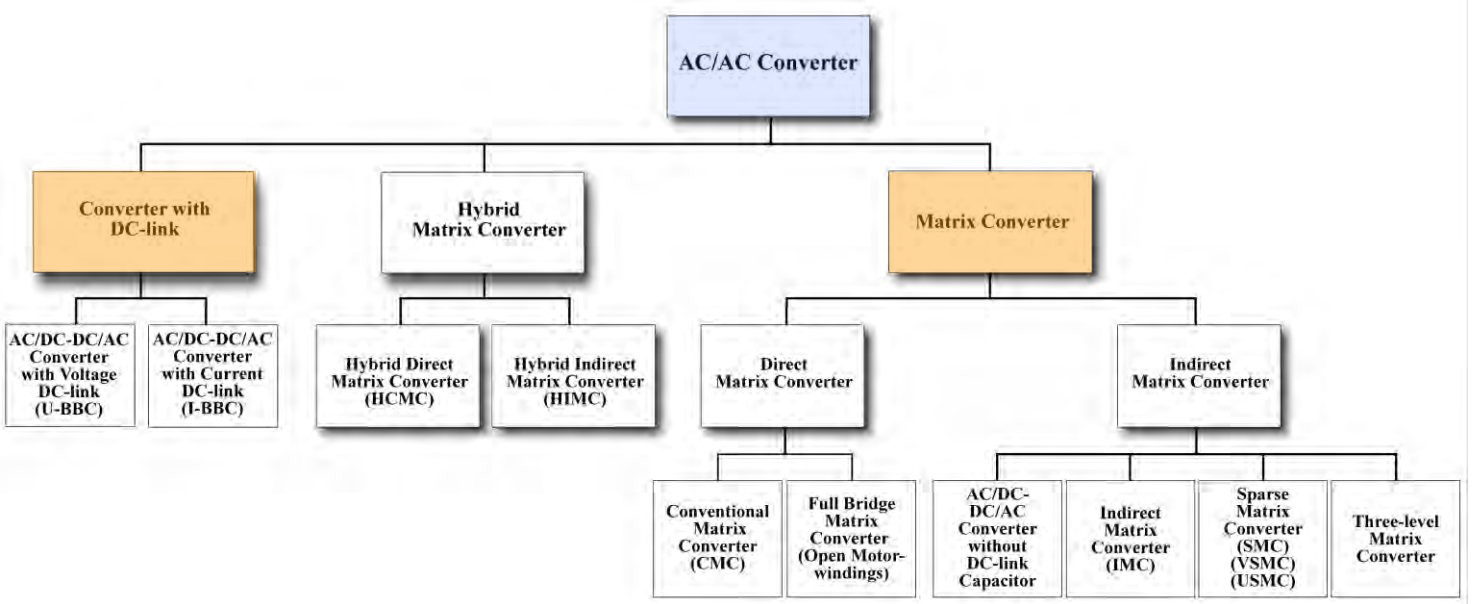
Derivation/Analysis of AC/AC MC Topologies

- Indirect Matrix Converter (IMC)
- Conv. Matrix Converter (CMC)

Comparative Evaluation

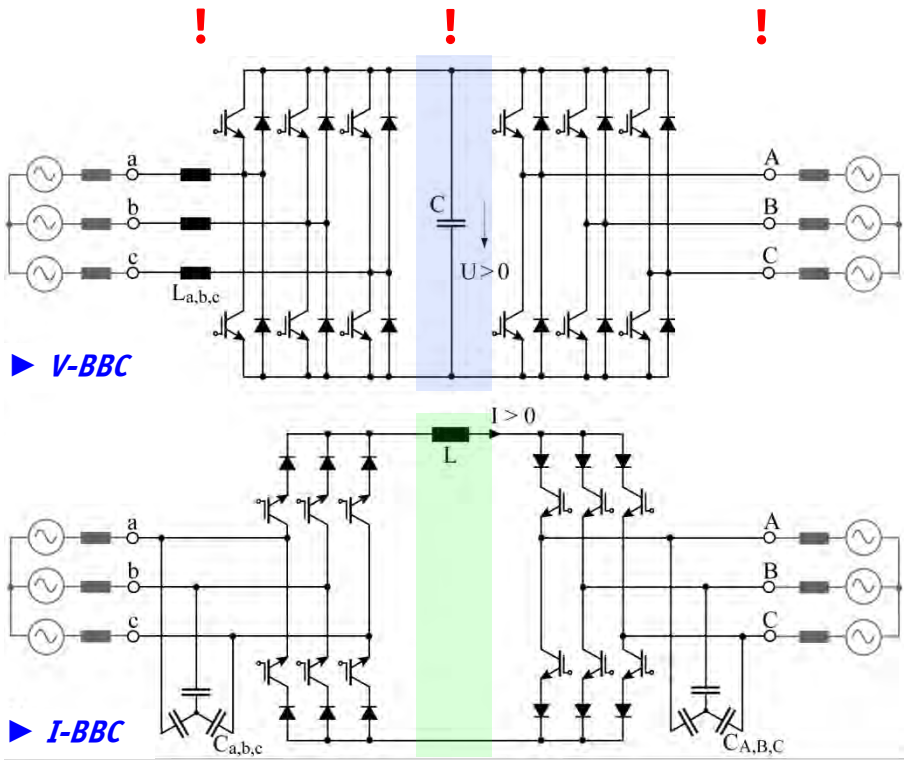
- V-BBC vs. CMC/IMC

Classification of Three-Phase AC-AC Converters

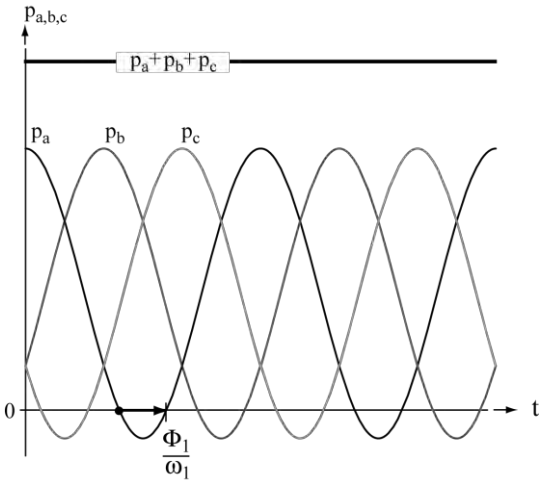


- *Converters with DC-Link*
- *Hybrid Converters*
- *Indirect / Direct Matrix Converters*

DC-Link AC-AC Converter Topologies



$$P = \frac{3}{2}\hat{U}_1 \cdot \hat{I}_1 \cos\Phi_1$$



Symmetric Three-Phase Mains

Phase Voltages

$$\begin{aligned} u_a &= \hat{U}_1 \cos(\omega_1 t) \\ u_b &= \hat{U}_1 \cos\left(\omega_1 \left(t - \frac{T}{3}\right)\right) \\ u_c &= \hat{U}_1 \cos\left(\omega_1 \left(t + \frac{T}{3}\right)\right) \end{aligned}$$

Phase Currents

$$\begin{aligned} i_a &= \hat{I}_1 \cos(\omega_1 t - \Phi_1) \\ i_b &= \hat{I}_1 \cos\left(\omega_1 \left(t - \frac{T}{3}\right) - \Phi_1\right) \\ i_c &= \hat{I}_1 \cos\left(\omega_1 \left(t + \frac{T}{3}\right) - \Phi_1\right) \end{aligned}$$

Instantaneous Power

$$\begin{aligned} p(t) = u_a i_a + u_b i_b + u_c i_c = {} & \frac{P}{3}(1 + \cos 2\omega_1 t) + \frac{Q}{3}\sin 2\omega_1 t \\ & + \frac{P}{3}\left(1 + \cos 2\omega_1 \left(t - \frac{T}{3}\right)\right) + \frac{Q}{3}\sin 2\omega_1 \left(t - \frac{T}{3}\right) \\ & + \frac{P}{3}\left(1 + \cos 2\omega_1 \left(t + \frac{T}{3}\right)\right) + \frac{Q}{3}\sin 2\omega_1 \left(t + \frac{T}{3}\right) \end{aligned}$$

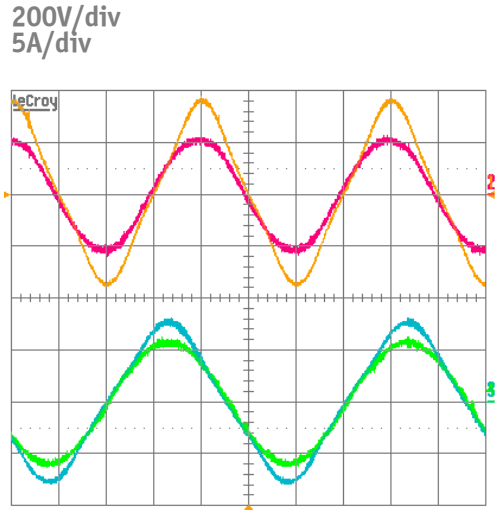
$$P = \frac{3}{2}\hat{U}_1 \cdot \hat{I}_1 \cos\Phi_1$$

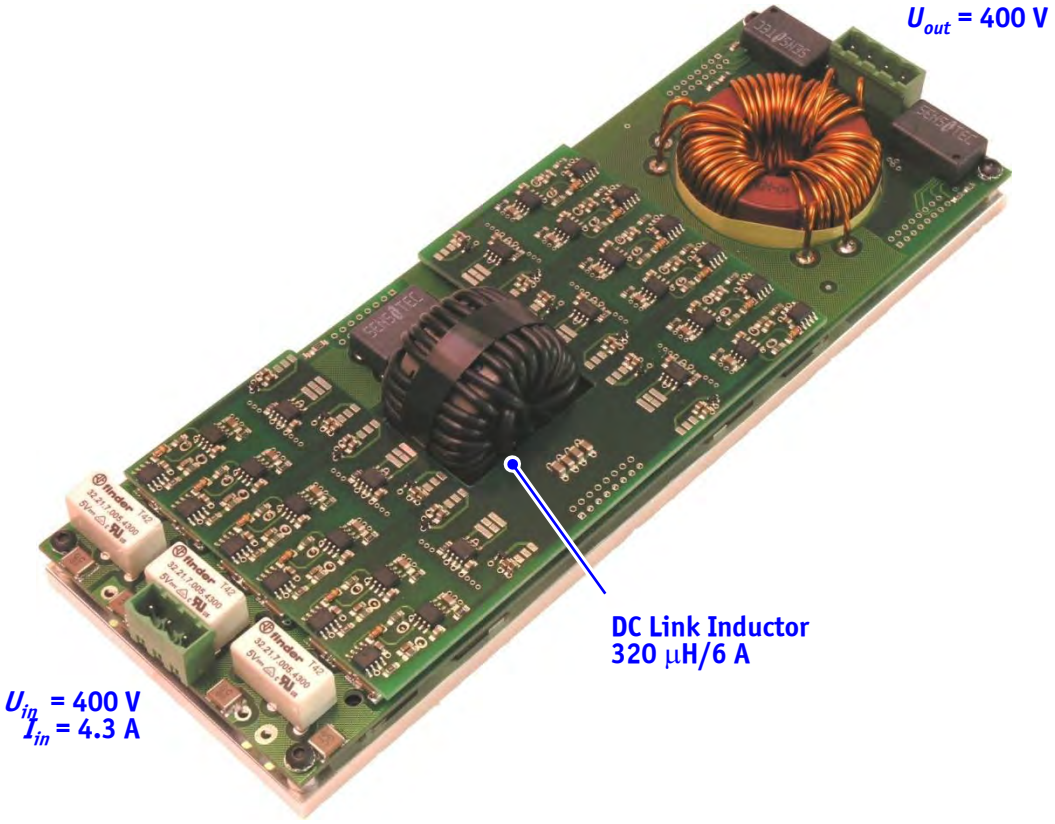
$$Q = \frac{3}{2}\hat{U}_1 \cdot \hat{I}_1 \sin\Phi_1$$

$$\begin{aligned} p(t) = {} & \frac{P}{3}(1 + \cos 2\omega_1 t) + \frac{P}{3}\left(1 + \cos 2\omega_1 \left(t - \frac{T}{3}\right)\right) \\ & + \frac{P}{3}\left(1 + \cos 2\omega_1 \left(t + \frac{T}{3}\right)\right) = 3\frac{P}{3} = P \end{aligned}$$

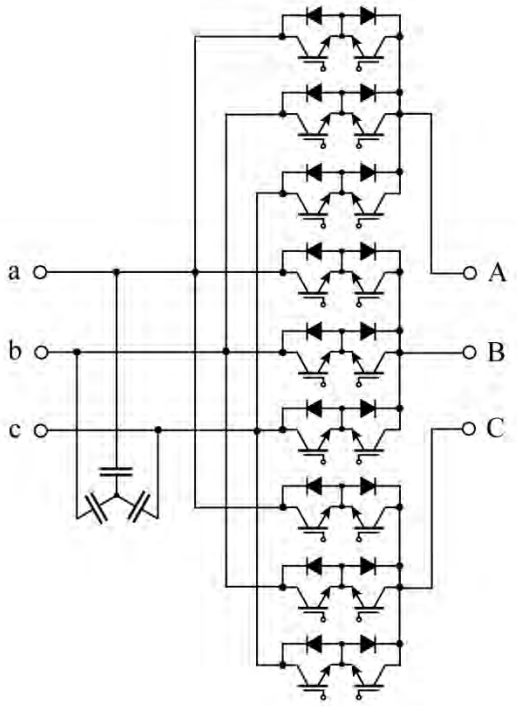
All-SiC JFET I-BBC Prototype

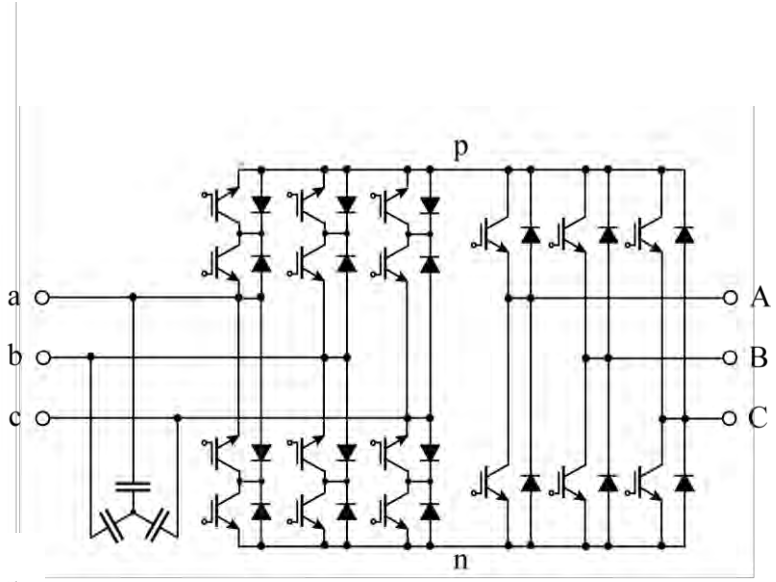
- P_{out} = 2.9 kVA
- f_S = 200 kHz
- 2.4 kVA / liter (42 W/in^3)
- 230 x 80 x 65 mm^3





Basic Matrix Converter Topologies





$$\frac{Q}{3}\left(\sin 2\omega_1 t + \sin 2\omega_1\left(t-\frac{T}{3}\right) + \sin 2\omega_1\left(t+\frac{T}{3}\right)\right) \equiv 0$$

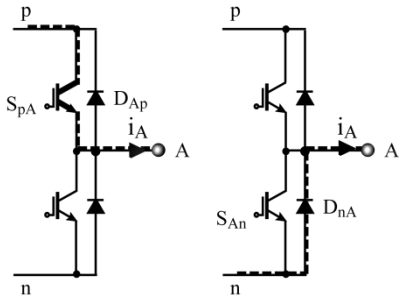
V-BBC

Voltage Space Vectors
Modulation
DC-Link Current

VSI Space Vector Modulation (1)

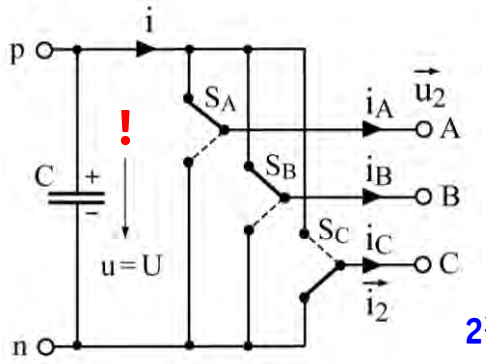
$$\vec{u}_{2,j} = \frac{2}{3}\left(u_{A,j} + \underline{a}u_{B,j} + \underline{a}^2 u_{C,j}\right)$$
$$u_{0,j} = \frac{1}{3}\left(u_{A,j} + u_{B,j} + u_{C,j}\right)$$

- Switching with Interlock Delay

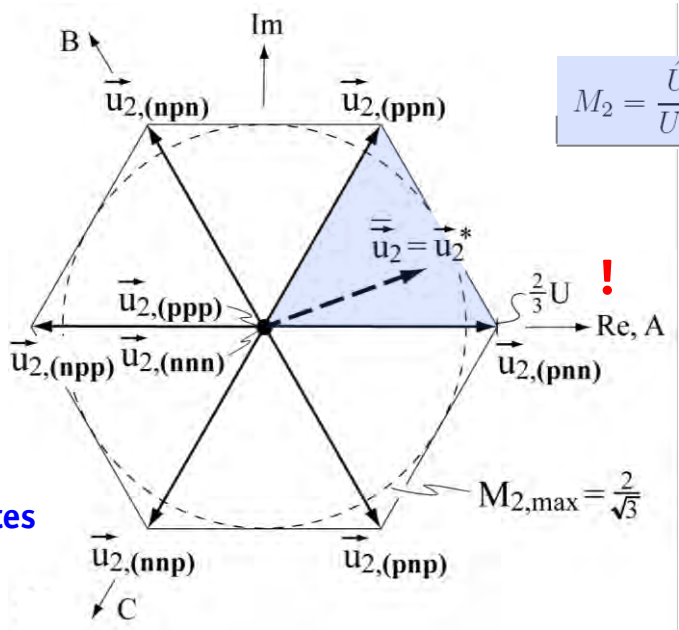


Output Voltage Reference Value

$$\vec{u}_2^* = \hat{U}_2^* e^{j\varphi_{\vec{u}_2^*}} = \hat{U}_2^* e^{j\omega_2^* t}$$



$2^3 = 8$ Switching States



$$M_2 = \frac{\hat{U}_2^*}{U/2}$$

VSI Space Vector Modulation (2)

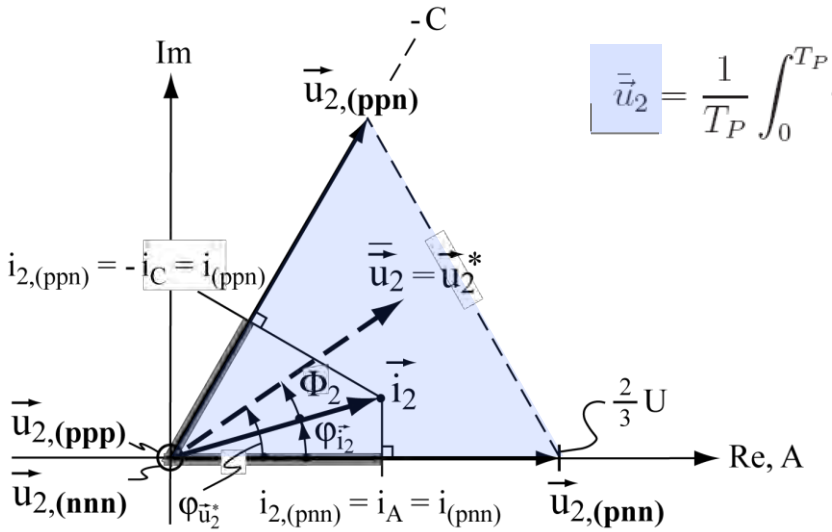
$$M_{2,\max} = \frac{\hat{U}^*_{2,\max}}{U/2} = \frac{2}{\sqrt{3}}$$

Switching State Sequence

$$\ldots \;\Big|_{t_\mu = 0}\quad (nnn) - (pnn) - (ppn) - (ppp)\;\Big|_{t_\mu = T_P/2}$$

$$(ppp) - (ppn) - (pnn) - (nnn)\;\Big|_{t_\mu = T_P}\quad \ldots$$

Formation of the Output Voltage



$$\bar{\vec{u}}_2 = \frac{1}{T_P}\int_0^{T_P} \vec{u}_{2,j}\,\mathrm{d}t_\mu = d_{(pnn)}\cdot\vec{u}_{2,(pnn)} + d_{(ppn)}\cdot\vec{u}_{2(ppn)}$$

$$= d_{(pnn)}\frac{2}{3}U + d_{(ppn)}\frac{2}{3}U\mathrm{e}^{j\pi/3}$$

$$= \vec{u}_2^*$$

Relative On-times

$$d_{(ppn)} = \frac{\sqrt{3}}{2}M_2 \sin\left(\varphi_{\vec{u}_2^*}\right)$$

$$d_{(pnn)} = \frac{\sqrt{3}}{2}M_2 \sin\left(\frac{\pi}{3} - \varphi_{\vec{u}_2^*}\right)$$

VSI Space Vector Modulation (3)

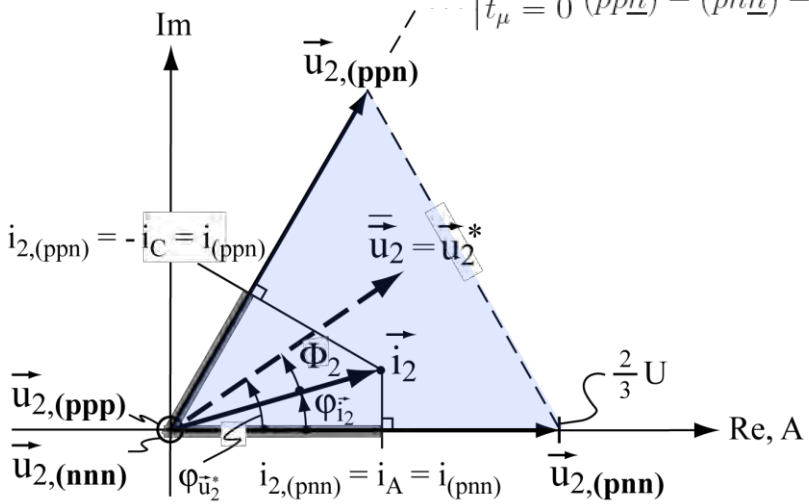
Freewheeling On-time

$$d_{(nnn)} + d_{(ppp)} = 1 - \left(d_{(ppn)} + d_{(pnn)}\right)$$

Discontinuous Modulation

$$\left|t_\mu = 0\ (\underline{p}nn) - (\underline{p}pn) - (\underline{p}pp)\right| t_\mu = T_P/2\ (\underline{p}pp) - (\underline{p}pn) - (\underline{p}nn) \left| t_\mu = T_P \cdots \right.$$

$$\left|t_\mu = 0\ (pp\underline{n}) - (pn\underline{n}) - (nn\underline{n})\right| t_\mu = T_P/2\ (nn\underline{n}) - (pn\underline{n}) - (pp\underline{n}) \left| t\mu = T_P \cdots \right.$$



Space Vector Orientation

$$\frac{d_{(ppn)}}{d_{(pnn)}} = \frac{\sin\left(\varphi_{\vec{u}_2^*}\right)}{\sin\left(\frac{\pi}{3} - \varphi_{\vec{u}_2^*}\right)}$$

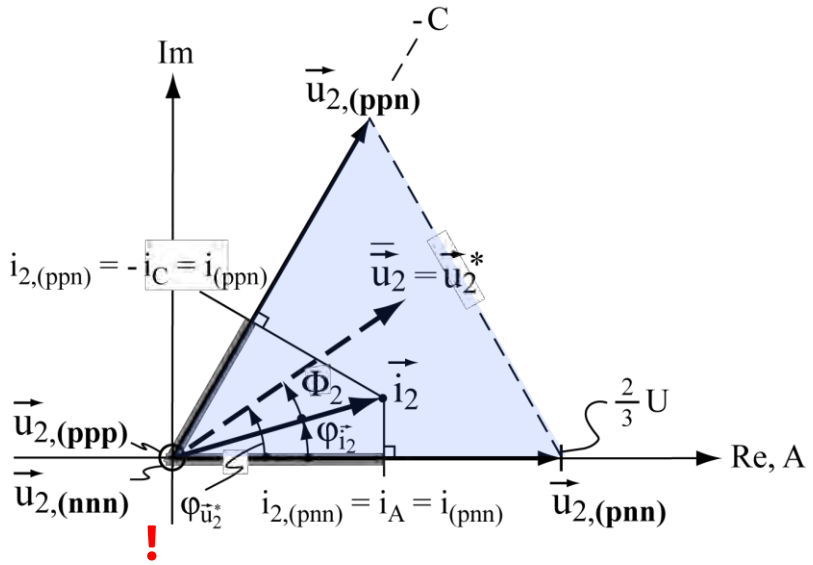
Modulation Limit

$$M_{2,\max} = \frac{\hat{U}^*_{2,\max}}{U/2} = \frac{2}{\sqrt{3}}$$

VSI Space Vector Modulation (4)

DC-Link Current Shape

$$i_j = i_{2,j}$$



$$\begin{aligned}
i_{(nnn)} &= 0 \\
i_{(nnp)} &= i_C \\
i_{(npn)} &= i_B \\
i_{(npp)} &= i_B + i_C = -i_A \\
i_{(pnn)} &= i_A \\
i_{(pnp)} &= i_A + i_C = -i_B \\
i_{(ppn)} &= i_A + i_B = -i_C \\
i_{(ppp)} &= 0
\end{aligned}$$

Local Average Value

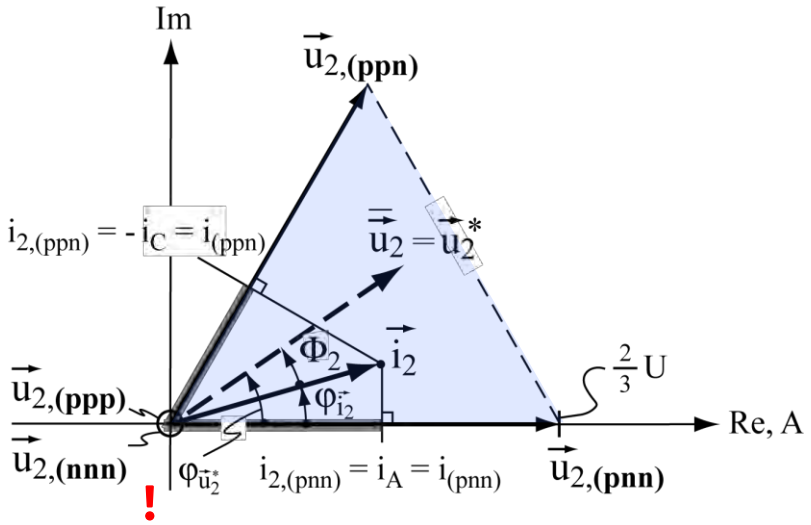
$$\bar{i} = \frac{1}{T_P} \int_0^{T_P} i_j \, \mathrm{d}t_\mu$$

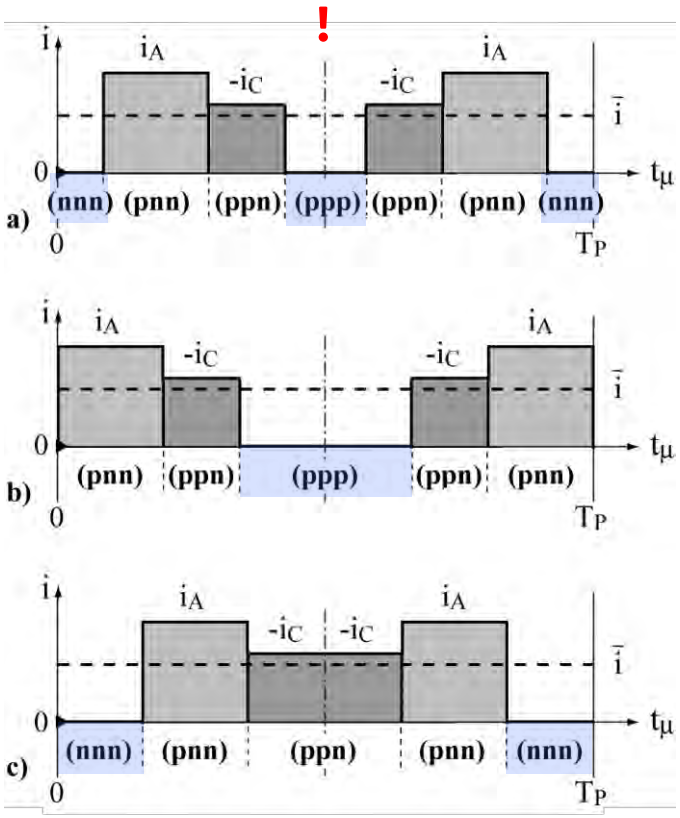
$$\bar{i} = -i_C d_{(ppn)} + i_A d_{(pnn)}$$

VSI Space Vector Modulation (5)

Local DC-Link Current Shape

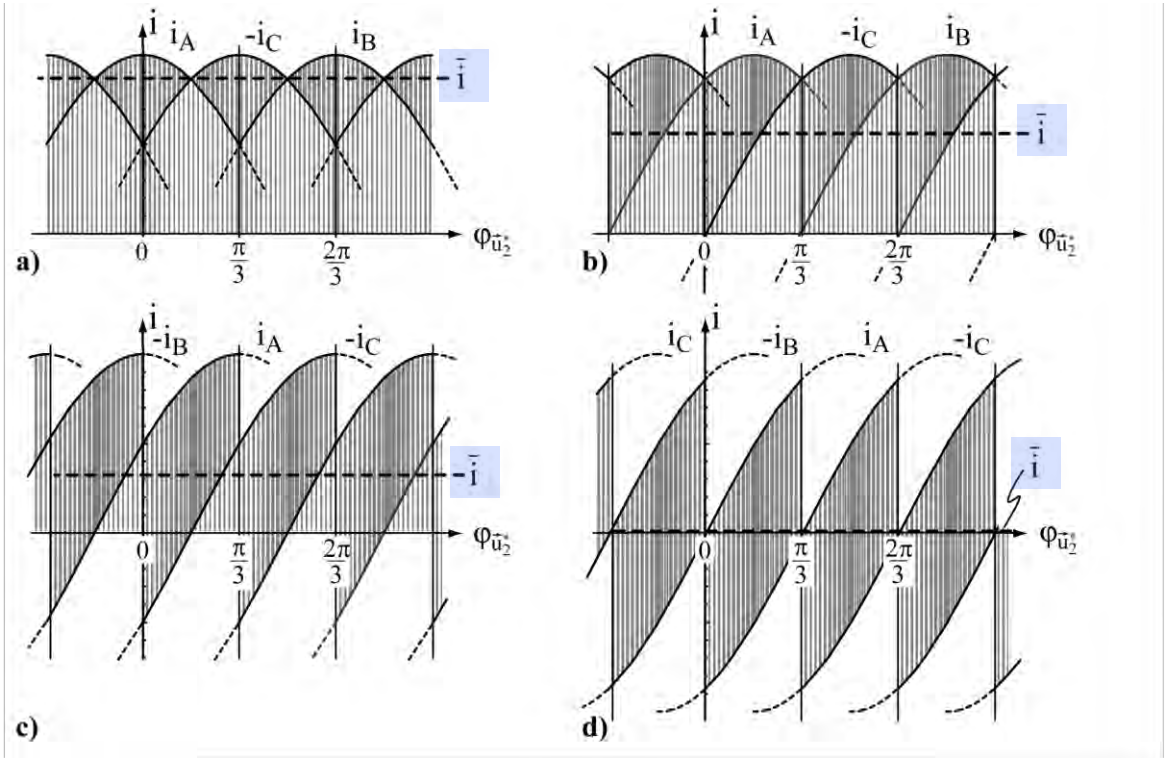
$$\bar{i} = I = \frac{3}{4} M_2 \hat{I}_2 \cos \Phi_2$$

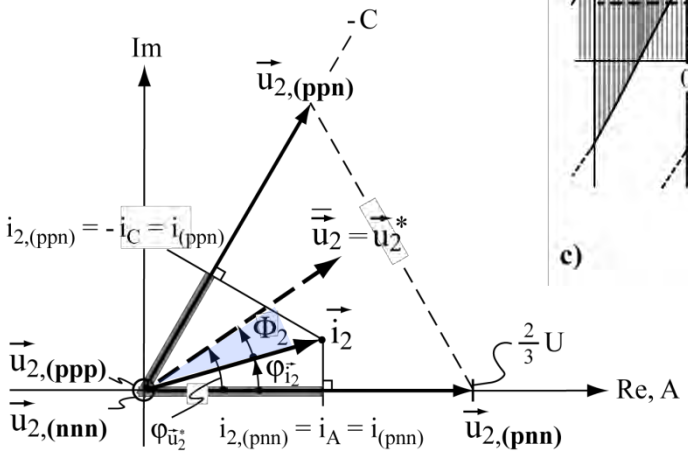




VSI DC-Link Current Waveform

Influence of Output Voltage Phase Displacement Φ_2 on DC-Link Current Waveform

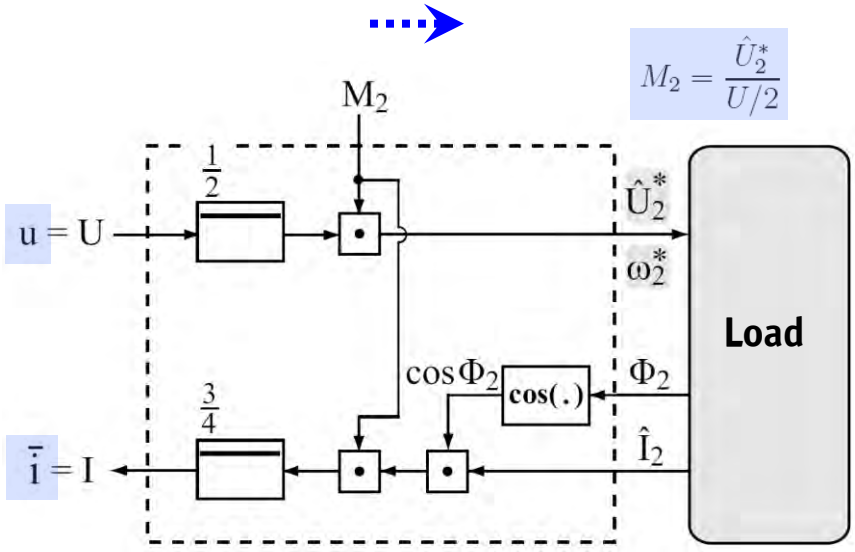




$$\bar{i} = I = \frac{3}{4} M_2 \hat{I}_2 \cos \Phi_2 \qquad M_2 = 2/\sqrt{3}$$

VSI Functional Equivalent Circuit

Voltage Conversion



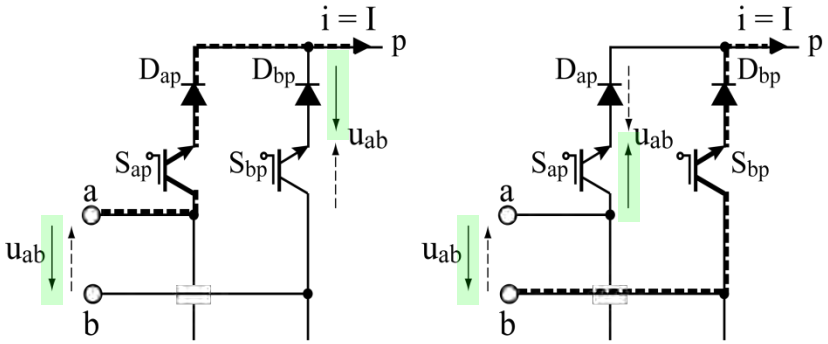
Current Conversion

I-BBC

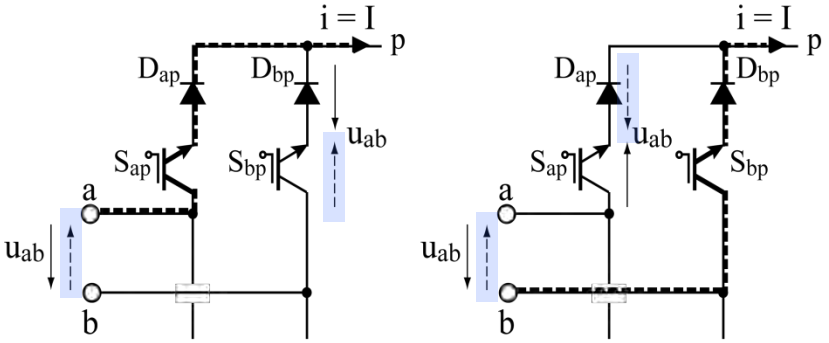
Current Space Vectors
Modulation
DC Link Voltage

CSR Commutation & Equivalent Circuit

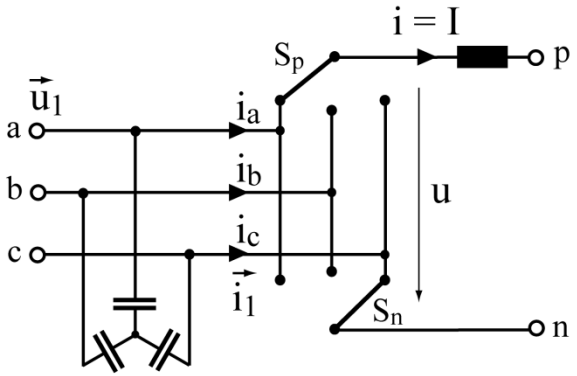
Forced Commutation



Natural Commutation



Equivalent Circuit



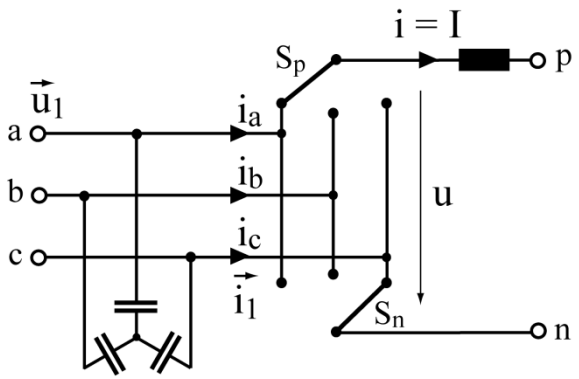
- $3^2 = 9$ Switching States
- Overlapping Switching

CSR Space Vector Modulation (1)

$$\vec{i}_k = \frac{2}{3}\left(i_{a,k} + \underline{a}\, i_{b,k} + \underline{a}^2\, i_{c,k}\right) \qquad \underline{a} = \mathrm{e}^{j2\pi/3}$$

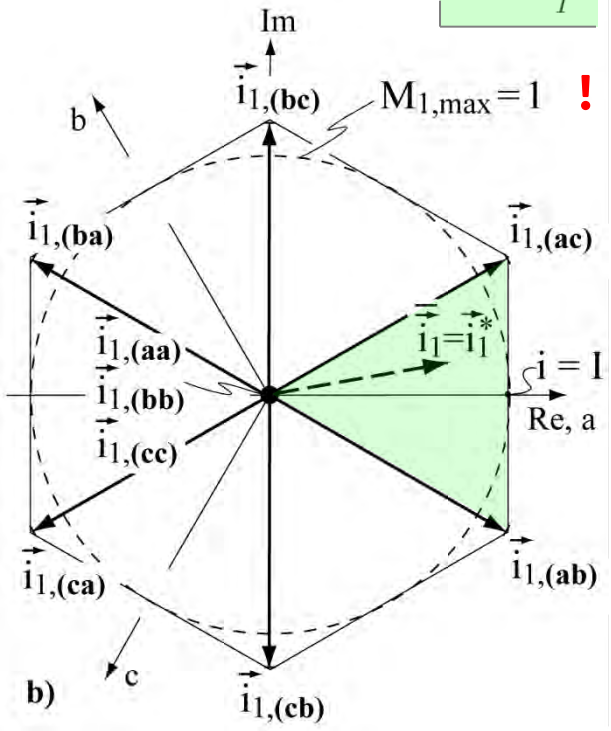
Input Current Reference Value

$$\vec{i}_1^{\,*} = \hat{I}_1^* \mathrm{e}^{j\varphi_{\vec{i}_1^*}} = \hat{I}_1^* \mathrm{e}^{j(\omega_1 t - \Phi_1^*)}$$



a)

$$M_1 = \frac{\hat{I}_1^*}{I}$$



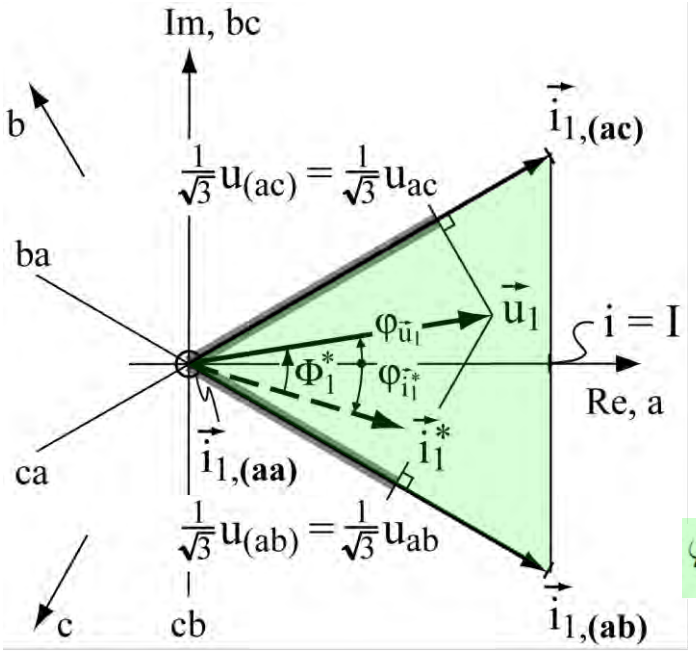
b)

CSR Space Vector Modulation (2)

Formation of the Input Current

$$|\vec{i}_{1,k}| = i_{1,k} = \quad 2/\sqrt{3} \cdot I$$

$$\vec{\bar{i}}_1 = \frac{1}{T_P} \int_0^{T_P} \vec{i}_{1,k}\, \mathrm{d}t_\mu = d_{(ac)} \cdot \vec{i}_{1,(ac)} + d_{(ab)} \cdot \vec{i}_{1,(ab)} = \vec{i}_1^{\,*}$$



$$\varphi_{\vec{i}_1^{\,*}} = \varphi_{\vec{u}_1} - \Phi_1^*$$

Relative On-times

$$d_{(ac)} = M_1 \sin\left(\frac{\pi}{6} + \varphi_{\vec{i}_1^{\,*}}\right)$$

$$d_{(ab)} = M_1 \sin\left(\frac{\pi}{6} - \varphi_{\vec{i}_1^{\,*}}\right)$$

$$d_{(aa)} = 1 - \left(d_{(ac)} + d_{(ab)}\right)$$

Space Vector Orientation

$$\frac{d_{(ac)}}{d_{(ab)}} = \frac{\sin\left(\frac{\pi}{6} + \varphi_{\vec{i}_1^{\,*}}\right)}{\sin\left(\frac{\pi}{6} - \varphi_{\vec{i}_1^{\,*}}\right)}$$

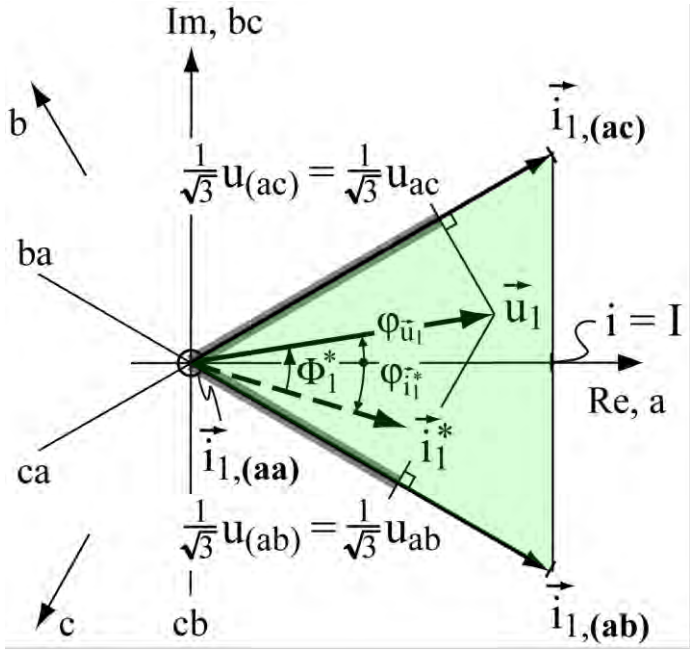
CSR Space Vector Modulation (3)

Switching State Sequence

$$\cdots \Big| t_\mu = 0 \quad (\underline{a}b)-(\underline{a}c)-(\underline{a}a) \Big| t_\mu = T_P/2 \quad (\underline{a}a)-(\underline{a}c)-(\underline{a}b) \Big| t_\mu = T_P \cdots$$

$$\cdots \Big| t_\mu = 0 \quad (\underline{a}c)-(\underline{a}b)-(\underline{a}a) \Big| t_\mu = T_P/2 \quad (\underline{a}a)-(\underline{a}b)-(\underline{a}c) \Big| t_\mu = T_P \cdots$$

$$\cdots \Big| t_\mu = 0 \quad (\underline{a}c)-(\underline{a}a)-(\underline{a}b) \Big| t_\mu = T_P/2 \quad (\underline{a}b)-(\underline{a}a)-(\underline{a}c) \Big| t_\mu = T_P \cdots$$



DC-Link Voltage Formation

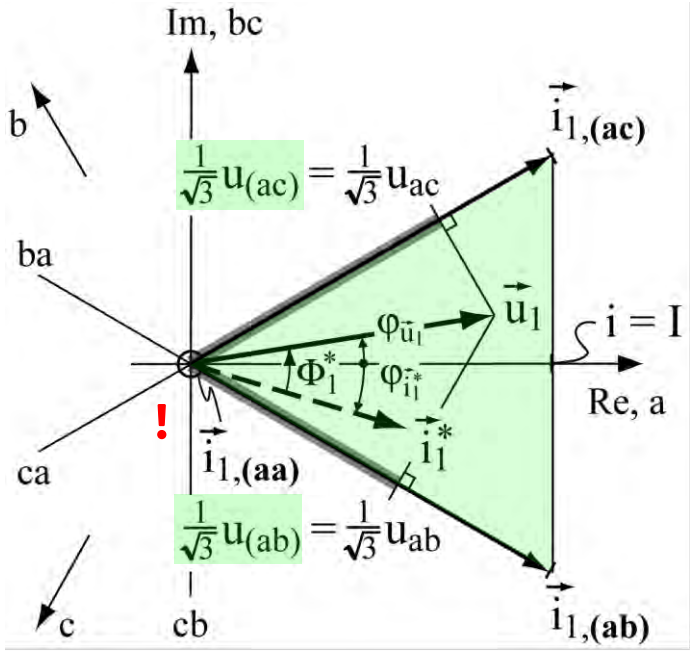
$$\begin{aligned}
u_{(ab)} &= u_a - u_b = u_{ab} \\
u_{(ba)} &= u_b - u_a = u_{ba} = -u_{ab} \\
u_{(bc)} &= u_b - u_c = u_{bc} \\
u_{(cb)} &= u_c - u_b = u_{cb} = -u_{bc} \\
u_{(ca)} &= u_c - u_a = u_{ca} \\
u_{(ac)} &= u_a - u_c = u_{ac} = -u_{ca} \\
u_{(aa)} &= u_{(bb)} = u_{(cc)} = 0
\end{aligned}$$

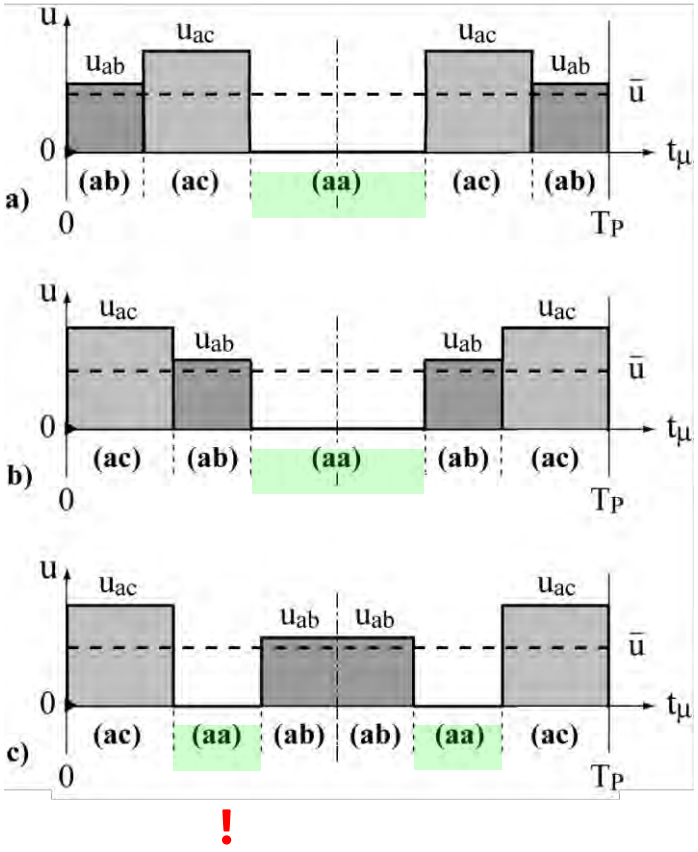
$$u_k = \sqrt{3} \cdot u_{1,k} \qquad \bar{u} = u_{ab} d_{(ab)} + u_{ac} d_{(ac)}$$

CSR Space Vector Modulation (4)

Local DC-Link Voltage Shape

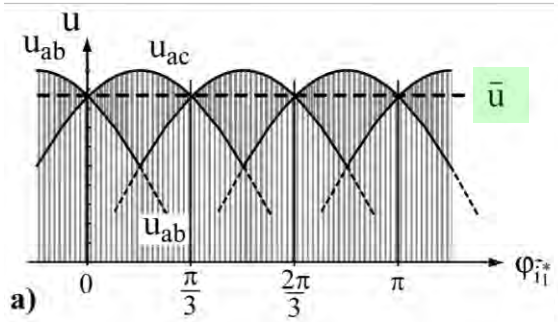
$$\bar{u} = \frac{3}{2} M_1 \hat{U}_1 \cos \Phi_1^*$$

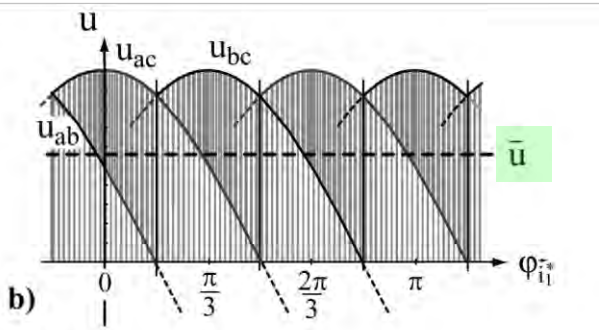


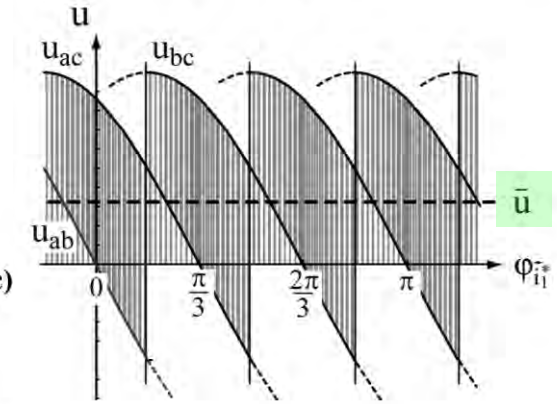


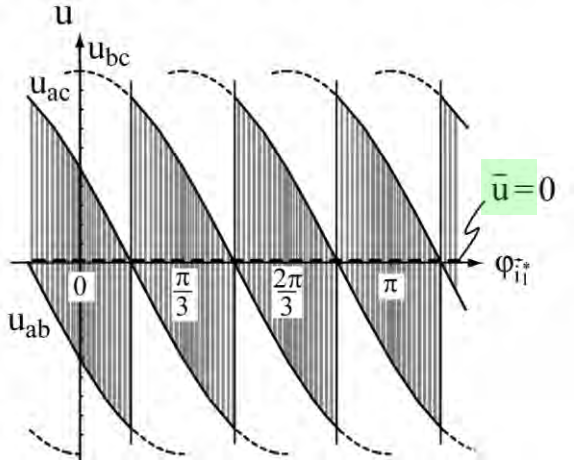
CSR DC-Link Voltage Waveform

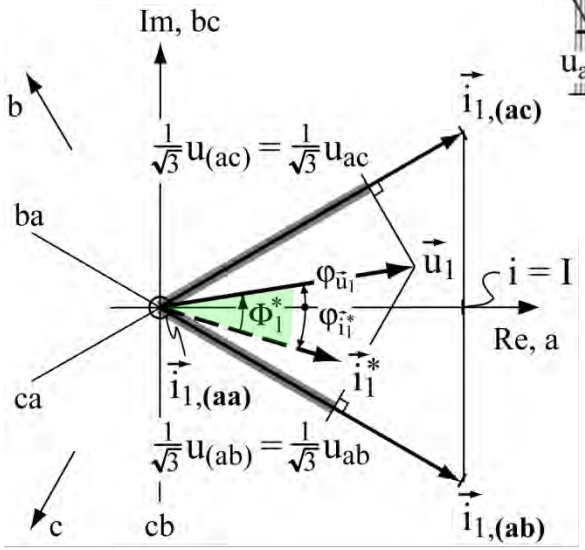
Influence of Input Current Phase Displacement Φ_1 on DC-Link Voltage Waveform









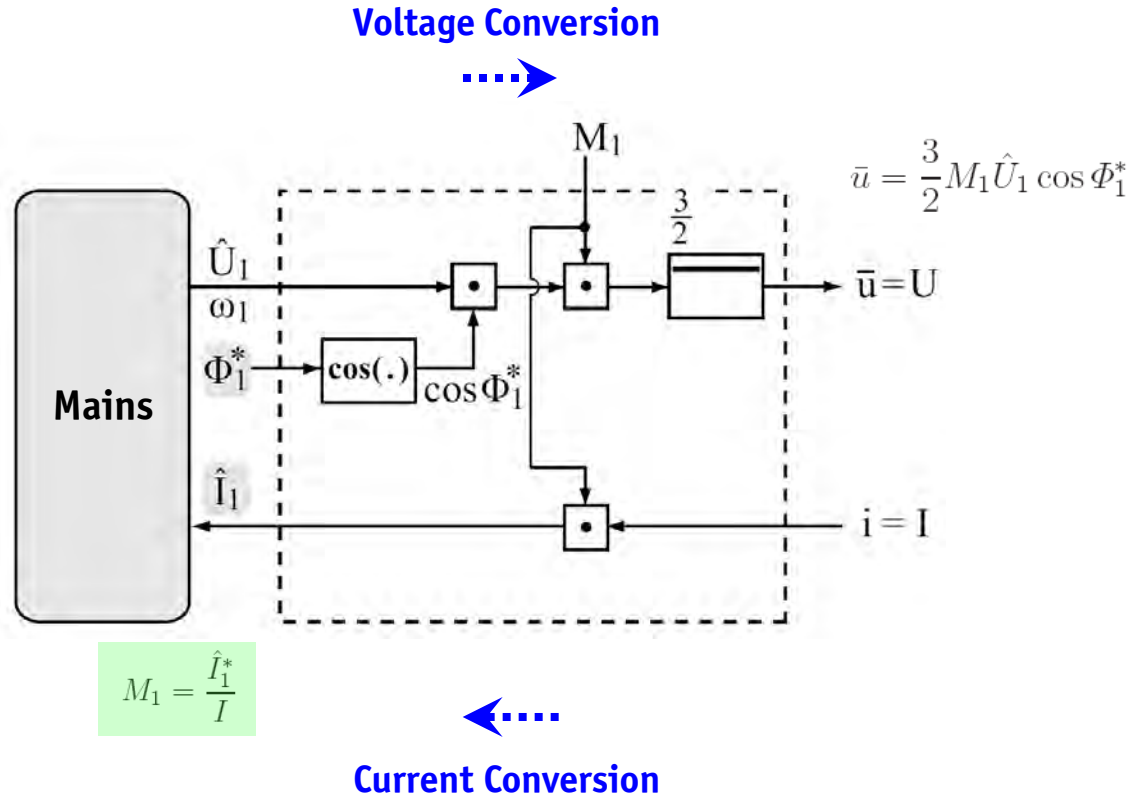


$$M_1 = \frac{\hat{I}_1^*}{\hat{I}}$$

!

$$\bar{u} = \frac{3}{2} M_1 \hat{U}_1 \cos \Phi_1^*$$

CSR Functional Equivalent Circuit

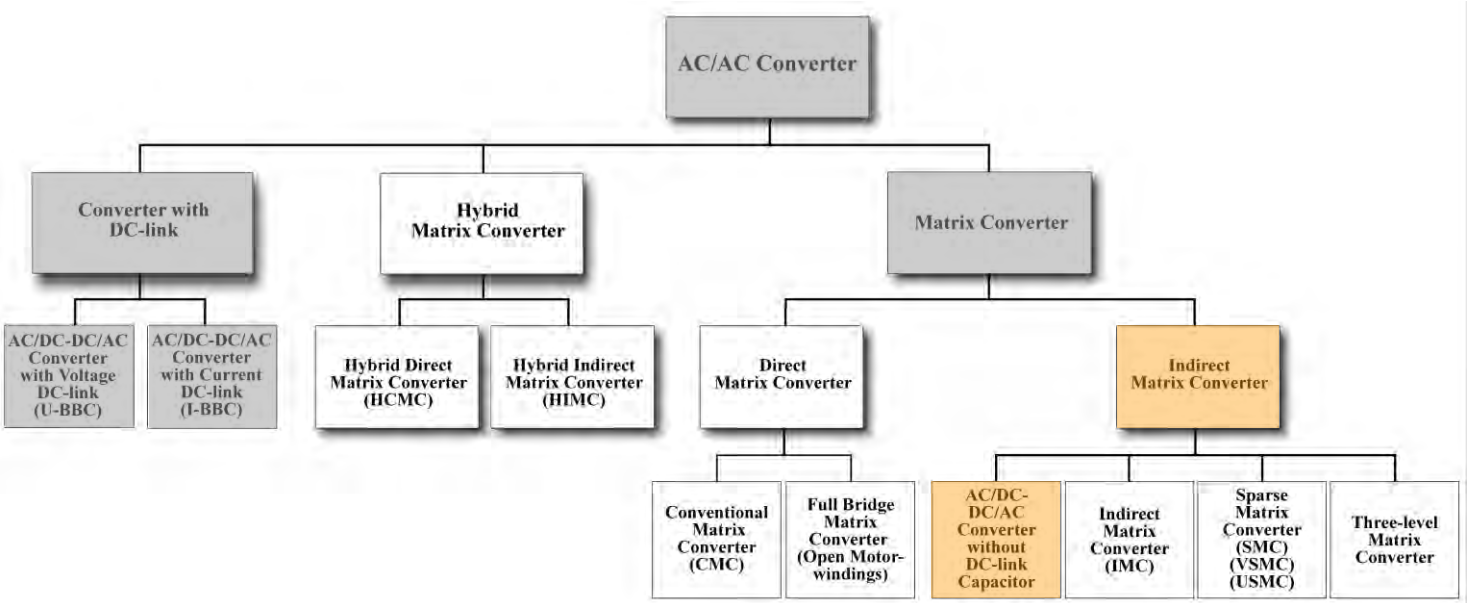


Derivation of MC Topologies

Fundamental Frequency Front End

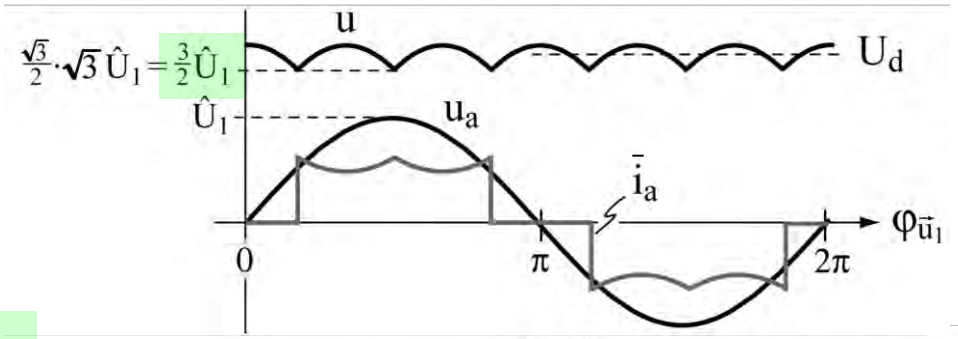
F^3E

Classification of Three-Phase AC-AC Converters



- *Converter without DC-Link Capacitor*

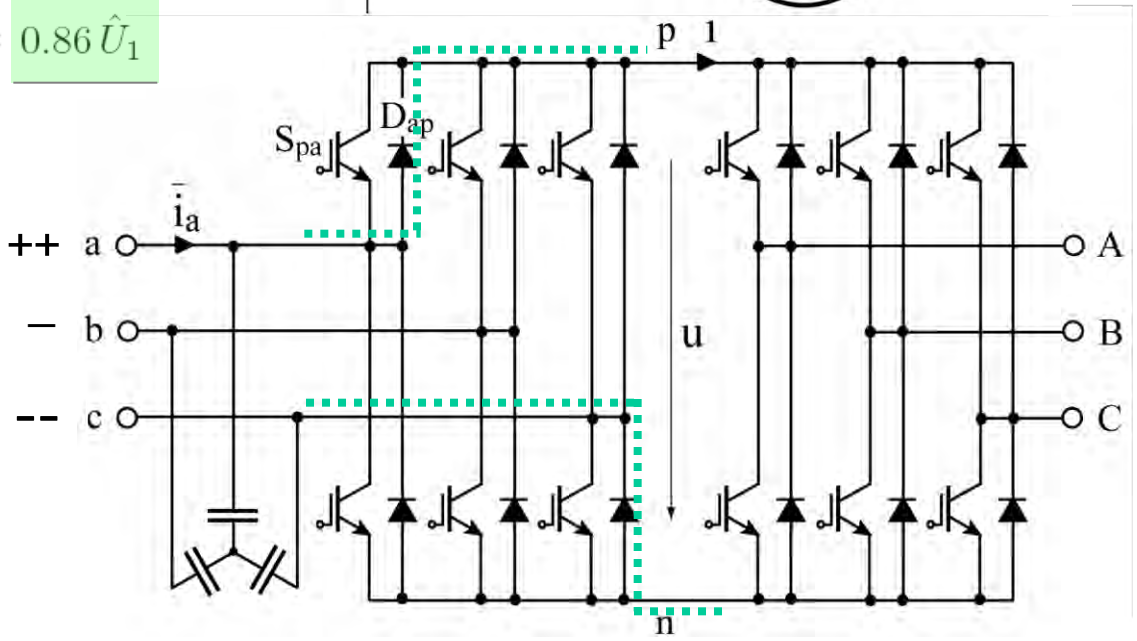
F³E Topology / Mains Behavior



$$u_{\min} = \frac{3}{2}\hat{U}_1$$

!

$$\hat{U}_2^* < \frac{\sqrt{3}}{2}\cdot\hat{U}_1 \approx 0.86\,\hat{U}_1$$



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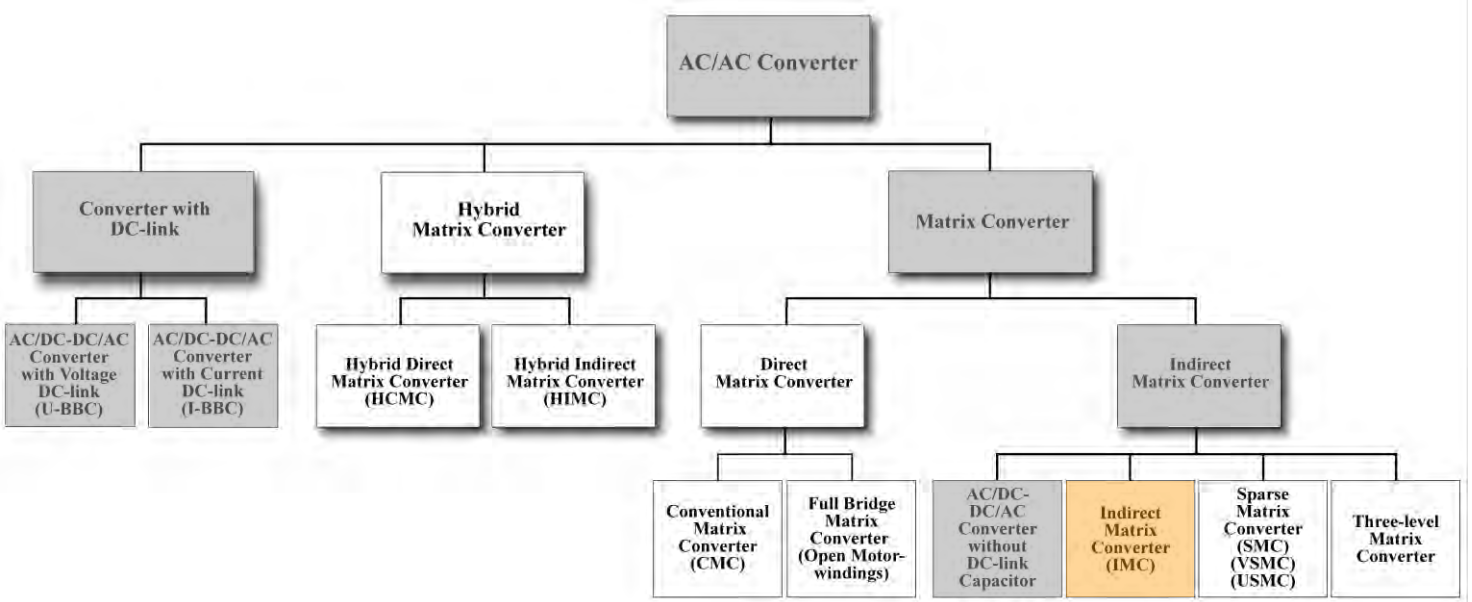
T. Lipo [13, 18, 20]
B. Piepenbreier [15]

Indirect Matrix Converter – IMC

Space Vectors
Modulation
Simulation
Experimental Results

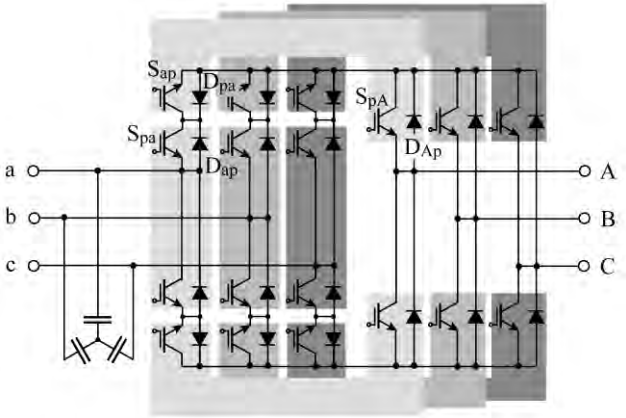
Classification of Three-Phase AC-AC Converters

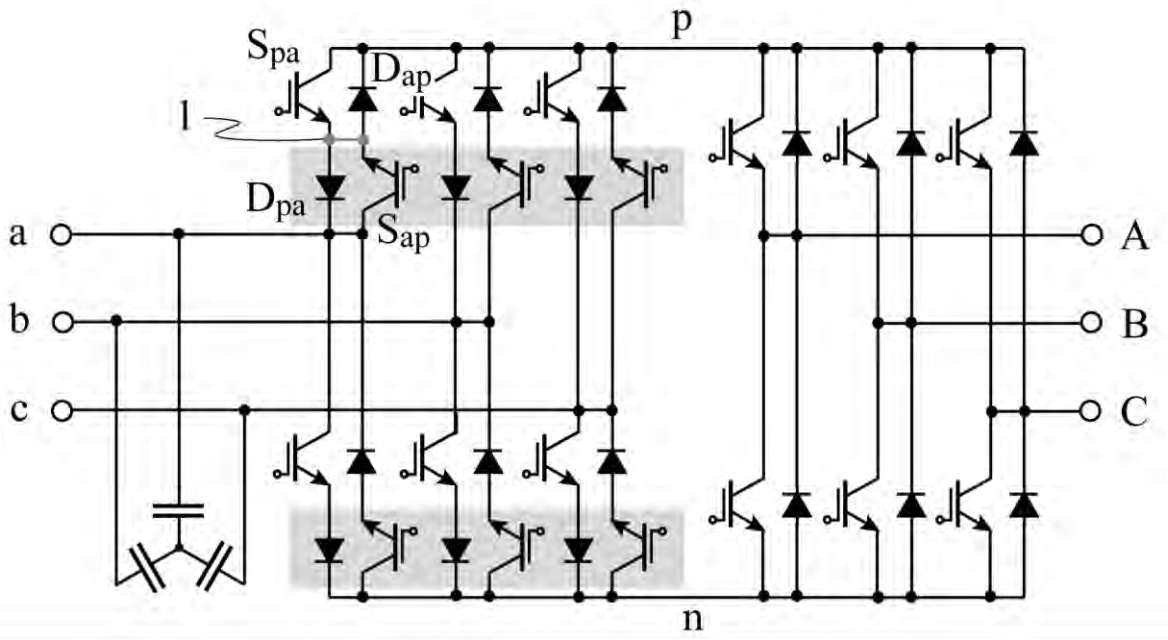


- *Indirect Matrix Converter*

IMC Topology Derivation

- *Extension of F³E-Topology*
- *Bidirectional CSR Mains Interface* !

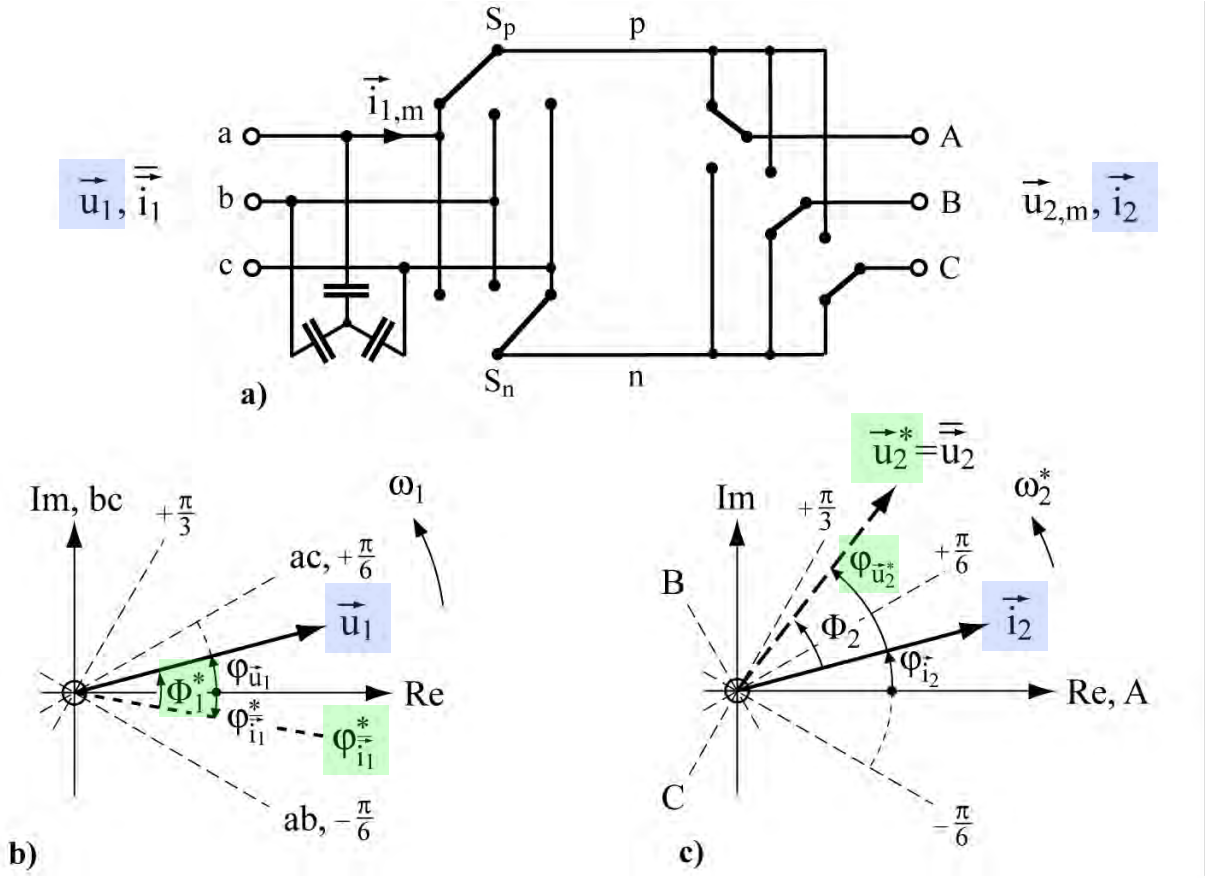




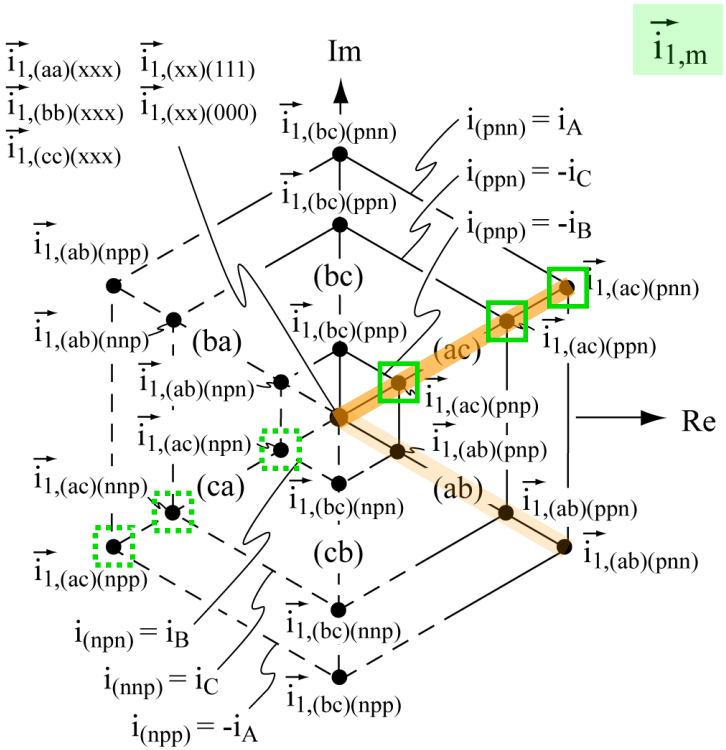
J. Holtz [16]
K. Shinohara [17]

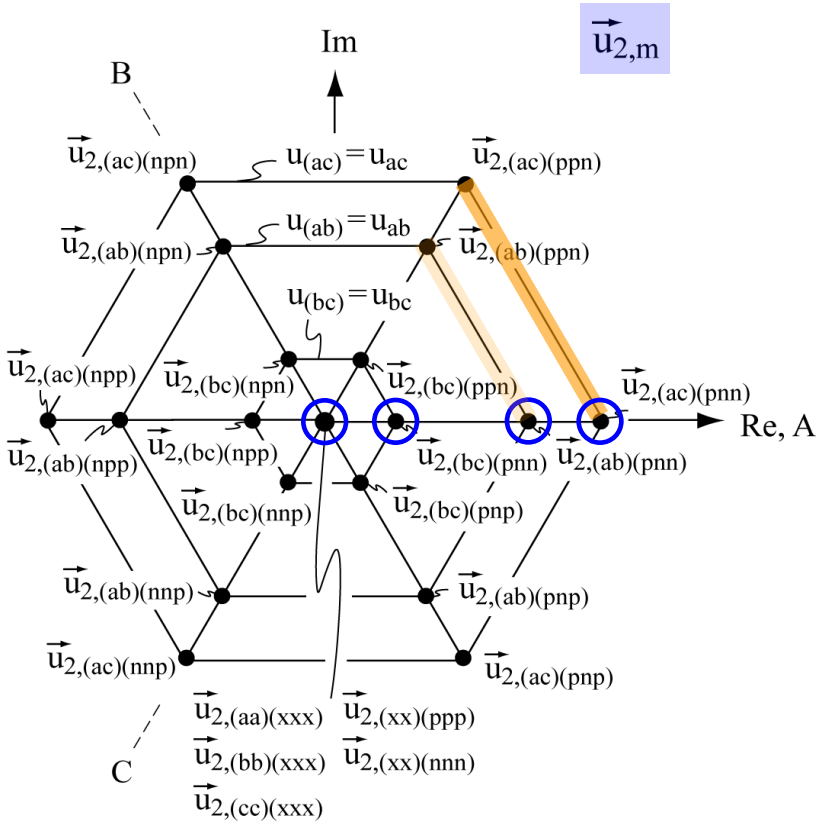
IMC Properties

► *Positive DC-Link Voltage Required* !

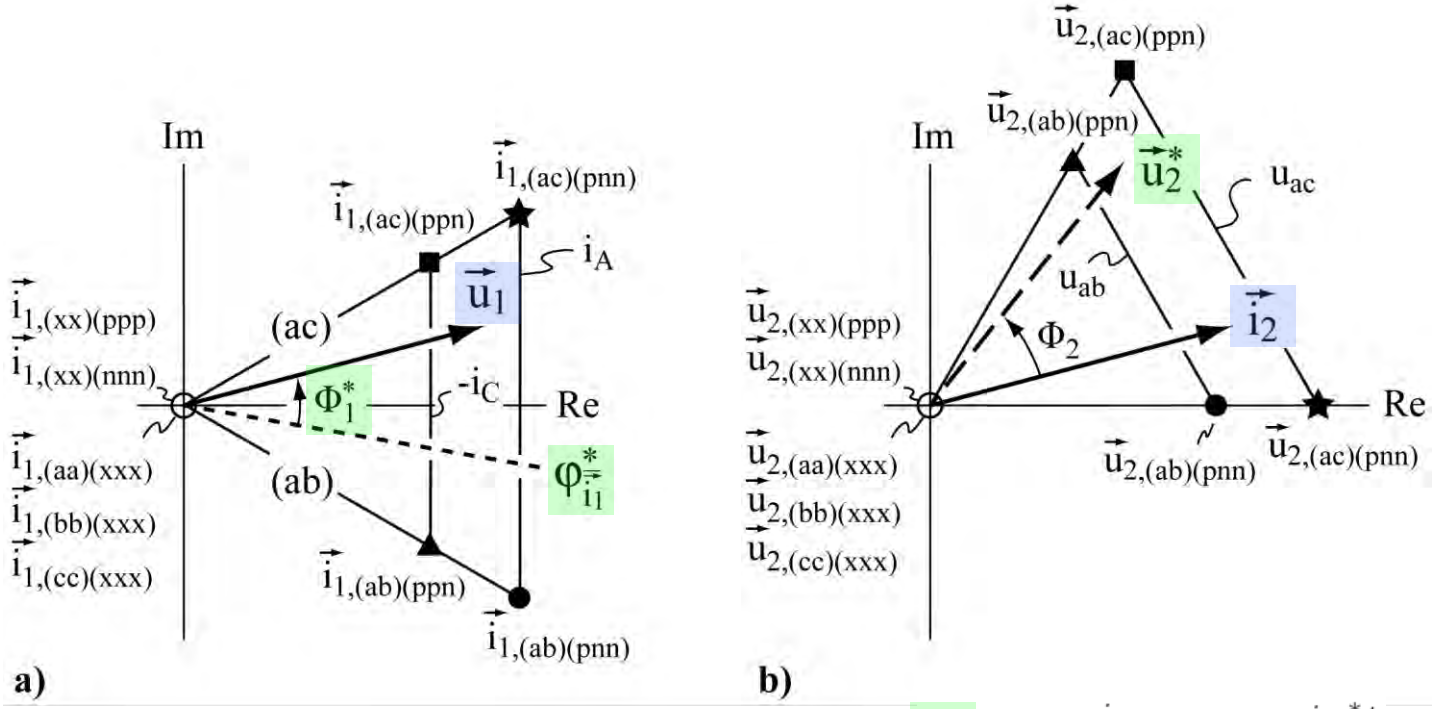


IMC Voltage and Current Space Vectors





IMC Space Vector Modulation (1)



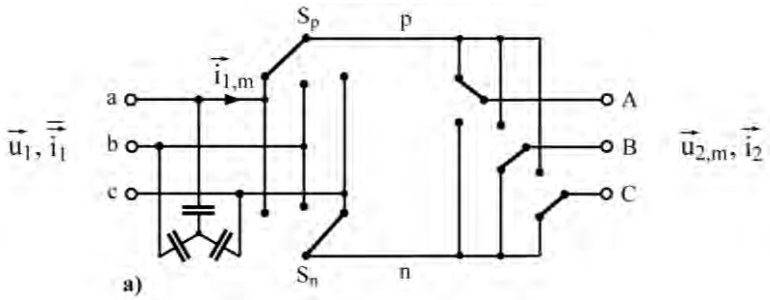
$$\vec{u}_1 = \hat{U}_1 e^{j\varphi_{\vec{u}_1}} = \hat{U}_1 e^{j\omega_1 t} \qquad \vec{i}_1 = \hat{I}_1 e^{j\varphi^*_{\vec{i}_1}}$$

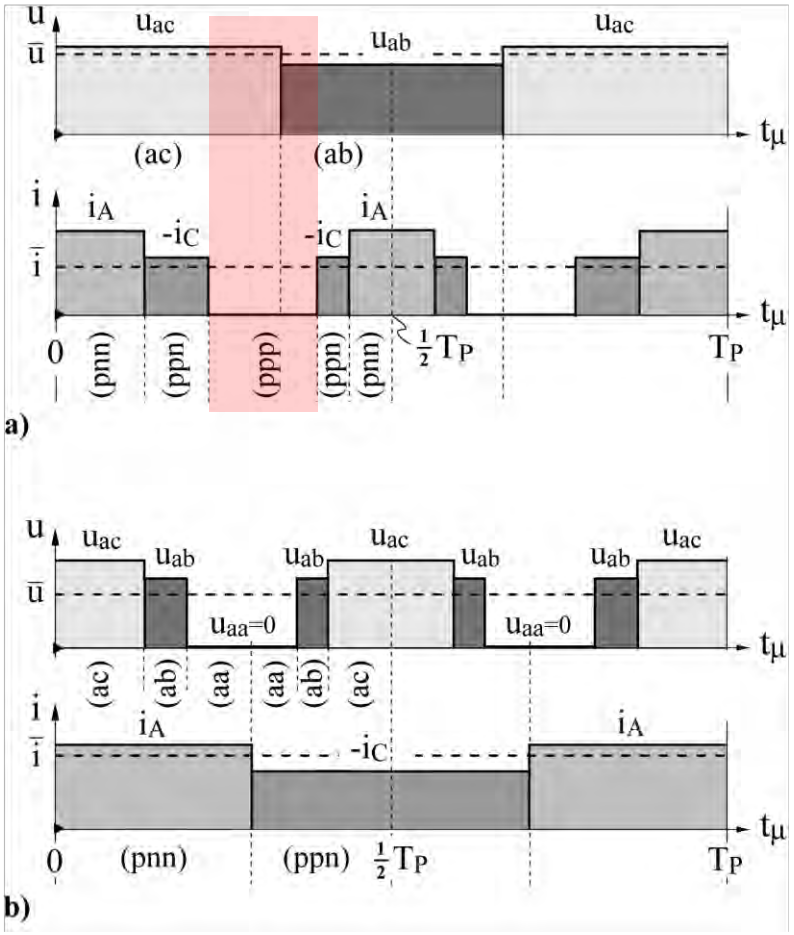
$$\vec{u}_2^* = \hat{U}_2^* e^{j\varphi_{\vec{u}_2^*}} = \hat{U}_2^* e^{j\omega_2^* t}$$

$$\vec{i}_2 = \hat{I}_2 e^{j\varphi_{\vec{i}_2}} = \hat{I}_2 e^{j\left(\varphi_{\vec{u}_2^*} - \Phi_2\right)}$$

IMC Space Vector Modulation (2)

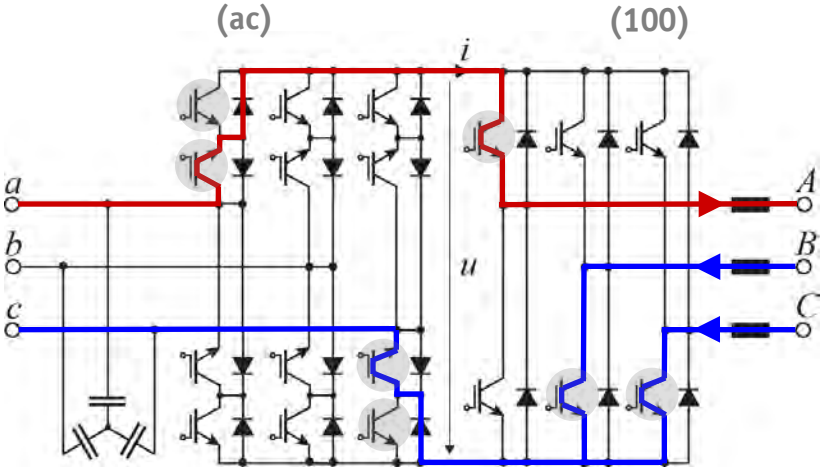
- *Zero Current Commutation* !
- *Zero Voltage Commutation*

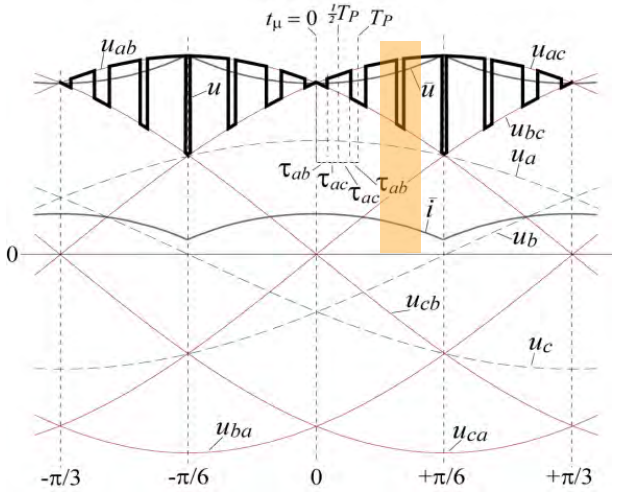




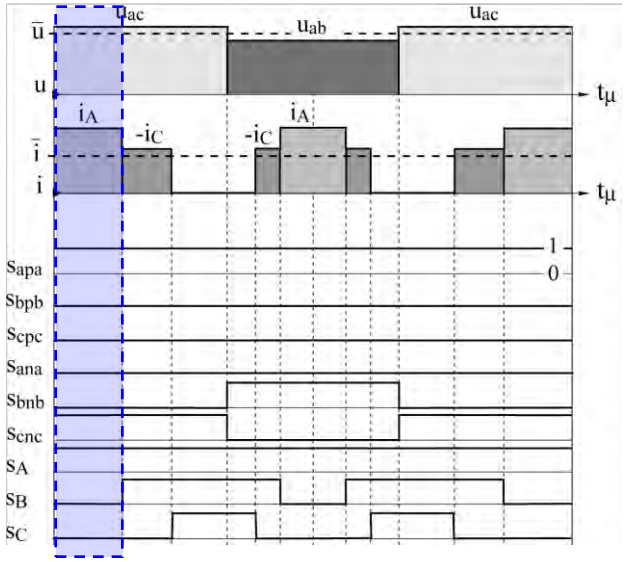
IMC Zero DC-Link Current Commutation (1)

DC-Link Voltage $u = u_{ac}$
DC-Link Current $i = i_A$





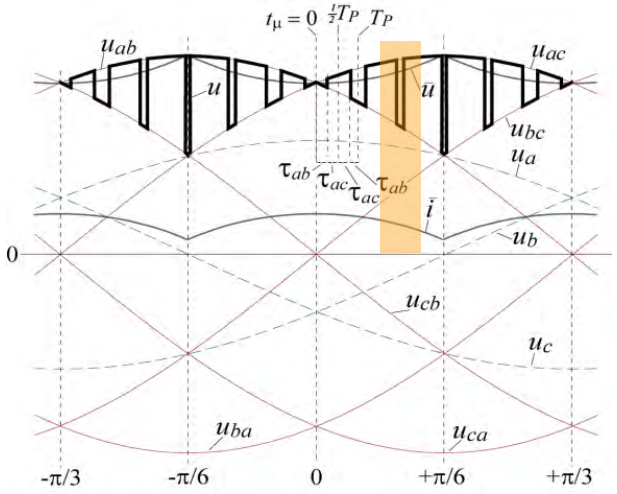
120°of Mains Period



DC link Voltage & Current

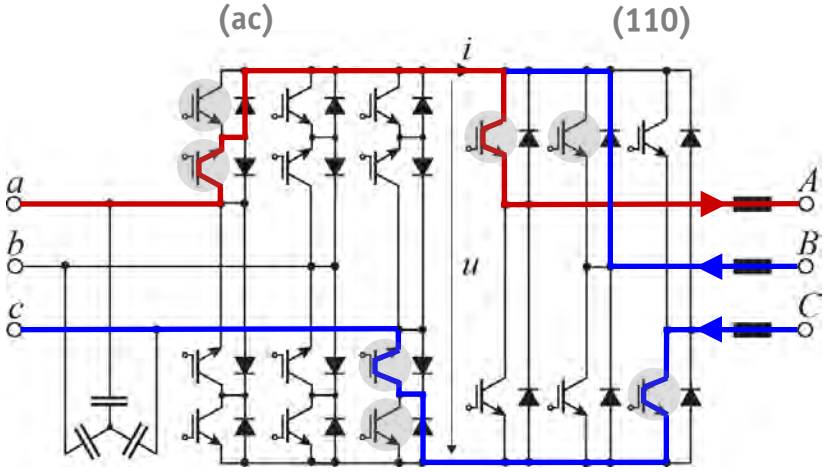
PWM Pattern

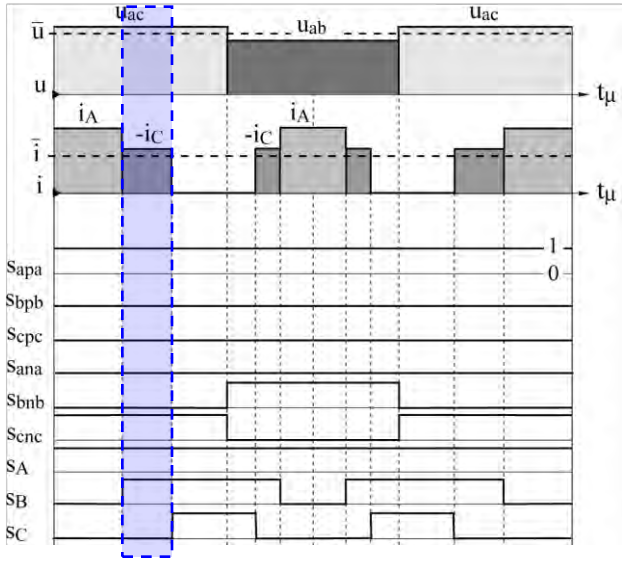
IMC Zero DC-Link Current Commutation (2)



120°of Mains Period

DC-Link Voltage $u = u_{ac}$
DC-Link Current $i = -i_c$



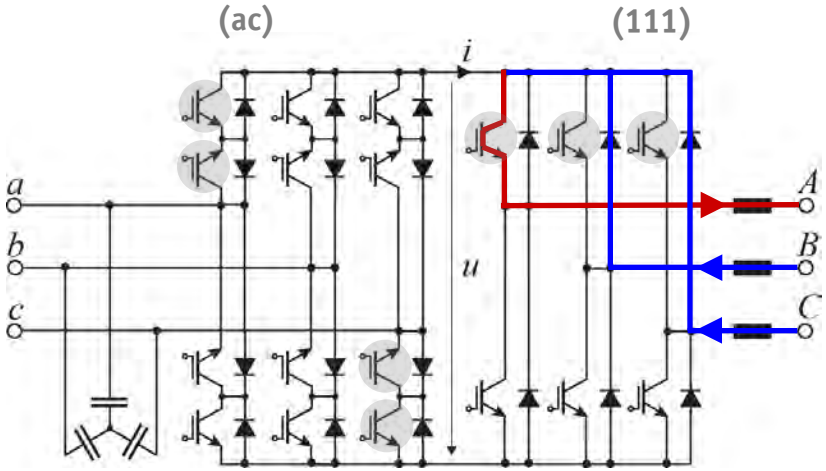


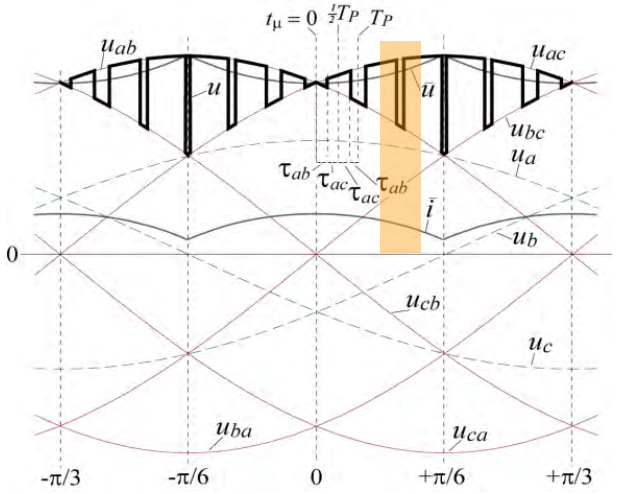
DC link Voltage & Current

PWM Pattern

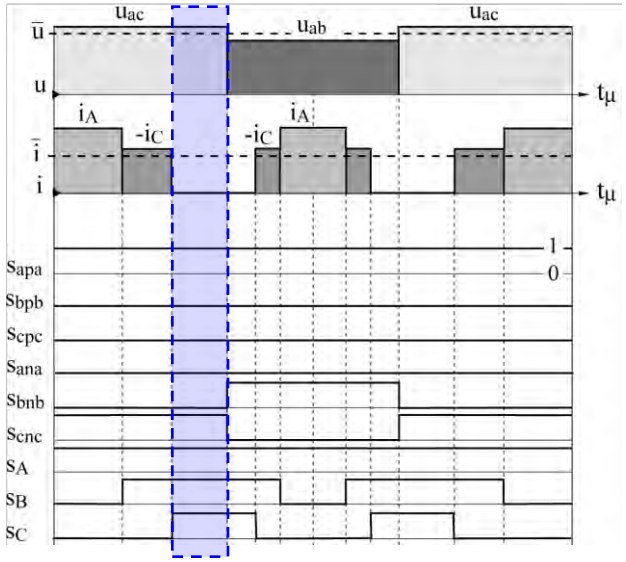
IMC Zero DC-Link Current Commutation (3)

DC-Link Voltage $u = u_{ac}$
DC-Link Current $i = 0$





120°of Mains Period

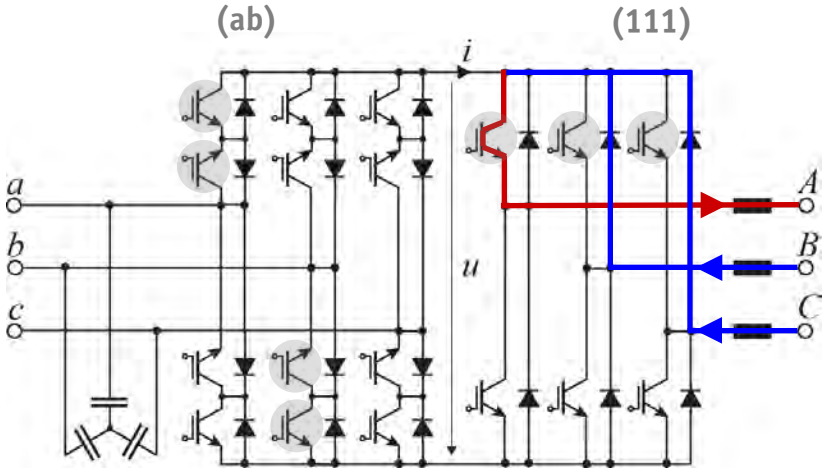


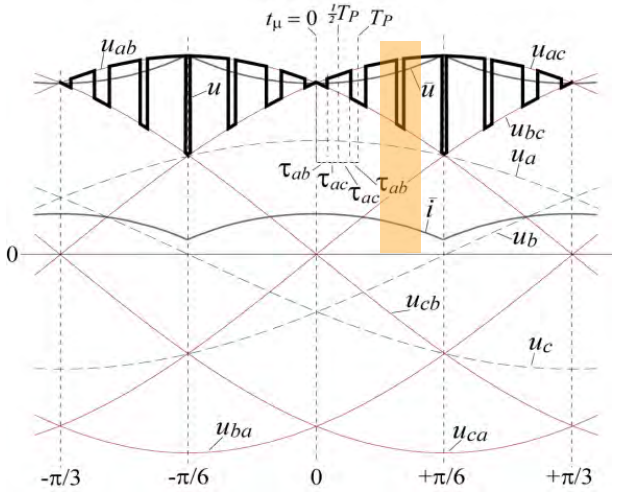
DC link Voltage & Current

PWM Pattern

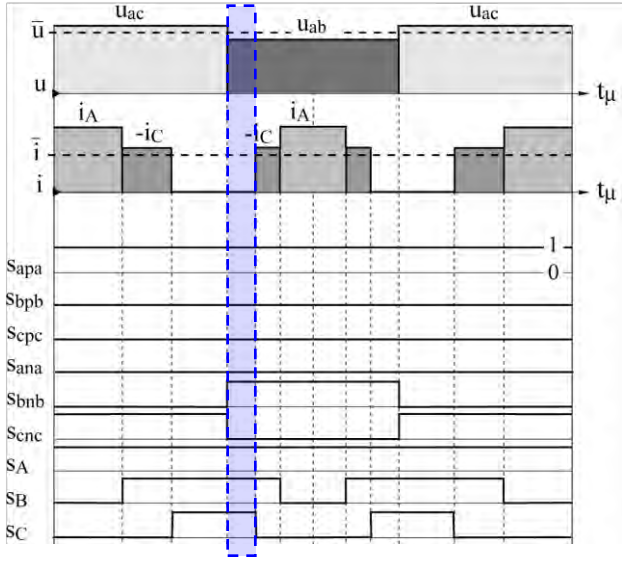
IMC Zero DC-Link Current Commutation (4)

DC-Link Voltage $u = u_{ab}$
DC-Link Current $i = 0$





120°of Mains Period

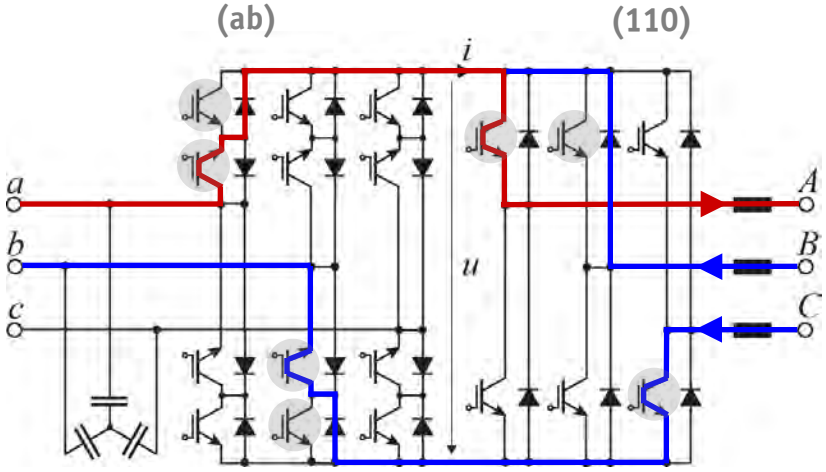


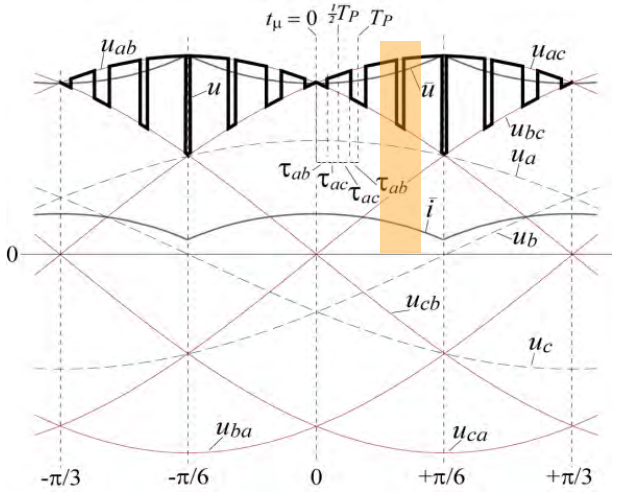
DC link Voltage & Current

PWM Pattern

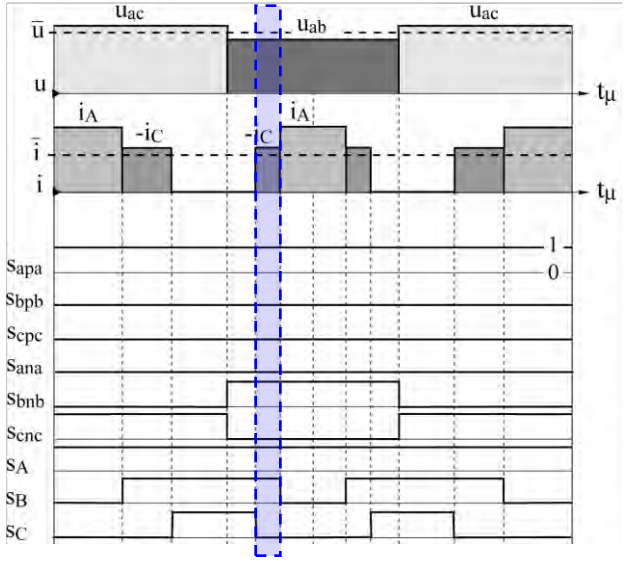
IMC Zero DC-Link Current Commutation (5)

DC-Link Voltage $u = u_{ab}$
DC-Link Current $i = -i_c$





120°of Mains Period

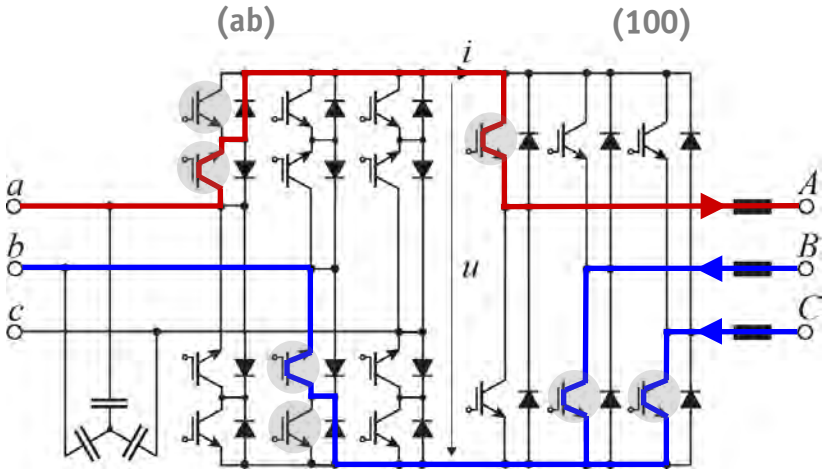


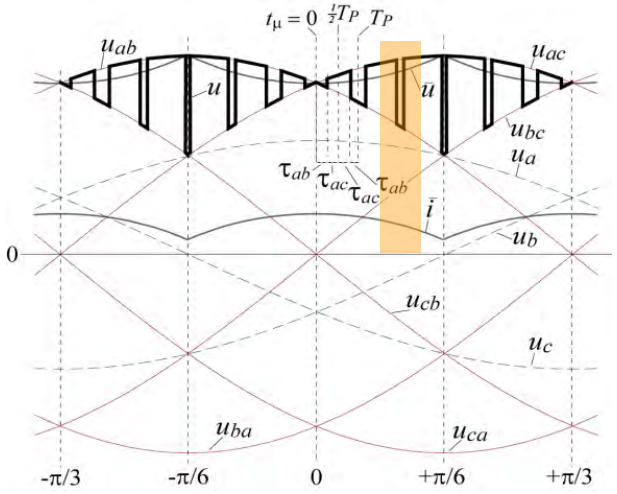
DC link Voltage & Current

PWM Pattern

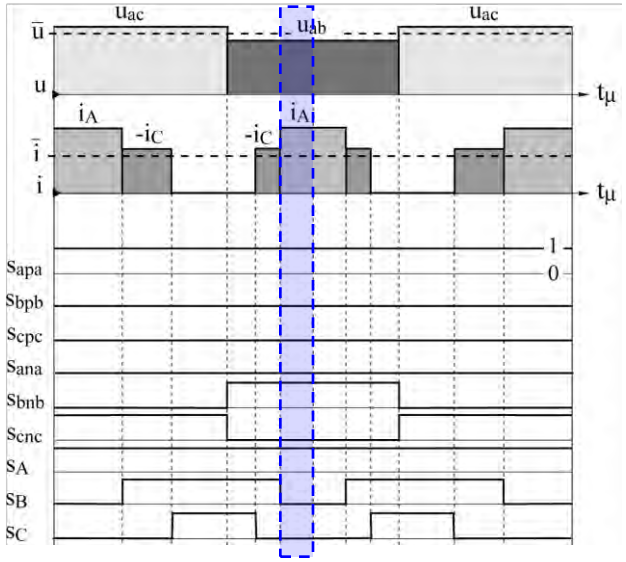
IMC Zero DC-Link Current Commutation (6)

DC-Link Voltage $u = u_{ab}$
DC-Link Current $i = i_A$





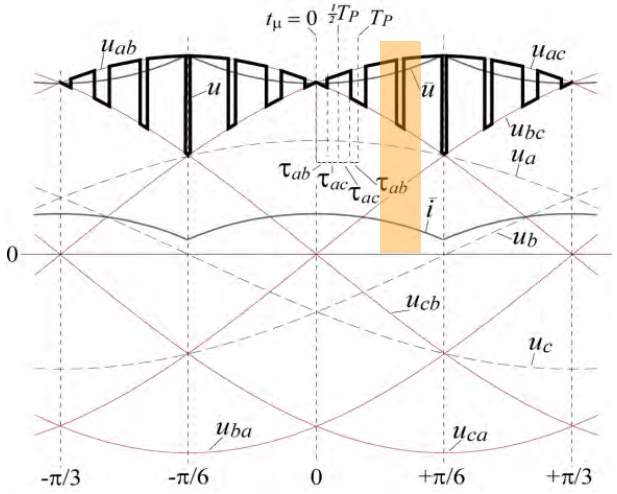
120°of Mains Period



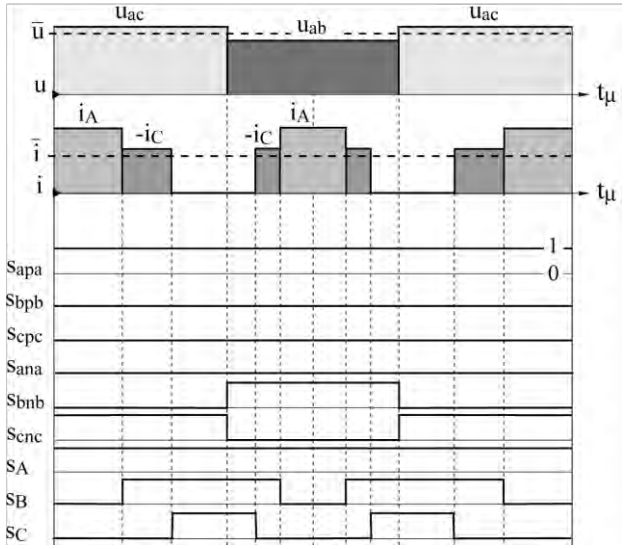
DC link Voltage & Current

PWM Pattern

IMC Zero DC-Link Current Commutation (7)



120°of Mains Period



DC link Voltage & Current

PWM Pattern

Summary

- **Simple and Robust** Modulation Scheme Independent of Commutation Voltage Polarity or Current Flow Direction
- **Negligible Rectifier Stage Switching Losses** Due to Zero Current Commutation

IMC Space Vector Modulation Calculation

Output Voltage Ref. Value

$$\vec{u}_2^* = \hat{U}_2^* e^{j\varphi_{\vec{u}_2^*}} = \hat{U}_2^* e^{j\omega_2^* t}$$

Input Current Ref. Angle $\varphi^*_{\vec{i}_1}$

$$\vec{i}_1 = \hat{I}_1 e^{j\varphi^*_{\vec{i}_1}} \qquad \varphi^*_{\vec{i}_1} = \varphi_{\vec{u}_1} - \Phi_1^*$$

Mains Voltage

$$\vec{u}_1 = \hat{U}_1 e^{j\varphi_{\vec{u}_1}} = \hat{U}_1 e^{j\omega_1 t}$$

Load Behavior

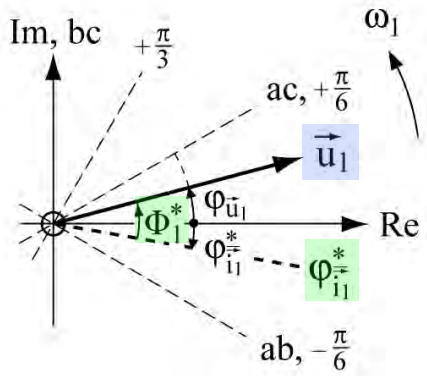
$$\vec{i}_2 = \hat{I}_2 e^{j\varphi_{\vec{i}_2}} = \hat{I}_2 e^{j\left(\varphi_{\vec{u}_2^*} - \Phi_2\right)}$$

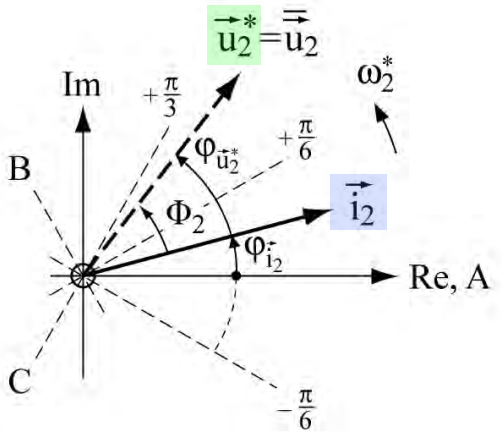
Assumptions

$$\varphi_{\vec{u}_1} \in \left[0, \frac{\pi}{6}\right]$$

$$\varphi_{\vec{u}_2^*} \in \left[0, \frac{\pi}{3}\right]$$

$$\varphi^*_{\vec{i}_1} \in \left[-\frac{\pi}{6}, \frac{\pi}{6}\right]$$





PWM Pattern is Specific for each Combination of Input Current and Output Voltage Sectors

Freewheeling Limited to Output Stage

$$d_{(ab)} + d_{(ac)} = 1$$

Input Current Formation

$$\begin{aligned}
\bar{i}_a &= \left(d_{(ab)} + d_{(ac)}\right) \bar{i} = \bar{i} \\
\bar{i}_b &= -d_{(ab)}\, \bar{i} \\
\bar{i}_c &= -d_{(ac)}\, \bar{i}
\end{aligned}$$

Desired Input Current

$$\begin{aligned}
\bar{i}_a &= \hat{I}_1 \cos \varphi^*_{\vec{i}_1} \\
\bar{i}_b &= \hat{I}_1 \cos \left(\varphi^*_{\vec{i}_1} - \frac{2\pi}{3} \right) \\
\bar{i}_c &= \hat{I}_1 \cos \left(\varphi^*_{\vec{i}_1} + \frac{2\pi}{3} \right)
\end{aligned}$$

Resulting Rectifier Stage Relative On-Times

$$d_{(ab)} = \frac{\sin\left(\frac{\pi}{6} - \varphi^*_{\vec{i}_1}\right)}{\cos \varphi^*_{\vec{i}_1}} \qquad d_{(ac)} = \frac{\sin\left(\frac{\pi}{6} + \varphi^*_{\vec{i}_1}\right)}{\cos \varphi^*_{\vec{i}_1}}$$

Absolute On-Times

$$\tau_{(ab)} = d_{(ab)} \frac{T_P}{2} \qquad \tau_{(ac)} = d_{(ac)} \frac{T_P}{2}$$

Mains Voltage

$$u_a = \hat{U}_1 \cos\left(\varphi_{\vec{u}_1}\right)$$

$$u_b = \hat{U}_1 \cos\left(\varphi_{\vec{u}_1} - \frac{2\pi}{3}\right)$$

$$u_c = \hat{U}_1 \cos\left(\varphi_{\vec{u}_1} + \frac{2\pi}{3}\right)$$

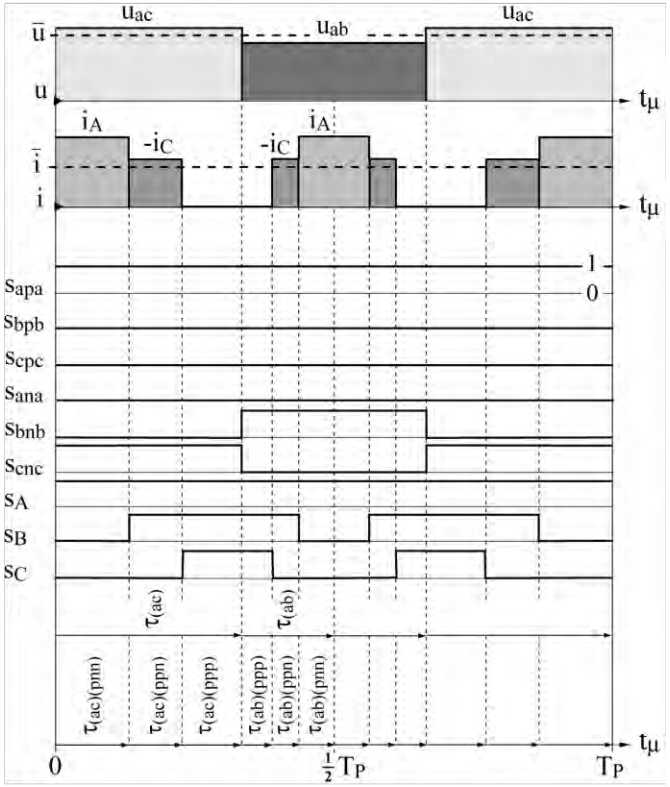
Available DC Link Voltage Values

$$u_{(ab)} = u_{ab} = u_a - u_b = \sqrt{3} \cdot \hat{U}_1 \cos\left(\varphi_{\vec{u}_1} + \frac{\pi}{6}\right)$$

$$u_{(ac)} = u_{ac} = u_a - u_c = \sqrt{3} \cdot \hat{U}_1 \cos\left(\varphi_{\vec{u}_1} - \frac{\pi}{6}\right)$$

Select Identical Duty Cycles of Inverter Switching States (100), (110) in τ_{ac} and τ_{ab} for Maximum Modulation Range

Switch Conducting the Largest Current is Clamped (over π/3-wide Interval)



Voltage Space Vectors Related to Active Inverter Switching States

$$\vec{u}_{2,(pnn)} = \frac{2}{3}u$$

$$\vec{u}_{2,(ppn)} = \frac{2}{3}u\,\mathrm{e}^{j\pi/3}$$

Output Voltage Formation

$$\begin{aligned}\bar{\vec{u}}_2 &= \frac{2/3}{T_P/2}\Big(\delta_{(ac)(pnn)}\tau_{(ac)}u_{ac} + \delta_{(ab)(pnn)}\tau_{(ab)}u_{ab} \\ &\qquad + \delta_{(ac)(ppn)}\tau_{(ac)}u_{ac}\mathrm{e}^{j\pi/3} + \delta_{(ab)(ppn)}\tau_{(ab)}u_{ab}\mathrm{e}^{j\pi/3}\Big) \\ &= \delta_{(pnn)}\frac{2}{3}\left(\frac{\tau_{(ac)}}{T_P/2}u_{ac} + \frac{\tau_{(ab)}}{T_P/2}u_{ab}\right) + \delta_{(ppn)}\frac{2}{3}\left(\frac{\tau_{(ac)}}{T_P/2}u_{ac} + \frac{\tau_{(ab)}}{T_P/2}u_{ab}\right)\mathrm{e}^{j\pi/3} \\ &= \delta_{(pnn)}\frac{2}{3}\left(d_{(ac)}u_{ac} + d_{(ab)}u_{ab}\right) + \delta_{(ppn)}\frac{2}{3}\left(d_{(ac)}u_{ac} + d_{(ab)}u_{ab}\right)\mathrm{e}^{j\pi/3}\end{aligned}$$

Local DC-link Voltage Average Value

$$\bar{u} = d_{(ac)}u_{ac} + d_{(ab)}u_{ab}$$

$$\bar{\vec{u}}_2 = \delta_{(pnn)}\frac{2}{3}\bar{u} + \delta_{(ppn)}\frac{2}{3}\bar{u}\,\mathrm{e}^{j\pi/3} \qquad \bar{\vec{u}}_2 = \vec{u}_2^{\,*}$$

Calculation of the Inverter Active Switching State On-Times can be directly based on $\bar{u}$!

DC-Link Voltage Local Average Value

$$\overline{u} = \frac{3}{2} \cdot \hat{U}_1 \frac{\cos\left(\varphi_{\vec{u}_1} - \varphi^*_{\vec{i}_1}\right)}{\cos\left(\varphi^*_{\vec{i}_1}\right)} = \frac{3}{2} \cdot \hat{U}_1 \frac{\cos\left(\Phi^*_1\right)}{\cos\left(\varphi^*_{\vec{i}_1}\right)}$$

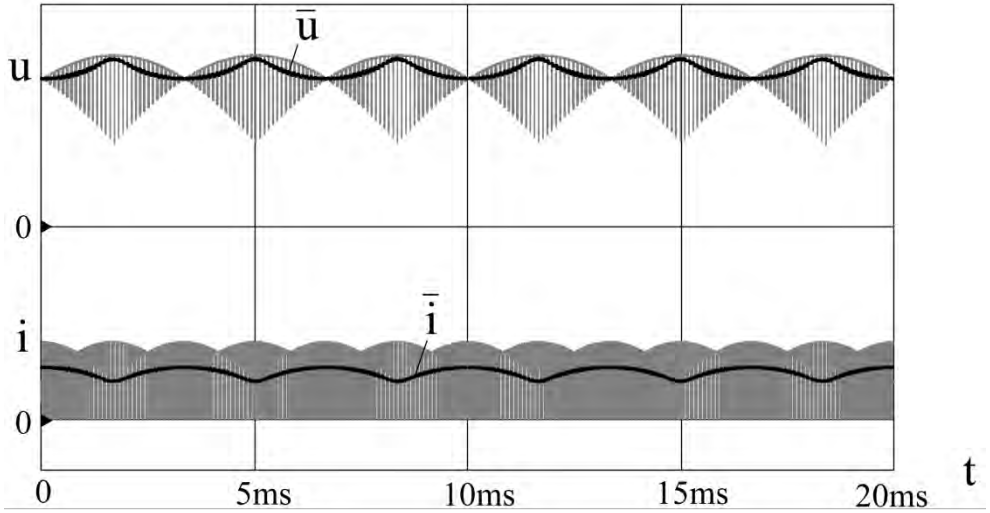
Minimum of DC-Link Voltage Local Average Value

$$\overline{u}_{\min} = \frac{3}{2} \hat{U}_1 \cos \Phi^*_1$$

Resulting IMC Output Voltage Limit

$$\hat{U}^*_{2,\max} \leq \frac{\sqrt{3}}{2} \cdot \hat{U}_1 \cos \Phi^*_1$$

Simulation of DC-Link Voltage and Current Time Behavior



Resulting Inverter Stage Relative On-Times

$$\delta_{(ppn)} = \frac{\sqrt{3}}{2} \cdot \frac{\hat{U}_2^*}{\overline{u}/2} \sin\left(\varphi_{\vec{u}_2^*}\right)$$

$$\delta_{(pnn)} = \frac{\sqrt{3}}{2} \cdot \frac{\hat{U}_2^*}{\overline{u}/2} \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right)$$

Resulting Inverter Stage Absolute On-Times

$$\tau_{(ac)(pnn)} = \frac{1}{2} T_P d_{(ac)} \delta_{(pnn)} = \frac{1}{2} T_P \frac{2}{\sqrt{3}} \frac{\hat{U}_2^*}{\hat{U}_1} \frac{1}{\cos \Phi_1^*} \sin\left(\frac{\pi}{6} + \varphi_{\vec{i}_1}^*\right) \cos\left(\varphi_{\vec{u}_2^*} + \frac{\pi}{6}\right)$$

$$\tau_{(ac)(ppn)} = \frac{1}{2} T_P d_{(ac)} \delta_{(ppn)} = \frac{1}{2} T_P \frac{2}{\sqrt{3}} \frac{\hat{U}_2^*}{\hat{U}_1} \frac{1}{\cos \Phi_1^*} \sin\left(\frac{\pi}{6} + \varphi_{\vec{i}_1}^*\right) \sin\left(\varphi_{\vec{u}_2^*}\right)$$

DC-link Voltage Local Average Value

$$\overline{i}_{(ac)} = \frac{1}{\tau_{(ac)}} \left(i_A \delta_{(pnn)} \tau_{(ac)} - i_C \delta_{(ppn)} \tau_{(ac)} \right) = i_A \delta_{(pnn)} - i_C \delta_{(ppn)}$$

$$\overline{i}_{(ab)} = \frac{1}{\tau_{(ab)}} \left(i_A \delta_{(pnn)} \tau_{(ab)} - i_C \delta_{(ppn)} \tau_{(ab)} \right) = i_A \delta_{(pnn)} - i_C \delta_{(ppn)}$$

Equal DC-link Current Local Average Values for Inverter Active Switching States

$$\overline{i} = \overline{i}_{(ac)} = \overline{i}_{(ab)} = \hat{I}_2 \frac{\hat{U}_2^*}{\hat{U}_1} \frac{\cos \Phi_2}{\cos \Phi_1^*} \cos \varphi^*_{\substack{\rightarrow \\ i_1}}$$

Local Average Value of Input Current in *a*

$$\overline{i}_a = \overline{i} = \hat{I}_1 \cos \varphi^*_{\substack{\rightarrow \\ i_1}}$$

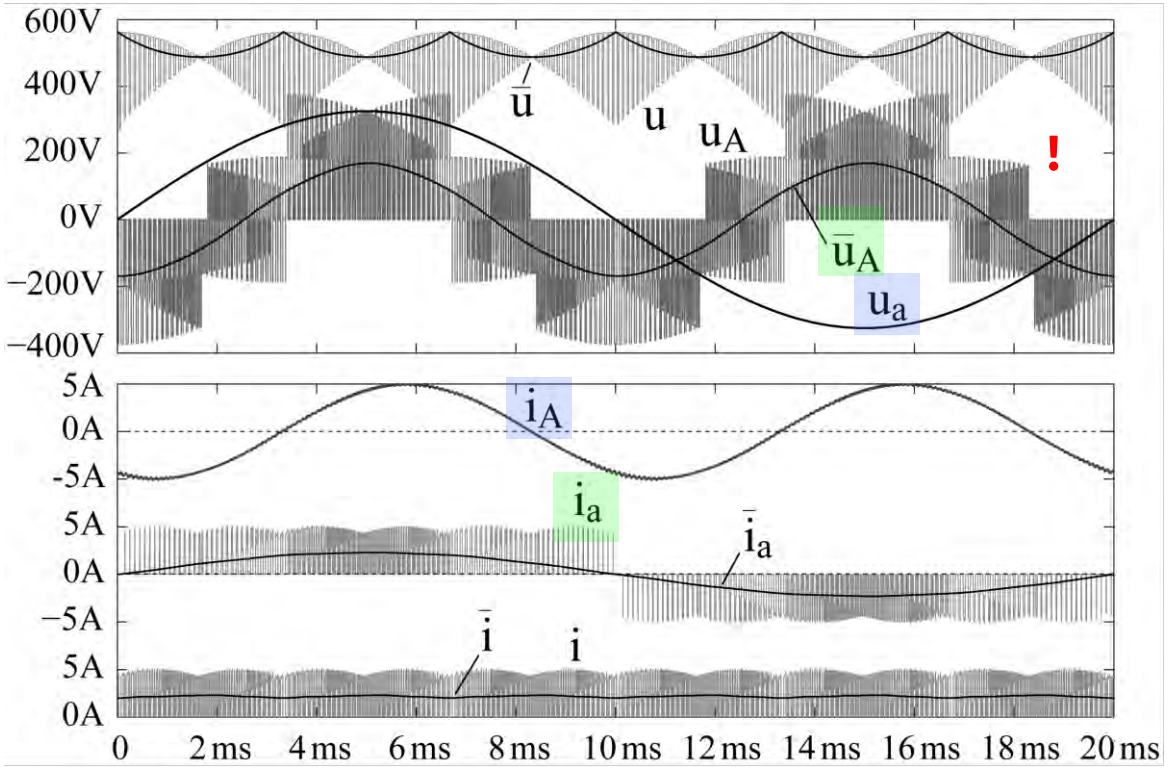
Resulting Input Phase Current Amplitude

$$\hat{I}_1 = \hat{I}_2 \frac{\hat{U}_2^*}{\hat{U}_1} \frac{\cos \Phi_2}{\cos \Phi_1^*}$$

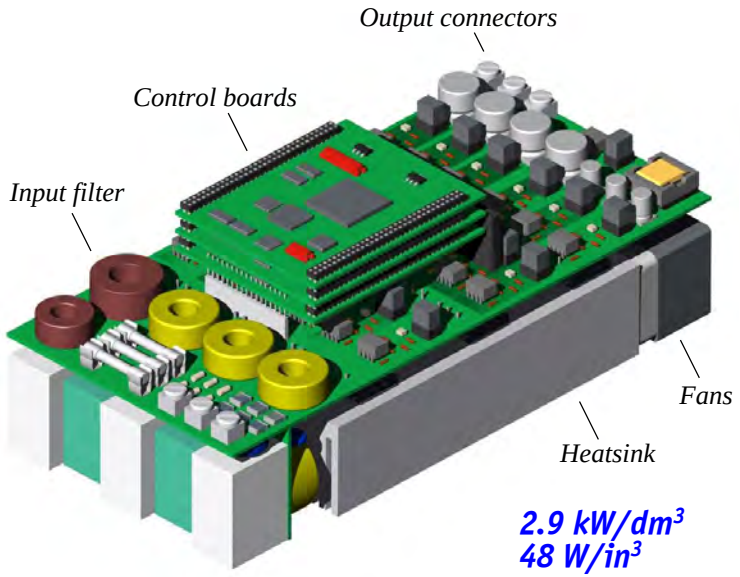
Power Balance of Input and Output Side

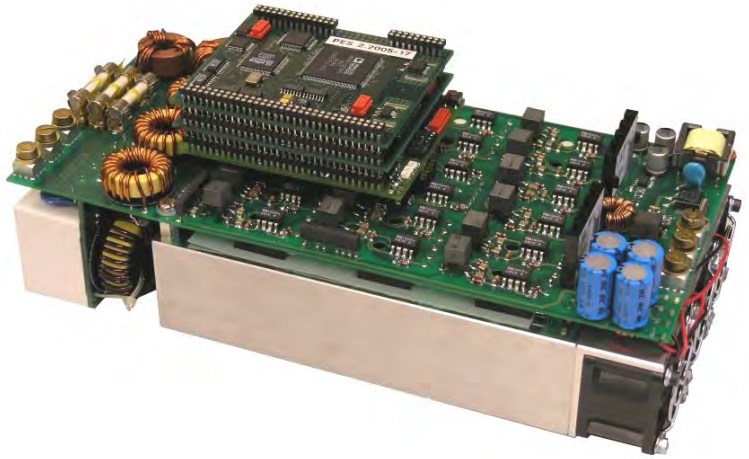
$$\overline{p} = P = \overline{u}\,\overline{i} = \frac{3}{2} \hat{U}_1 \hat{I}_1 \cos \Phi_1^* = \frac{3}{2} \hat{U}_2^* \hat{I}_2 \cos \Phi_2$$

IMC Simulation Results



RB-IGBT IMC Experimental Results (1)





2.9 kW/dm³
48 W/in³

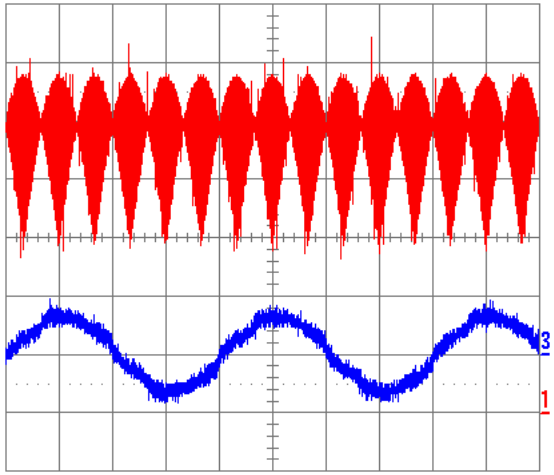
Efficiency 95%

Input RMS voltage	*400V*
Output Power	*6.8 kVA*
Rectifier Switching Frequency	*12.5 kHz*
Inverter Switching Frequency	*25 kHz*

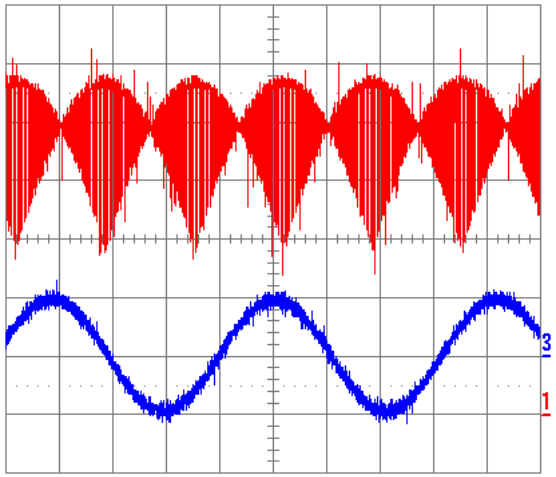
RB-IGBT IMC Experimental Results (2)

U_{12} = 400V
P_{out} = 1.5 kW
f_{out} = 120 Hz
f_S = 12.5 kHz / 25kHz

DC Link Voltage



Input Current

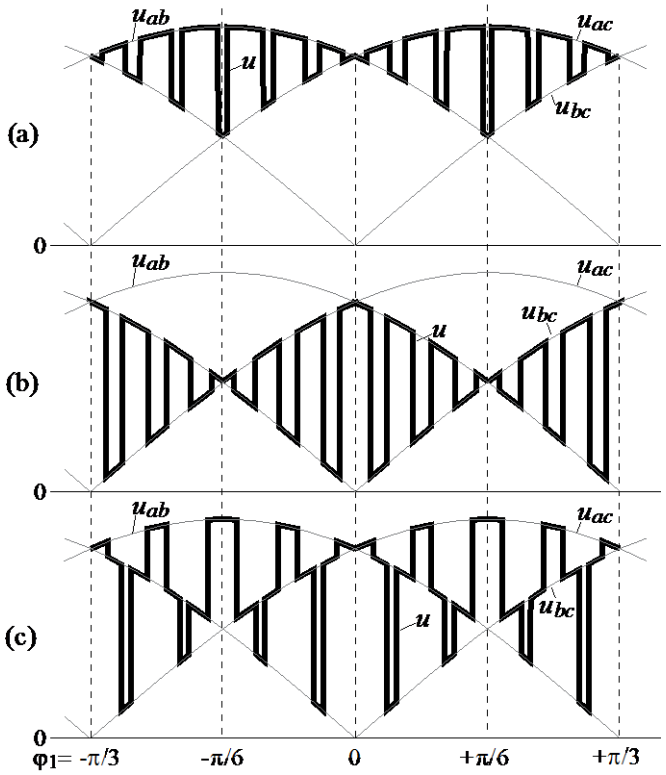


Output Current

100 V/div
5A/div

Alternative Modulation Schemes

► LV and Three-Level Medium Voltage Modulation



High Output Voltage Modulation (HVM)

$$\hat{U}_2 = 0 \ldots \frac{\sqrt{3}}{2} \cdot \hat{U}_1$$

Low Output Voltage Modulation (LVM)

$$\hat{U}_2 = 0 \ldots \frac{1}{2} \cdot \hat{U}_1$$

Three-Level Modulation

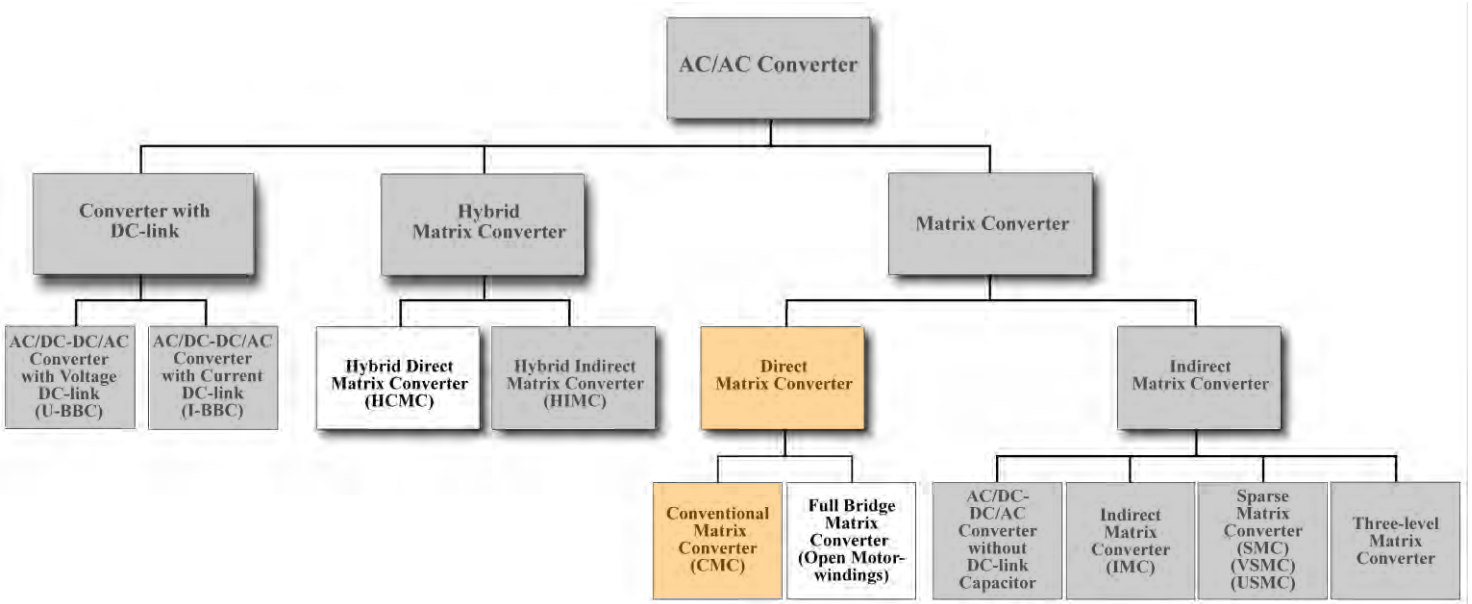
$$\hat{U}_2 = \frac{1}{2} \ldots \frac{\sqrt{3}}{2} \cdot \hat{U}_1$$

Weighted Combination of HVM and LVM

Conventional Matrix Converter - CMC

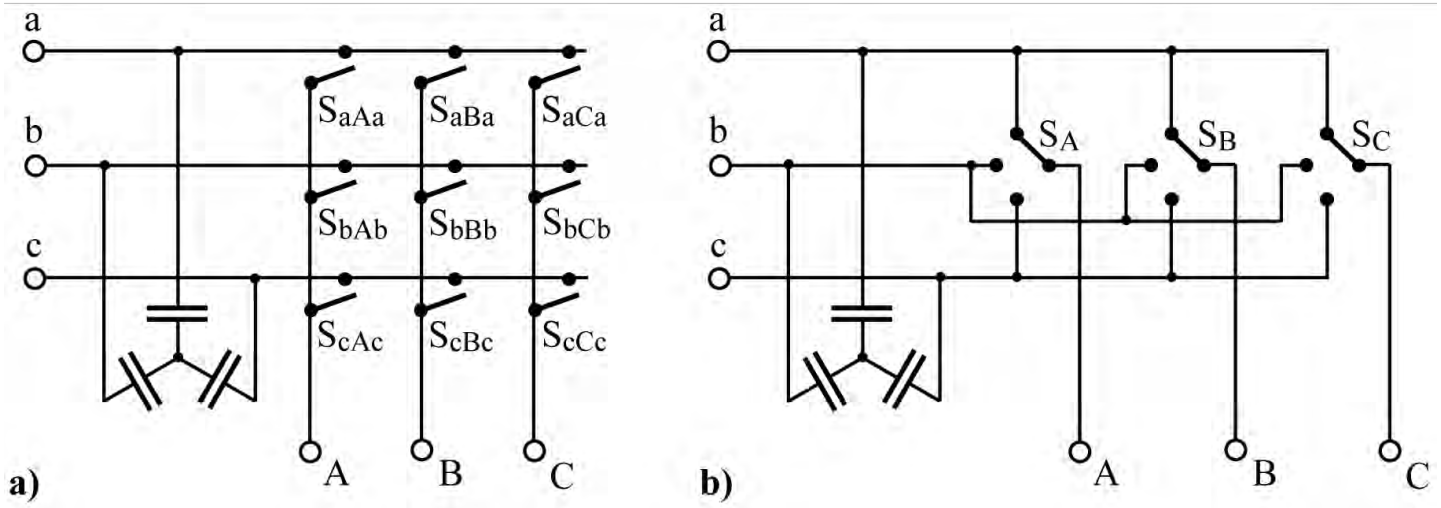
Modulation
Multi-Step Commutation

Classification of Three-Phase AC-AC Converters



- *Conventional Matrix Converter*

Conventional Matrix Converter – CMC



- ***Quasi Three-Level Characteristic***

CMC Classification of Switching States

Group I

Freewheeling States

(aaa) (bbb) (ccc)

Group II

Generating Stationary Output Voltage and Input Current Space Vectors

(cca)	(ccb)	(aab)	$u_{AB} = 0$
(aac)	(bbc)	(bba)	
(acc)	(bcc)	(baa)	$u_{BC} = 0$
(caa)	(cbb)	(abb)	
(cac)	(cbc)	(aba)	$u_{CA} = 0$
(aca)	(bcb)	(bab)	

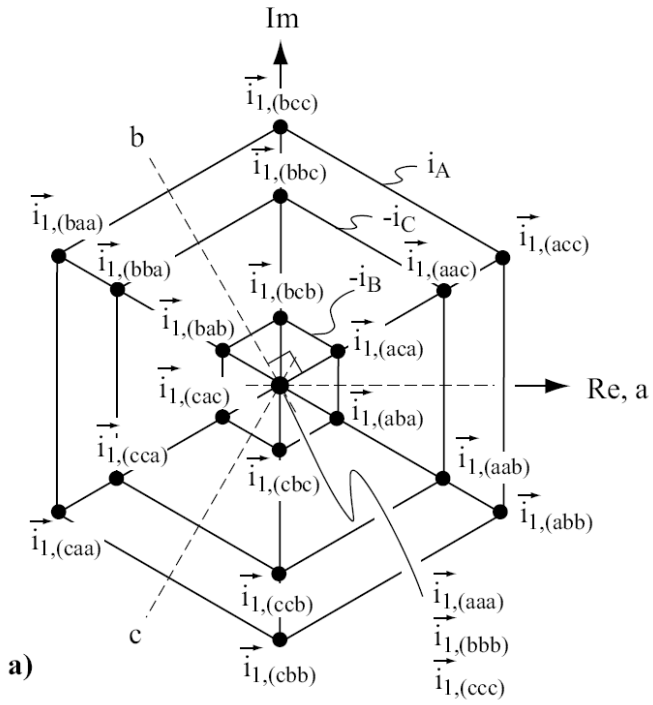
Group III

Generating Rotating Space Vectors

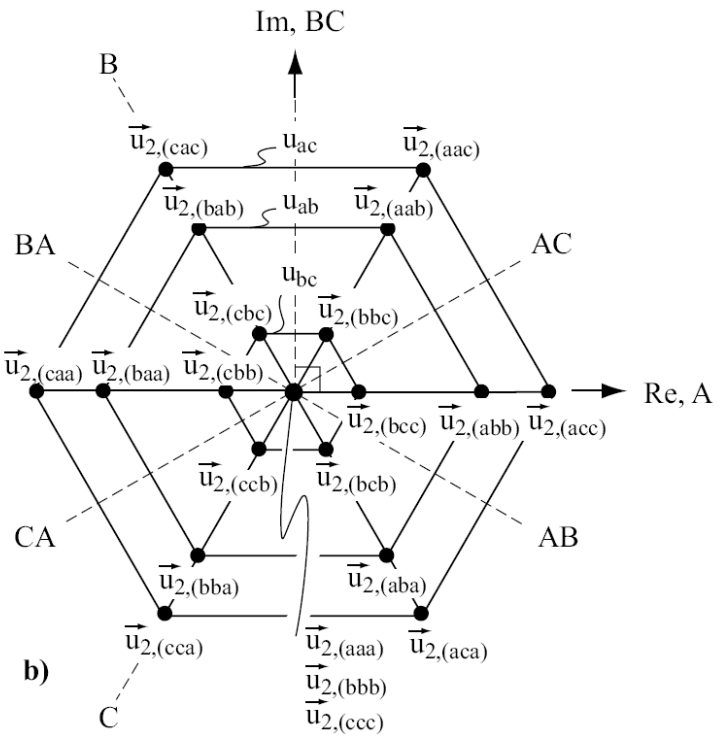
(abc) (cab) (bca) *Positive Sequence*

(acb) (cba) (bac) *Negative Sequence*

CMC Stationary Space Vectors



Input Current Space Vectors



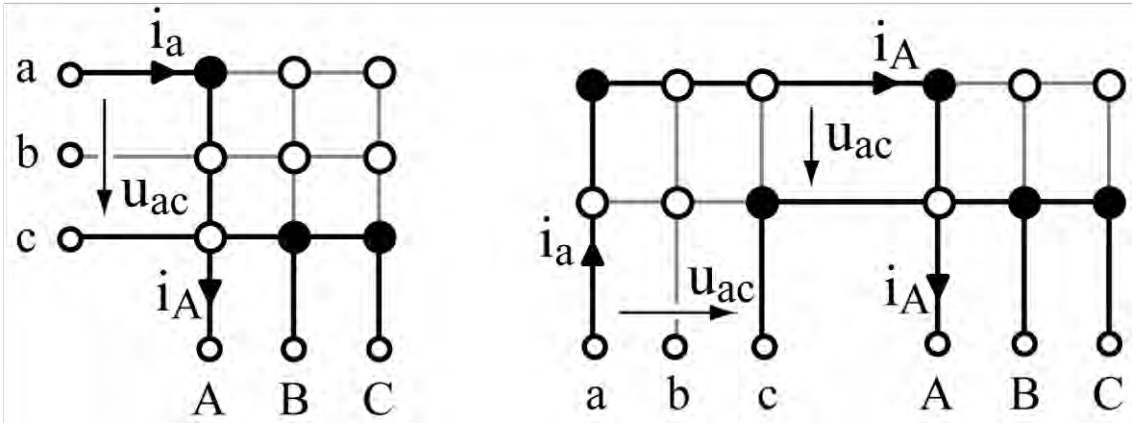
Output Voltage Space Vectors

CMC/IMC Relation (1)

Correspondence of Switching States

$$\vec{u}_{2,(acc)} = \vec{u}_{2,(ac)(pnn)}$$

$$\vec{i}_{1,(acc)} = \vec{i}_{1,(ac)(pnn)}$$



- *Indirect Space Vector Modulation*

P. Ziogas [12]
L. Huber / D. Borojevic

CMC/IMC Relation (2)

$\varphi_{\vec{u}_2^*} \in [0, \pi/6]$

Correspondence of Switching States

- **IMC**

$$\ldots|_{t_\mu = 0} \quad (ac)(pnn) - (ac)(ppn) - (ac)(ppp) - (ab)(ppp) - (ab)(ppn) - (ab)(pnn)|_{t_\mu = T_P/2}$$
$$(ab)(pnn) - (ab)(ppn) - (ab)(ppp) - (ac)(ppp) - (ac)(ppn) - (ac)(pnn)|_{t_\mu = T_P} \quad \ldots$$

- **CMC**

$$\ldots|_{t_\mu = 0} \quad (acc) - (aac) - (aaa) - (aaa) - (aab) - (abb)|_{t_\mu = T_P/2}$$
$$(abb) - (aab) - (aaa) - (aaa) - (aac) - (acc)|_{t_\mu = T_P} \quad \ldots$$

$\varphi_{\vec{u}_2^*} \in [\pi/6, \pi/3]$

- **IMC**

$$\ldots|_{t_\mu = 0} \quad (ac)(ppn) - (ac)(pnn) - (ac)(nnn) - (ab)(nnn) - (ab)(pnn) - (ab)(ppn)|_{t_\mu = T_P/2}$$
$$(ab)(ppn) - (ab)(pnn) - (ab)(nnn) - (ac)(nnn) - (ac)(pnn) - (ac)(ppn)|_{t_\mu = T_P} \quad \ldots$$

- **CMC**

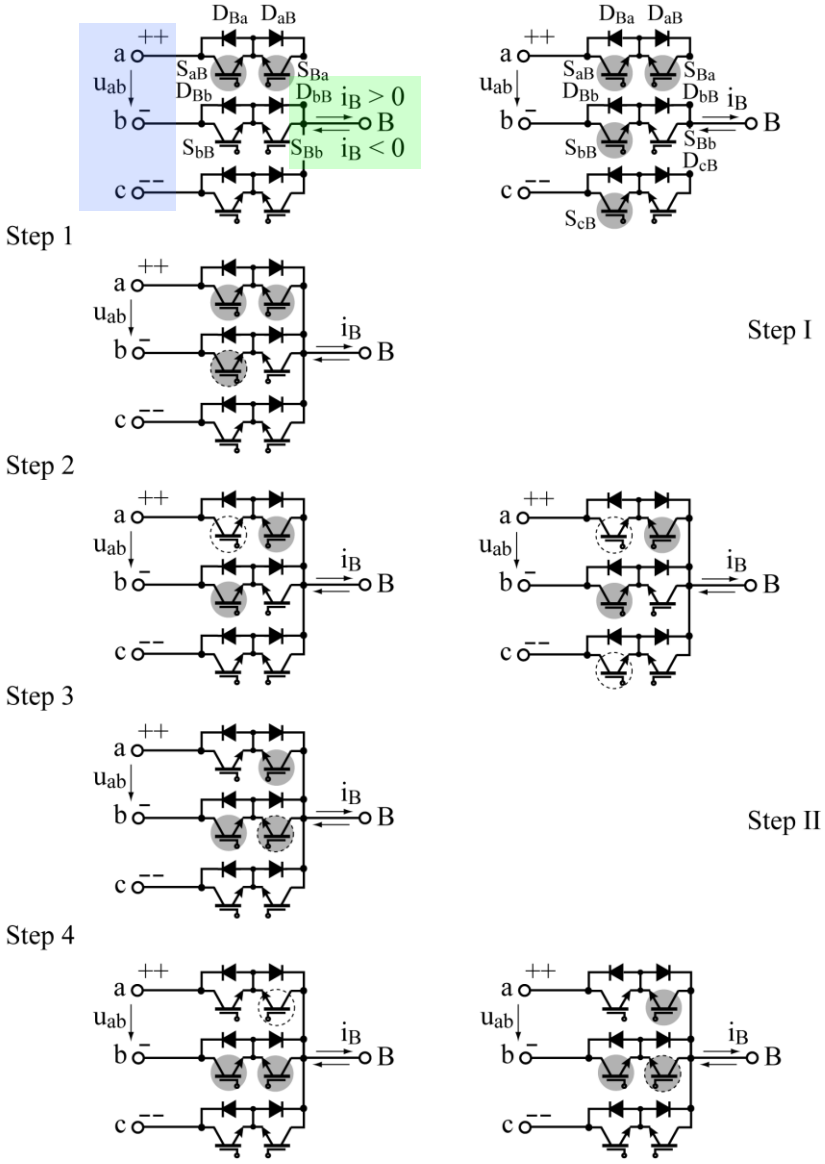
$$\ldots|_{t_\mu = 0} \quad (aac) - (acc) - (ccc) - (bbb) - (abb) - (aab)|_{t_\mu = T_P/2}$$
$$(aab) - (abb) - (bbb) - (ccc) - (acc) - (aac)|_{t_\mu = T_P} \quad \ldots$$

CMC Multi-Step Commutation

J. Oyama / T. Lipo
N. Burany
P. Wheeler
W. Hofmann

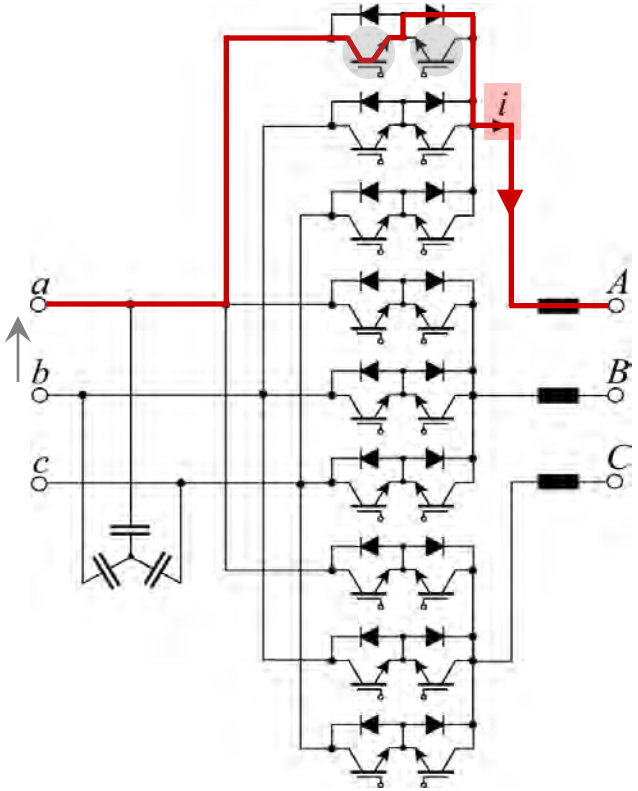
Example: *u*-Dependent Commutation

- *Four-Step Commutation*
- *Two-Step Commutation*



4-Step Commutation of CMC (1)

Example: *i*-Dependent Commutation



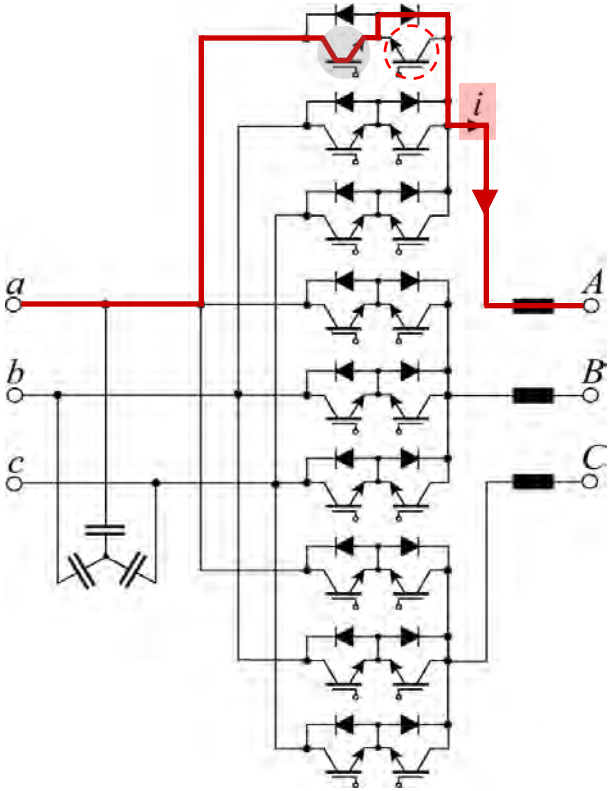
Constraints

- **No Short Circuit of Mains Phases**
- **No Interruption of Load Current**

Assumption: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

4-Step Commutation of CMC (2)

1st Step: Off



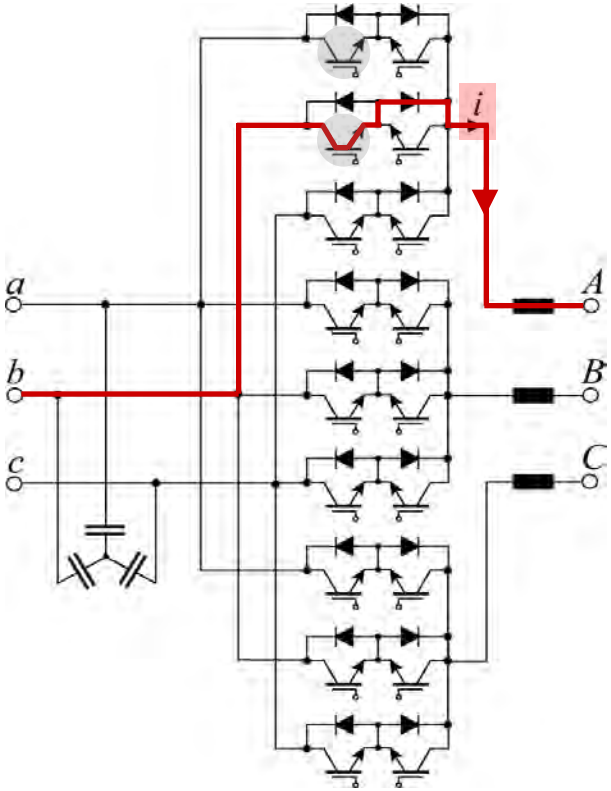
Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

4-Step Commutation of CMC (3)

1st Step: Off
2nd Step: On



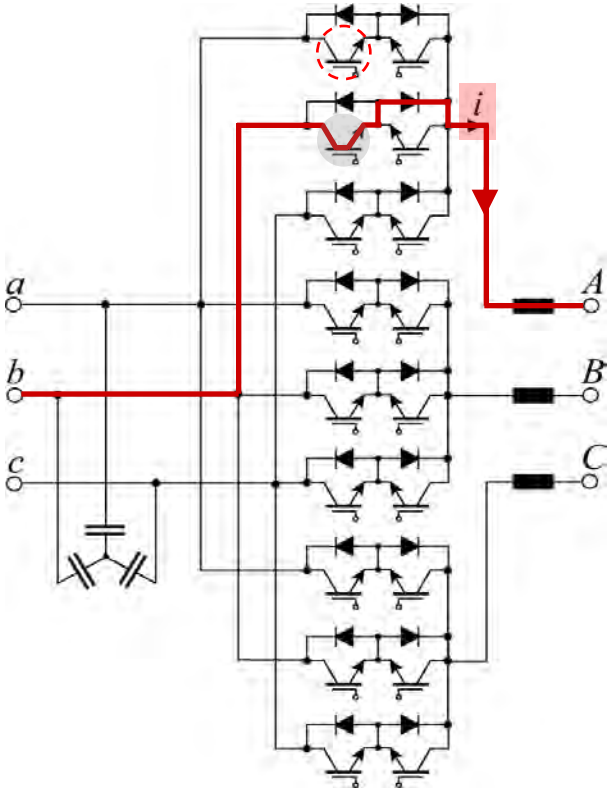
Constraints

- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

4-Step Commutation of CMC (4)

1st Step: Off
2nd Step: On
3rd Step: Off



Constraints

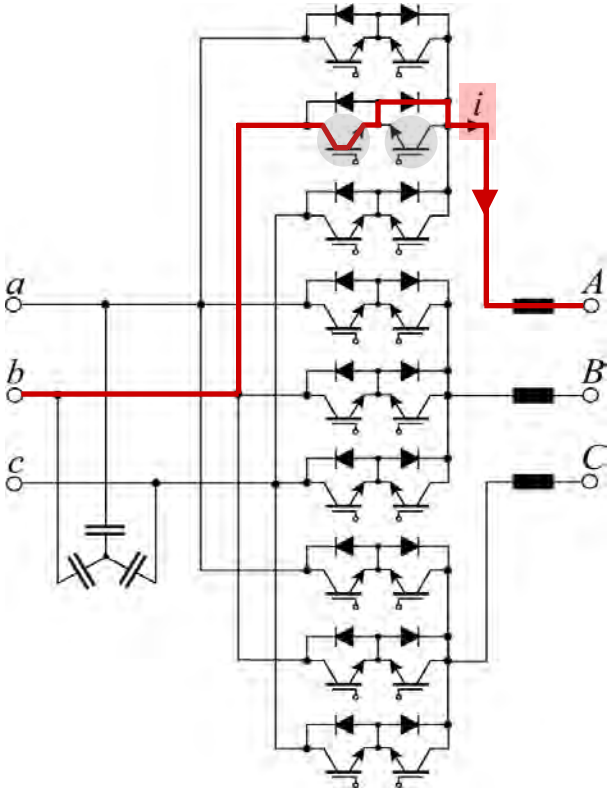
- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

4-Step Commutation of CMC (5)

1st Step: Off
2nd Step: On
3rd Step: Off
4th Step: On

Sequence Depends on Direction of Output Current !

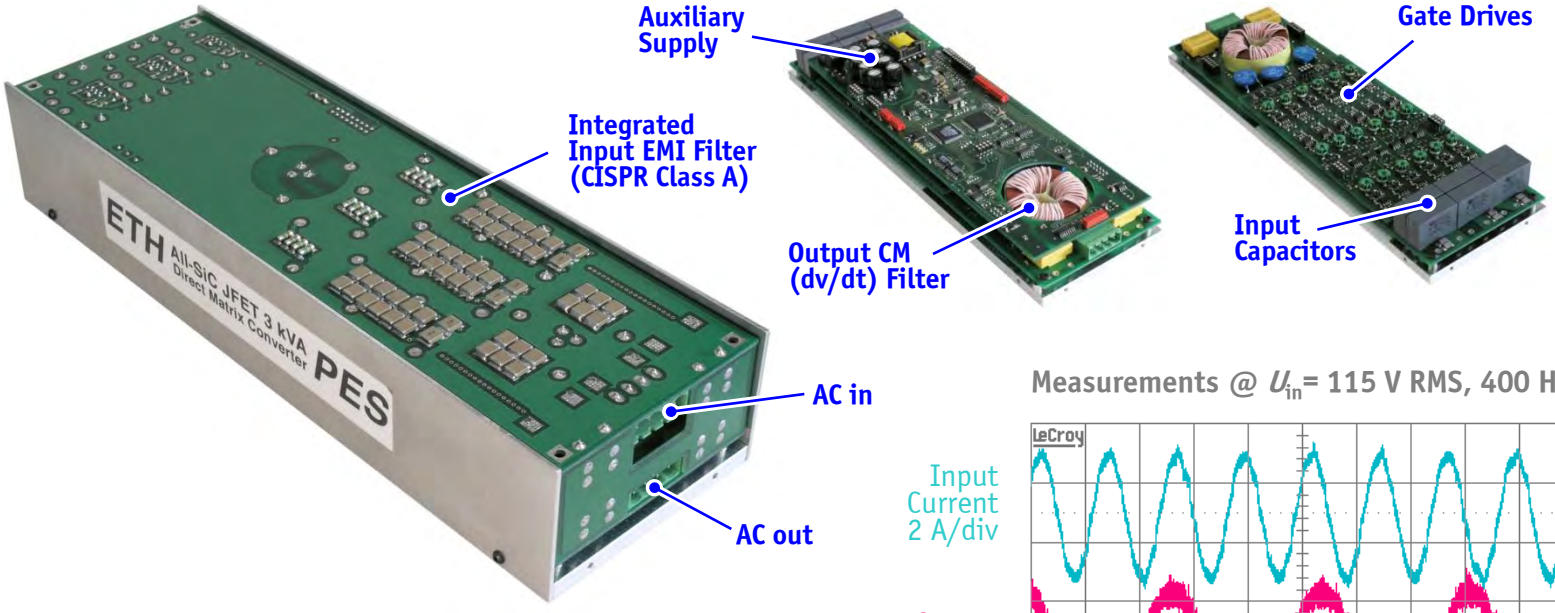


Constraints

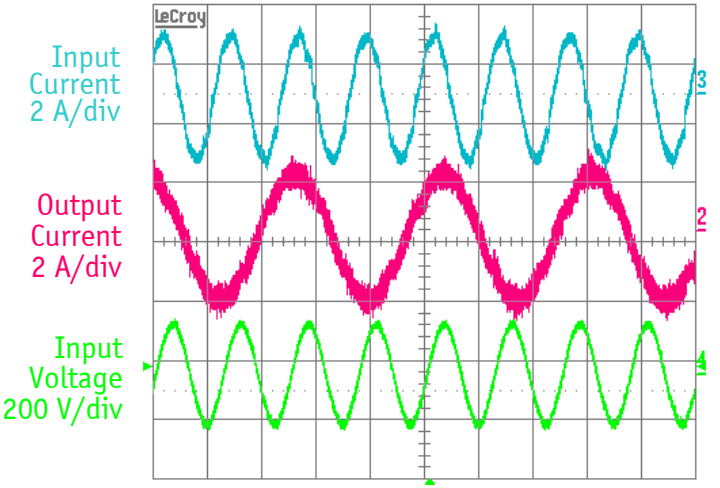
- No Short Circuit of Mains Phases
- No Interruption of Load Current

Assumption: $i > 0$, $u_{ab} < 0$, $aA \rightarrow bA$

All-SiC JFET Conventional direct Matrix Converter



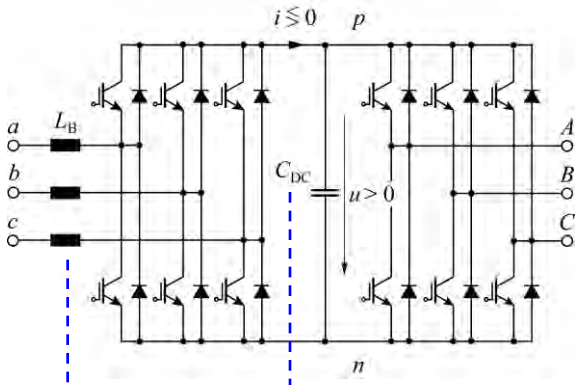
Measurements @ U_{in} = 115 V RMS, 400 Hz



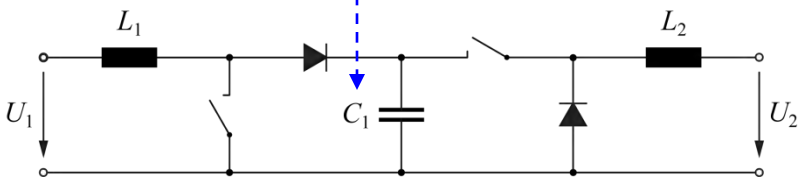
- P_{out} = 3 kVA, η = 93.1% (at 200 kHz)
- $f_{S,nom}$ = 144 kHz ($f_{S,design}$ = 200 kHz)
- 3 kVA/dm³ (50W/in³) with 1200 V/6 A SiC JFET
- ≈ 8 kVA/dm³ (135W/in³) with 1200 V/ 20 A SiC JFET
- 273 x 82 x 47mm³ = 1.05 dm³ (64 in³)

Control Properties of AC-AC Converters (1)

Voltage DC-Link B2B Conv. (V-BBC)

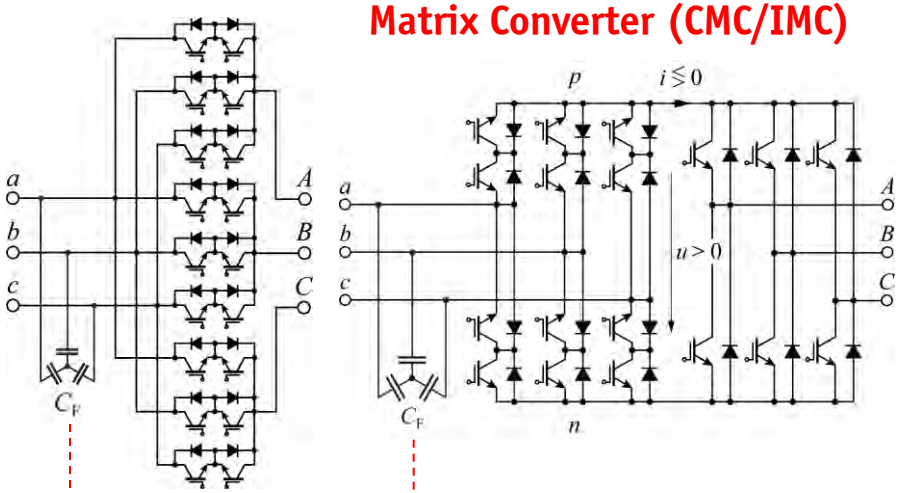


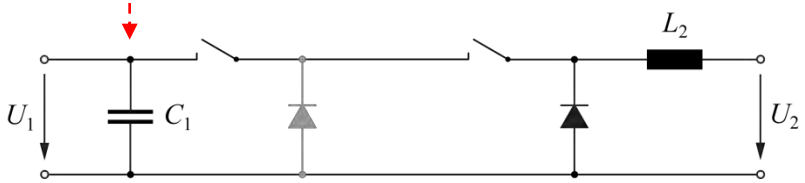
DC/DC Control Equiv. Circ.



- Boost-Buck-Type Converter
- Max. Output Voltage can be Maintained during Low Mains Condition

Matrix Converter (CMC/IMC)



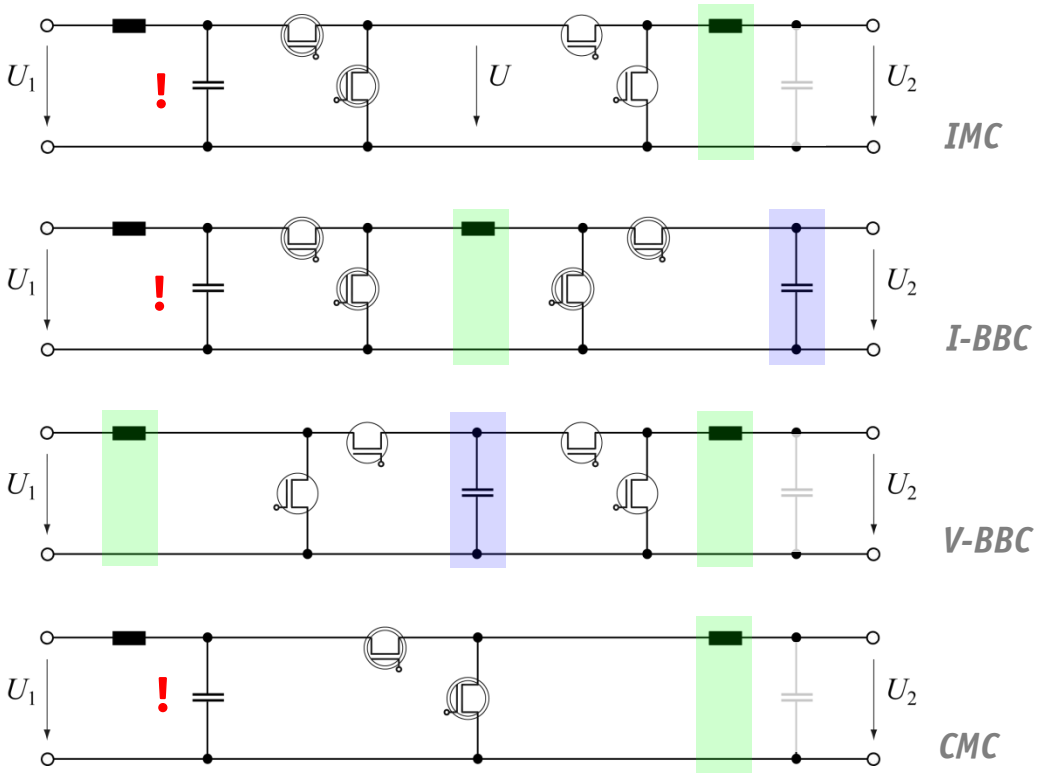


- Buck-Type Converter
- Maximum Output Voltage is Limited by Actual Input Voltage $\hat{U}_2 = 0.866 \cdot \hat{U}_1$

Control Properties of AC-AC Converters (2)

DC-DC Equivalent Circuits

! *Uncontrolled Input Filter*



Control Properties of AC-AC Converters (3)

■ Voltage DC-Link B2B Converter (V-BBC)

- ▶ Input Current (in Phase with Input Voltage)
- ▶ DC-Link Voltage

} 2 Cascaded Control Loops

- ▶ Output Current (Torque and Speed of the Motor)

} 2 Cascaded Control loops

■ Matrix Converter (CMC / IMC)

- ▶ Output Current (Torque and Speed of the Motor)

} 2 Cascaded Control Loops

- ▶ Optional: Input Current (Formation of Input Current still Depends on the Impressed Output Current)

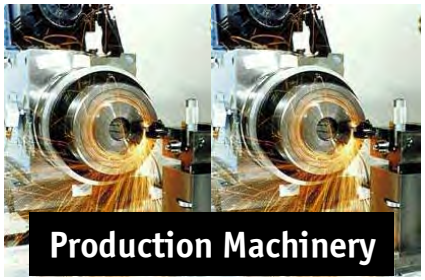
Comparative Evaluation

DC Link Converters
Matrix Converters

Application Areas of Three-Phase PWM Converters

Bidirectional Power Flow

Unidirectional Power Flow

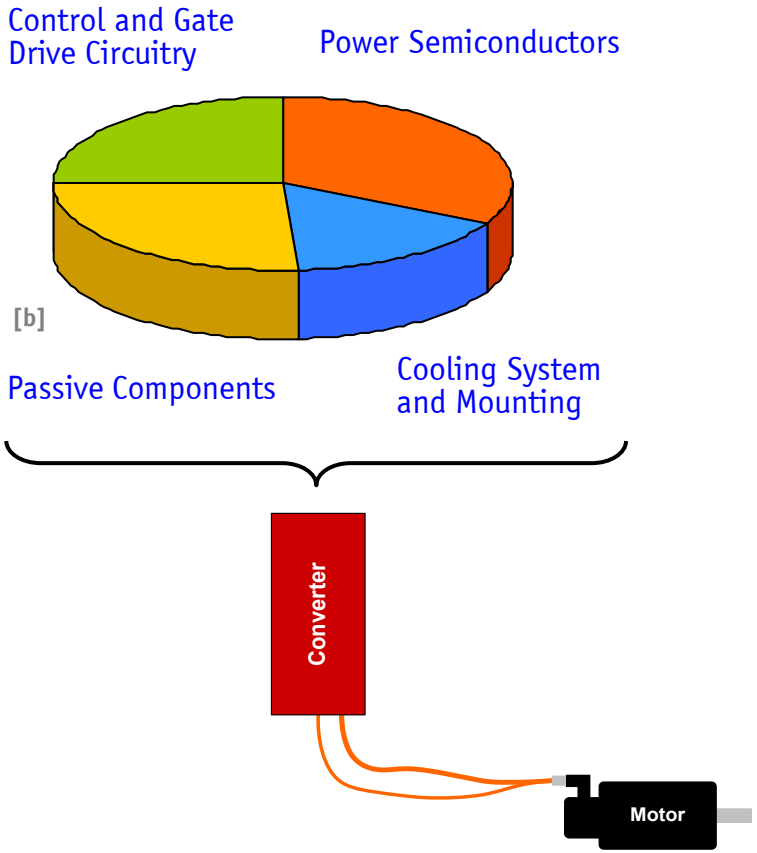


60% of Worldwide Ind. Energy Used by Electric Motor Drives! [a]

[a] "Study on Worldwide Energy Consumption", ECPE Workshop, 2008

Motivation

▶ Cost Allocation of VFD Converters



▶ Status Quo ⇒ Motivation

- Holistic Converter System Comparisons are (still) Rarely Found
- Comprehensive Comparisons Involves a Multi-Domain Converter Design
- Voltage-Source-Type Converter Topologies are Widely Used

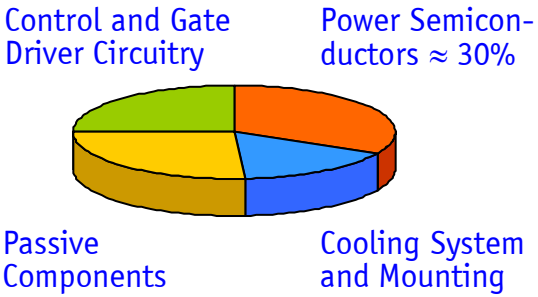
▶ Focus of the Investigation

- Bidirectional Three-Phase AC/DC/AC and AC/AC Converters
- Low Voltage Drives
- Power Level from 1 kVA to few 10 kVA

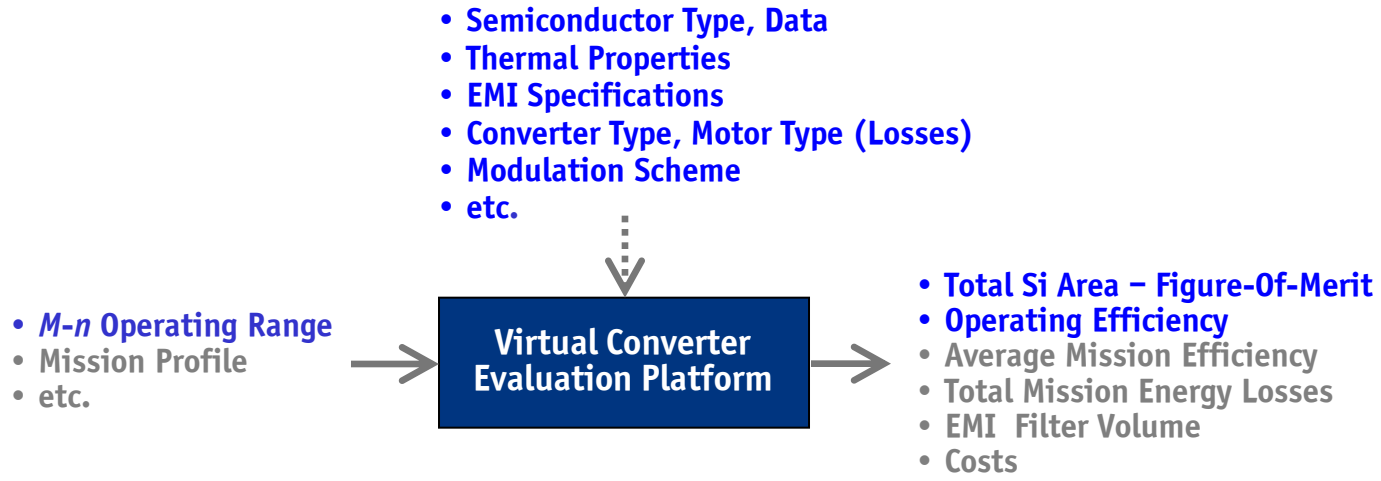
[b]: Based on "ECPE Roadmap on Power Electronics, 2008"

Comparative Evaluation – Virtual Converter Evaluation Platform

- **Define Application / Mission Profile**
  - ***M-n* Operating Rage (Continuous / Overload Requirement)**
  - **Torque at Standstill**
  - **Motor Type**
  - **etc.**

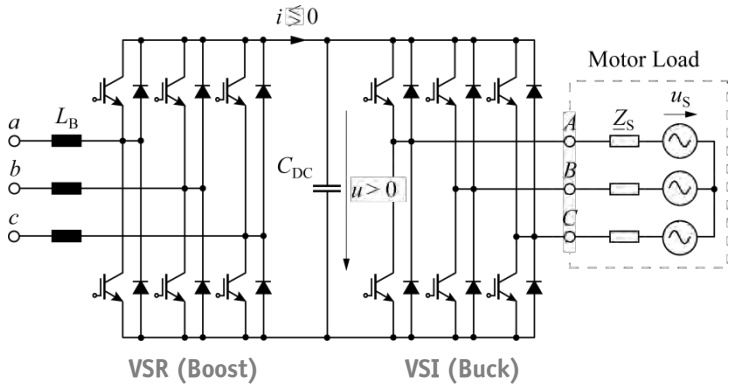


- **Compare Required Total Silicon Area (e.g. for T_J< 150°C, T_C= 95°C)**
  - **Guarantee Optimal Partitioning of Si Area between IGBTs and Diodes**

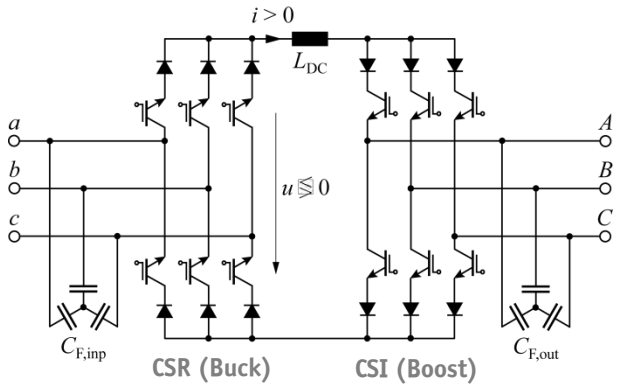


Considered Converter Topologies – V-BBC, I-BBC, IMC, and CMC

With Intermediate Energy Storage

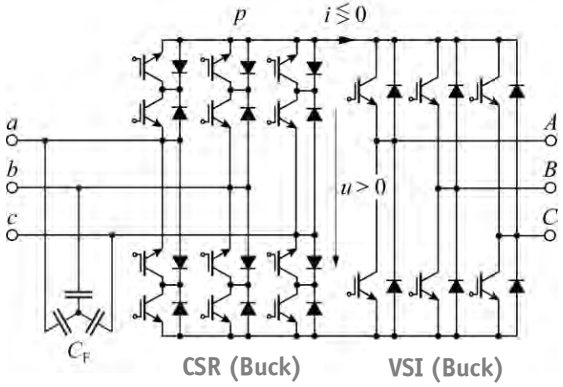


Voltage Source Back-to-Back Converter (V-BBC)
"State-of-the-Art" Converter System



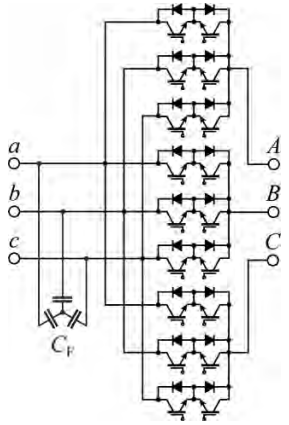
Current Source Back-to-Back Converter (I-BBC)

Without Intermediate Energy Storage



Indirect Matrix Converter (IMC)

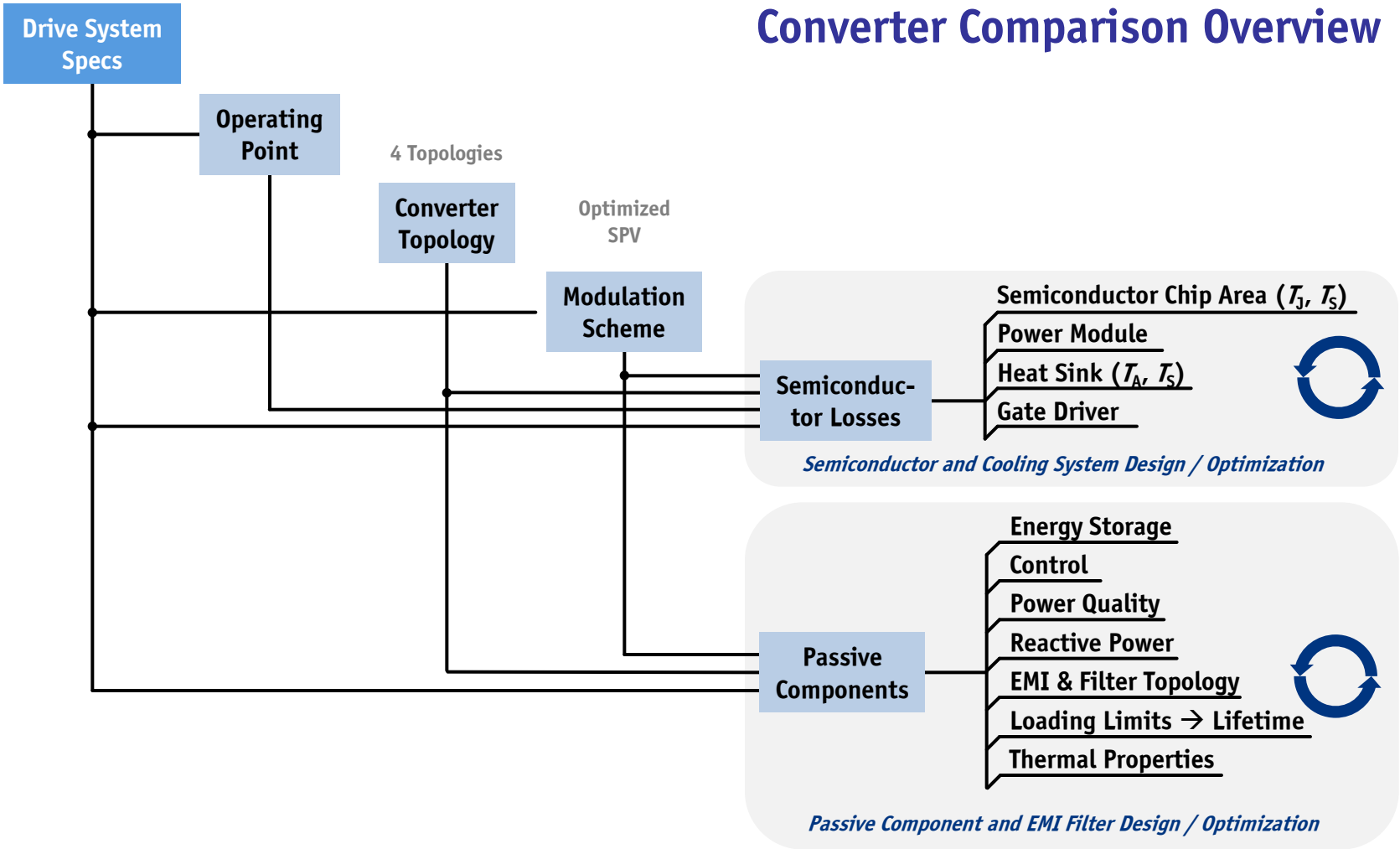
$U_{2,max} = 0.866\ U_1$



$U_{2,max} = 0.866\ U_1$

Conventional (Direct) Matrix Converter (CMC)

Converter Comparison Overview



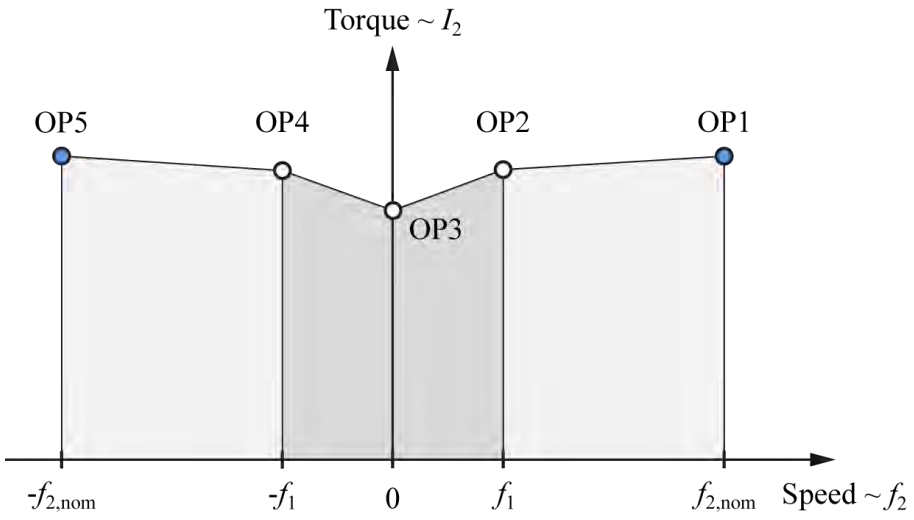
Comparative Evaluation (1) – Specifications and Operating Points

Main Converter Specifications

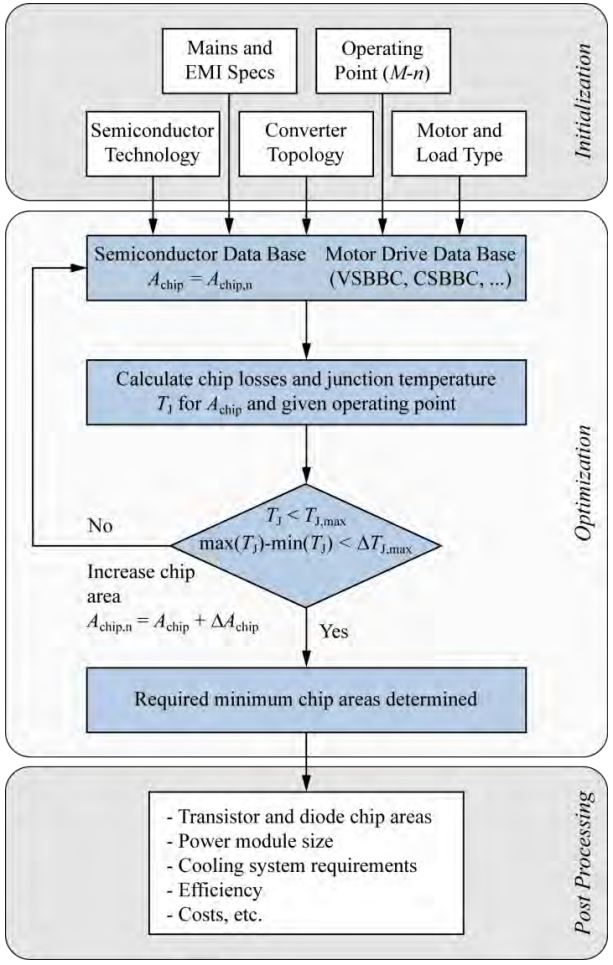
- 3 x 400 V / 50 Hz, 15 kVA
  f_{sw} = [8 ... 72] kHz
  U_{DC} = 700 V (VSBBC)
- PMSM, Matched to Converter
  (L_S in mH range, $\Phi_2 \approx 0°$)
- EMI Standard, CISPR 11
  QP Class B (66 dB at 150 kHz)
- Ambient Temperature T_A = 50°C
  Sink Temperature T_S = 95°C
  Max. Junction Temperature $T_{J,max}$ =150°C
  (for T_A = 20°C $\Rightarrow$ T_S = 65°C, $T_{J,max}$ = 20°C)

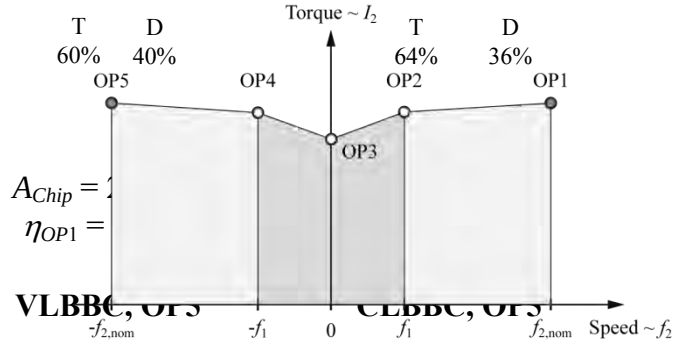
Torque Speed Plane

OP1/OP5 Nominal Motor/Generator Operation (90% $U_{2,max}$)
OP2/OP4 Motor/Generator Operation for $f_2 = f_1$
OP3 Motor Operation at Stand-still $f_2 = 0$



Comparative Evaluation (2) – Semicond. Area Based Comparison





A_{Chip} = 2
η_{OP1} =

VLBBC, OP3 CLBBC, OP3 IMC, O

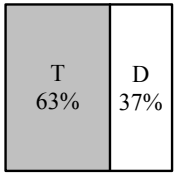
A_{Chip} = 5.0
η_{OP1} = 95

IMC, O

T 60% D 36% T 64% D 36% T 57%

► **Minimum Chip Area Required to Fulfill the Junction Temperature Limit $T_{J,max}$ (150°C)**

VLBBC, OP1&5	CLBBC, OP1&5	IMC, OP
A_{Chip} = 3.0 cm^2 η_{OP5} = 96.8%	A_{Chip} = 4.4 cm^2 η_{OP5} = 94.2%	A_{Chip} = 4.7 η_{OP5} = 95



ETH Zurich [49]

T 64% D 36% T 62%

VLBBC, OP3	CLBBC, OP3	IMC, O
A_{Chip} = 3.4 cm^2	A_{Chip} = 4.4 cm^2	A_{Chip} = 5.9

Semiconductor and Cooling System Modeling

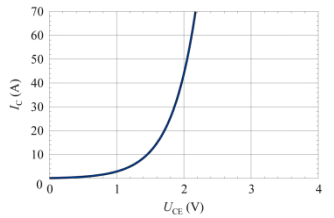
Semiconductor Database

- 1200 V Si IGBT4 and EmCon4 Diodes (Infineon)
- 1200 V normally-on SiC JFET (SiCED)

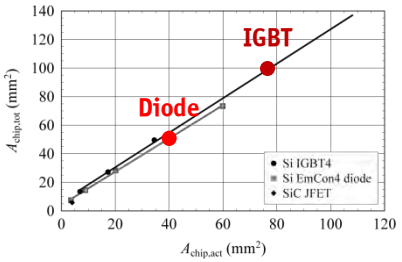
Component Level

System Level

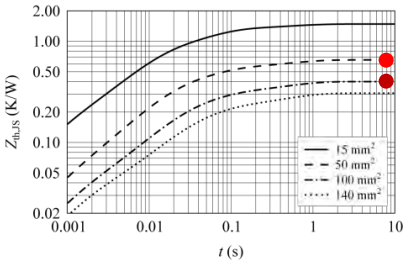
Losses as $f(A_{chip}, I, U, \text{and } T_j)$

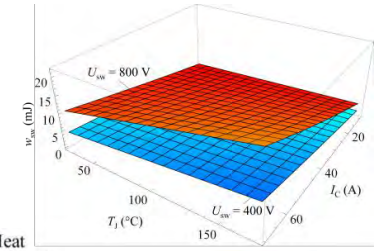


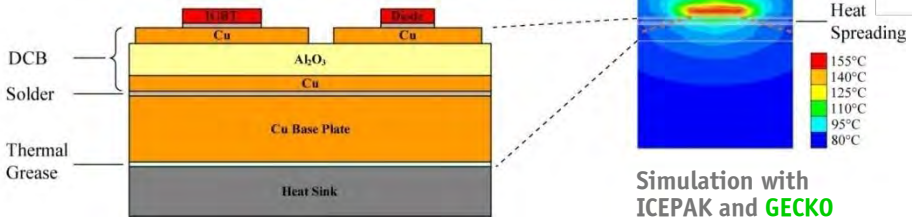
Scaling of Chip Area



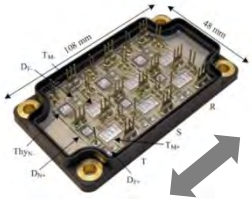
Transient Thermal Impedance

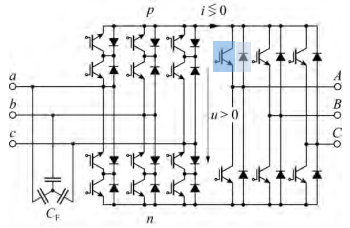


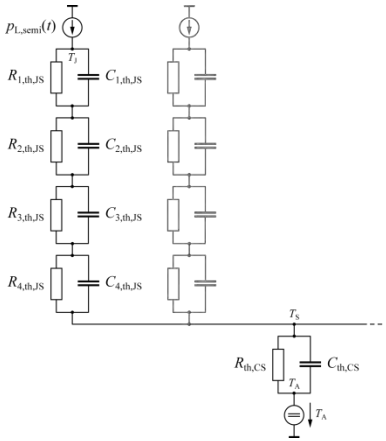




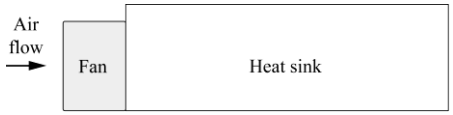
Simulation with ICEPAK and GECKO

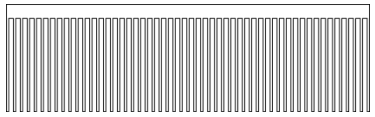






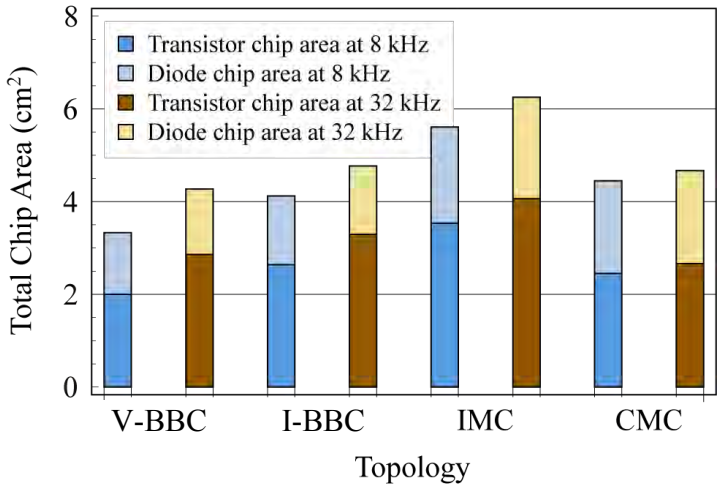
Cooling Performance



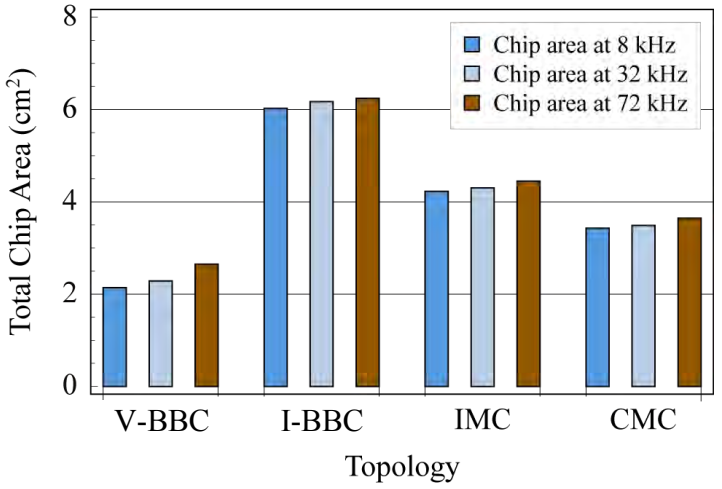


Comp. Evaluation (3) – Semiconductor Chip Areas (OP1 & OP5)

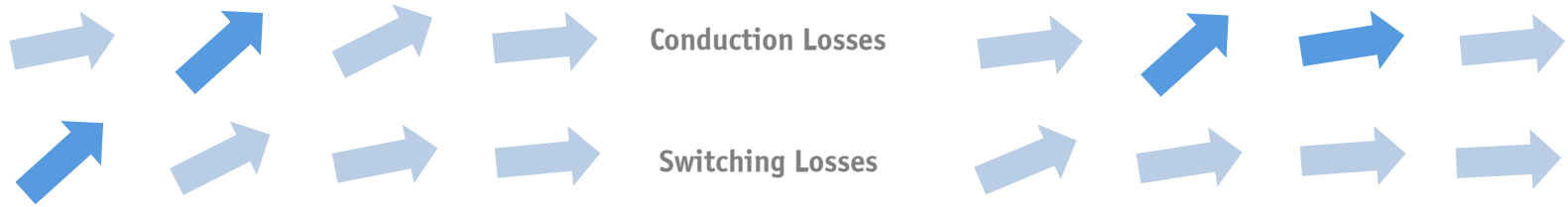
1200 V Si IGBT4 and EmCon4 Diodes



1200 V Normally-On SiC JFETs (SiCED)



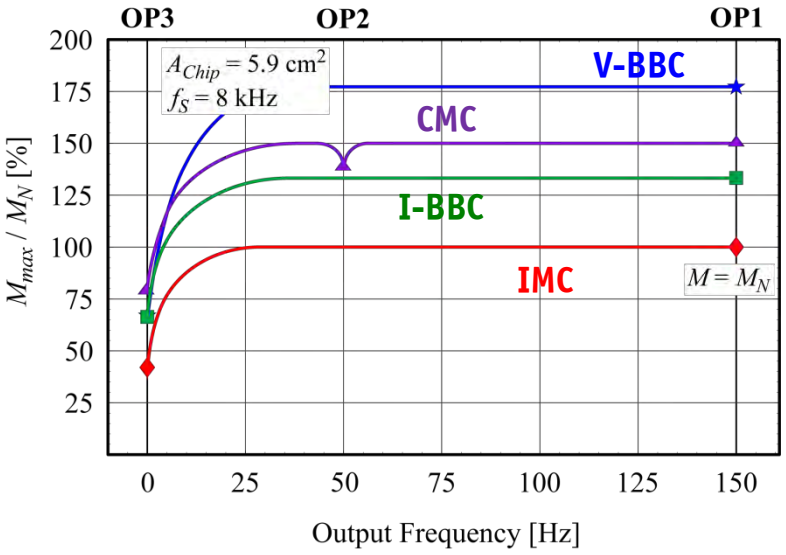
Resulting Sensitivities



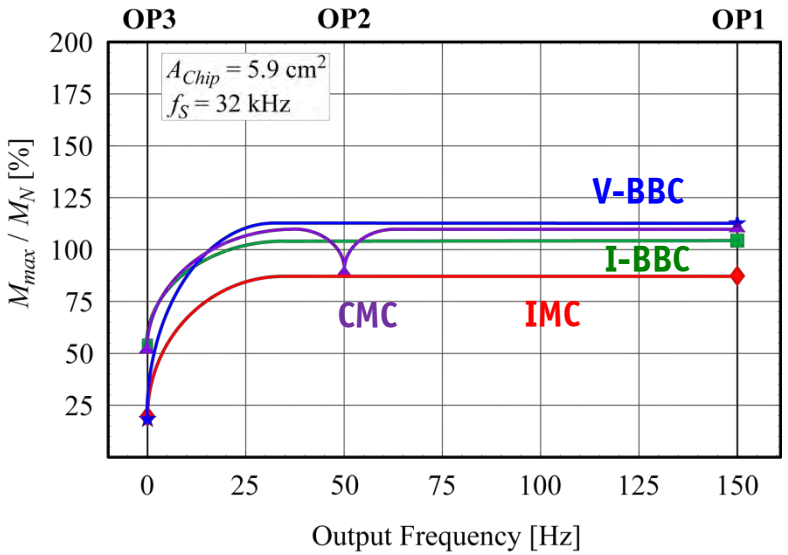
Comparative Evaluation (4) – Torque Envelope for Equal A_{chip}

► For OP1 (P_{2N} = 15 kVA) and OP3 (Stand-Still)

8 kHz: A_{Chip} ≈6 cm², Referenced to IMC



32 kHz: Available Chip Area A_{Chip} ≈6 cm²



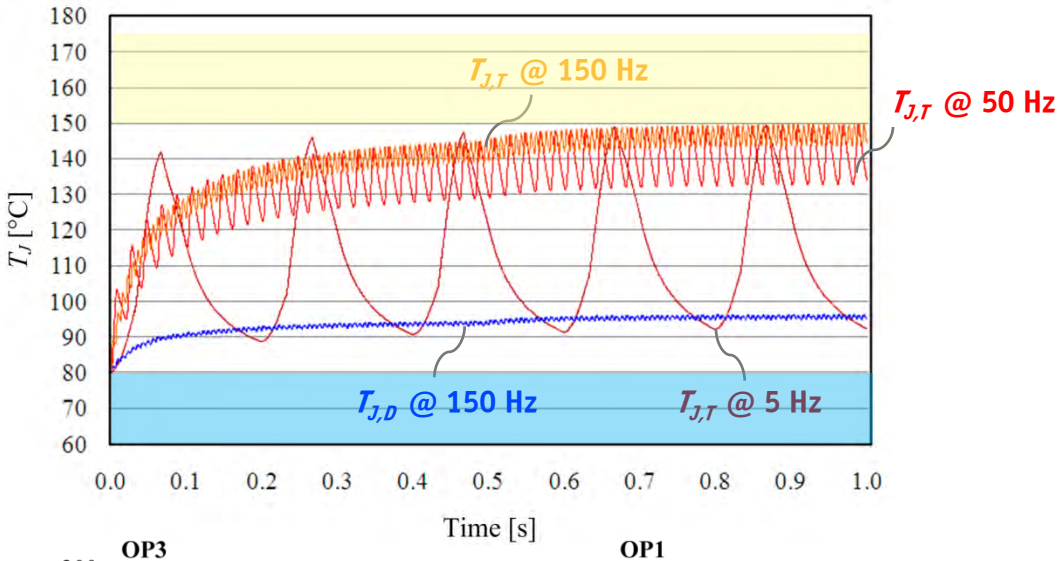
Note: Design at Thermal Limit – A More Conservative Design would be Applied for a Product!

Verification by Electro-Thermal Simulation Shown for IMC

Junction Temperatures OP1

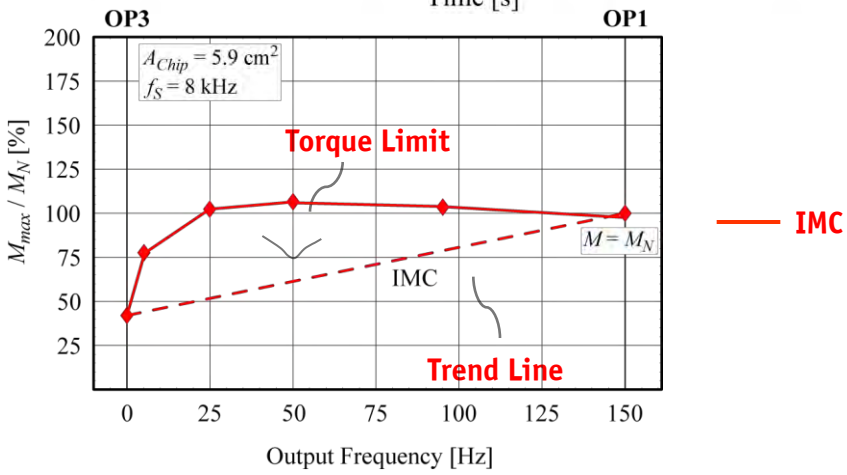
- Suggested Algorithm to Optimally Select the Semiconductor Chip Area Matches well at OP1 and OP3

Evaluated for OP1 @ 8 kHz



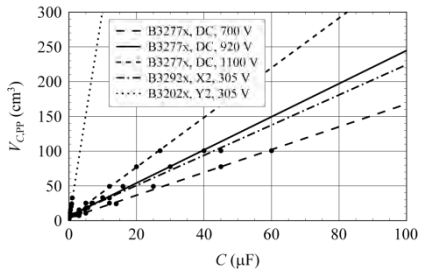
Torque at OP1 and OP3

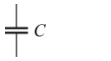
- Suggested Algorithm allows for Accurate Torque Estimation at OP1 and OP3
- Torque Limit Line Requires a Thermal Impedance Model of the Module (R-C Network)



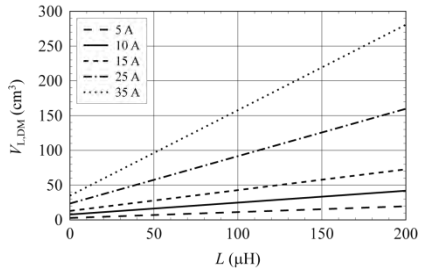
Passive Component and EMI Input Filter Modeling

Component Level

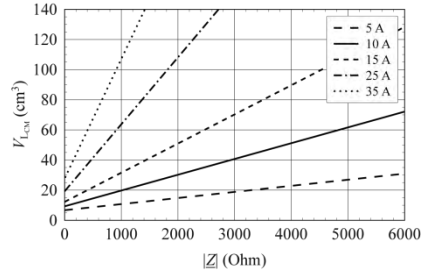




$I_{C,rms,max}$
$du/dt\,|_{max}$
T_{op} = 70°C
MTTF data



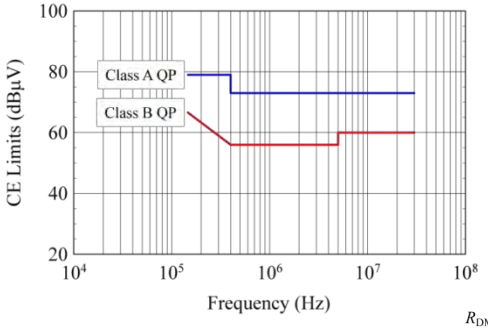
$\Delta L_{0,Imax}$
$T_{op,max}$ = 100°C



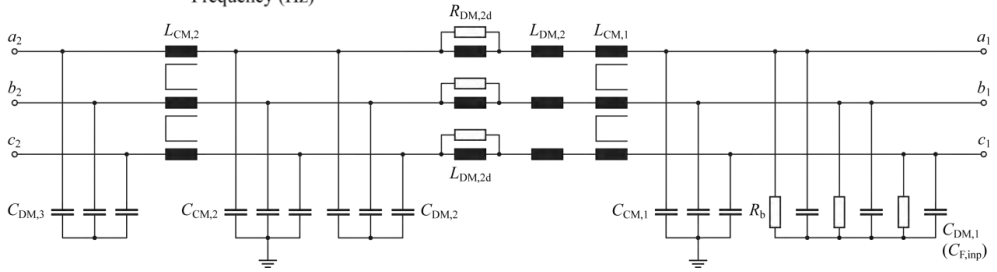
$T_{op,max}$ = 100°C

System Level

EMI Input Filter Topology



- CISPR 11 (Compliant to IEC/EN) EMI Standard for CE
- Filter Design Margin
  DM Design Margin: 6 dB
  CM Design Margin: 8-10 dB

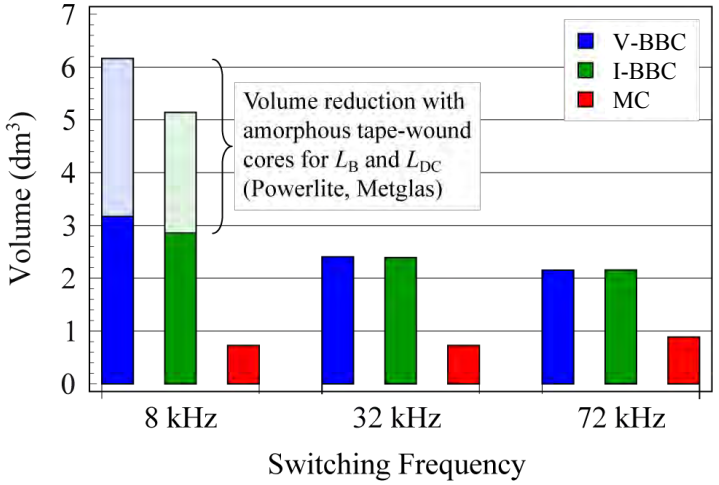


Design Criteria and Constraints

- Ripple-Based ($C_{F,inp}$, $C_{F,out}$, L_B)
- Reactive Power ($C_{F,inp}$)
- Control-Based (C_{DC}, L_{DC})
- Energy-Based (C_{DC}, L_{DC})

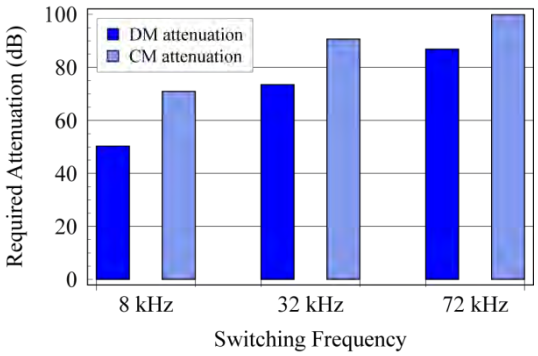
Comparative Evaluation (5) – Attenuation, Volume of Passives

Volume of Passive Components

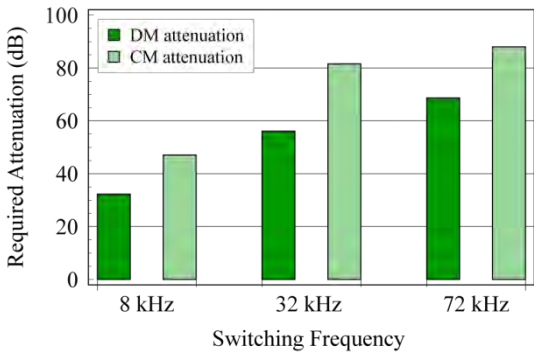


- V-BBC Requ. 15 dB More Atten.

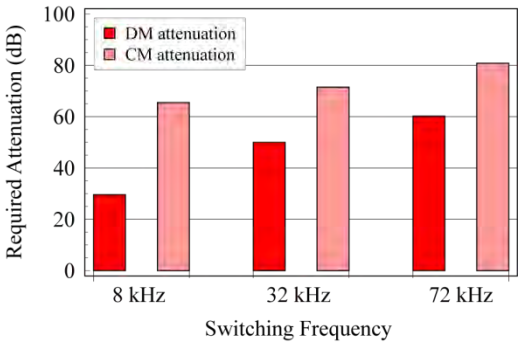
V-BBC



I-BBC

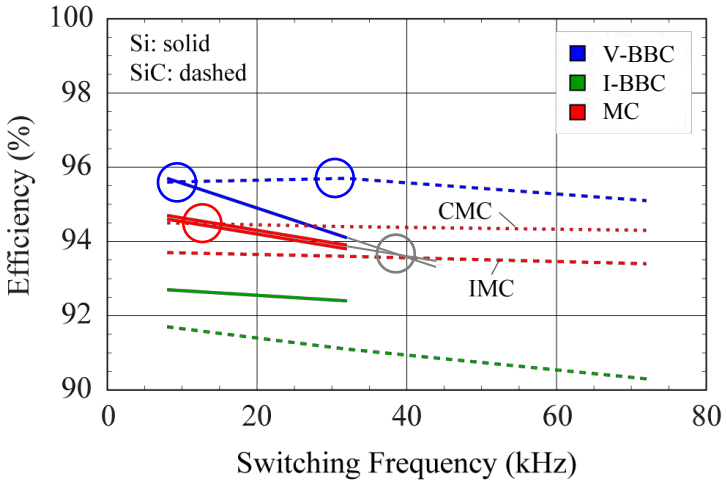


MC (IMC/CMC)

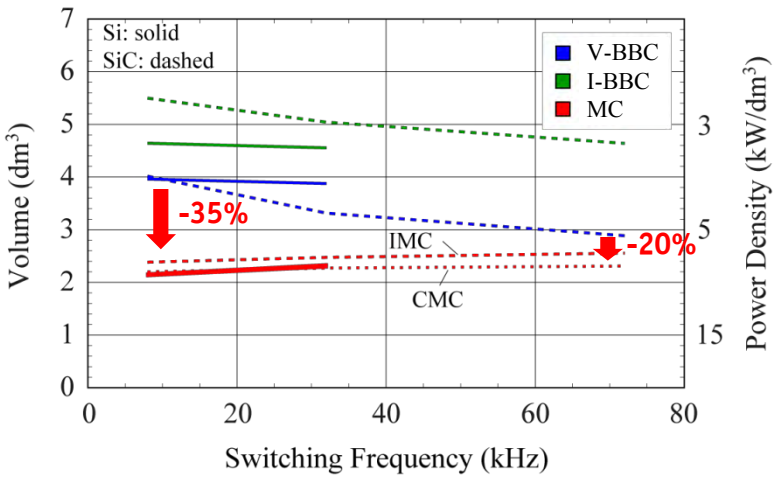


Comparative Evaluation (6) – Total Efficiency and Volume

Efficiency vs. Switching Frequency



Volume vs. Switching Frequency

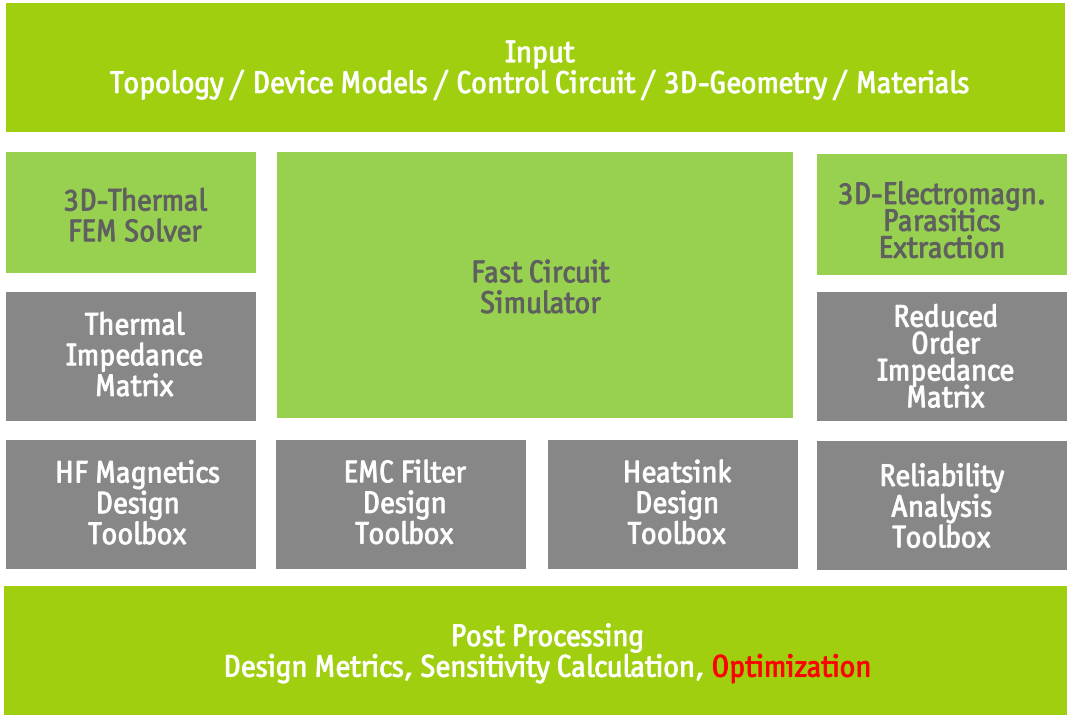


- **V-BBC: Local Optimum at 35 kHz for SiC JFETs**
- **MC: Significant Volume Reduction**

Multi-Domain Simulation Software

GECKO RESEARCH

GeckoCIRCUITS

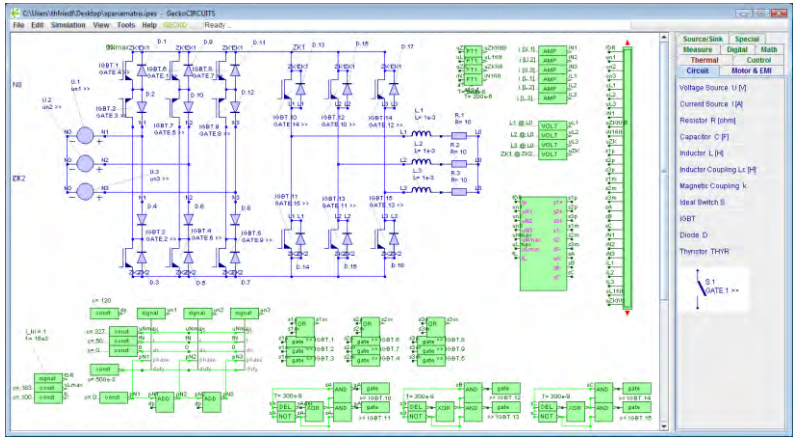


Device & Material Database
Control Toolbox
Optimization Toolbox

Overview of Gecko-Software Demonstration

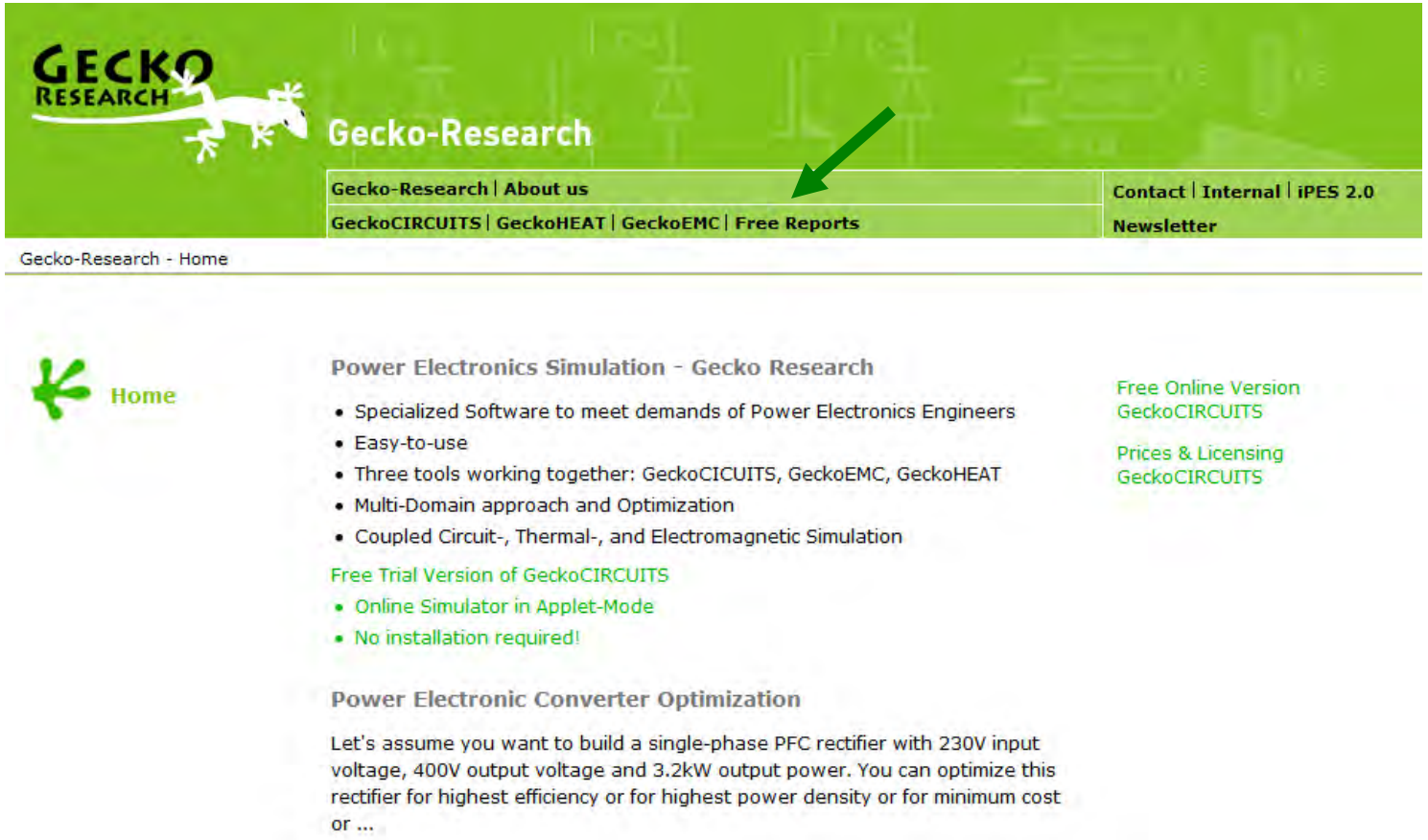
- *Gecko-CIRCUITs: Basic Functionality*

- *Indirect Matrix Converter (IMC)*
  - *IMC Simulation with Controlled AC Machine*
  - *Specify Semiconductor Characteristics*
  - *Simulate Semiconductor Junction Temperature*
  - *etc.*



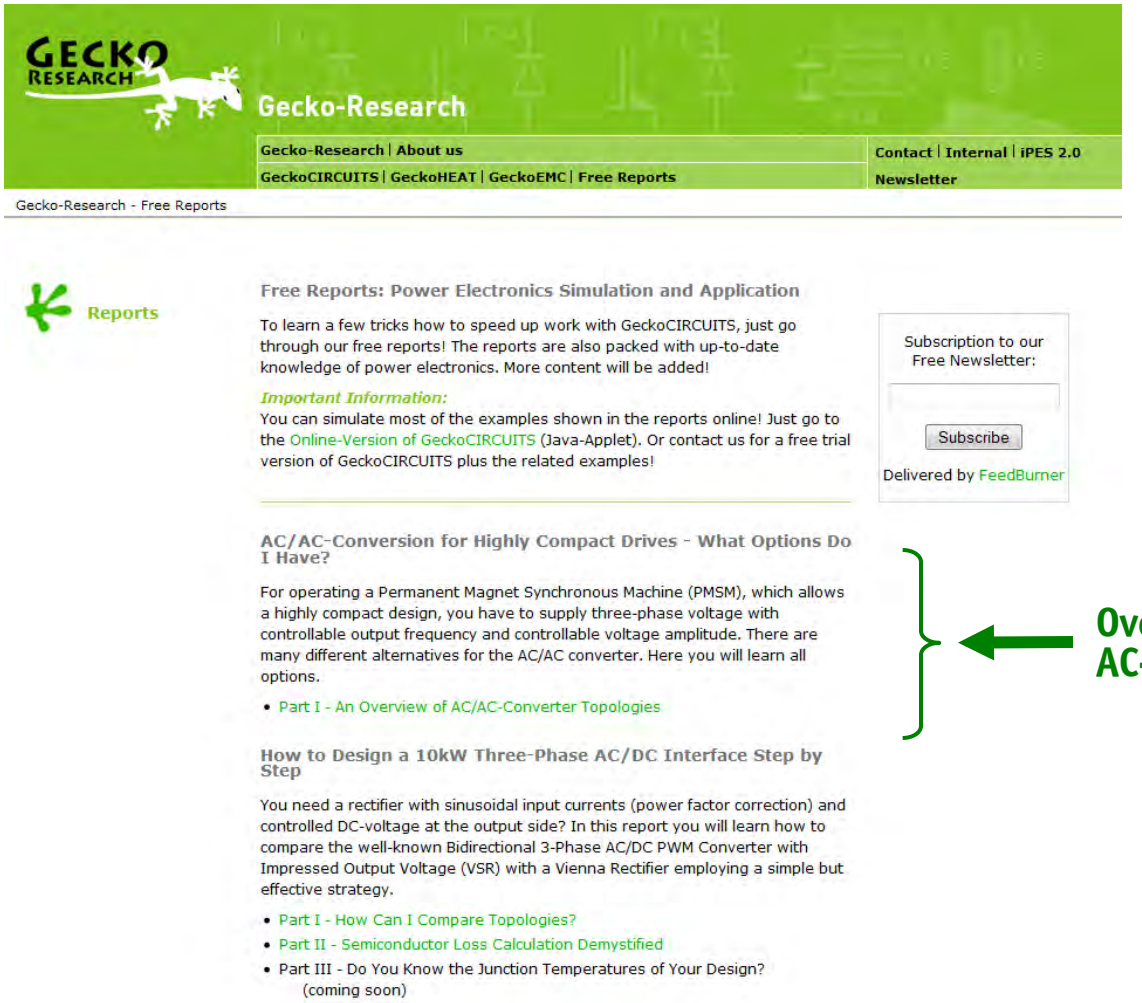
- *Gecko EMC: Basic Functionality*

Further Information Regarding Gecko-Research



www.gecko-research.com

Gecko-Research Application Notes (1)



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AC/AC-Conversion for Highly Compact Drives - What Options Do I Have?

For operating a Permanent Magnet Synchronous Machine (PMSM), which allows a highly compact design, you have to supply three-phase voltage with controllable output frequency and controllable voltage amplitude. There are many different alternatives for the AC/AC converter. Here you will learn all options.

- Part I - An Overview of AC/AC-Converter Topologies

How to Design a 10kW Three-Phase AC/DC Interface Step by Step

You need a rectifier with sinusoidal input currents (power factor correction) and controlled DC-voltage at the output side? In this report you will learn how to compare the well-known Bidirectional 3-Phase AC/DC PWM Converter with Impressed Output Voltage (VSR) with a Vienna Rectifier employing a simple but effective strategy.

- Part I - How Can I Compare Topologies?
- Part II - Semiconductor Loss Calculation Demystified
- Part III - Do You Know the Junction Temperatures of Your Design? (coming soon)

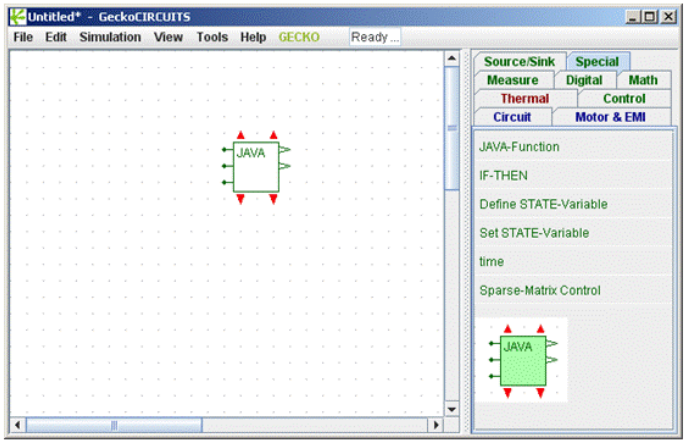
Overview of AC-AC Converters

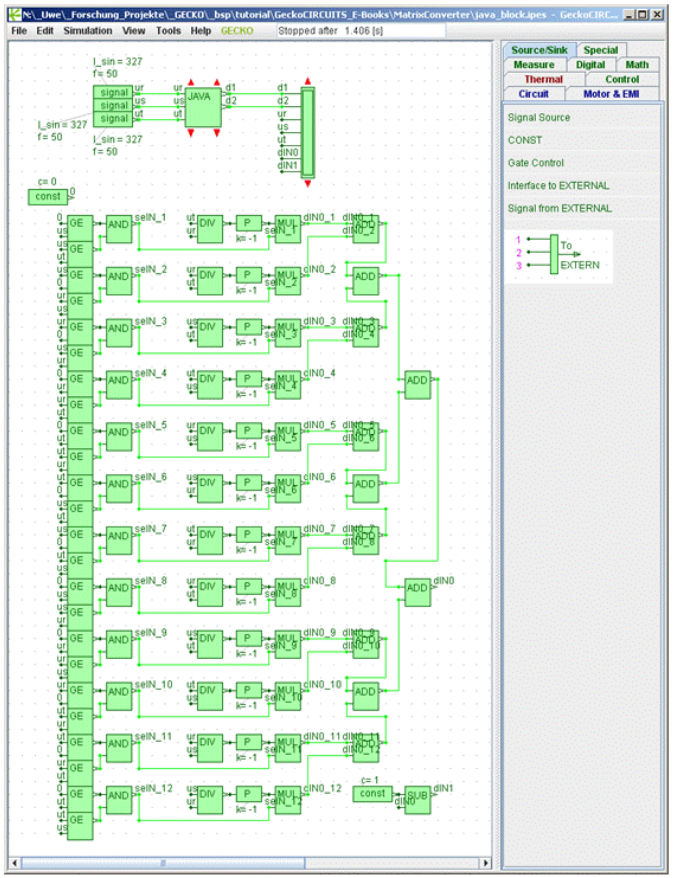
Gecko-Research Application Notes (2)

Useful Hints for e.g. How to Implement Sector Detection for SV Modulation

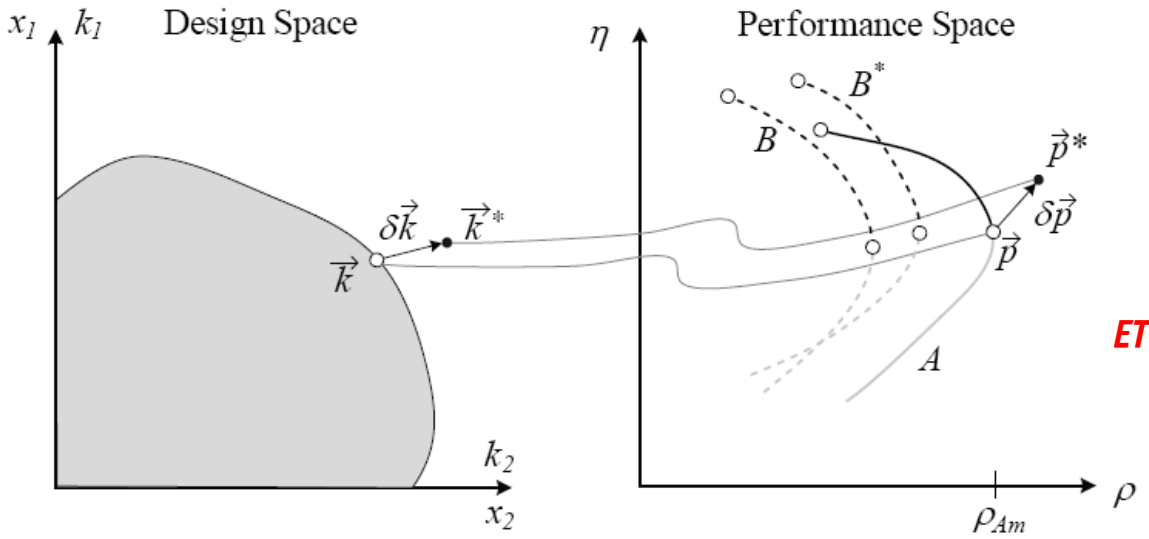
► JAVA Code Block

- Integration of Complex Control Code; Enhances Overview and Transparency
- Code can Virtually be Copied to DSP C-Code Generator (Minor Syntax Adaptations)





Power Electronics Converter Optimization



ETH Zurich [50]

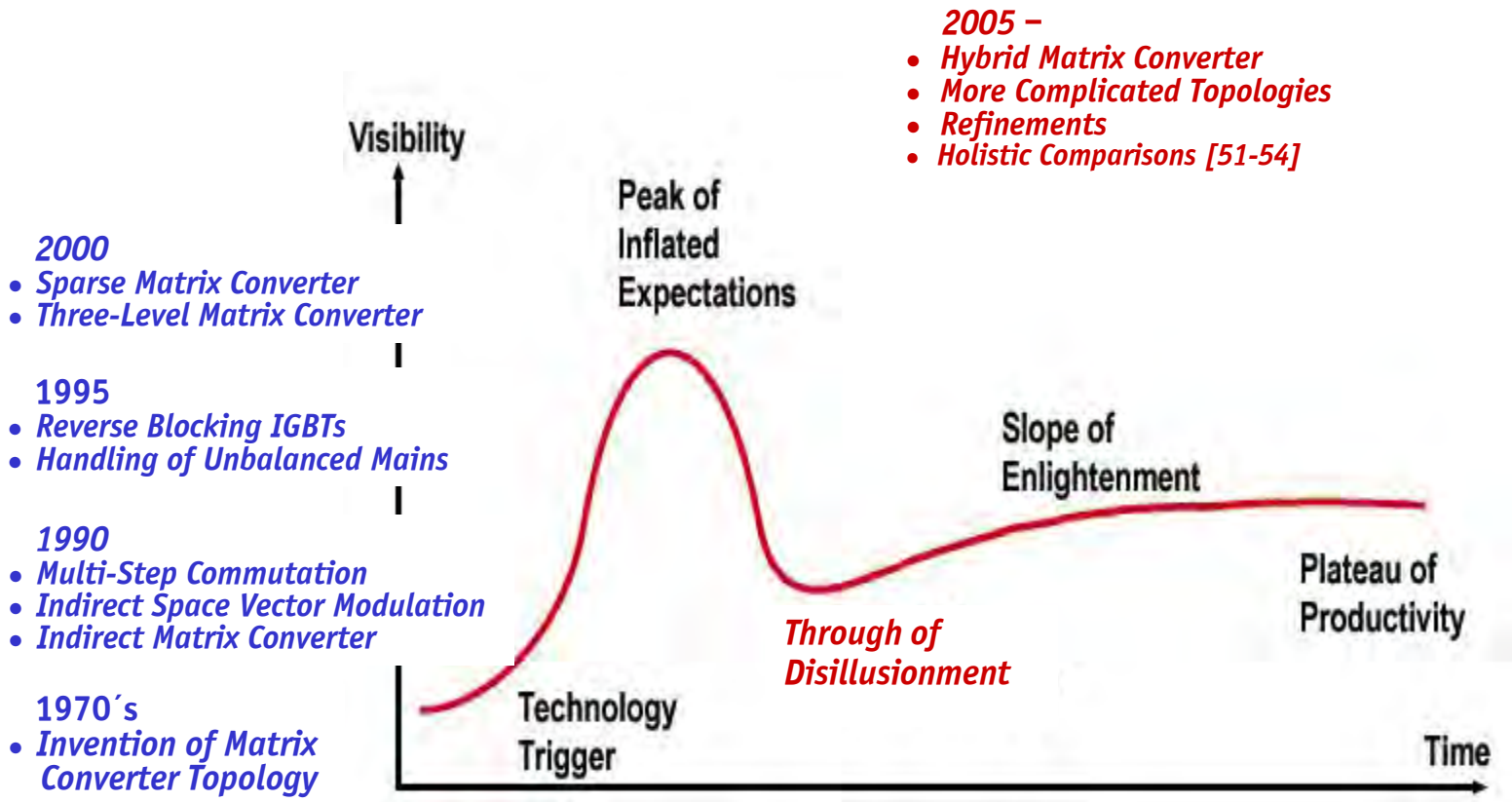
Goal: Optimization Toolbox

- *Guided Step-by-Step Converter Design Procedure to Enable Optimal Utilization of Technological Base and Optimal Matching between Design Specifications and Final Performance*

Conclusions

Hype Cycle of Technologies

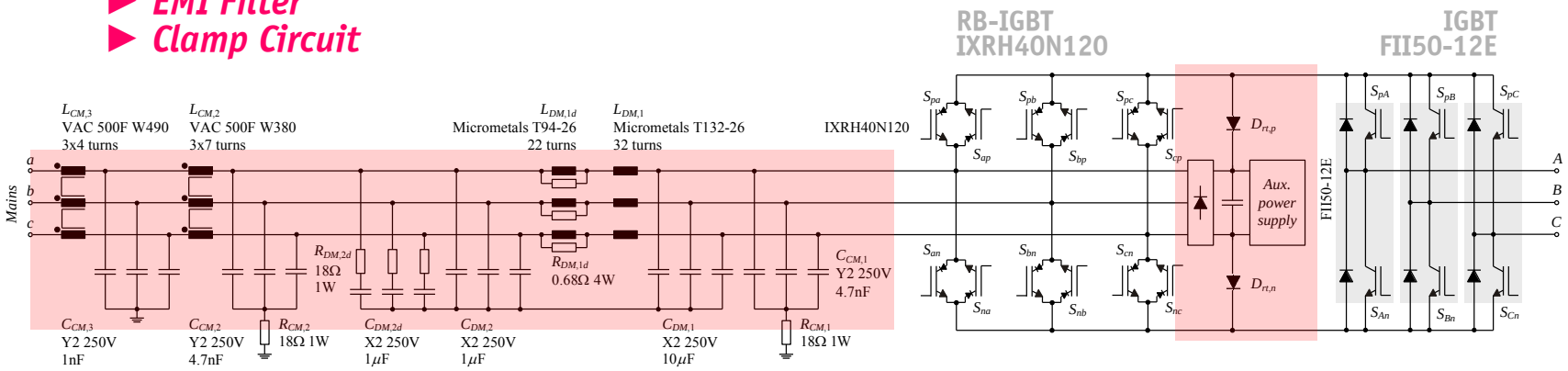
-Gartner Group



Conclusions (1)

- *MC is NOT an All-SiC Solution*
  - *Industry Engineers Missing Experience*
  - *86% Voltage Limit / Application of Specific Motors / Silicon Area*
  - *Limited Fault Tolerance*
  - *Braking in Case of Mains Failure*
  - *Costs and Complexity Challenge*
  - *Voltage DC Link Converter could be Implemented with Foil Capacitors*
- *MC does NOT offer a Specific Advantage without Drawback*

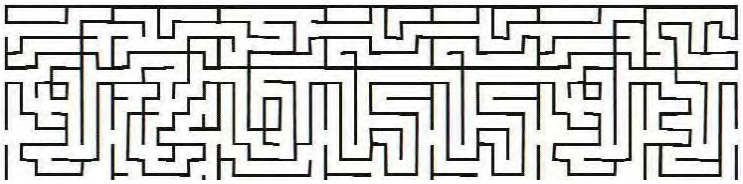
- *EMI Filter*
- *Clamp Circuit*



Conclusions (2)

- *Research MUST Address Comprehensive System Evaluations*
  - *MC Promising for High Switching Frequency*
  - *Consider Specific Application Areas*
  - *Consider Life Cycle Costs*
  - *etc.*
- *V-BBC is a Tough Competitor*
- *F^3E Might Offer a Good Compromise*
- *Most Advantageous Converter Concept Depends on Application and on whether a CUSTOM Drive Design is Possible*
- *Integration of Multiple Functions (as for MC) Nearly ALWAYS Requires a Trade-off*

End of Part 2



Thank You !

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Johann W. Kolar (F´10) received his Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria. Since 1984 he has been working as an independent international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel PWM converter topologies, and modulation and control concepts, e.g., the VIENNA Rectifier and the Three-Phase AC-AC Sparse Matrix Converter. Dr. Kolar has published over 350 scientific papers in international journals and conference proceedings and has filed 75 patents. He was appointed Professor and Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich on Feb. 1, 2001.

The focus of his current research is on AC-AC and AC-DC converter topologies with low effects on the mains, e.g. for power supply of data centers, More-Electric-Aircraft and distributed renewable energy systems. Further main areas of research are the realization of ultra-compact and ultra-efficient converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and EMI filtering, multi-domain/multi-scale modeling / simulation and multi-objective optimization, physical model based lifetime prediction, pulsed power, bearingless motors, and Power MEMS.

He received the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005, the Best Paper Award of the ICPE in 2007, the 1st Prize Paper Award of the IEEE IAS IPCC in 2008, and the IEEE IECON Best Paper Award of the IES PETC in 2009. He also received an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003. He initiated and/or is the founder / co-founder of 4 Spin-off Companies targeting ultra high speed drives, multi-domain/level simulation, ultra-compact/efficient converter systems and pulsed power/electronic energy processing. In 2006, the European Power Supplies Manufacturers Association (EPSMA) awarded the Power Electronics Systems Laboratory of ETH Zurich as the leading academic research institution in Power Electronics in Europe.

Dr. Kolar is a Fellow of the IEEE and a Member of the IEEJ and of International Steering Committees and Technical Program Committees of numerous international conferences in the field (e.g. Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). He is the founding Chairman of the IEEE PELS Austria and Switzerland Chapter and Chairman of the Education Chapter of the EPE Association. From 1997 through 2000 he has been serving as an Associate Editor of the IEEE Transactions on Industrial Electronics and since 2001 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.

Michael Hartmann (M'09) was born in Feldkirch, Austria, on May 26, 1978. After he finished the HTL-Rankweil (Telecommunications), he started to work at Omicron Electronics in Klaus (Austria) as a hardware development engineer. There, his work was focused on measurements techniques for power system testing.

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He received the 1st Prize Paper Award of the IEEE IAS IPCC in 2008 and the IEEE IAS Transactions Prize Paper Award in 2009.