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Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich




The Essence of Three-Phase PFC Rectifier Systems

J. W. Kolar, J. Mühlethaler

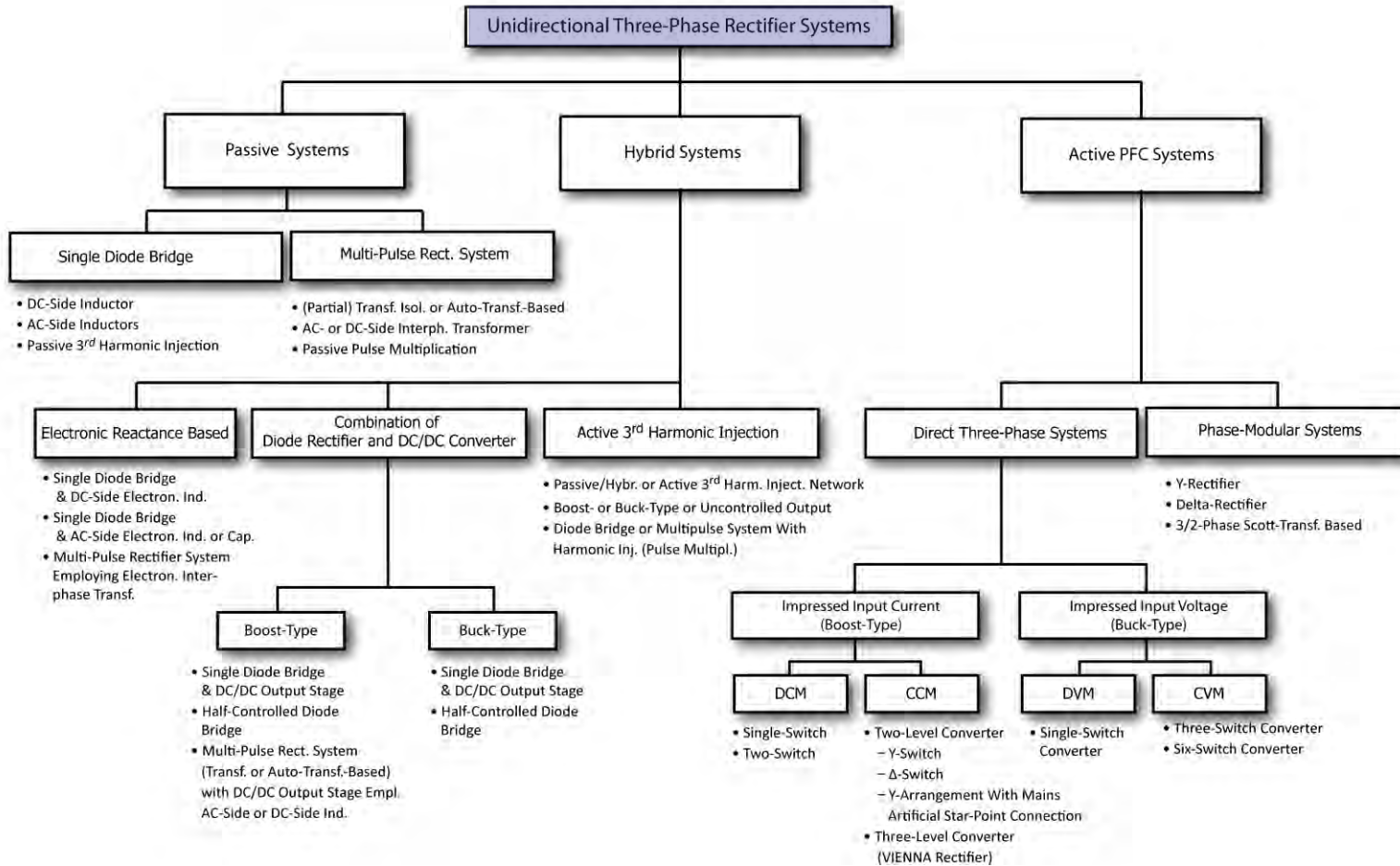
Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch



Schedule / Outline

- 14:00 — ▶ **Introduction**
▶ **Passive and Hybrid Rectifier Systems**
- 15:10 — ▶ **Phase-Modular Active PFC Rectifier Systems**
-  Coffee Break
- 15:30 — ▶ **Boost-Type Active PFC Rectifier Systems**
▶ **Buck-Type Active PFC Rectifier Systems**
- 17:00 — ▶ **Conclusions / Questions / Discussion**

► Classification of Unidirectional Rectifier Systems



► Classification of Unidirectional Rectifier Systems

■ Definitions and Characteristics

- **Passive Rectifier Systems**
 - Line Commutated Diode Bridge/Thyristor Bridge - Full/Half Controlled
 - Low Frequency Output Capacitor for DC Voltage Smoothing
 - Only Low Frequency Passive Components Employed for Current Shaping, No Active Current Control
 - No Active Output Voltage Control

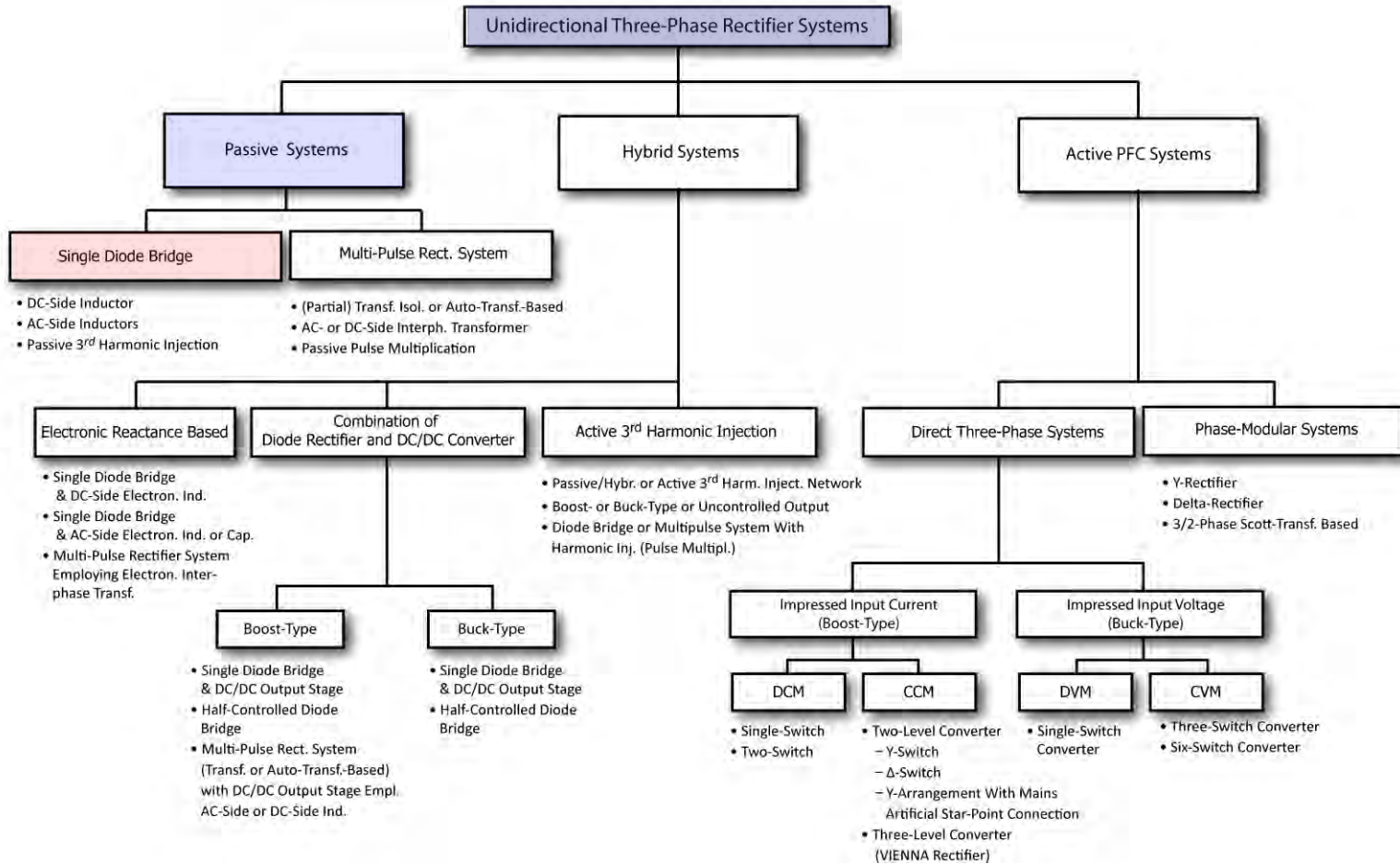
- **Hybrid Rectifier Systems**
 - Low Frequency and Switching Frequency Passive Components and/or
 - Mains Commutation (Diode/Thyristor Bridge - Full/Half Controlled) and/or Forced Commutation
 - Partly Only Current Shaping/Control and/or Only Output Voltage Control
 - Partly Featuring Purely Sinusoidal Mains Current

- **Active Rectifier Systems**
 - Controlled Output Voltage
 - Controlled (Sinusoidal) Input Current
 - Only Forced Commutations / Switching Frequ. Passive Components

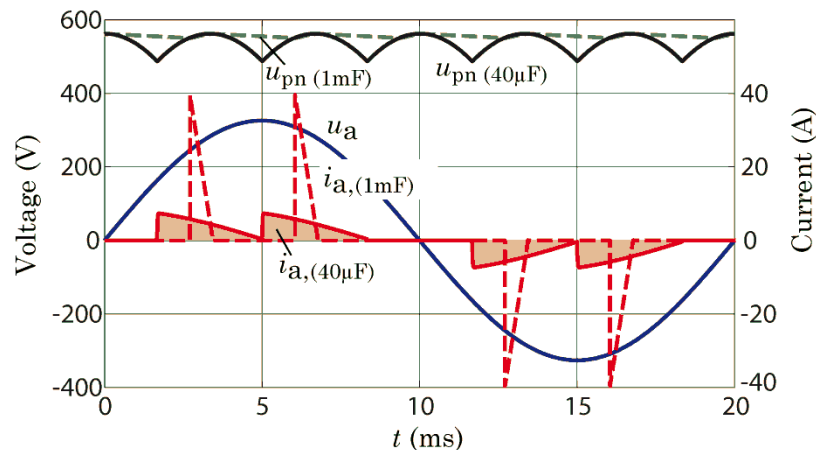
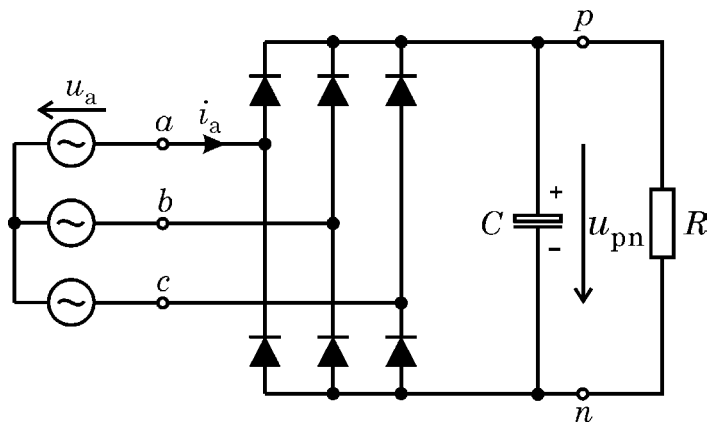
- **Phase-Modular Systems**
 - Phase Rectifier Modules of Identical Structure
 - Phase Modules connected in Star or in Delta
 - Formation of Three Independent Controlled DC Output Voltages

- **Direct Three-Phase Syst.**
 - Only One Common Output Voltage for All Phases
 - Symmetrical Structure of the Phase Legs
 - Phase (and/or Bridge-)Legs Connected either in Star or Delta

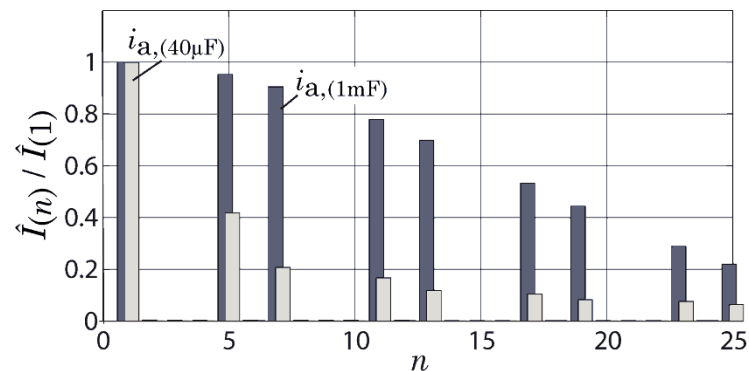
► Classification of Unidirectional Rectifier Systems



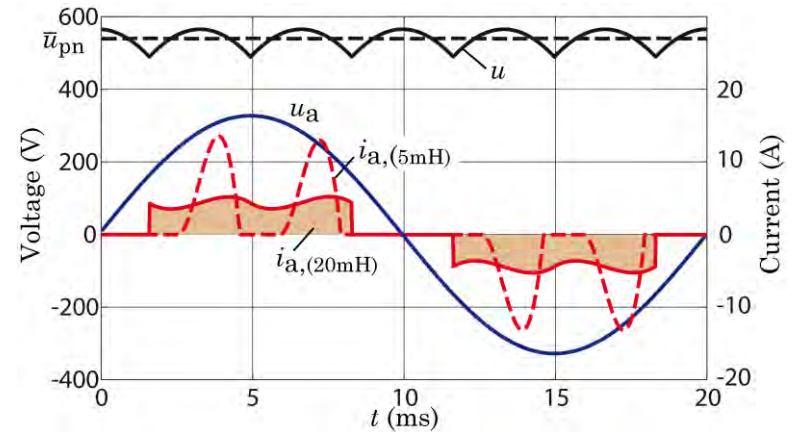
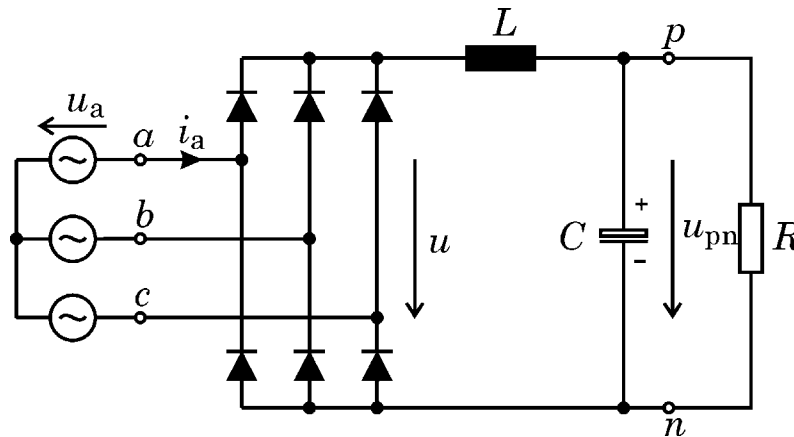
► Diode Bridge Rectifier with Capacitive Smoothing



$U_{LL} = 3 \times 400 \text{ V}$
 $f_N = 50 \text{ Hz}$
 $P_{out} = 2.5 \text{ kW} \quad (R=125 \Omega)$
 $C = 1 \text{ mF}; 40 \mu\text{F}$
 $X_c/R = 0.025; 0.636$

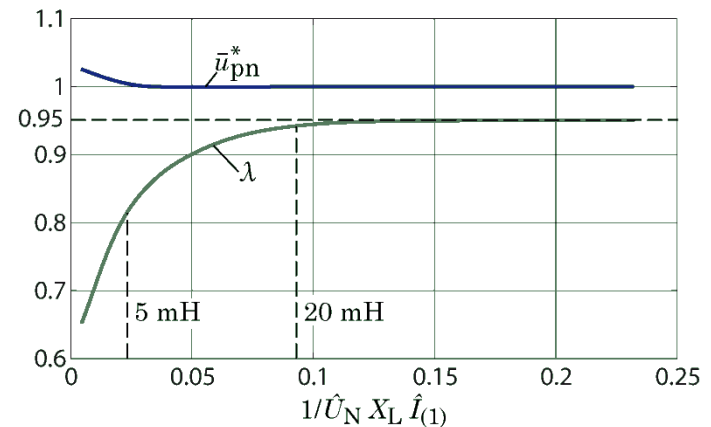


► Diode Bridge Rectifier / DC-Side Inductor and Output Capacitor

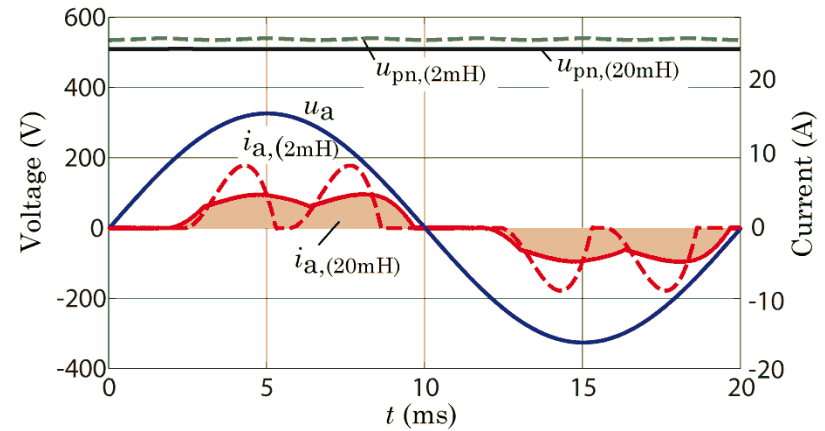
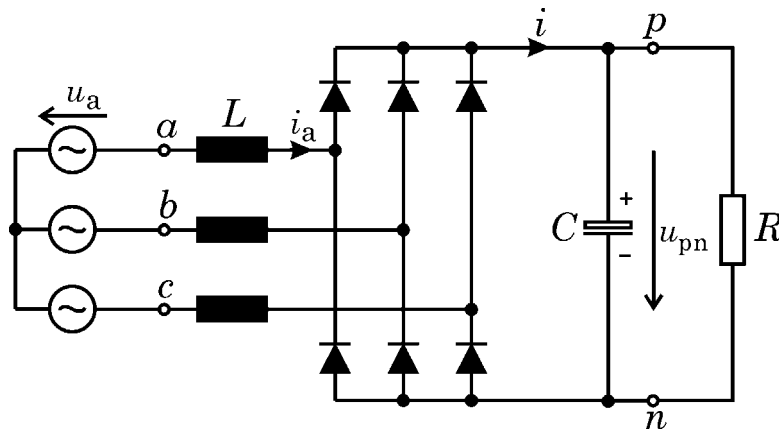


$$\bar{u}_{pn}^* = \frac{\bar{u}_{pn}}{\frac{\pi}{3} \hat{U}_{N,LL}}$$

$U_{LL} = 3 \times 400 \text{ V}$
 $f_N = 50 \text{ Hz}$
 $P_{out} = 2.5 \text{ kW} \text{ (} R=125 \Omega \text{)}$
 $C = 1 \text{ mF}$
 $L = 5 \text{ mH}; 20 \text{ mH}$

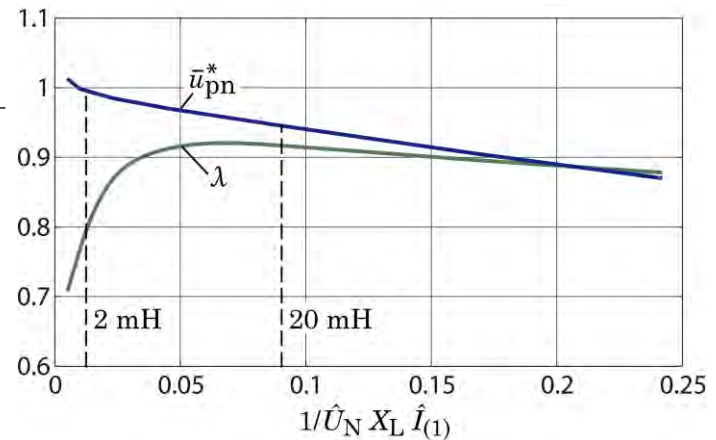


► Diode Bridge Rectifier / AC-Side Inductor and Output Capacitor

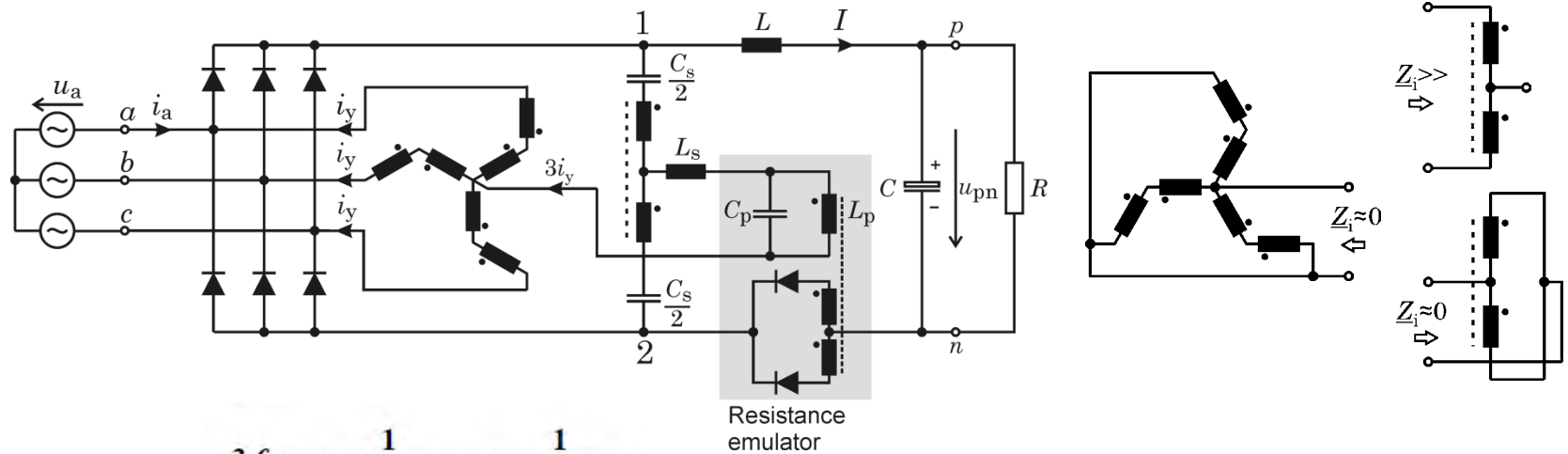


$$\bar{u}_{pn}^* = \frac{\bar{u}_{pn}}{\frac{\pi}{3} \hat{U}_{N,LL}}$$

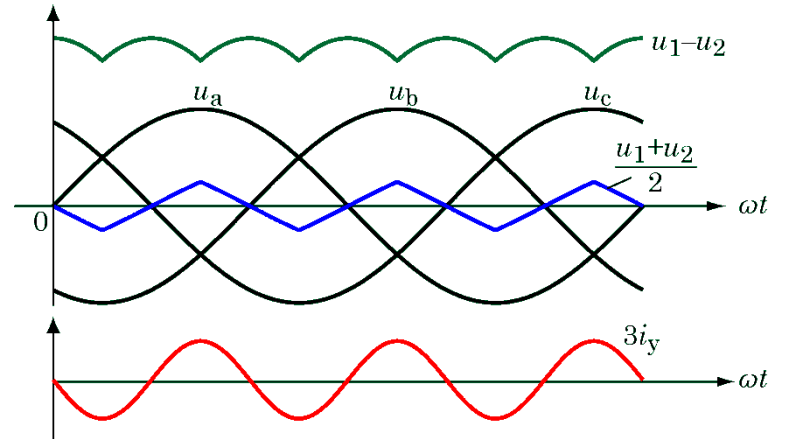
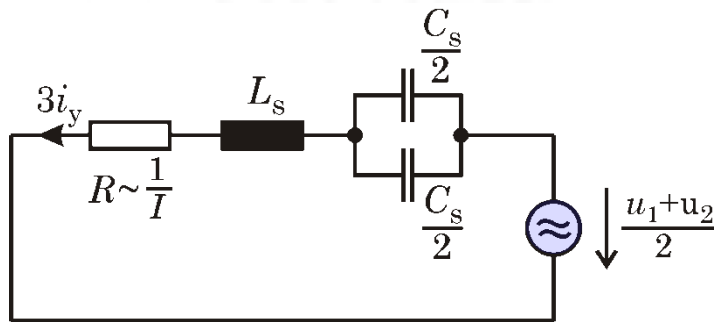
$U_{LL} = 3 \times 400 \text{ V}$
 $f_N = 50 \text{ Hz}$
 $P_{out} = 2.5 \text{ kW} \text{ (} R=125 \Omega \text{)}$
 $C = 1 \text{ mF}$
 $L = 2 \text{ mH; } 20 \text{ mH}$



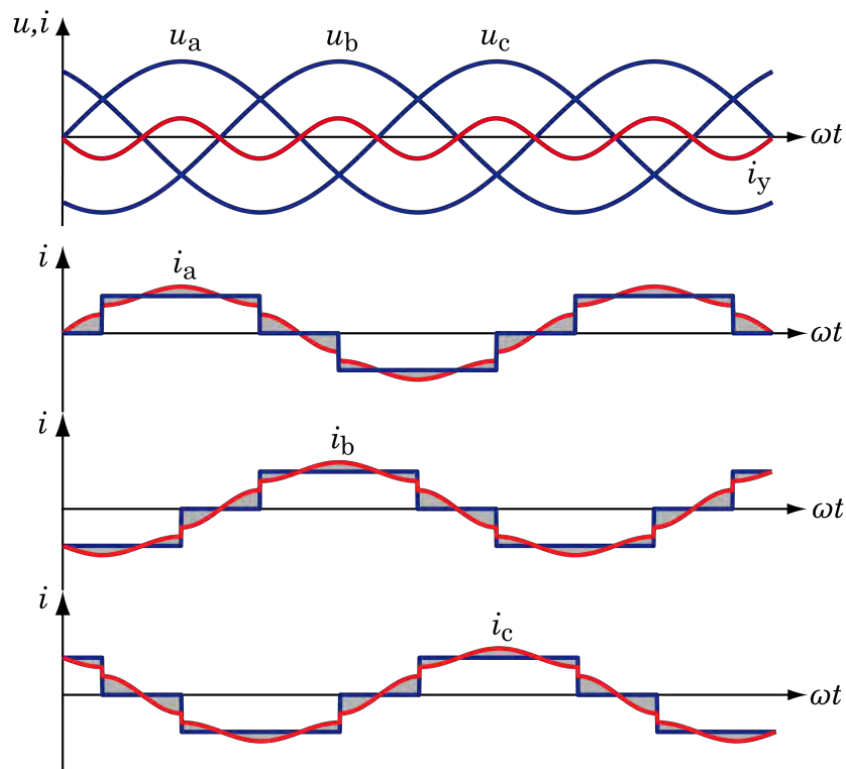
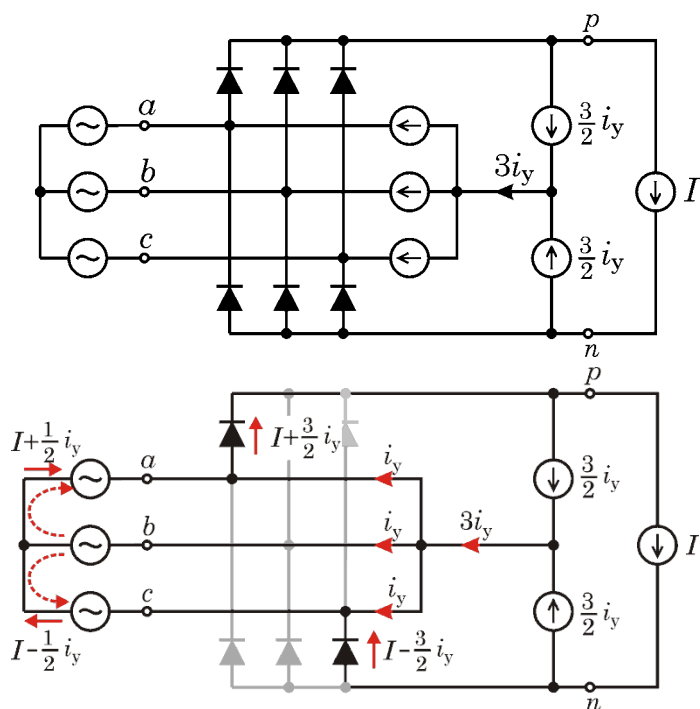
► Passive 3rd Harmonic Injection



$$3f_N = \frac{1}{2\pi\sqrt{L_S C_S}} = \frac{1}{2\pi\sqrt{L_P C_P}}$$

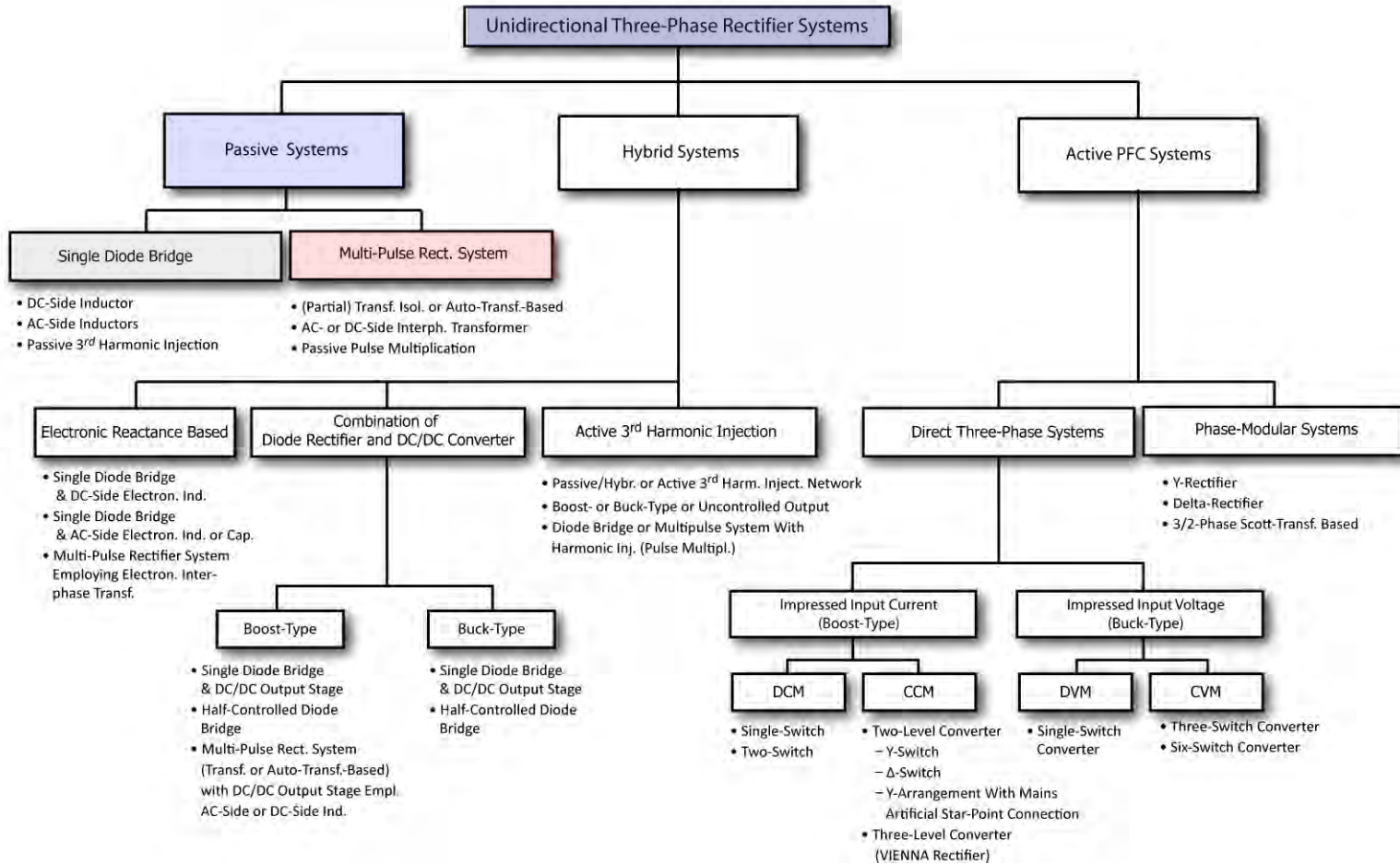


► Passive 3rd Harmonic Injection



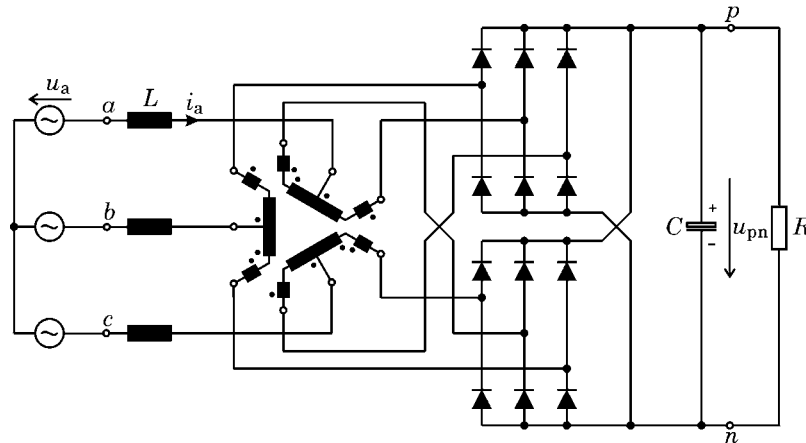
- Minimum THD of Phase Current for $i_y = 1/2 I$
- $\text{THD}_{\min} = 5 \%$

► Classification of Unidirectional Rectifier Systems

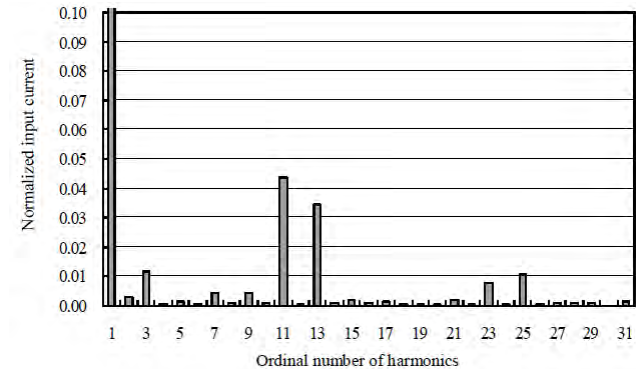
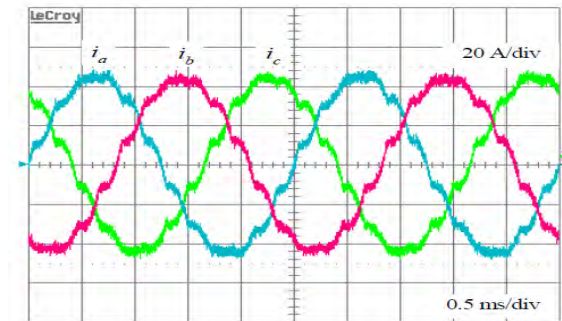
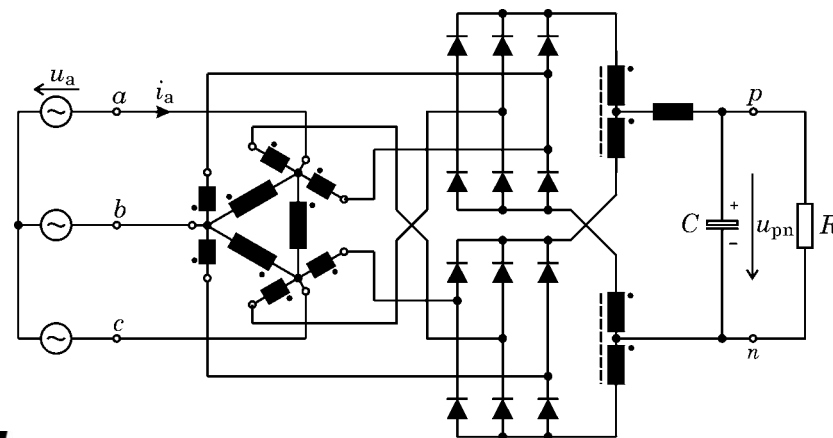


Auto-Transformer-Based-12-Pulse Rectifier Systems

AC-Side Interphase Transf. (Impr. DC Voltage)

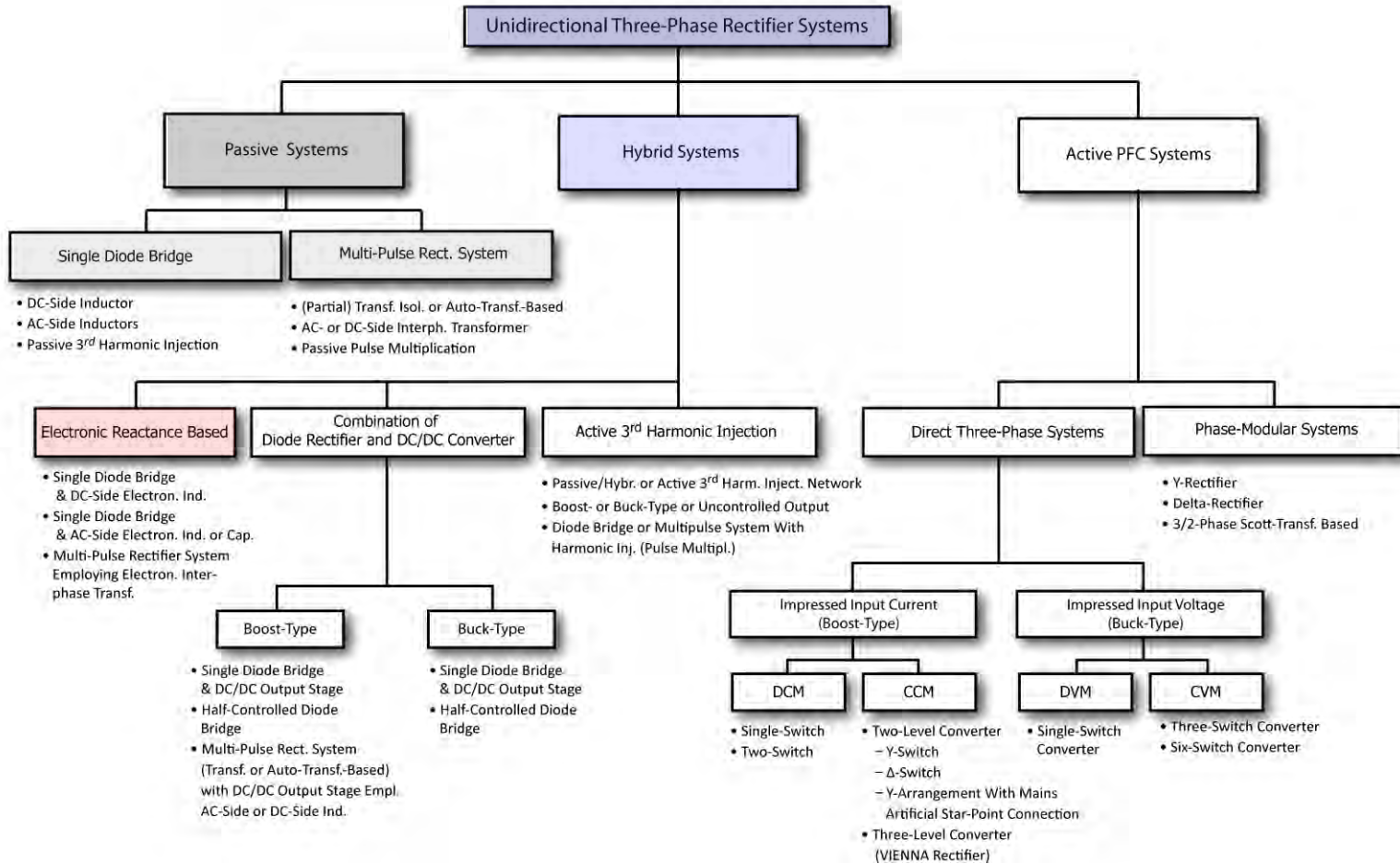


DC-Side Interphase Transf. (Impr. DC Current)

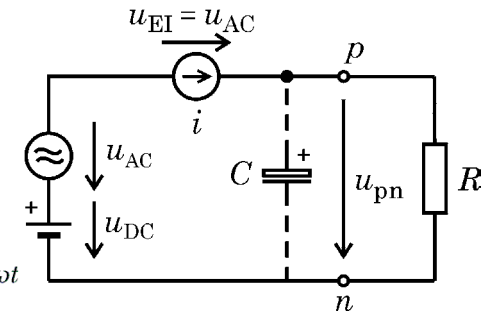
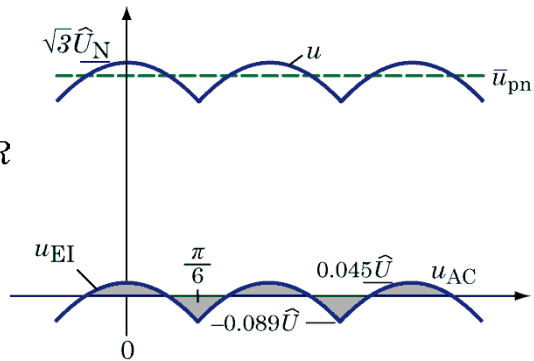
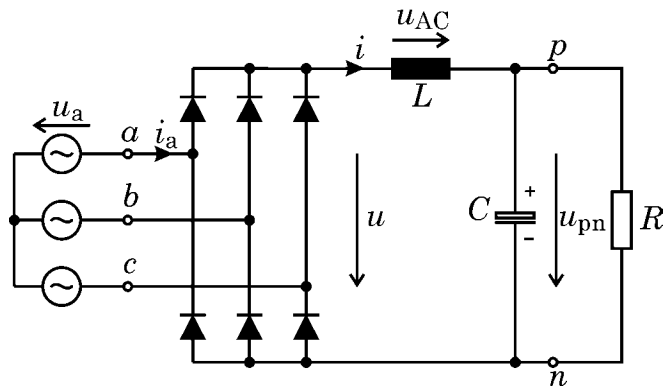


DC-Side Interphase Transformer can be omitted in Case of Full Transformer Isolation of Both Diode Bridges

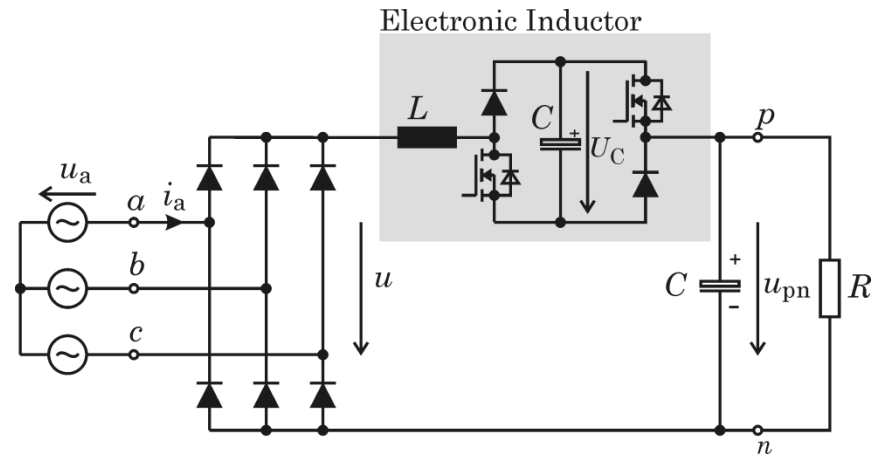
► Classification of Unidirectional Rectifier Systems



► Diode Bridge and DC-Side Electronic Inductor (EI)

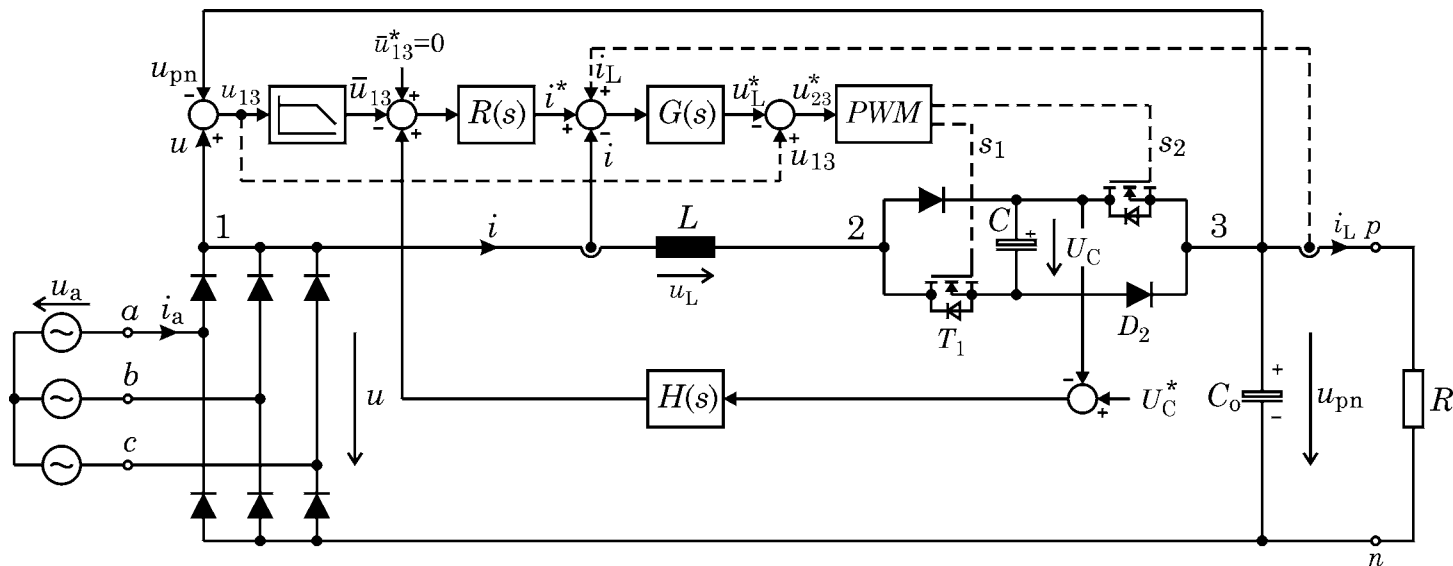


- + Only Fract. of Output Power Processed
- + High Efficiency and Power Density
- Not Output Voltage Control
- EMI Filtering Required



► Diode Bridge and DC-Side Electronic Inductor (EI)

■ Control Structure



- Current Control could Theoretically Emulate Infinite Inductance Value but Damping (Parallel Ohmic Component) has to be Provided for Preventing Oscillations

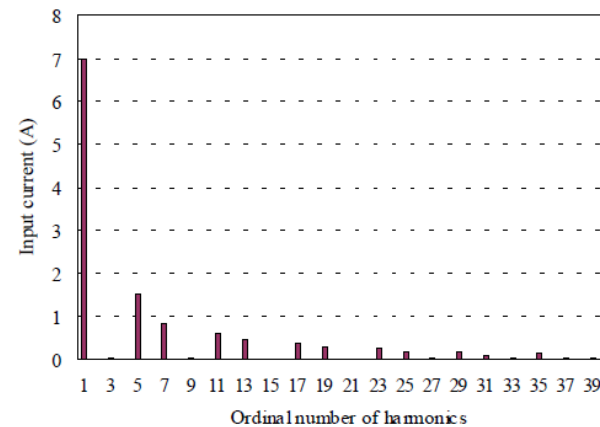
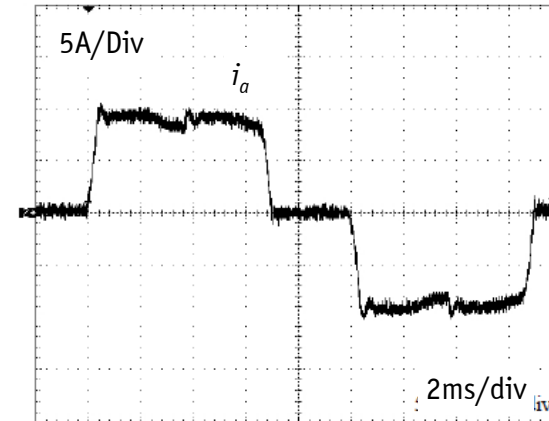
► Diode Bridge and DC-Side Electronic Inductor (EI)

■ Experimental Results

$U_{LL} = 3 \times 400 \text{ V}$
 $P_o = 5 \text{ kW}$
 $f_s = 70 \text{ kHz}$
 $C = 4 \times 330 \mu\text{F} / 100 \text{ V}$

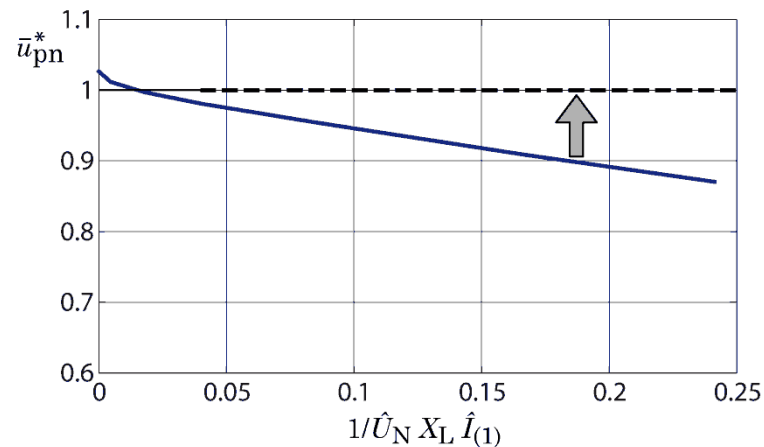
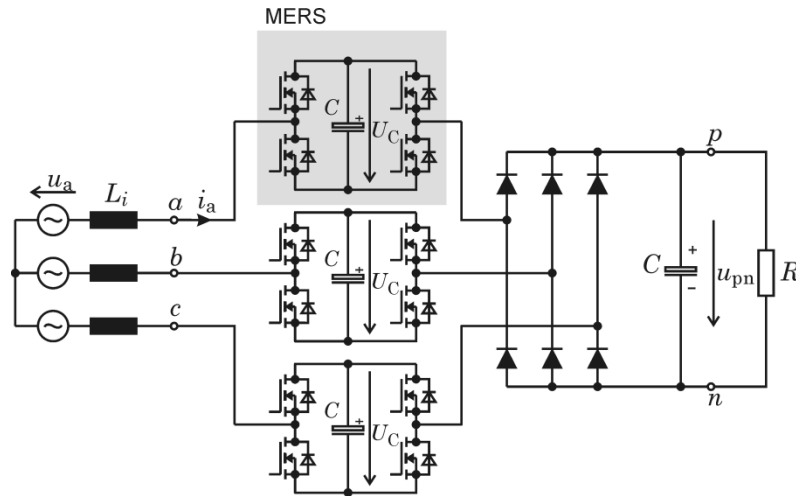


$\eta = 98.3 \%$
 $\lambda = 0.955$
 $\text{THD} = 28.4 \%$

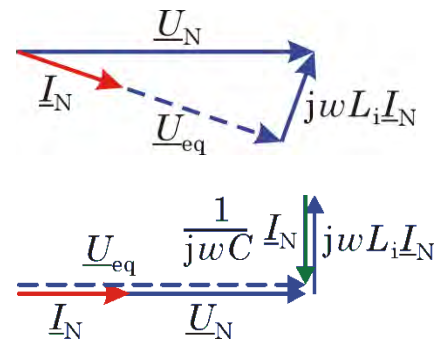
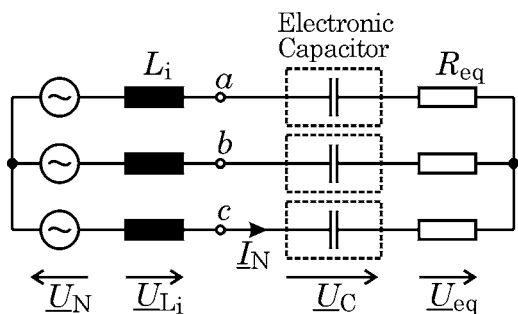


► Diode Bridge and DC-Side EI or Electronic Capacitor

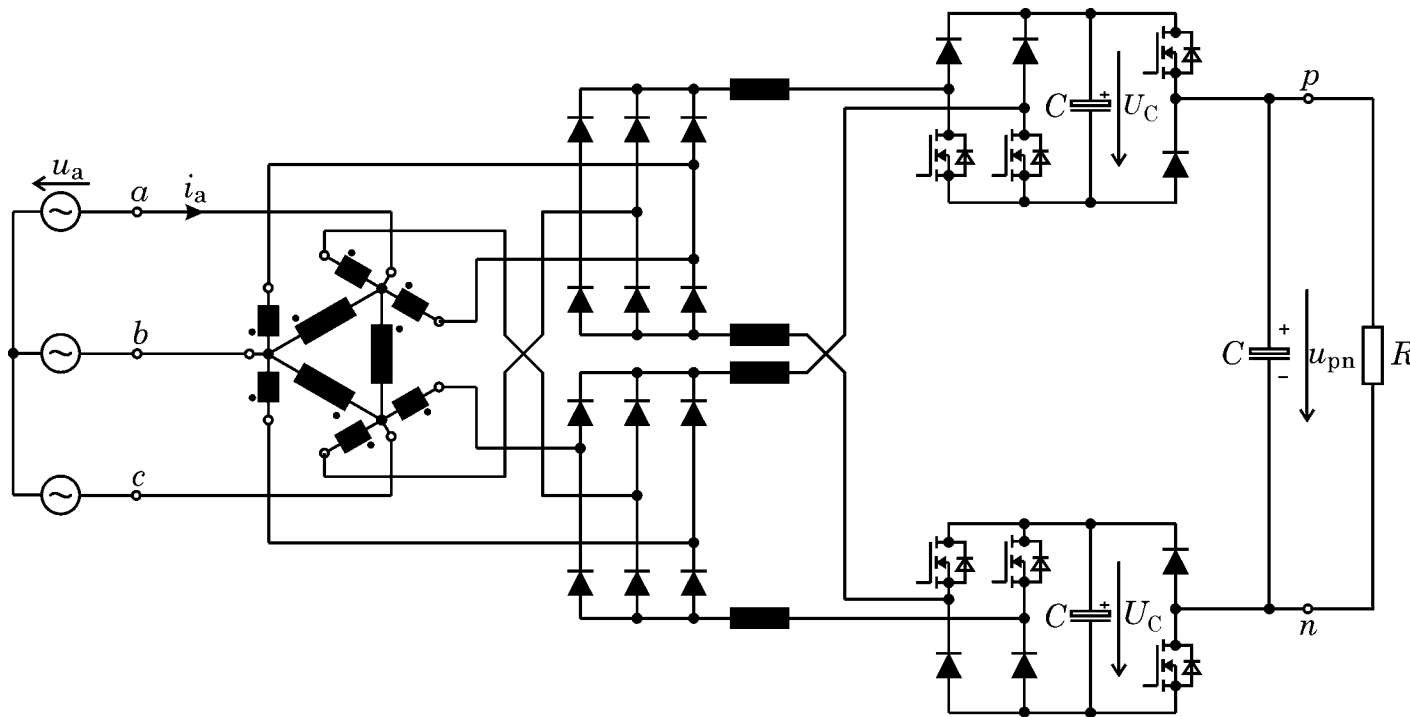
■ MERS Concept (Magnetic Energy Recovery Switch)



Fundamental Frequency Equivalent Circuit

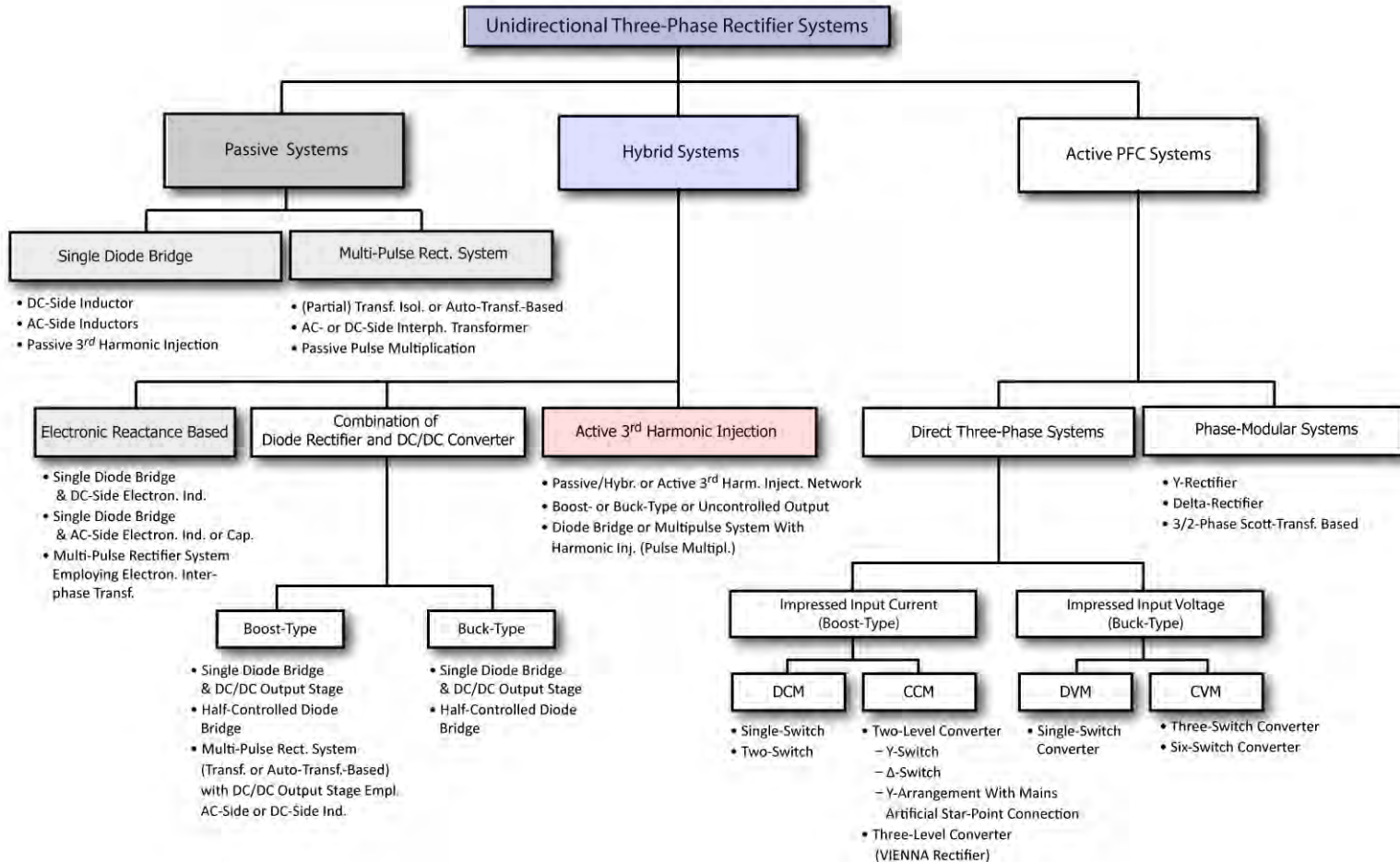


► 12-Pulse Rectifier Employing Electr. Interphase Transformer (EIT)

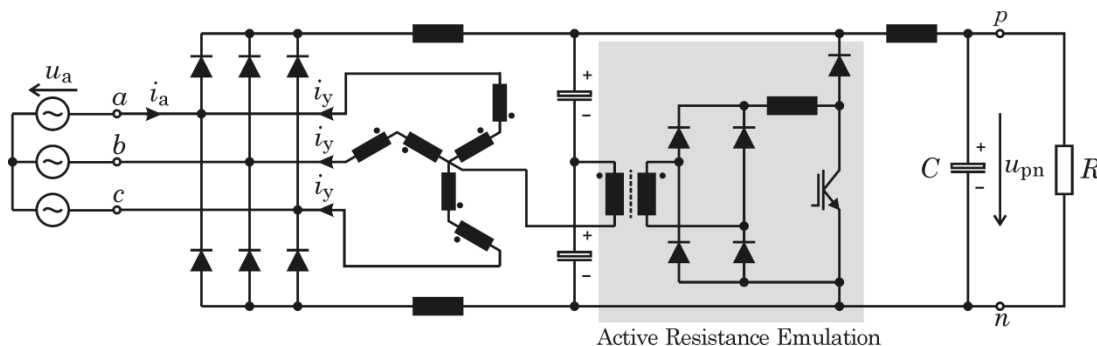


- Switching Frequency DC-Side Inductors
- Proper Control of the EIT Allows to Achieve *Purely Sinusoidal* Mains Current !

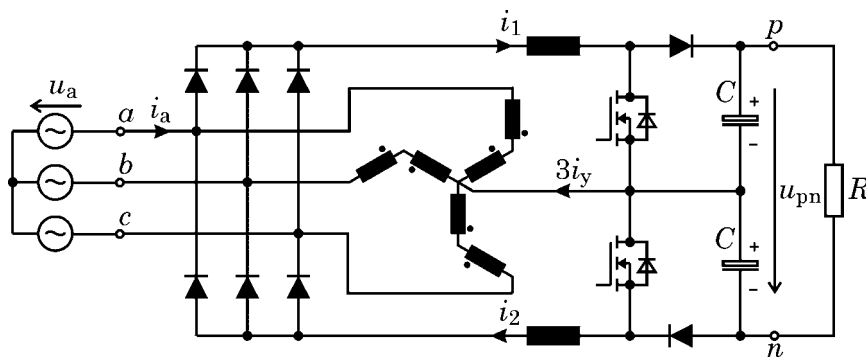
► Classification of Unidirectional Rectifier Systems



▶ Active 3rd Harmonic Injection into All Phases



- No Output Voltage Control
- Mains Current Close to Sinusoidal Shape



e.g.: $i_1 = I + 3/2 i_y$
 $i_2 = I - 3/2 i_y$

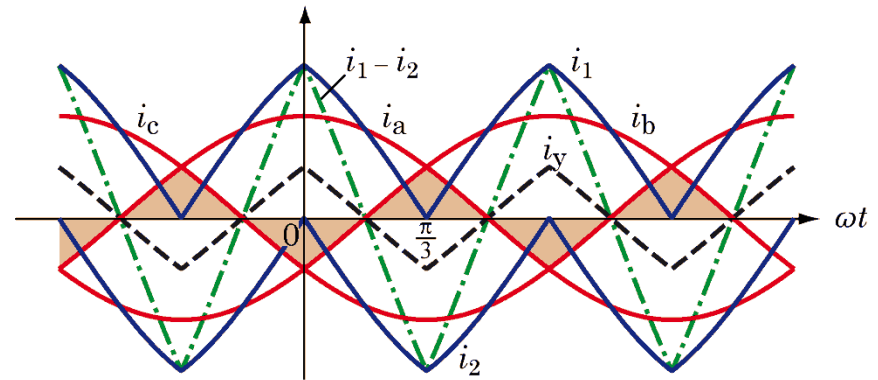
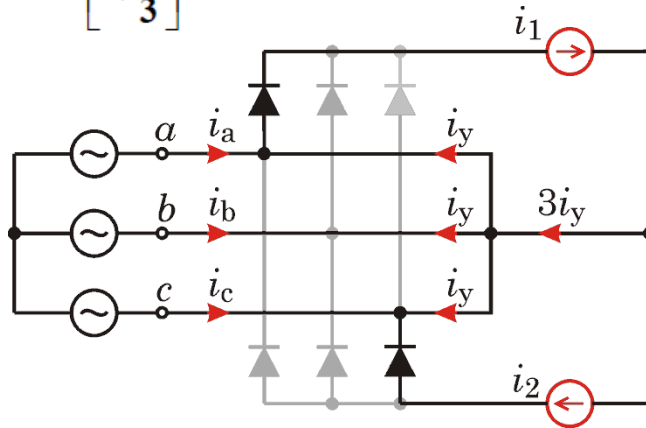
CCL: $3i_y = i_1 - i_2$

Minnesota Rectifier

- Controlled Output Voltage
- Purely Sinusoidal Shape of Mains Current

▶ Active 3rd Harmonic Injection into All Phases

$$\omega t \in \left[0, \frac{\pi}{3} \right]$$



$$i_a = \hat{I} \cos(\omega t)$$

$$i_b = \hat{I} \cos\left(\omega t - \frac{2\pi}{3}\right)$$

$$i_c = \hat{I} \cos\left(\omega t + \frac{2\pi}{3}\right)$$

$$i_y = -i_b$$

$$i_1 = i_a + i_y$$

$$i_2 = -(i_c + i_y)$$

$$i_a + i_b + i_c = 0$$

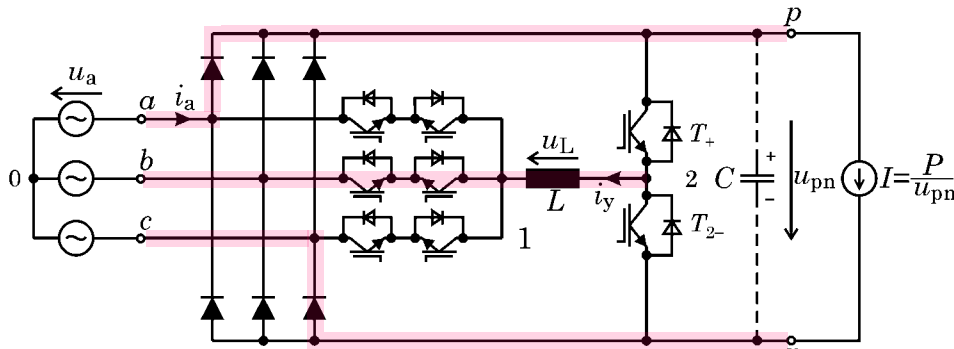
$$\begin{aligned} i_1 - i_2 &= i_a + i_y + i_c + i_y = \\ &= -i_b + 2i_y = 3i_y \end{aligned}$$



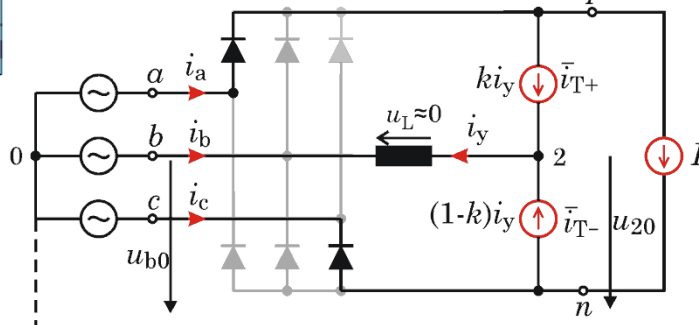
- Current Control Implementation with **Boost-Type DC/DC Converter (Minnesota Rectifier)** or with **Buck-Type Topology**

► Active 3rd Harmonic Inj. Only into One Phase (I)

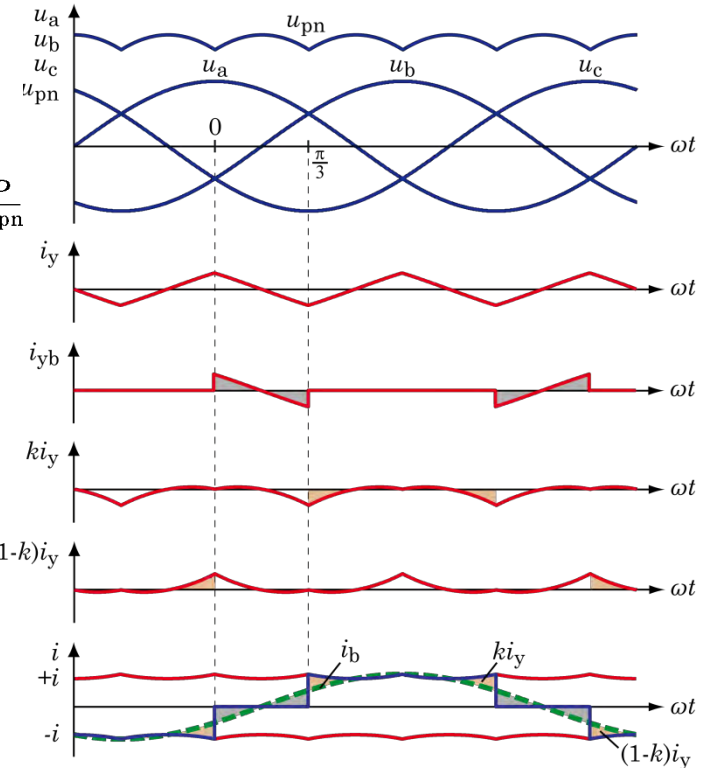
- + Purely Sinusoidal Mains Current (Only for Const. Power Load)
- + Low Current Stress on Active Semicond. / High Efficiency
- + Low Complexity
- No Output Voltage Control



$$\omega t \in \left[0, \frac{\pi}{3} \right]$$



- T_+, T_- Could be Replaced by Passive Network



■ Proof of Sinusoidal Mains Current Shape for $\omega t \in \left[0, \frac{\pi}{3}\right]$

- Current to be Inj. Into Phase b : $i_y = -i_b$

- Local Avg. Ind. Voltage / Bridge Leg (T_+ , T_-) Output Voltage:

$$\bar{u}_L \approx 0 \quad \text{and/or} \quad \bar{u}_{20} = u_{b0}$$

- Bridge Leg Voltage Formation:

$$\bar{u}_{20} = u_{b0} = k \cdot u_{a0} + (1-k)u_{c0}$$

$$u_{b0} = k \cdot u_{ac} + u_{c0}$$

$$k = \frac{u_{bc}}{u_{ac}}$$

- Bridge Leg Current Formation:

$$\bar{i}_{T_+} = k \cdot i_y = -k \cdot G \cdot u_{b0} = -G \cdot u_{b0} \frac{u_{bc}}{u_{ac}}$$

- Constant Power Load Current:

$$\begin{aligned} i &= \frac{P}{u_{ac}} = \frac{u_{ac} \cdot i_a + u_{bc} \cdot i_b}{u_{ac}} \\ &= G \frac{u_a \cdot u_{ac} + u_b \cdot u_{bc}}{u_{ac}} = G \left(u_{a0} + u_{b0} \frac{u_{bc}}{u_{ac}} \right) \end{aligned}$$

■ Sinusoidal Mains Current:

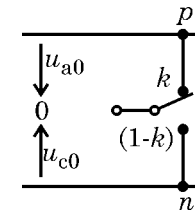
$$i + \bar{i}_{T_+} = G \cdot u_{a0} = i_a$$



$$i_a = G \cdot u_{a0}$$

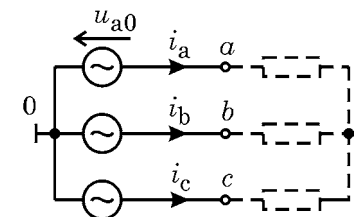
$$i_b = G \cdot u_{b0}$$

$$i_c = G \cdot u_{c0}$$



Condition:

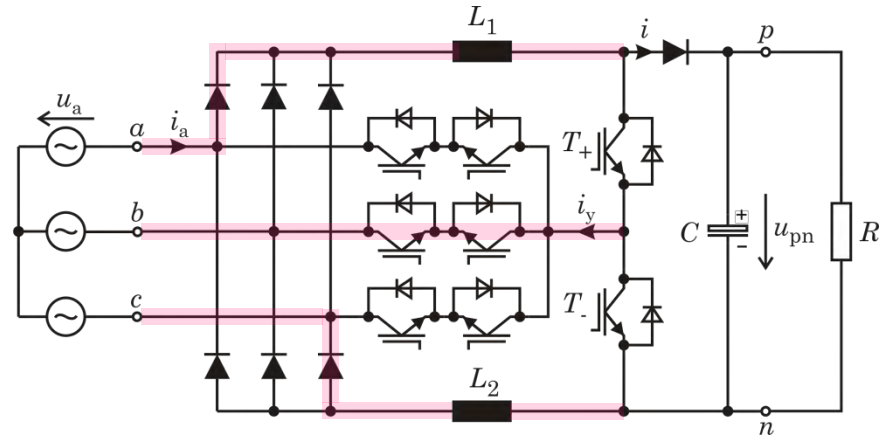
$$i_a + i_b + i_c = 0$$



► Active 3rd Harmonic Inj. Only into One Phase (II)

■ Boost-Type Topology

- + Controlled Output Voltage
- + Purely Sinusoidal Mains Current
- Power Semiconductors Stressed with Line-to-Line and/or Full Output Voltage



■ Proof of Sinusoidal Mains Current Shape for $\omega t \in \left[0, \frac{\pi}{3}\right]$ (1)

- 4 Different Switching States:

T_+ on, T_- off	}	k_1
T_+ off, T_- on	}	k_2
T_+ off, T_- off	}	$k_3 = (1 - k_1 - k_2)$
T_+ on, T_- on	}	

3 Different States Regarding the Current Paths with Relative On-Times k_1 , k_2 , and k_3

■ Proof of Sinusoidal Mains Current Shape for $\omega t \in \left[0, \frac{\pi}{3}\right]$ (2)

- Current to be Injected into b :

$$i_y^* = -i_b^*$$

$$i_a^* = G \cdot u_{a0}$$

- Inductor Voltages:

$$\bar{u}_{L,1}^* \approx 0 \quad \bar{u}_{L,2}^* \approx 0$$

$$i_b^* = G \cdot u_{b0}$$

$$i_c^* = G \cdot u_{c0}$$

- Bridge Leg (T_+ , T_-): Voltage Form.:

$$k_1 u_{ab} + k_2 (u_{ab} - U_{pn}) + (1 - k_1 - k_2) u_{ab} \stackrel{!}{=} 0$$

$$k_2 = \frac{u_{ab}}{U_{pn}}$$

$$k_1 (u_{bc} - U_{pn}) + k_2 u_{bc} + (1 - k_1 - k_2) u_{bc} \stackrel{!}{=} 0$$

$$k_1 = \frac{u_{bc}}{U_{pn}}$$

- Constant Power, Load Current:

$$\bar{i} = \frac{P}{U_{pn}} = \frac{u_{ab} i_a - u_{bc} i_c}{U_{pn}} = -k_1 i_c + k_2 i_a$$

- Current Formation in T_+ :

$$\bar{i}_{T_+} = k_1 i_y^* + (1 - k_1 - k_2) i_a^*$$

Condition: $i_a^* + i_b^* + i_c^* = 0$

■ Sinusoidal Mains Current:

$$\bar{i}_{T_+} + \bar{i}^* = i_a^*$$



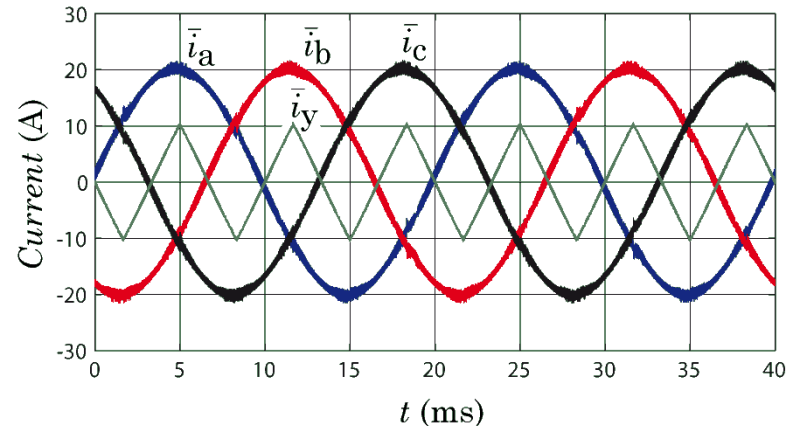
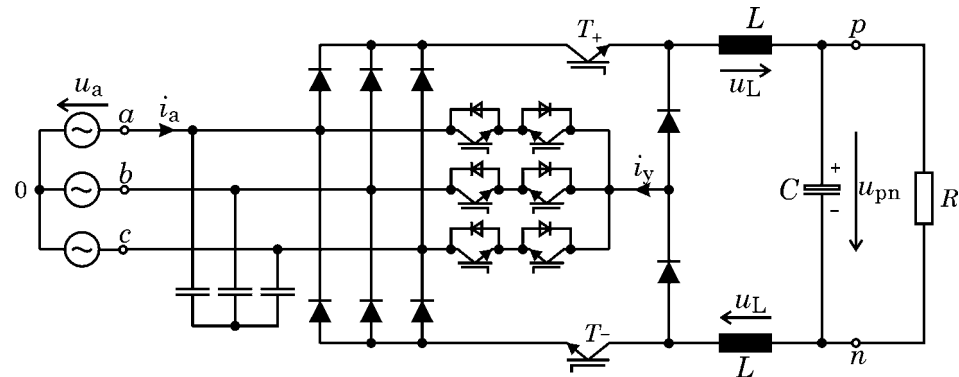
▶ Active 3rd Harmonic Inj. Only into One Phase (III)

■ Buck-Type Topology

- + **Controlled Output Voltage**
- + **Purely Sinusoidal Mains Current**
- + **Low Current Stress on the Inj. Current Distribution Power Transistors / High Eff.**
- + **Low Control Complexity**

- **Higher Number of Active Power Semiconductors than Active Buck-Type PWM Rect. (but Only T_+ , T_- Operated with Switching Frequency)**

$$\begin{aligned}
 U_{N,LL} &= 400V_{\text{rms}} \\
 U_{pn} &= 400V_{\text{DC}} \\
 P &= 10\text{kW}
 \end{aligned}$$



- **Patent Pending**
- **Switches Distributing the Injected Current could be Replaced by Passive Network**

■ Proof of Sinusoidal Mains Current Shape for $\omega t \in \left[0, \frac{\pi}{3}\right]$

- Current to be Inj. into Phase *b*:

$$i_y = -i_b$$

Duty Cycles: $T_+ \} k_1$
 $T_- \} k_2$

- Current Formation:

$$k_1 I = i_a \quad k_2 I = -i_c$$

$$i_y = -(1 - k_1)I + (1 - k_2)I = -i_b$$

$$i_a + i_b + i_c = 0$$

$$i_a = G \cdot u_{a0}$$

$$i_b = G \cdot u_{b0}$$

$$i_c = G \cdot u_{c0}$$

- Local Avg. Ind. Voltage :

$$\bar{u}_L \approx 0$$

- Voltage Formation:

$$k_1 u_a + (1 - k_1)u_b - (k_2 u_c + (1 - k_2)u_b) = u_{pn}$$

$$k_1 u_{ab} - k_2 u_{cb} = u_{pn}$$

$$i_a u_{ab} + i_c u_{cb} = u_{pn} I$$

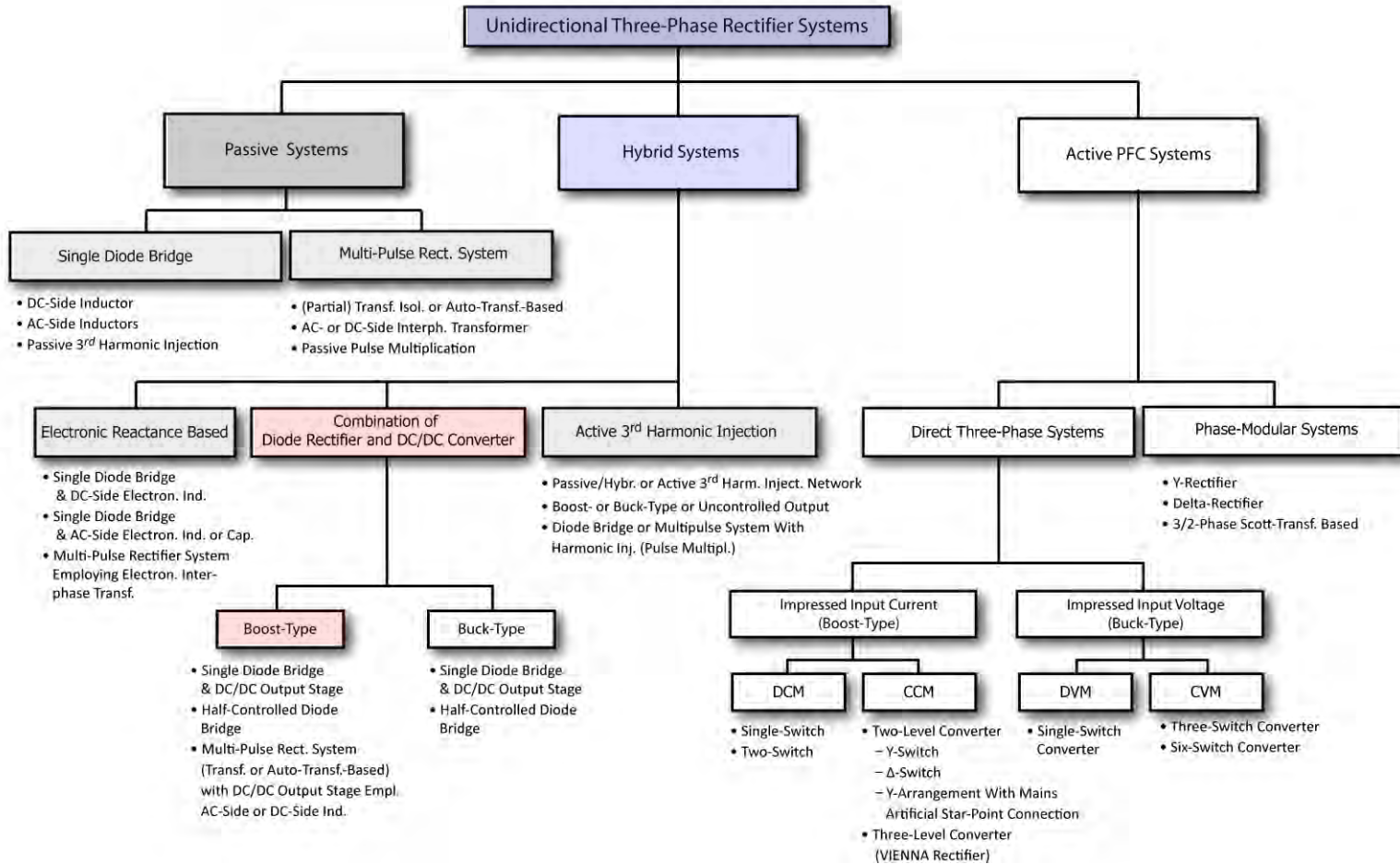
$$k_1 I = i_a$$

$$k_2 I = -i_c$$

$$i_a u_{ab} + i_c u_{cb} = P = \text{const.}$$

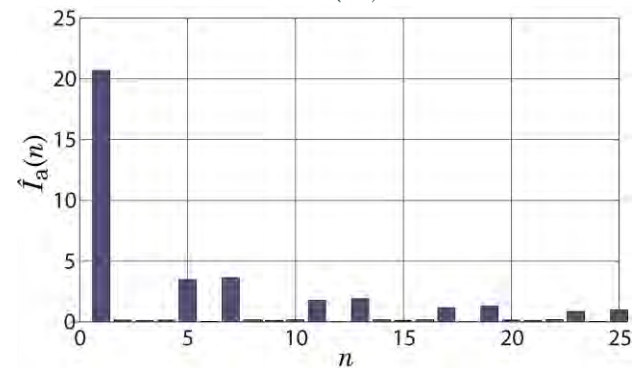
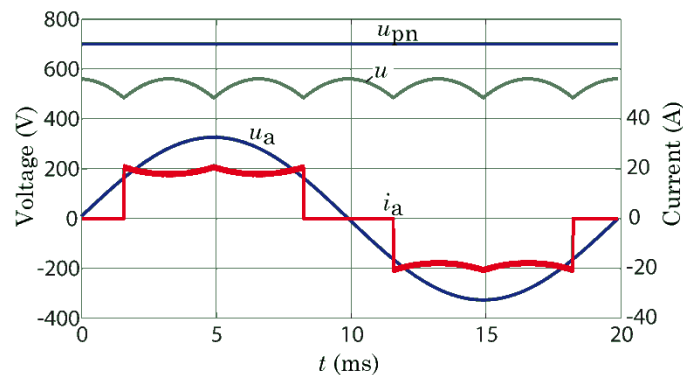
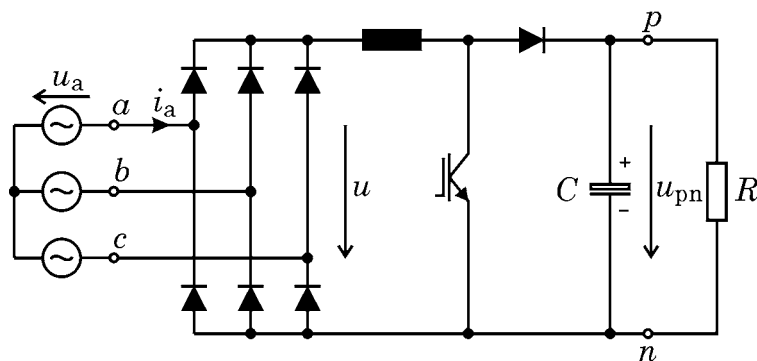
$$I = \text{const.} \rightarrow u_{pn} = \text{const.}$$

► Classification of Unidirectional Rectifier Systems



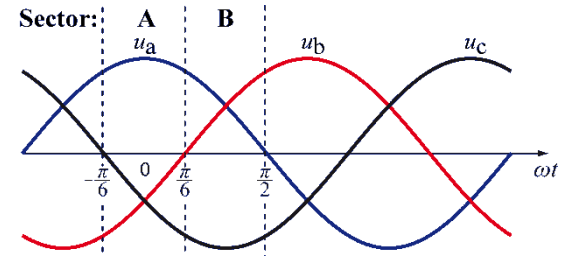
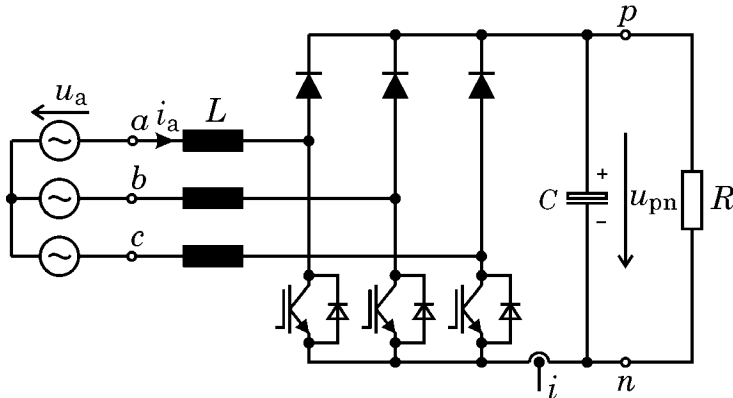
► Diode Bridge Combined with DC/DC Boost Converter

$U_{LL} = 3 \times 400 \text{ V}$ ($f_N = 50 \text{ Hz}$)
 $P_{out} = 10 \text{ kW}$
 $\lambda = 0.952$
 $\text{THD} = 32 \%$



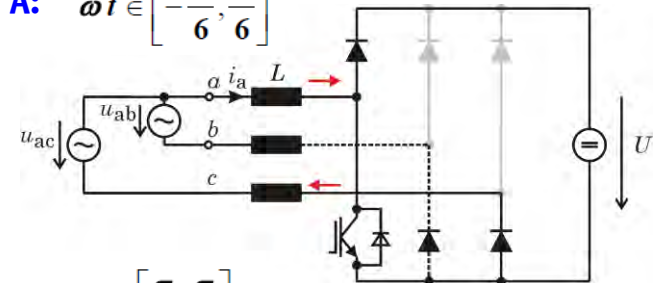
- Other Diode Bridge Output Current Impressing DC/DC Converter Topologies (e.g. SEPIC, Cuk) result in Same Mains Current Shape

► Half-Controlled Rectifier Bridge Boost Converter

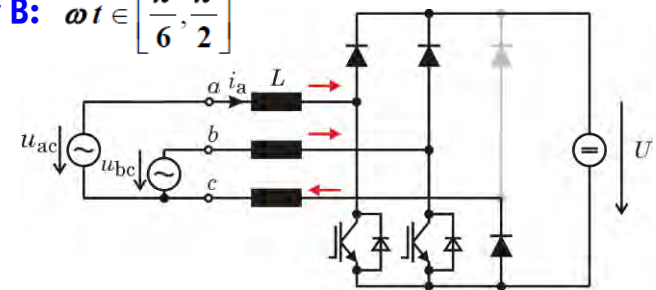


- Sinusoidal Current Control Only in Sectors with 2 Positive Phase Voltages, e.g. in Sector B
- In other Sectors, Only One Phase Current could be Shaped, e.g. in Sector A
- + Controlled Output Voltage ($U > \sqrt{6} \hat{U}$)
- + Low Complexity (e.g. Single Curr. Sensor)
- + Low Conduction Losses
- Block Shaped Mains Current

Sector A: $\omega t \in \left[-\frac{\pi}{6}, \frac{\pi}{6}\right]$



Sector B: $\omega t \in \left[\frac{\pi}{6}, \frac{\pi}{2}\right]$



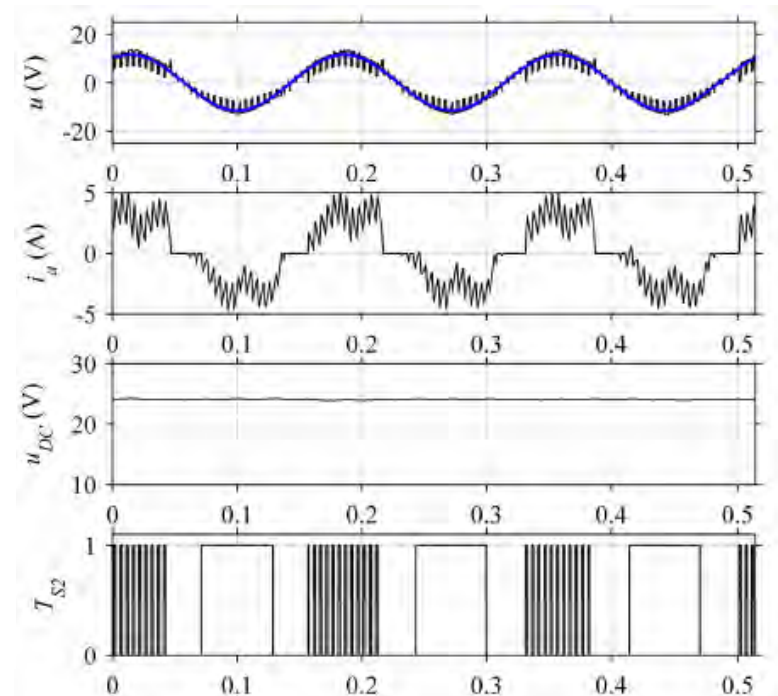
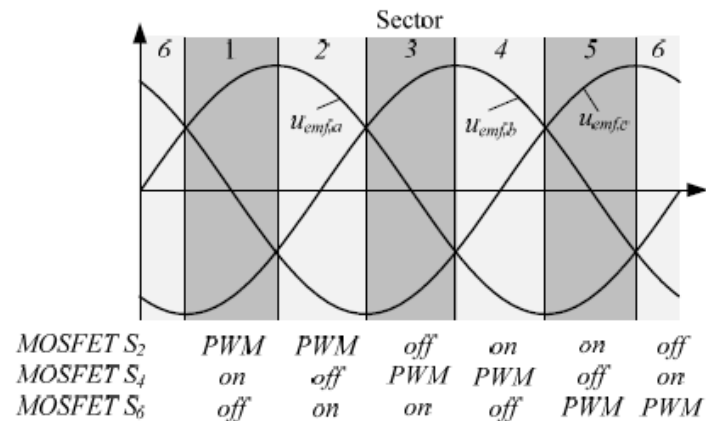
► Half-Controlled Rectifier Bridge Boost-Type Converter

■ Current Control Concepts

Option 1: All Switches Simultaneously Controlled with Same Duty-Cycle (Synchr. Modulation)

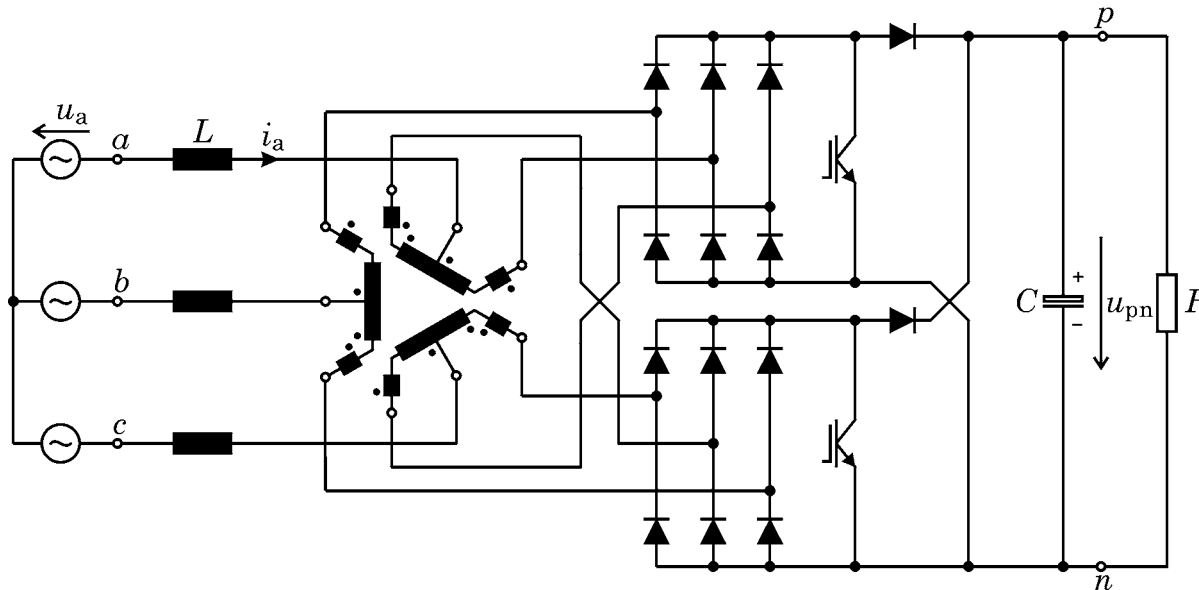
Option 2: Only Phase with most Positive Voltage is Modulated, Switch of Phase with most Neg. Voltage is Cont. Turned on for Lowering Conduction Losses in Case of Switch Implementation with MOSFETs. Middle Phase Switch is OFF; Results in Block Shaped Mains Current

Control Acc. to Option 2



► Boost-Type Auto-Transf.-Based 12-Pulse Hybrid Rectifier

■ Impressed Diode Bridge Output Voltages



- + Output Voltage Controlled
- + Sinusoidal Mains Current Shaping Possible
- Active Converter Stage Processes Full Output Power
- Low Frequency Magnetics Employed

► Boost-Type Auto-Transf.-Based 12-Pulse Hybrid Rectifier

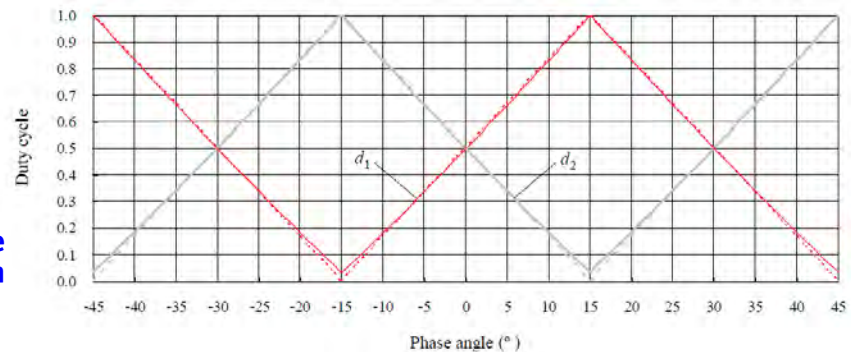
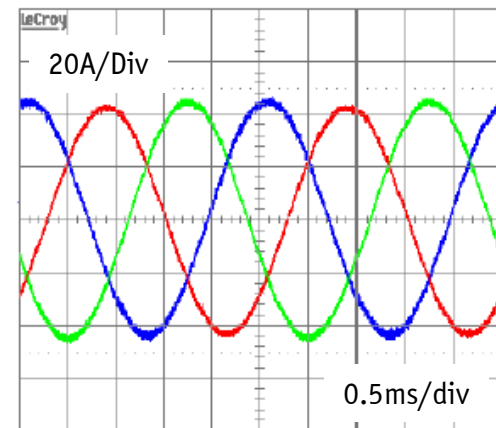
■ Experimental Results (Impressed Diode Bridge Output Voltages)

$U_{LL} = 3 \times 115 \text{ V (400 Hz)}$
 $P_o = 10 \text{ kW}$
 $U_o = 520 \text{ V}$
 $f_s = 60 \text{ kHz}$
 $\text{THD}_i = 3.1\%$



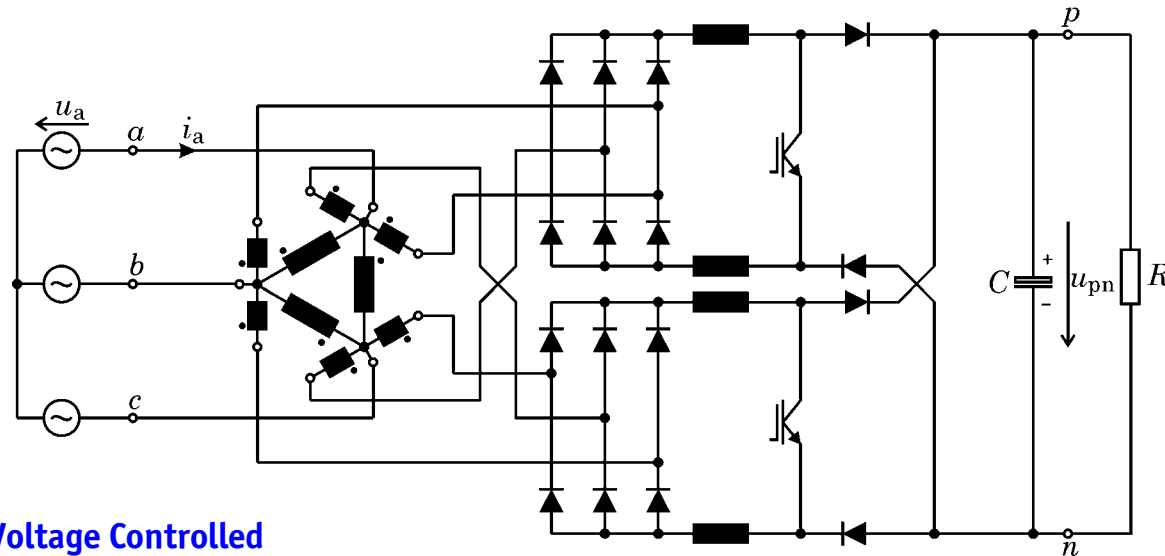
Duty Cycle
Variation

Input Currents



► Boost-Type Auto-Transf.-Based 12-Pulse Hybrid Rectifier

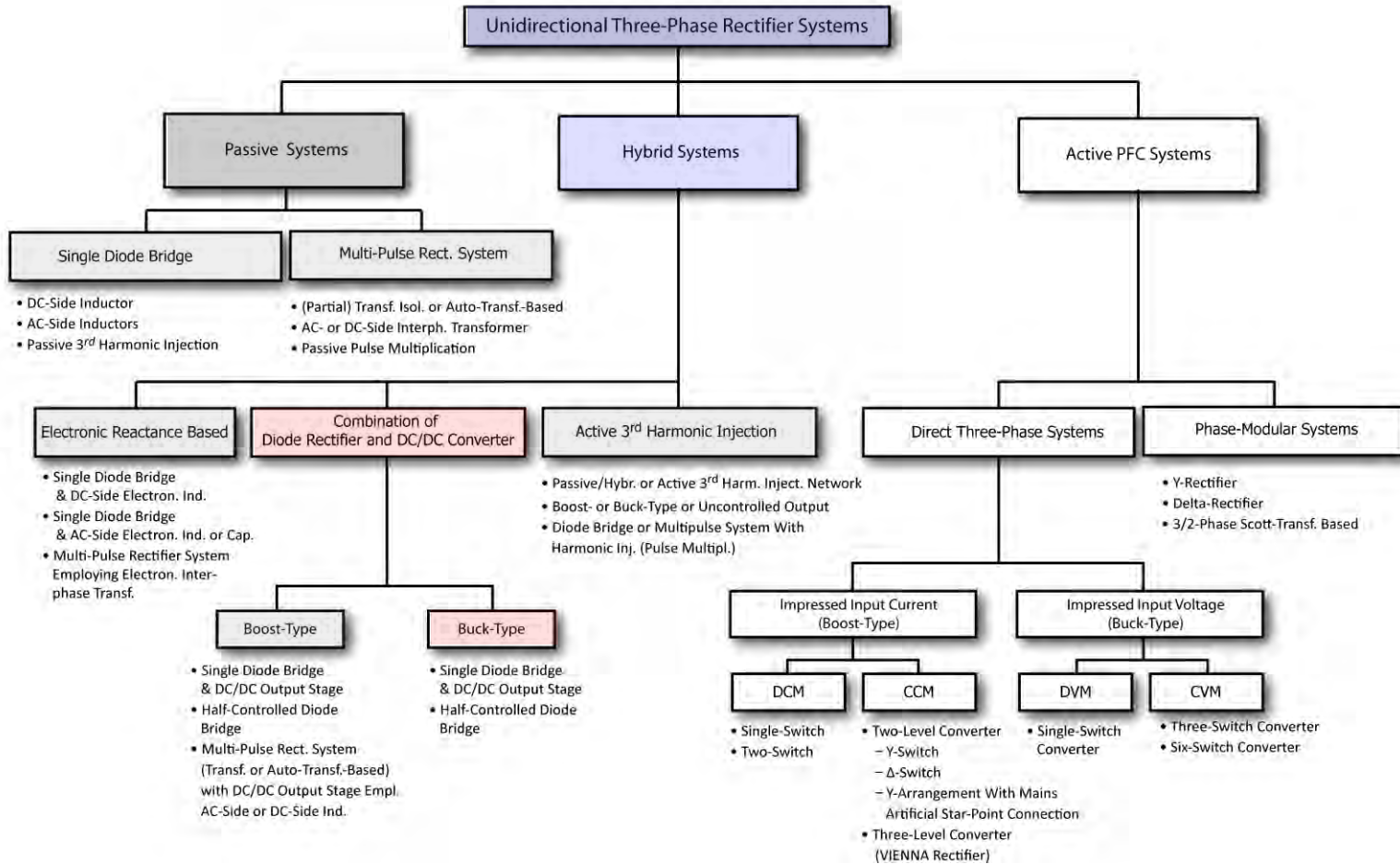
■ Impressed Diode Bridge Output Currents



- + Output Voltage Controlled
- + Sinusoidal Mains Current Shaping Possible
- Active Converter Stage Processes Full Output Power
- Low Frequency Magnetics Employed

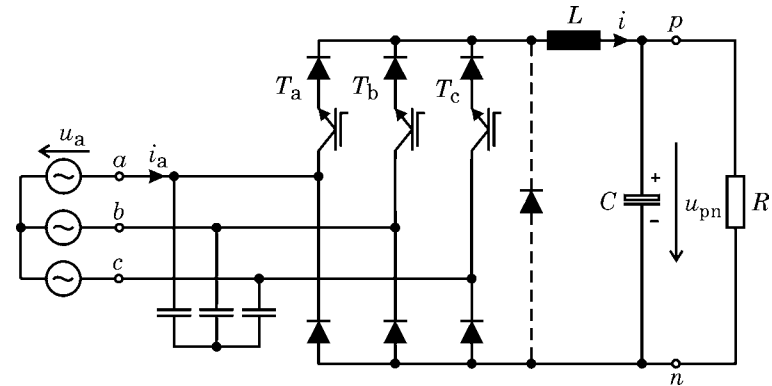
► Wide Variety of Further Topologies for Pulse Multiplication (e.g. 12p → 36p) which Process Only Part of Output Power but don't Provide Output Voltage Control

► Classification of Unidirectional Rectifier Systems

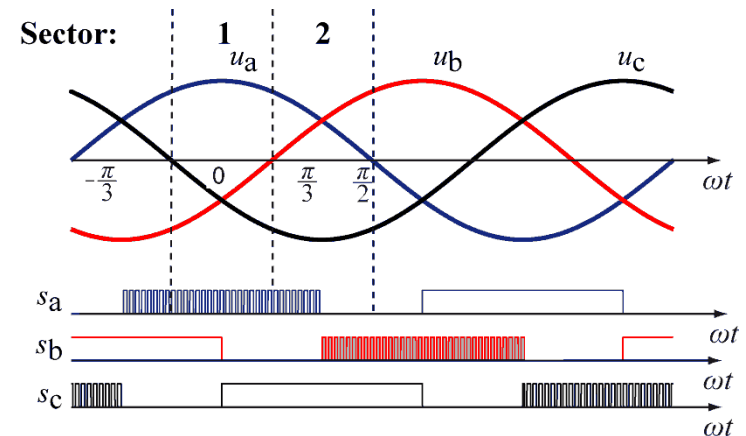


► Half-Controlled Rectifier Bridge Buck-Type Converter

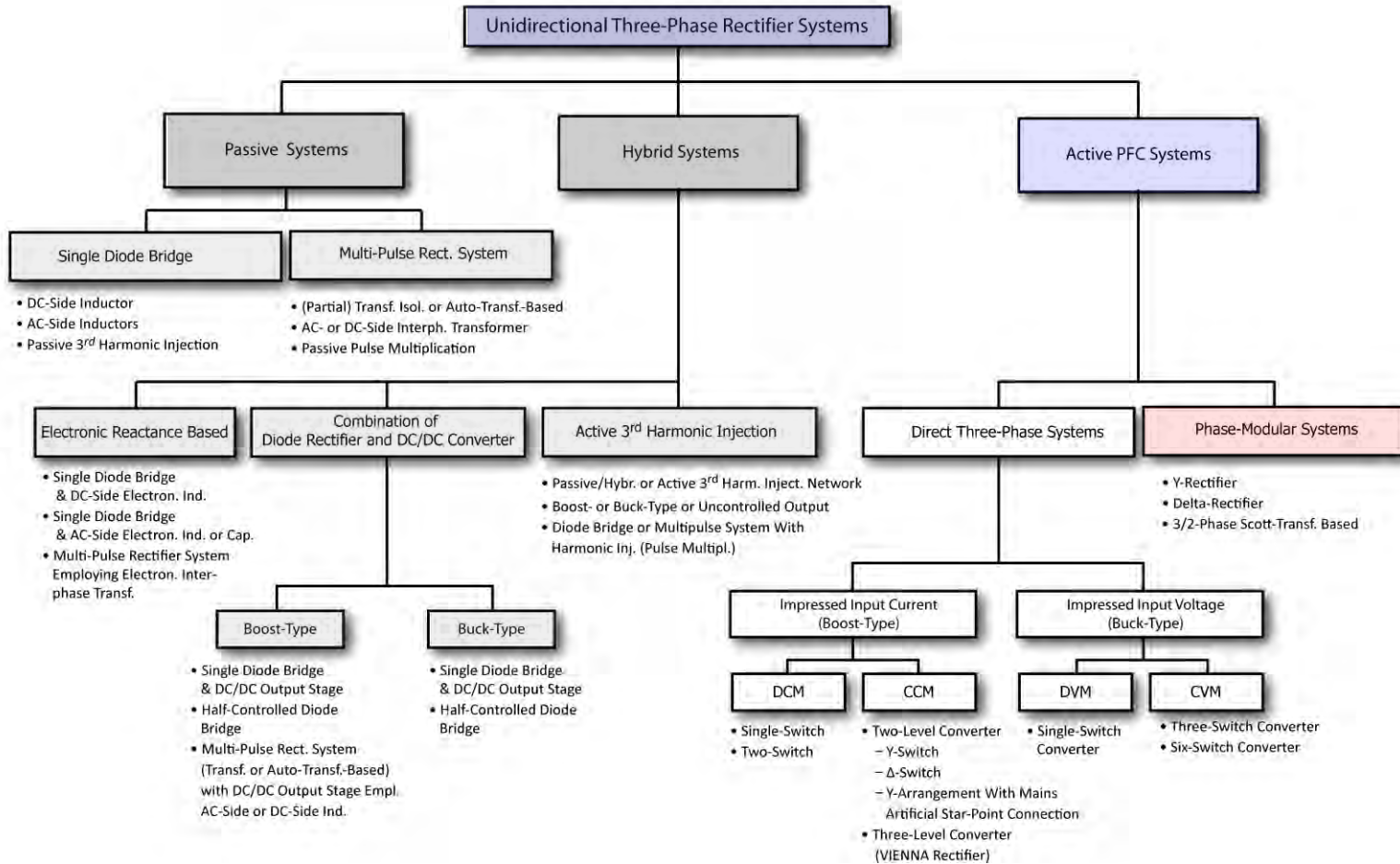
- + **Controlled Output Voltage**
- + **Low Complexity**
- + **Low Conduction Losses**
- **Block Shaped Mains Current**



- **Topology Limits Input Current Shaping to Intervals with Positive Phase Voltage**
 - Sector 1: Only i_a could be Controlled**
 - Sector 2: i_a and i_b could be Controlled**
- **Low Complexity Control: Only Current of Phase with most Positive Voltage Controlled; Switch of Phase with most Neg. Voltage Turned On Cont. for Providing a Free-Wheeling Path**

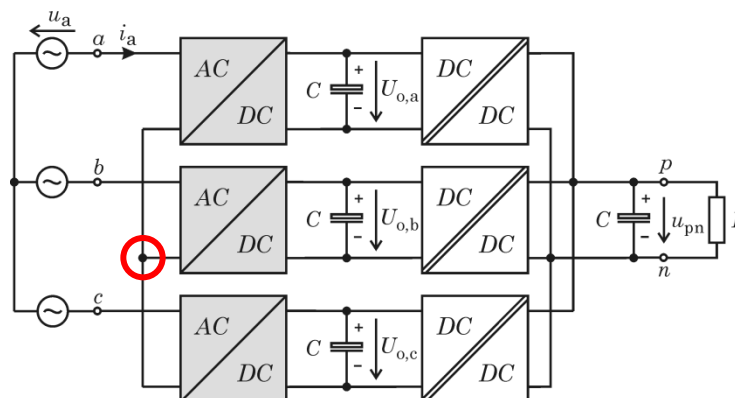


► Classification of Unidirectional Rectifier Systems

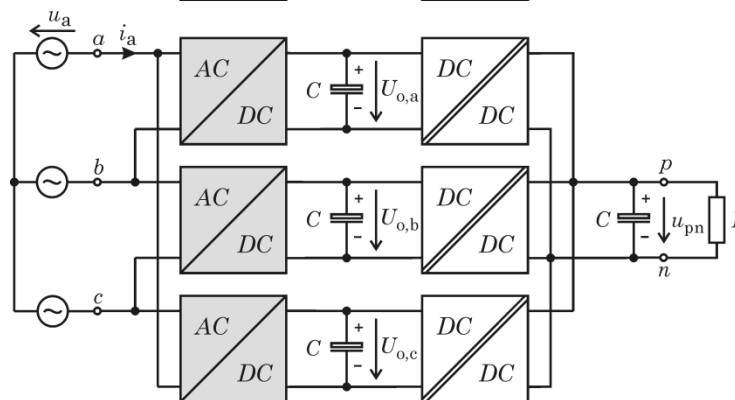


► Phase-Modular Rectifier Topologies

■ Y-Rectifier

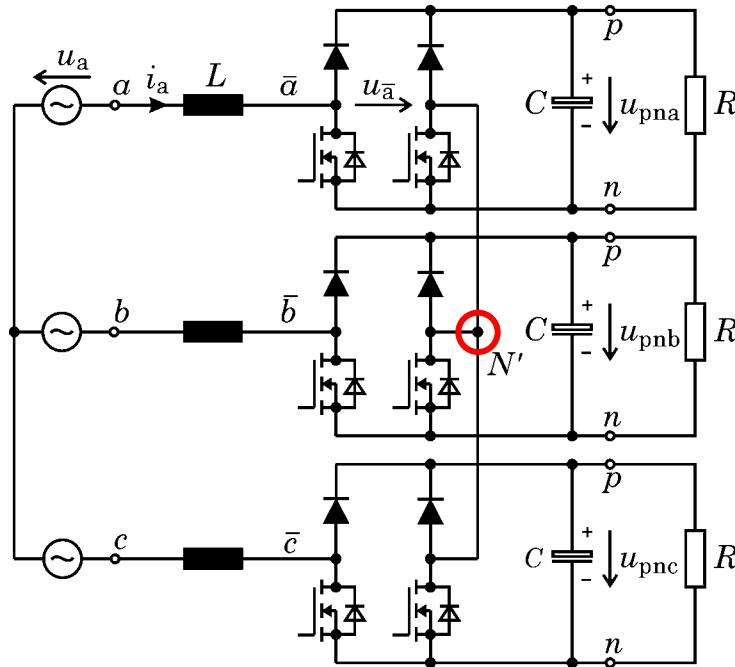


■ Δ-Rectifier

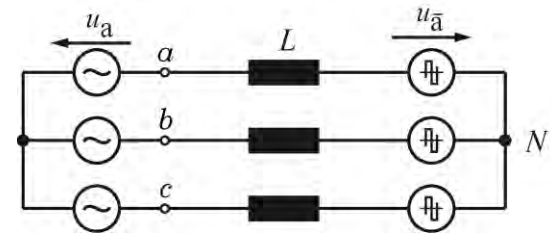


- Individual DC Output Voltages of the Phase Units
- Isolated DC/DC Converter Stages Required for Forming Single DC Output

► Y-Rectifier



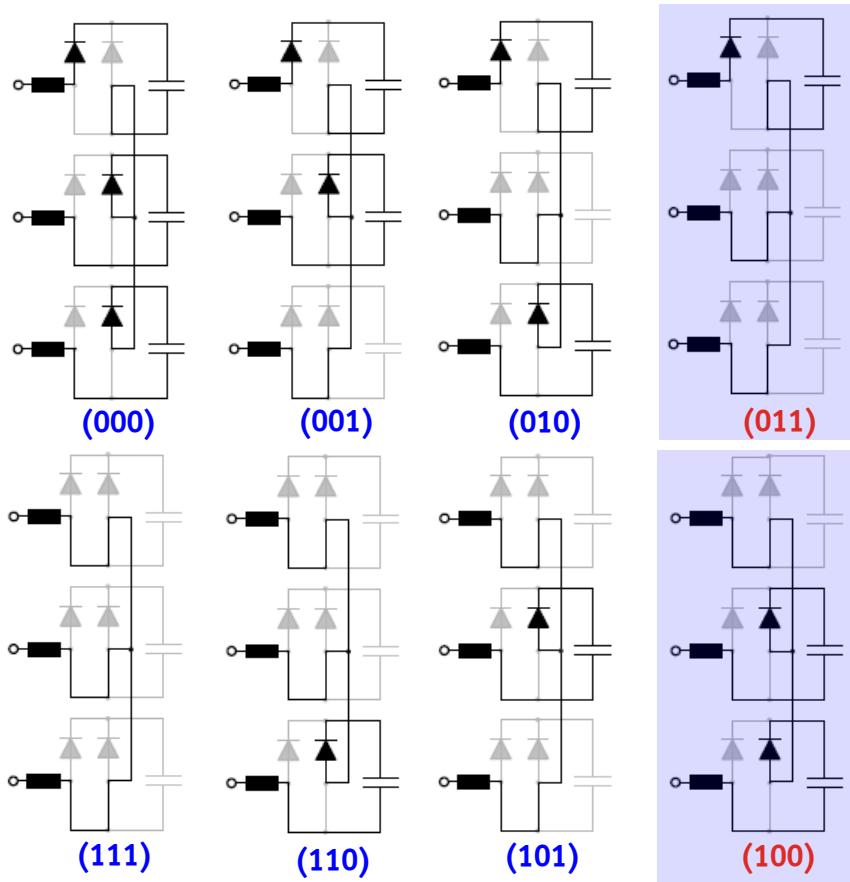
AC-Side Equivalent Circuit



- Basic AC-Side Behavior Analogous to Direct Three-Phase Three-Level Rectifier Systems

► Y-Rectifier

- Cond. States for $i_a > 0, i_b < 0, i_c < 0$ in Dep. on Transistor Switching States ($S_a S_b S_c$)

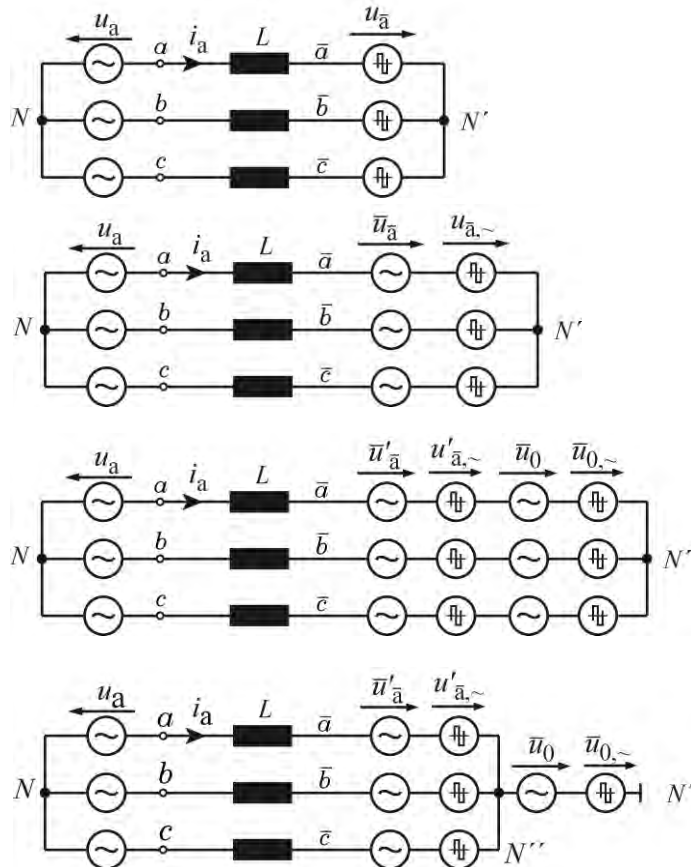


Switching States (011) and (100)

- Redundant Concerning Formation of $u_{\bar{a}\bar{b}}, u_{\bar{b}\bar{c}}, u_{\bar{c}\bar{a}}$
- Inverse Concerning Charging of C_a and C_c (and C_b)

► Y-Rectifier

■ Equivalent Circuit and Voltage Formation



$$u_{\bar{a}} = \bar{u}_{\bar{a}} + u_{\bar{a},\sim}$$

$$u_{\bar{b}} = \bar{u}_{\bar{b}} + u_{\bar{b},\sim}$$

$$u_{\bar{c}} = \bar{u}_{\bar{c}} + u_{\bar{c},\sim}$$

$$u_{\bar{a}} = u'_{\bar{a}} + u_0 \quad u'_{\bar{a}} + u'_{\bar{b}} + u'_{\bar{c}} \stackrel{!}{=} 0$$

$$u_{\bar{b}} = u'_{\bar{b}} + u_0$$

$$u_{\bar{c}} = u'_{\bar{c}} + u_0$$

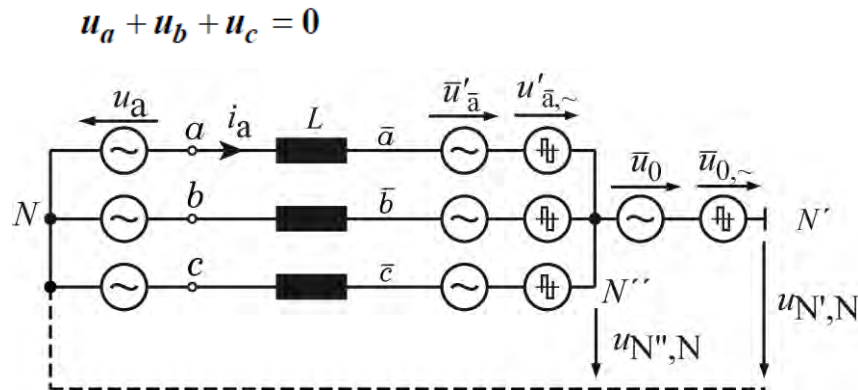
$$\Rightarrow u_0 = \frac{1}{3}(u_{\bar{a}} + u_{\bar{b}} + u_{\bar{c}})$$

$$\begin{aligned} \bar{u}_{\bar{a}} &= \bar{u}'_{\bar{a}} + \bar{u}_0 \\ u_{\bar{a},\sim} &= u'_{\bar{a},\sim} + u_{0,\sim} \end{aligned}$$

(shown at the Example of Phase a)

► Y-Rectifier

■ Equivalent Circuit and Voltage Formation



$$u_a = L \frac{di_a}{dt} + \bar{u}'_{\bar{a}} + u'_{\bar{a},\sim} + u_{N'',N}$$

$$u_b = L \frac{di_b}{dt} + \bar{u}'_{\bar{b}} + u'_{\bar{b},\sim} + u_{N'',N}$$

$$u_c = L \frac{di_c}{dt} + \bar{u}'_{\bar{c}} + u'_{\bar{c},\sim} + u_{N'',N}$$

$$0 = 0 + 0 + 0 + 3u_{N'',N}$$

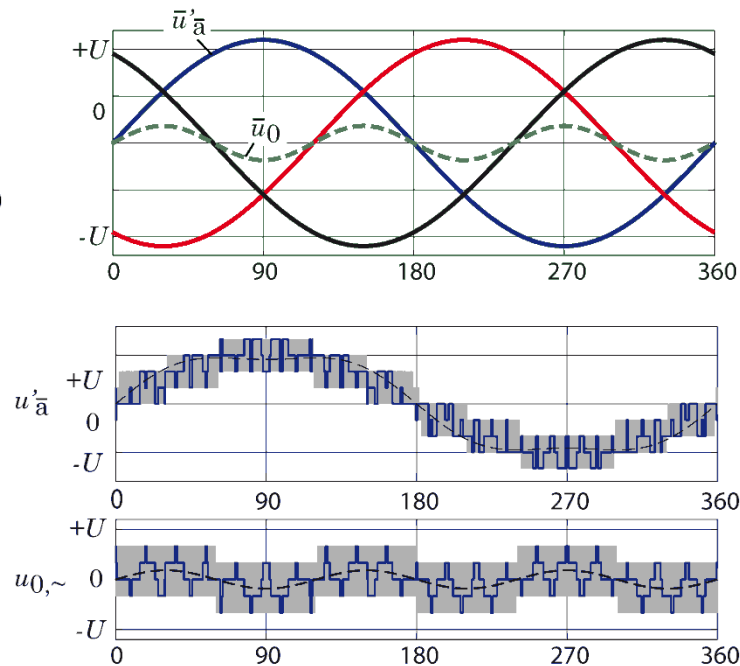
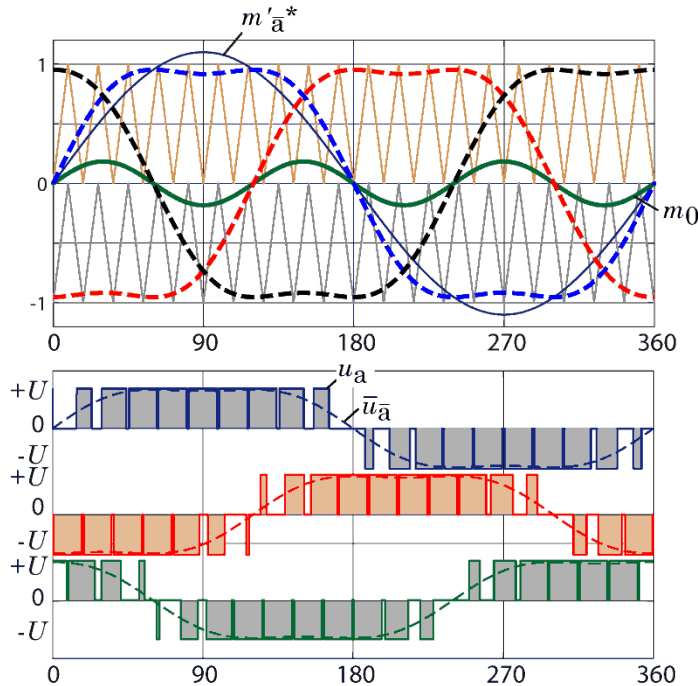


$$u_{N'',N} = 0$$

- Voltage of the Star Point N' Defined by u_0 (CM-Voltage)

► Y-Rectifier

■ Modulation and Voltage Formation



$$m'_a = \frac{\bar{u}'_a}{U}$$

$$m_0 = \frac{\bar{u}_0}{U}$$

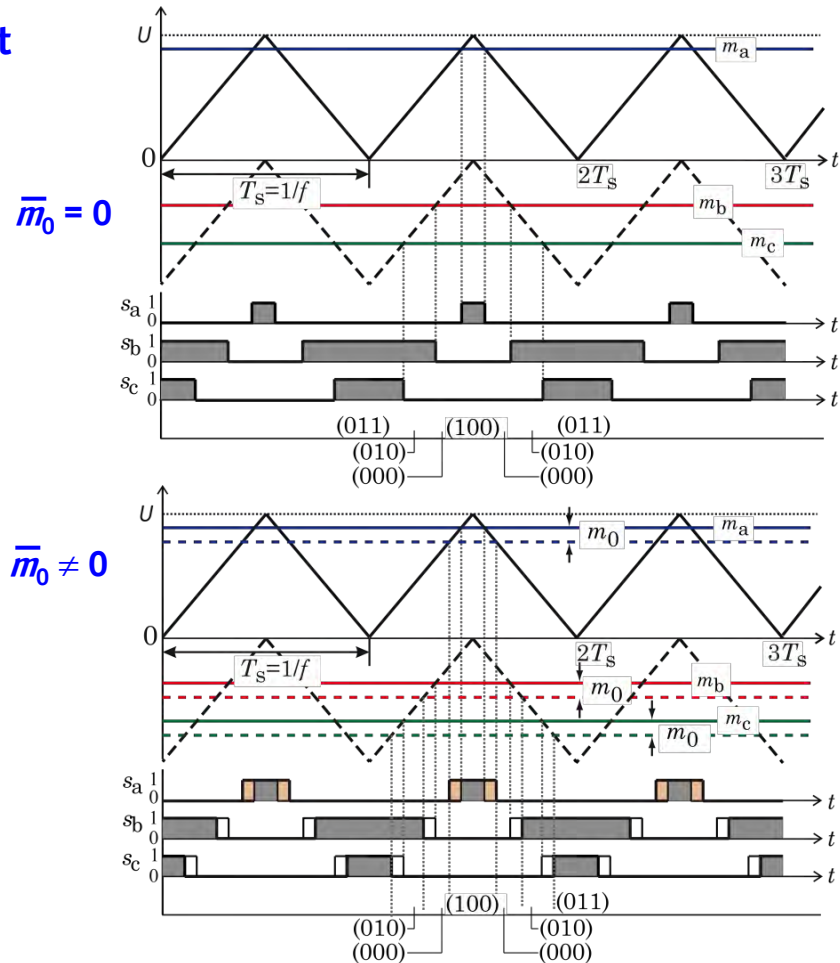
$$u_{0,\sim} = u_{NN',\sim}$$

- Addition of m_0 Increases Modulation Range from $\hat{U}_a = U$ to $\hat{U}_a = 2/\sqrt{3}U$
- Potential of Star Point N' Changes with LF (\bar{u}_0) and Switching Frequency ($u_{0,\sim}$)

► Y-Rectifier

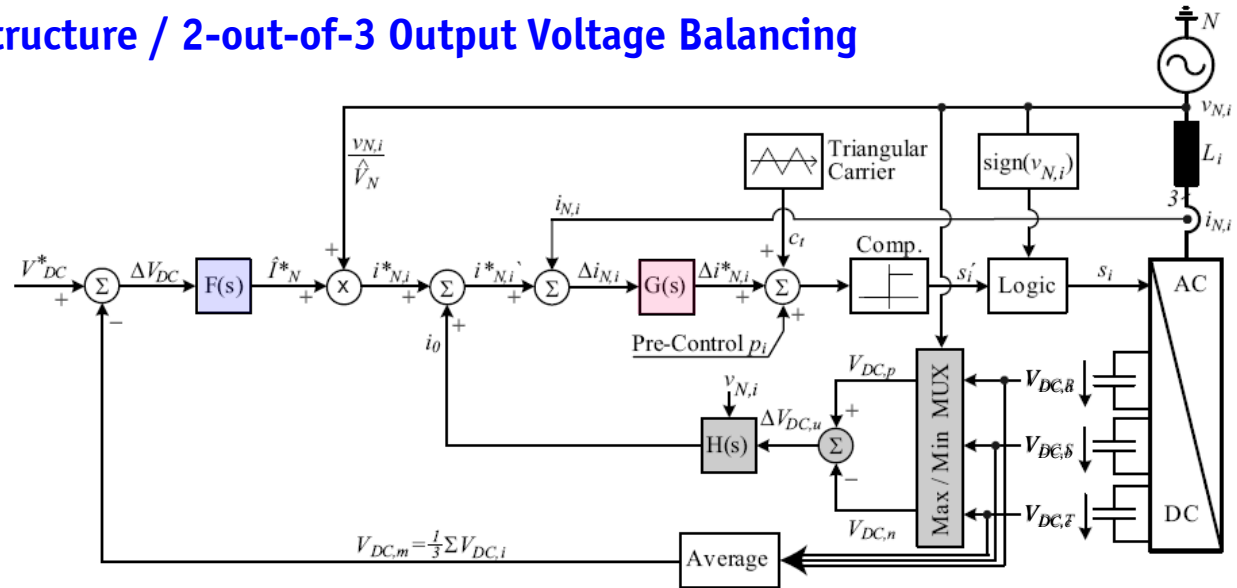
■ Balancing of Phase-Module DC-Output Voltages by DC Component of u_0 (\bar{m}_0)

- \bar{m}_0 Only Changes the On-Time of Redundant Switching Stages, e.g. (100) and (011)
- No Influence on the AC-Side Current Formation– Allows Balancing of the Module Output Voltages Independent of Input Current Shaping



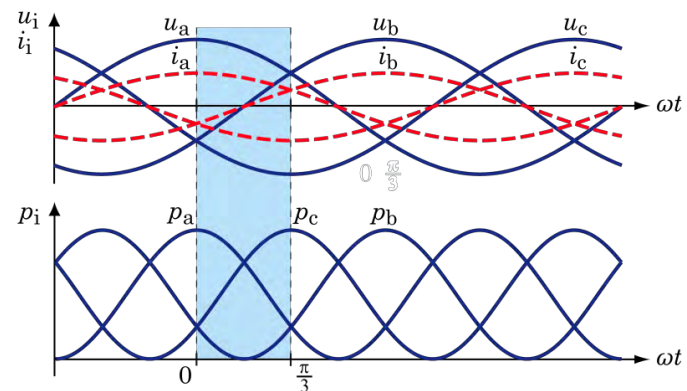
Y-Rectifier

Control Structure / 2-out-of-3 Output Voltage Balancing



E.g.: $\omega t \in \left[0, \frac{\pi}{3}\right]$ $\max(u_a, u_b, u_c) = u_a$
 $\min(u_a, u_b, u_c) = u_c$

- Output Voltage Balancing Considers Only Output Cap. Voltage of Phase with Max. Voltage (e.g. Phase a) and Phase with Min. Voltage (e.q. Phase b).



► Y-Rectifier

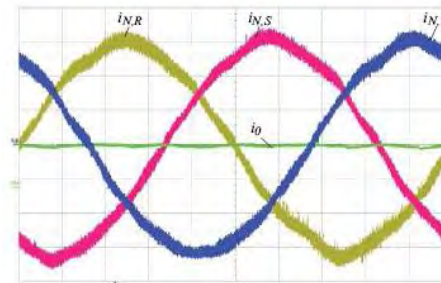
■ Experimental Verification of Output Voltage Balancing

- Symm. Loading $P_a = P_b = P_c = 1000 \text{ W}$
- Asymm. Loading $P_a = 730 \text{ W}, P_b = P_c = 1000 \text{ W}$

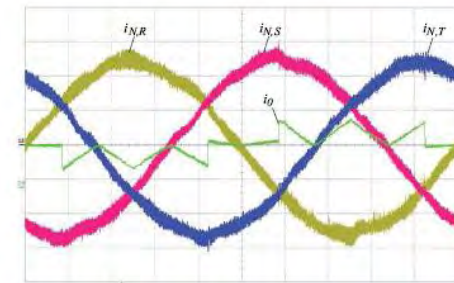
$U_N = 3 \times 230 \text{ V (50 Hz)}$
 $P_o = 3 \times 1 \text{ kW}$
 $U_o = 400 \text{ V}$
 $f_s = 58 \text{ kHz}$
 $L = 2.8 \text{ mH (on AC-side)}$
 $C = 660 \text{ }\mu\text{F}$



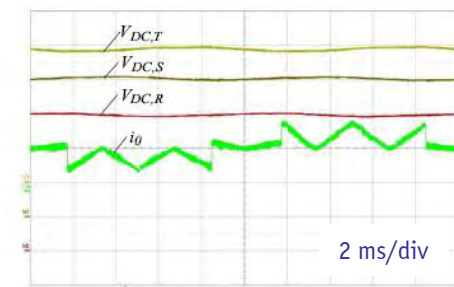
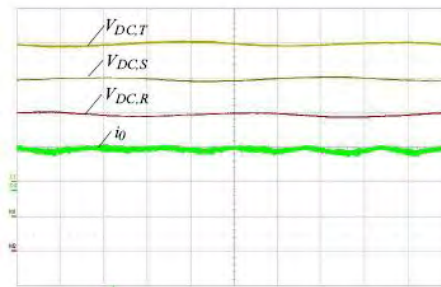
Symm. Loading



Asymm. Loading

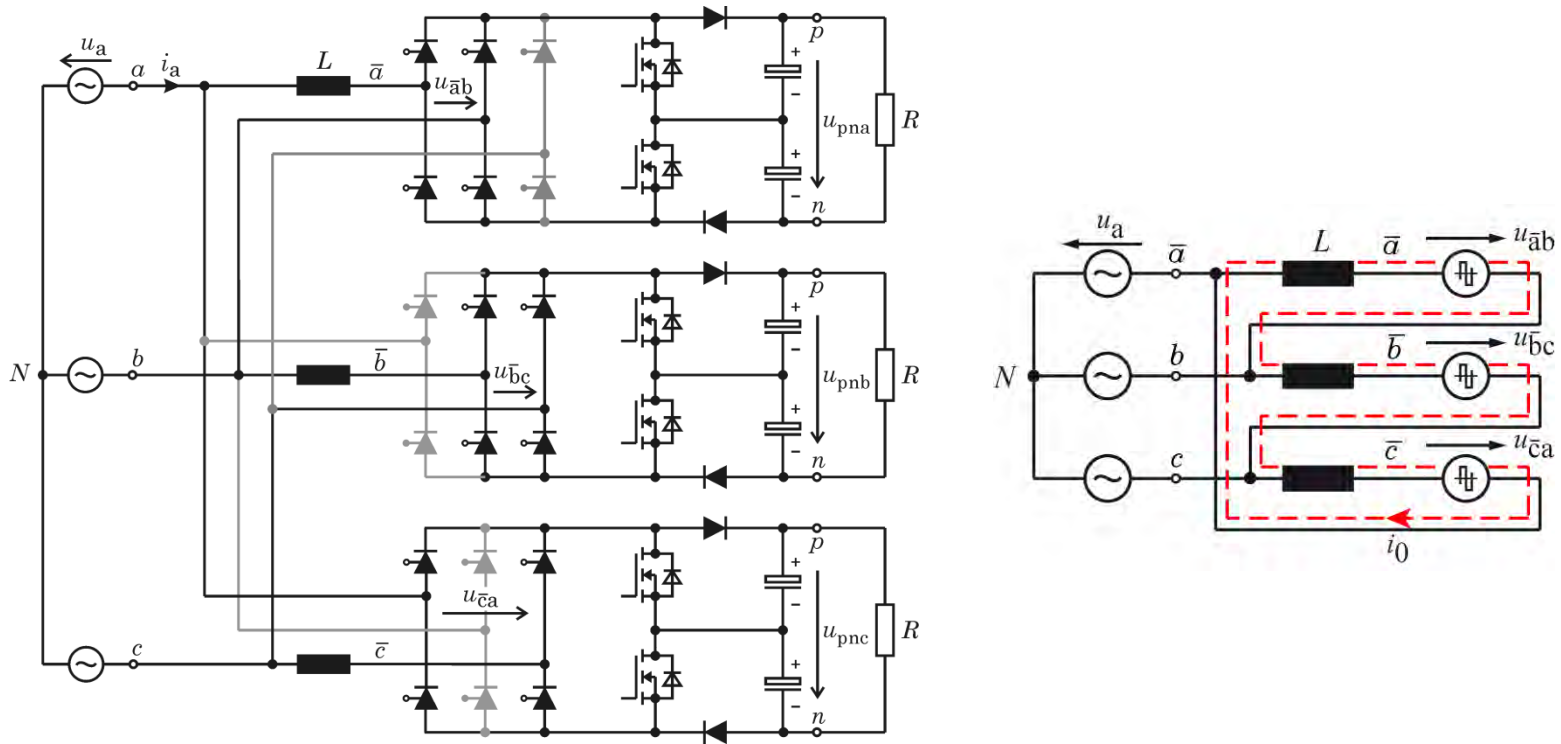

 Input Phase Currents, Control Signal i_0 , Output Voltages

$i_{N,i}: 1 \text{ A/div}$
 $V_{DC,i}: 100 \text{ V/div}$



2 ms/div

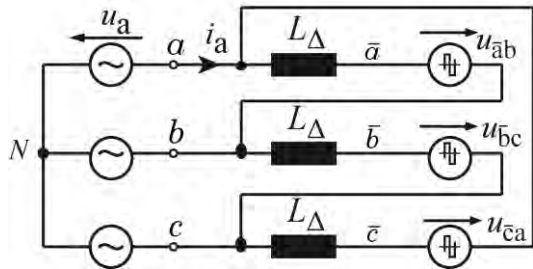
► Δ -Rectifier



- Connection of Each Module to All Phases / Rated Power also Available for Phase Loss !

► Δ -Rectifier

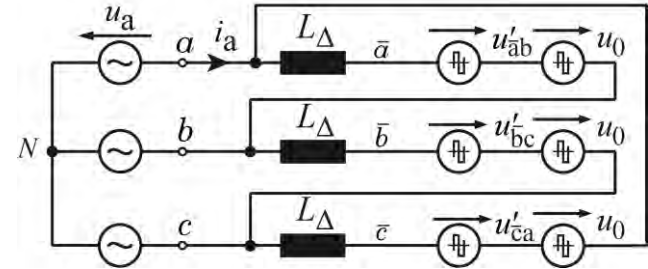
■ Derivation of Equivalent Circuit / Circulating Current Component i_0



$$u_{\bar{a}b} = u'_{\bar{a}b} + u_0$$

$$u_{\bar{b}c} = u'_{\bar{b}c} + u_0$$

$$u_{\bar{c}a} = u'_{\bar{c}a} + u_0$$

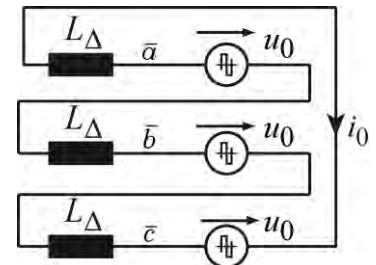
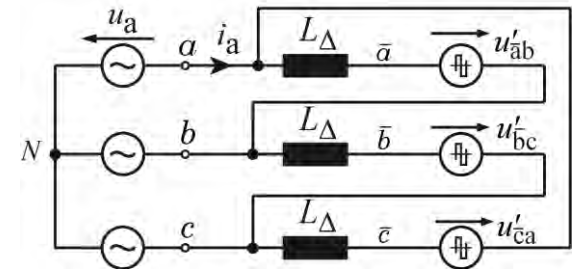


Def.: $u'_{\bar{a}b} + u'_{\bar{b}c} + u'_{\bar{c}a} = 0$

- Mains Phase Current Formed by $u'_{\bar{a}b}$, $u'_{\bar{b}c}$, $u'_{\bar{c}a}$ and u_a , u_b , u_c
- Circulating Current i_0 Formed by u_0

$$u_0 = \frac{1}{3}(u_{\bar{a}b} + u_{\bar{b}c} + u_{\bar{c}a})$$

- u_0 and/or i_0 , which does not appear in i_a , i_b and i_c , can be Maximized by Proper Synchron. of Module PWM Carrier Signals; Accordingly, Switching Frequency Components of $u'_{\bar{a}b}$, $u'_{\bar{b}c}$ and $u'_{\bar{c}a}$ are Minimized



► Δ -Rectifier

■ Y-Equivalent Circuit Describing Mains Current Formation

- **Equiv. Conc. No-Load Voltage at Terminals a, b, c (No Circ. Current i_0 , i.e. No Voltage Drop across L_Δ)**

$$u_{ab} = u'_{\bar{a}b} = u_{\bar{a}'} - u_{\bar{b}'}$$

$$u_{bc} = u'_{\bar{b}c} = u_{\bar{b}'} - u_{\bar{c}'}$$

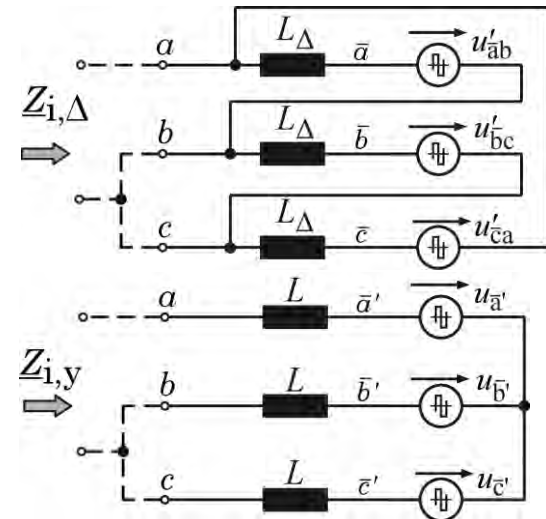
- **Equiv. Y-Voltage Syst. should not Contain Zero Sequ. Comp.**

$$u_{\bar{a}'} + u_{\bar{b}'} + u_{\bar{c}'} \stackrel{!}{=} 0 \quad \Rightarrow \quad \begin{aligned} u'_{\bar{b}c} &= u_{\bar{b}'} - (-u_{\bar{a}'} - u_{\bar{b}'}) \\ u'_{\bar{b}c} &= 2u_{\bar{b}'} + u_{\bar{a}'} \end{aligned}$$

$$u_{\bar{a}'} = \frac{1}{3}(u'_{\bar{a}b} - u'_{\bar{c}a})$$

$$u_{\bar{b}'} = \frac{1}{3}(u'_{\bar{b}c} - u'_{\bar{a}b})$$

$$u_{\bar{c}'} = \frac{1}{3}(u'_{\bar{c}a} - u'_{\bar{b}c})$$



- **Equiv. Concerning Input Impedance between any Terminals**

$$\underline{Z}_{i,\Delta} = \underline{Z}_{i,y} \quad \Rightarrow \quad L_\Delta // L_\Delta = \frac{1}{2}L_\Delta = L_Y + L_Y // L_Y = \frac{3}{2}L_Y$$

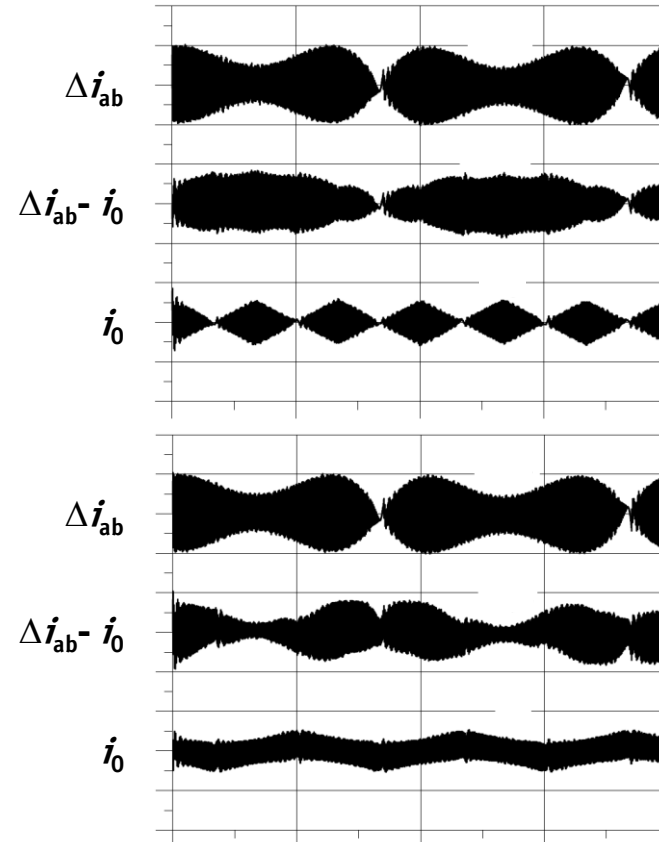
$$L_Y = \frac{1}{3}L_\Delta$$

► Δ -Rectifier

■ Circulating Current Max. / Minimization of Mains Current Ripple

$U_{LL} = 3 \times 480 \text{ V (50 Hz)}$
 $P_o = 5 \text{ kW}$
 $U_o = 800 \text{ V}$
 $f_s = 25 \text{ kHz}$
 $L = 2.1 \text{ mH (on AC-Side)}$

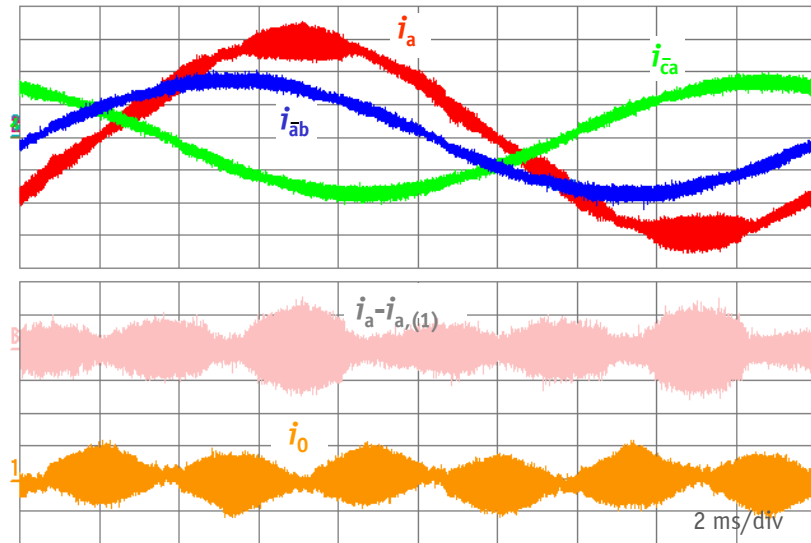
- For Proper Phase Shift of Module PWM Carrier Signals a Share of the Line-to-Line Current Ripple can be Confined into the Delta Connection.



► Δ -Rectifier

■ Experimental Results

$U_{LL} = 3 \times 480 \text{ V (50 Hz)}$
 $P_o = 5 \text{ kW}$
 $U_o = 800 \text{ V}$
 $f_s = 25 \text{ kHz}$
 $L = 2.1 \text{ mH (on AC-Side)}$



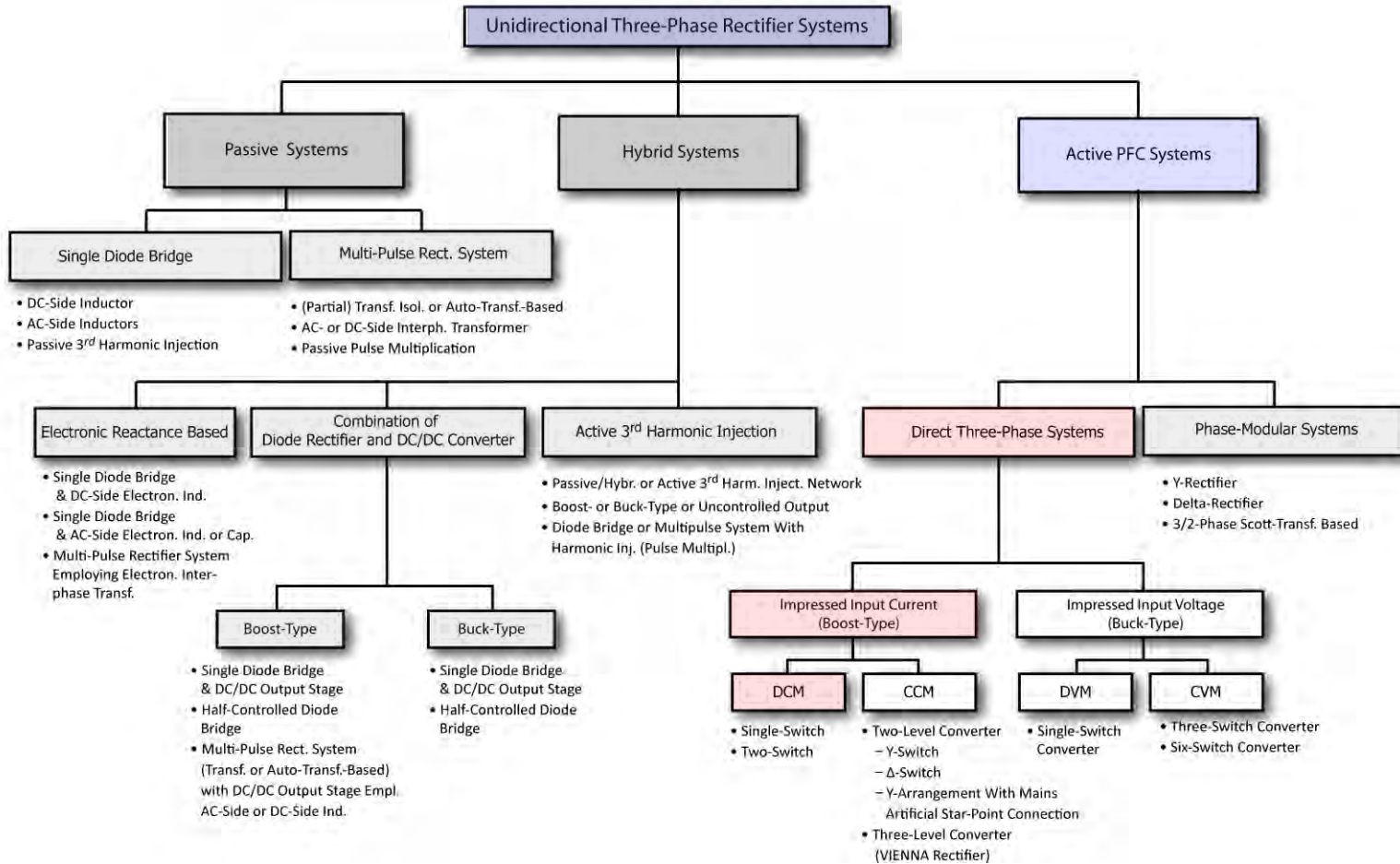
$i_a, i_{ab}, i_{ca}: 5 \text{ A/div}; \quad i_a - i_{a,(1)}, i_0: 2 \text{ A/div}$

- Formation of Input Phase Current $i_a = i_{ab} - i_{ca}$
- Circulating Zero Sequence Current i_0

Coffee Break !

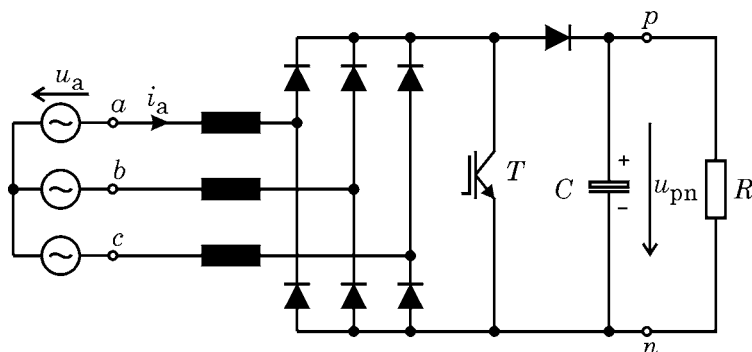


► Classification of Unidirectional Rectifier Systems

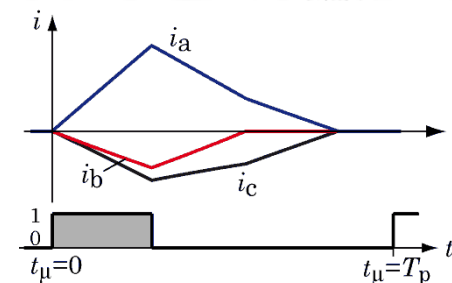
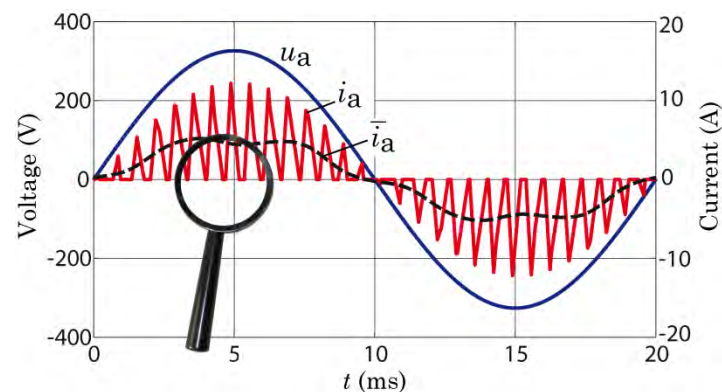


► Single-Switch + Boost-Type DCM Converter Topology

- + Low Complexity / Single Switch
- + No PWM, Constant Duty Cycle Operation
- + No Current Measurement
- High Peak Current Stress
- Low Freq. Distortion of Mains Currents / Dep. on U_{pn}/\hat{U}
- High EMI Filtering Effort

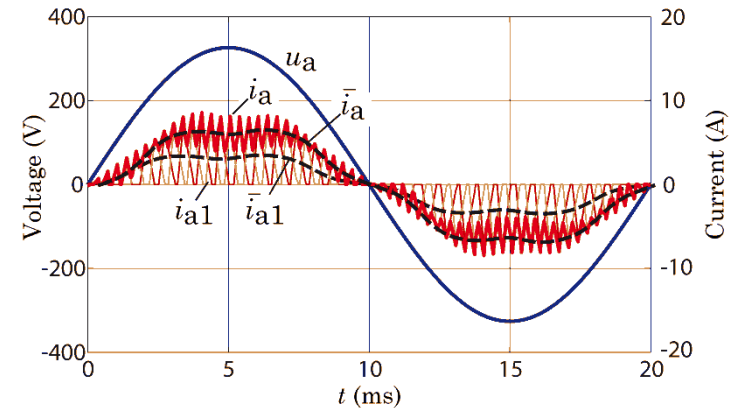
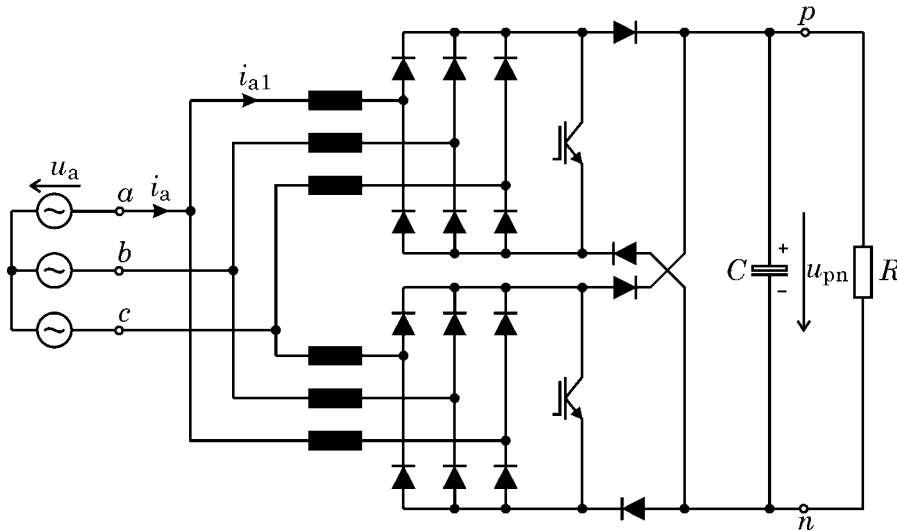


$U_{LL} = 3 \times 400 \text{ V (50Hz)}$
 $P_o = 2.5 \text{ kW}$
 $U_o = 800 \text{ V}$
 $\text{THD}_i = 13.7 \%$



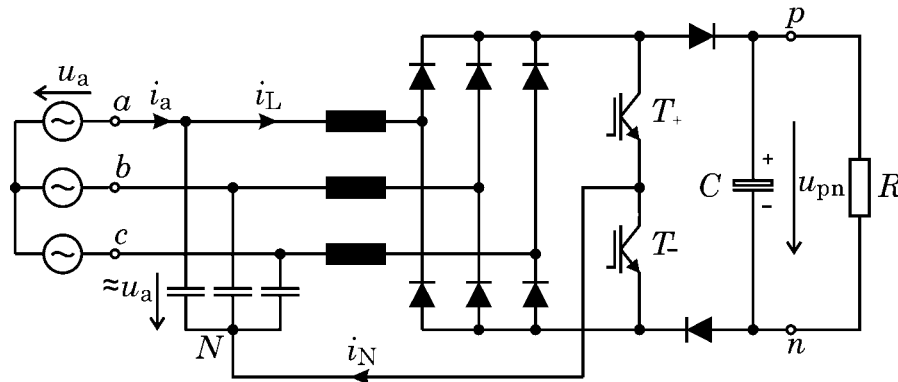
- Improvement of Mains Current Shape by 6th Harmonic Duty Cycle Modulation or Boundary Mode Operation
- Reduction of EMI Filtering Effort by Interleaving

▶ Two Interleaved Single-Switch Boost-Type DCM Converter Stages



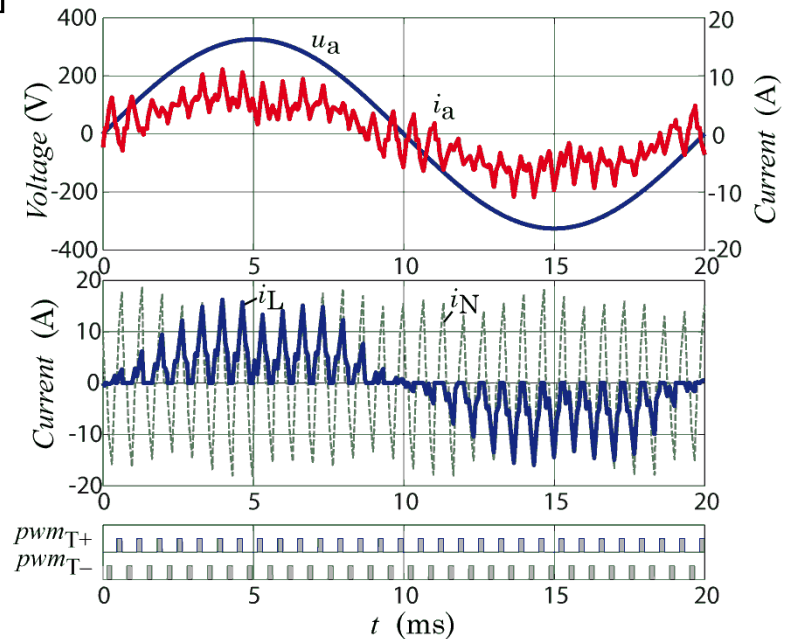
- + Interleaving Reduces Switching Frequency Input Current Ripple
- + For Low Power Only One Unit Could be Operated – Higher Efficiency
- Low Frequency Mains Current Distortion Still Remaining
- Relatively High Implementation Effort

► Two-Switch Boost-Type DCM Converter Topology

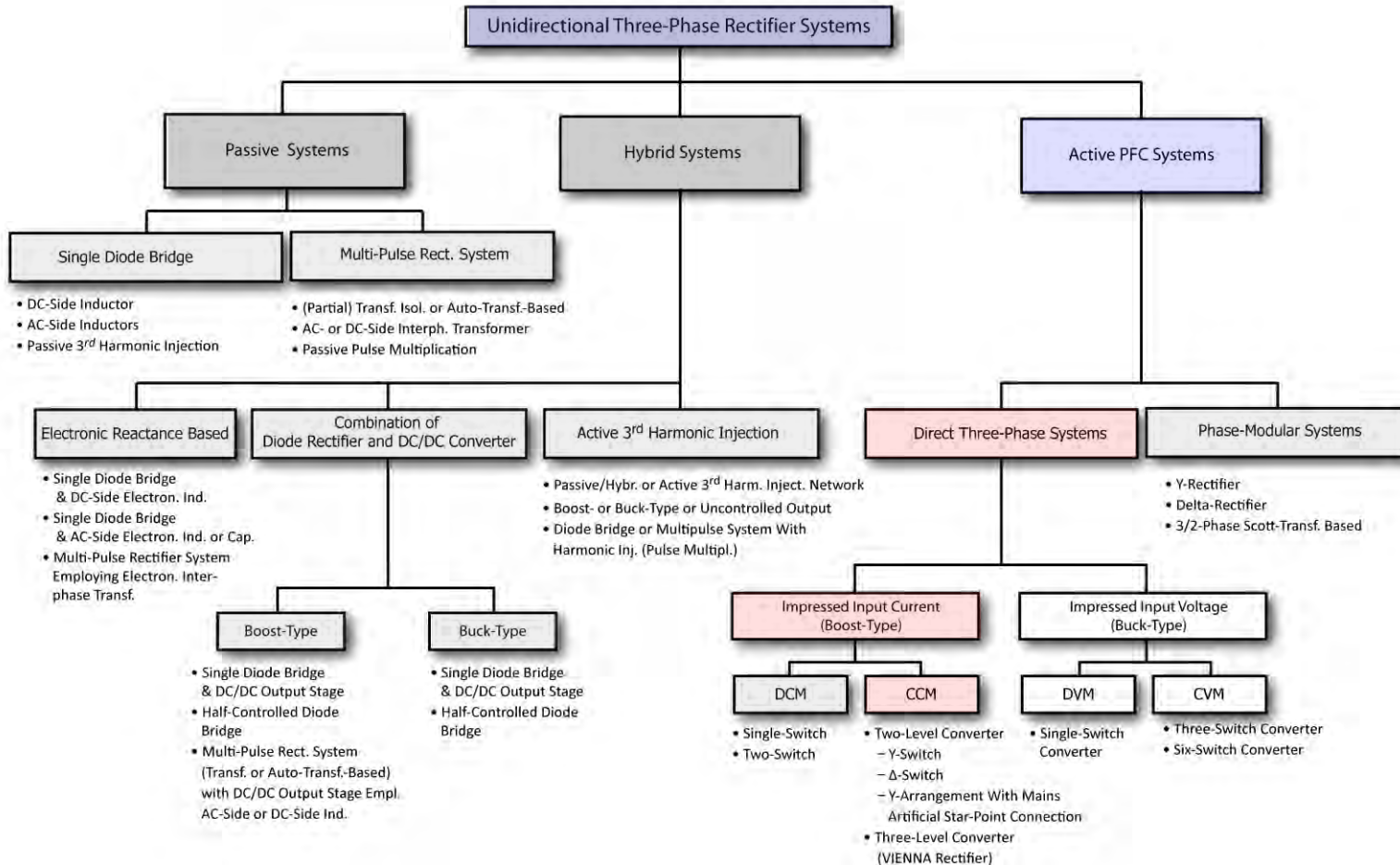


$$\begin{aligned}
 U_{LL} &= 3 \times 400 \text{ V} \\
 P_o &= 2.5 \text{ kW} \\
 U_o &= 700 \text{ V} \\
 THD_i &= 9 \%
 \end{aligned}$$

- + Slightly Lower THD_I for same U_{pn}/\hat{U}_N Component as Single-Switch DCM Converter
- Large Switching Frequency CM Output Voltage Comp.
- High Input Capacitor Current Stress
- Artificial Capacitive Neutral Point N
- Decoupling of the Phases
- Pros and Cons. as for Single-Switch Converter
- T_+ and T_- Could also be Gated Simultaneously



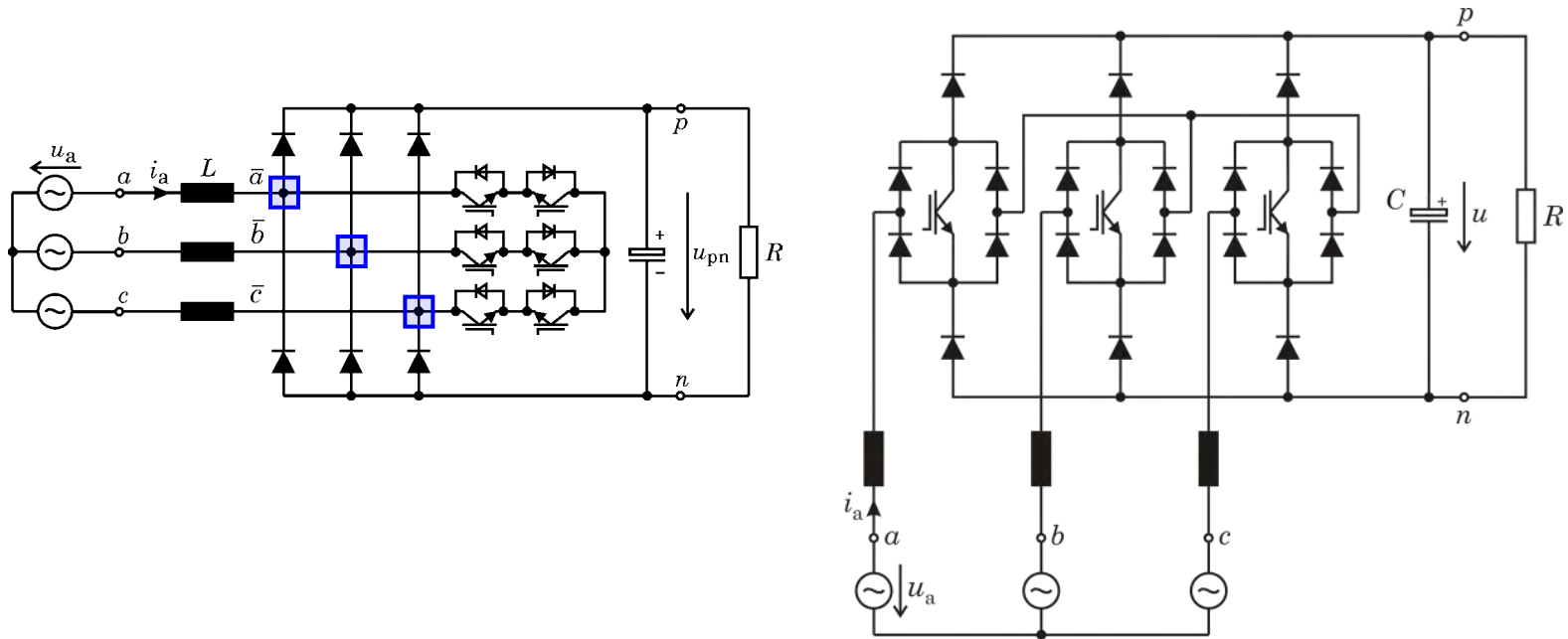
► Classification of Unidirectional Rectifier Systems



Two-Level CCM Boost-Type PFC Rectifier Systems

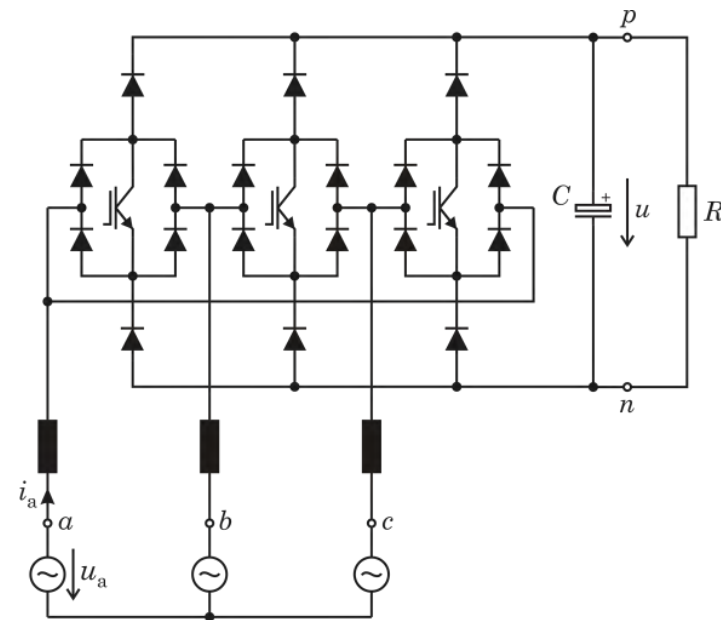
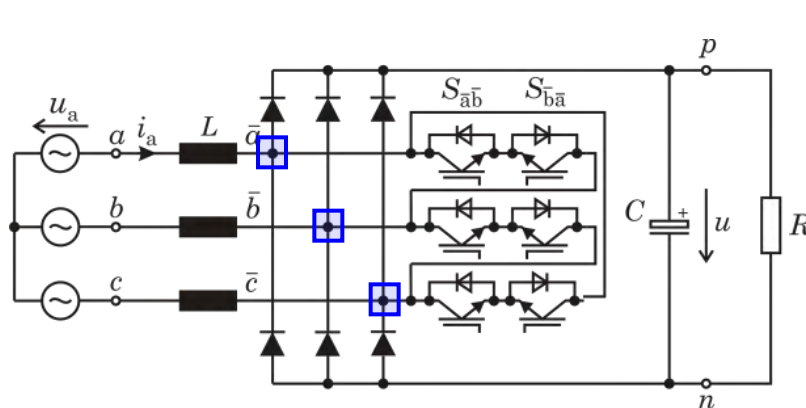
- *Y-Switch Rectifier*
- *Δ -Switch Rectifier*

► Y-Switch Rectifier

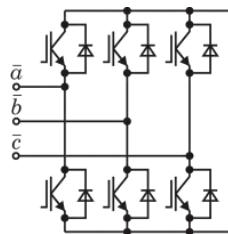


- Proper Control of Power Transistors Allows Formation of PWM Voltages at \bar{a} , \bar{b} , \bar{c} and/or Impression of Sinusoidal Mains Current

► Δ -Switch Rectifier



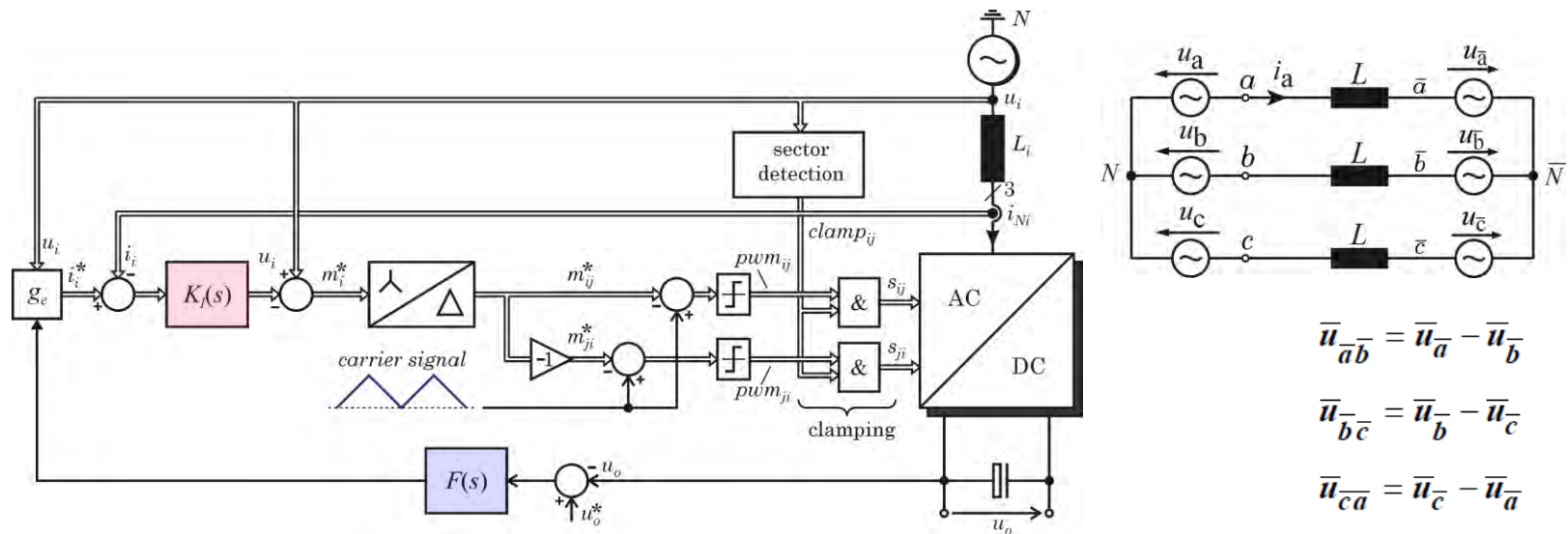
- Δ -Switch Rectifier Features Lower Conduction Losses Compared to Y-Switch System
- Active Switch Could be Implemented with Six-Switch Power Module



► Δ -Switch Rectifier

■ Equivalent Circuit / Mains Current Control

- Reference Voltages, i.e. the Output of the Phase Current Controllers Need to be Transformed into Δ -Quantities



- Mains Currents Controlled in Phase with Mains Voltages u_a, u_b, u_c
- Voltage Formation at a, b, c is Determined by Switching State of $S_{\bar{a}b\bar{a}}, S_{\bar{b}c\bar{b}}, S_{\bar{c}a\bar{c}}$ and AND Input Current Direction/Magnitude
- Always Only Switches Corresponding to Highest and Lowest Line-to-Line Voltage are Pulsed
- Switch of Middle Phase Turned Off Continuously

$$\bar{u}_{\bar{a}b} = \bar{u}_{\bar{a}} - \bar{u}_{\bar{b}}$$

$$\bar{u}_{\bar{b}c} = \bar{u}_{\bar{b}} - \bar{u}_{\bar{c}}$$

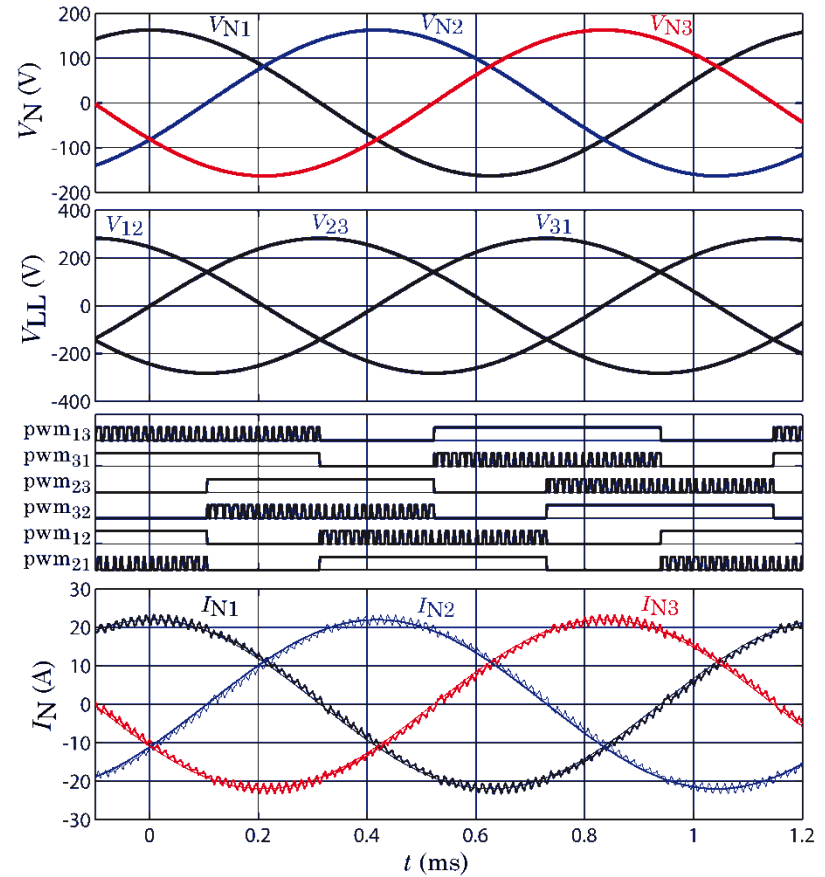
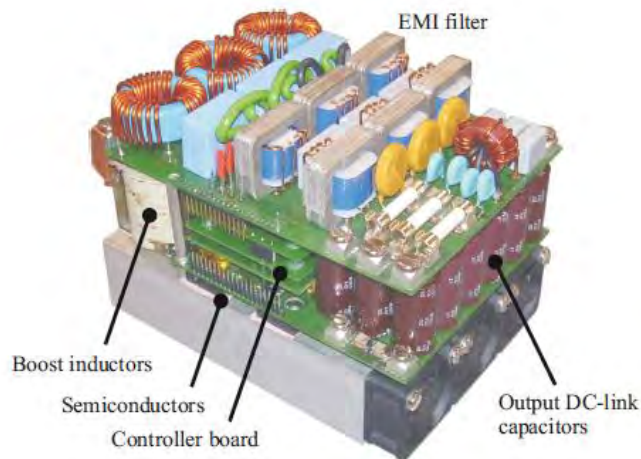
$$\bar{u}_{\bar{c}a} = \bar{u}_{\bar{c}} - \bar{u}_{\bar{a}}$$

► Δ -Switch Rectifier

■ Modulation

$U_{LL} = 115 \text{ V (400Hz)}$
 $P_o = 5 \text{ kW}$
 $U_o = 400 \text{ V}$
 $f_s = 72 \text{ kHz}$

Power Density: 2.35 kW/dm^3

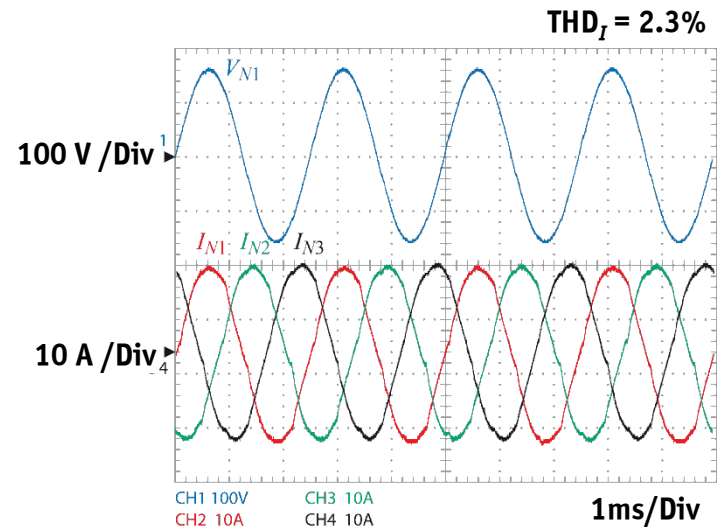
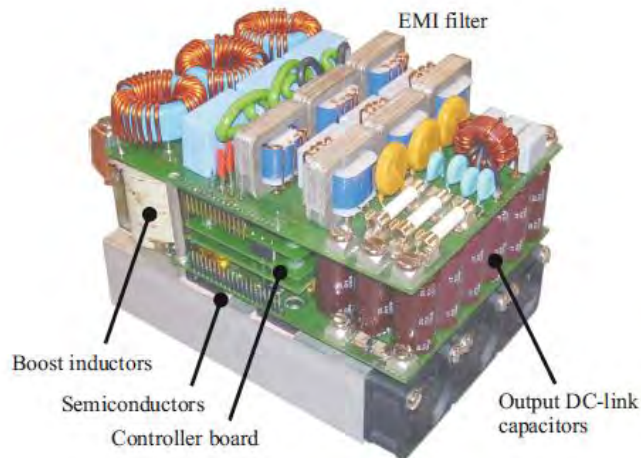


▶ Δ -Switch Rectifier

■ Experimental Analysis

$U_{LL} = 115 \text{ V (400Hz)}$
 $P_o = 5 \text{ kW}$
 $U_o = 400 \text{ V}$
 $f_s = 72 \text{ kHz}$

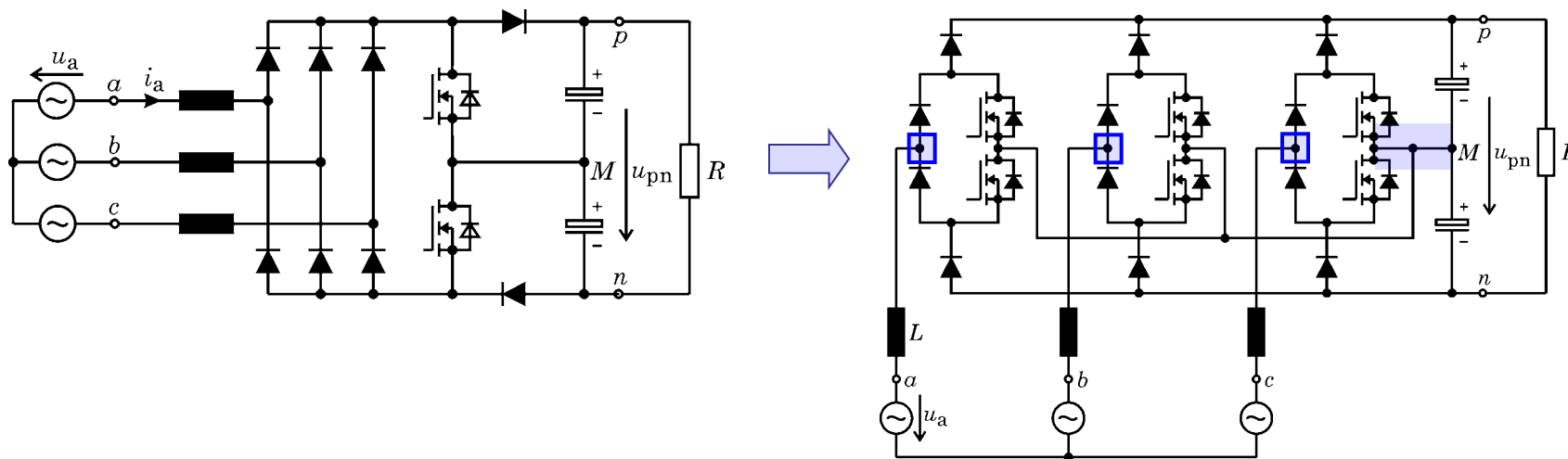
Power Density: 2.35 kW/dm^3



Three-Level Boost-Type CCM PFC Rectifier System

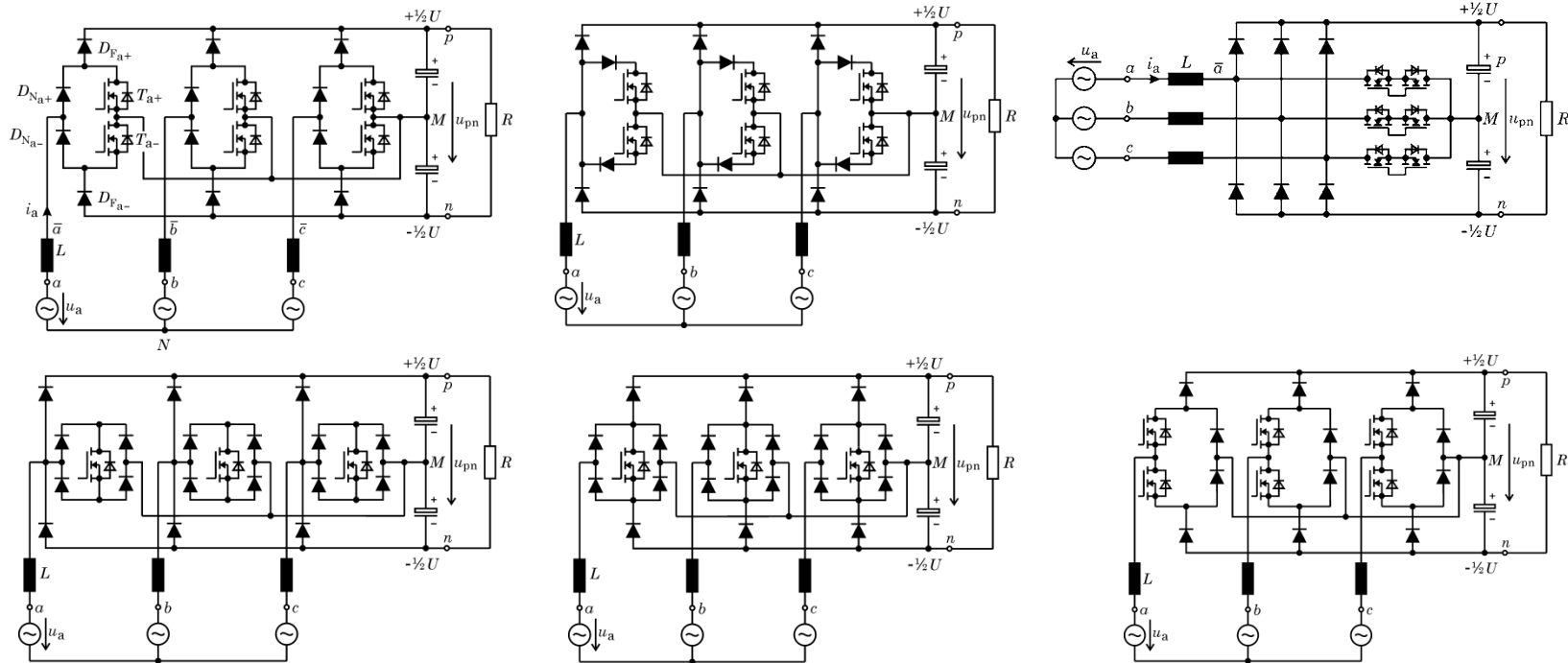
- *Derivation of Circuit Topologies*

► Derivation of Three-Level Rectifier Topologies (1)



- Sinusoidal Mains Current Shaping Requires Independent Controllability of the Voltage Formation of the Phases

► Derivation of Three-Level Rectifier Topologies (2)



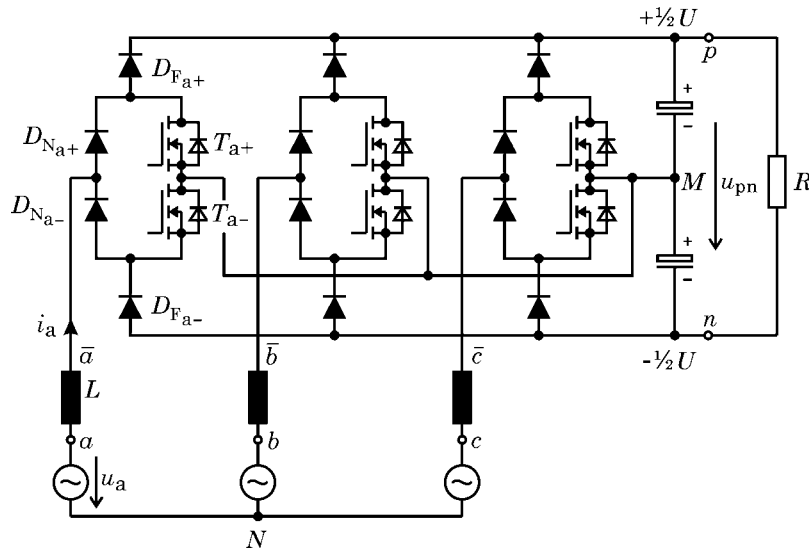
• Three-Level Characteristics

- + Low Input Inductance Requ.
- + Low Switching Losses,
- + Low EMI
- Higher Circuit Complexity
- Control of Output Voltage Center Point Required

Three-Level PFC Rectifier Analysis

- *Input Voltage Formation*
- *Modulation / Sinusoidal Input Current Shaping*
- *Output Center Point Formation*
- *Control*
- *Design Considerations*
- *EMI Filtering*
- *Digital Control*
- *Experimental Analysis*

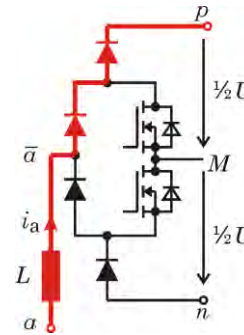
► Input Voltage Formation



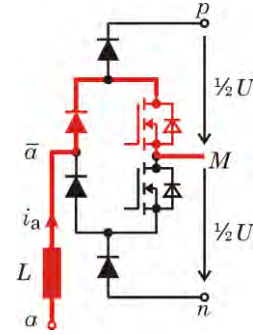
- Voltage Formation

$$u_{\bar{a}M} = (1 - s_a) \text{sign}(i_a) \frac{U}{2}$$

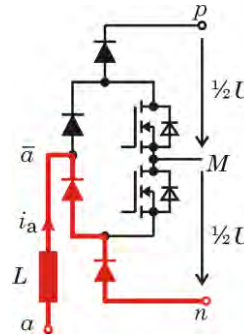
is Determined by Phase Switching State
AND Direction of Phase Current



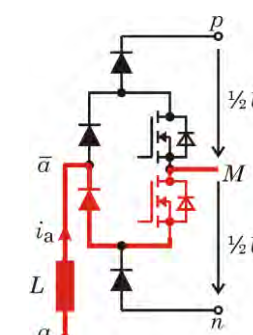
$s_a = 0$
 $T_{a+}, T_{a-}: \text{OFF}$
 $u_{\bar{a}M} = +\frac{1}{2}U$



$s_a = 1$
 $T_{a+}, T_{a-}: \text{ON}$
 $u_{\bar{a}M} = 0$



$s_a = 0$
 $T_{a+}, T_{a-}: \text{OFF}$
 $u_{\bar{a}M} = -\frac{1}{2}U$

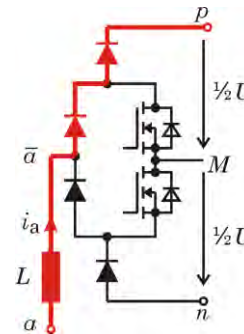


$s_a = 1$
 $T_{a+}, T_{a-}: \text{ON}$
 $u_{\bar{a}M} = 0$

► Semiconductor Blocking Voltage Stress

■ Blocking Voltage Definition

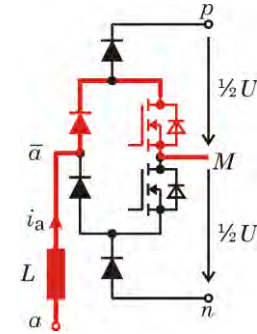
- D_{F+} : Limited to U_+ via Parasitic Diode of T_{a+}
- D_{N+} : Not Dir. Def. by Circuit Structure
- D_{N-} : Not Dir. Def. by Circuit Structure
- D_{F-} : Limited to U_- via Paras. Diode of T_{a-}
- T_{a+} : Limited to U_+ via D_{F+}
- T_{a-} : Limited to U_- via D_{F-}



$$s_a = 0$$

$$T_{a+}, T_{a-}: \text{OFF}$$

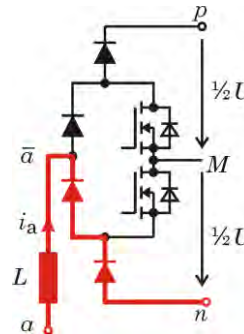
$$u_{\bar{a}M} = +\frac{1}{2}U$$



$$s_a = 1$$

$$T_{a+}, T_{a-}: \text{ON}$$

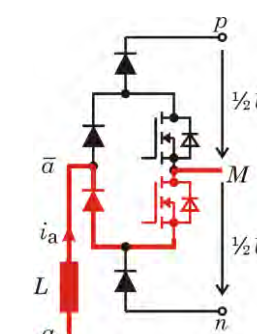
$$u_{\bar{a}M} = 0$$



$$s_a = 0$$

$$T_{a+}, T_{a-}: \text{OFF}$$

$$u_{\bar{a}M} = -\frac{1}{2}U$$

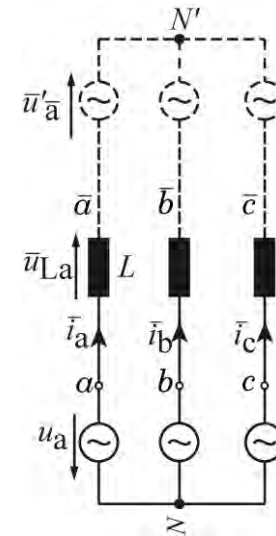
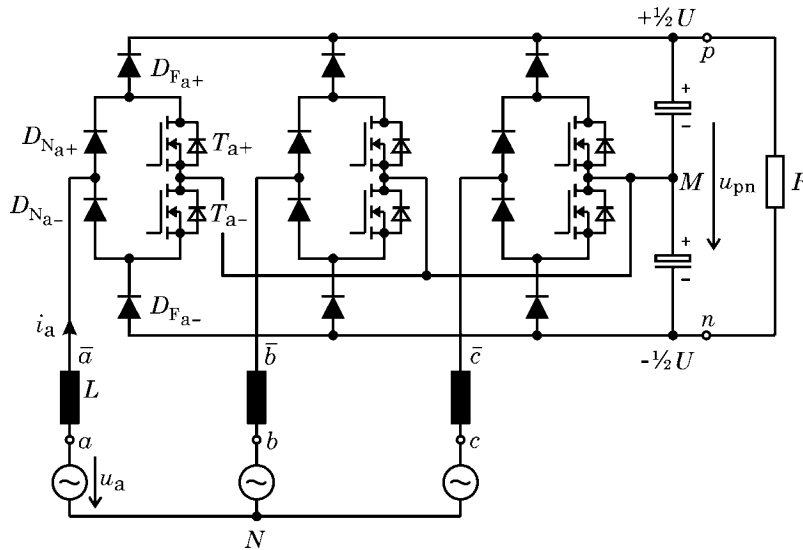


$$s_a = 1$$

$$T_{a+}, T_{a-}: \text{ON}$$

$$u_{\bar{a}M} = 0$$

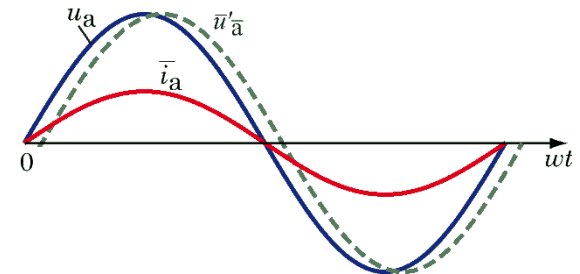
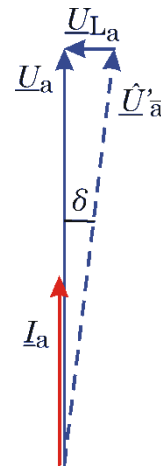
► Impression of Input Current Fund. (Ohmic Fund. Mains Behavior)



$$\delta = 0,1^\circ \dots 0,3^\circ \quad (50/60 \text{ Hz})$$

$$\delta = 1^\circ \dots 3^\circ \quad (360 \text{ Hz} \dots 800 \text{ Hz})$$

- Difference of Mains Voltage (e.g. u_a) and Mains Frequency Comp. of Voltage Formed at Rectifier Bridge Input (e.g. $\bar{u}'_{\bar{a}}$) Impresses Mains Current (e.g. i_a)



► PWM / Formation of $\bar{u}_a, \bar{u}_b, \bar{u}_c$ / AC-Side Equiv. Circuit (1)

- Def. of Modulation Index:

$$M = \frac{\hat{U}_{\bar{a}}}{\frac{1}{2}U} \quad \left(0 \dots \frac{2}{\sqrt{3}}\right)$$

- Zero-Sequence Signal to Achieve Ext. Mod. Range

$$u_{\bar{a}0} = u'_a + u_0$$

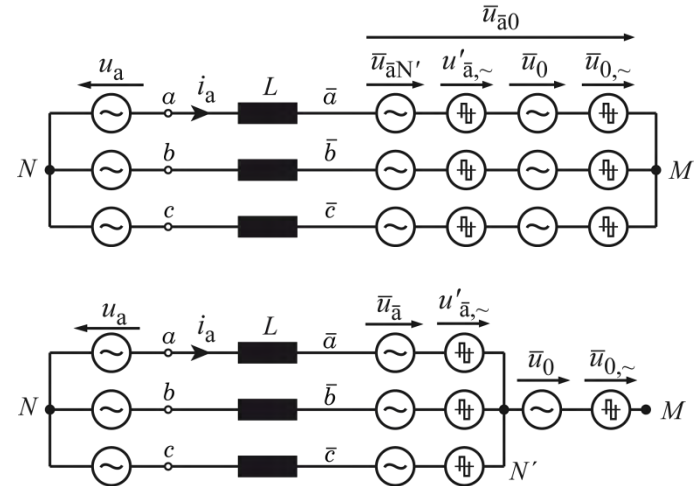
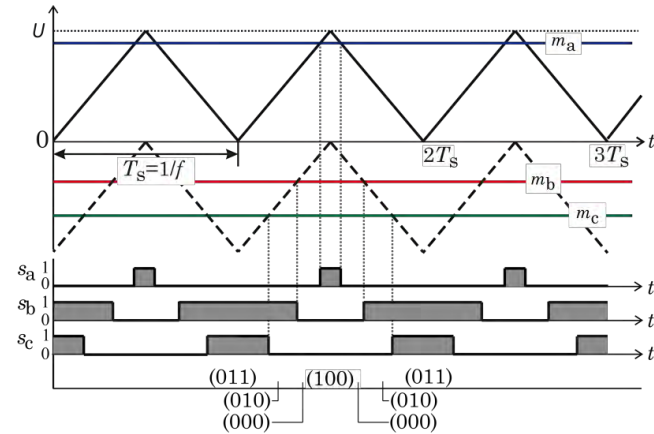
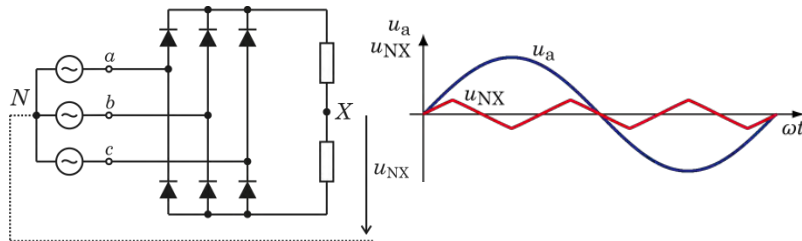
$$u_{\bar{b}0} = u'_b + u_0$$

$$u_{\bar{c}0} = u'_c + u_0$$

$$u'_a + u'_b + u'_c = 0$$

$$u_0 = \frac{1}{3}(u_{\bar{a}0} + u_{\bar{b}0} + u_{\bar{c}0})$$

- Generation of u_0 i.e. 3rd Harmonic Signal



► PWM / Formation of $\bar{u}_a, \bar{u}_b, \bar{u}_c$ / AC-Side Equiv. Circuit (2)

 $\bar{u}'_a, \bar{u}'_b, \bar{u}'_c$

Impression of Mains Current Fundamental
 in Combination with u_a, u_b, u_c

$$u'_a = u_{aN'} = \bar{u}'_a + u_{a\sim}$$

$$u'_b = u_{bN'} = \bar{u}'_b + u_{b\sim}$$

$$u'_c = u_{cN'} = \bar{u}'_c + u_{c\sim}$$

 $\bar{u}'_{a\sim}, \bar{u}'_{b\sim}, \bar{u}'_{c\sim}$

Causing the Switching Frequ.
 Ripple of the Mains Currents and/or
DM Filtering Requirement

Note: $u_{NN'} = 0$

$$u_{a0} = u'_a + u_0$$

$$u_{b0} = u'_b + u_0$$

$$u_{c0} = u'_c + u_0$$

 \bar{u}_0

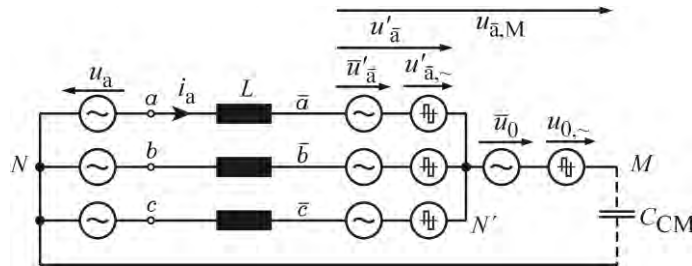
Low Frequency Zero Sequence Component
 for Extending the Modulation Range from
 $M = 0 \dots 1$ (Sinusoidal Modulation) to $M = 0 \dots \frac{2}{\sqrt{3}}$

$$u_0 = \bar{u}_0 + u_{0\sim}$$

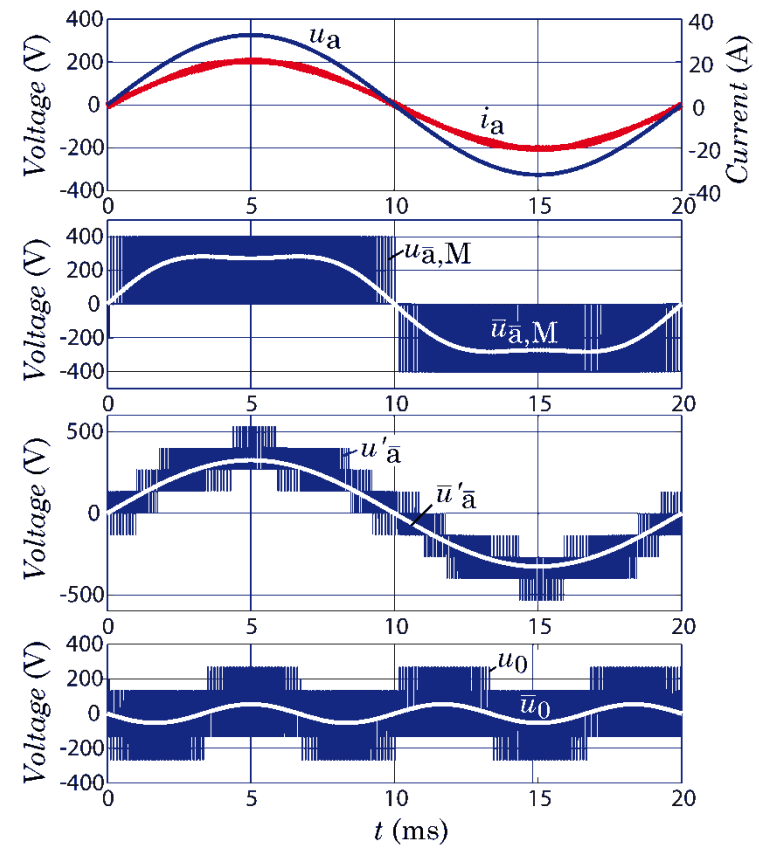
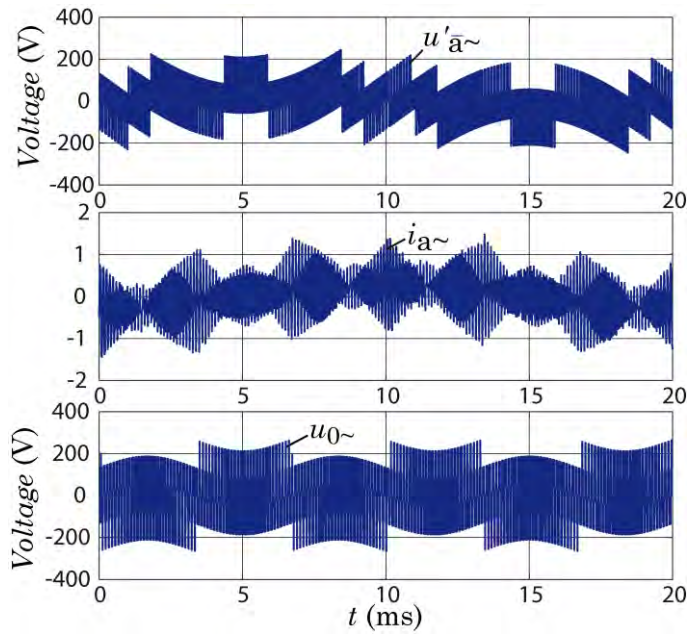
 $u_{0\sim}$

Switching Frequency CM Voltage Fluctuation
 of the Output → Resulting in CM Current and/or
CM Filtering Requirement

► Time Behavior of the Components of Voltages $u_{\bar{a}}, u_{\bar{b}}, u_{\bar{c}}$



$$i_a = \bar{i}_a + i_{a\sim}$$



► Local Average Value of Center Point Current

- Derivation of Low-Frequency Component \bar{i}_M of Center Point Current Assuming a 3rd Harmonic Component of u_0 as Employed for Increasing the Modulation Range)

Assumption: $i_a > 0, i_b < 0, i_c < 0$

$$m_a = m'_a + m_0 = M_1 \cdot \cos(\omega t) + M_3 \cdot \cos(3\omega t)$$

$$m_b = m'_b + m_0 = M_1 \cdot \cos\left(\omega t - \frac{2\pi}{3}\right) + M_3 \cdot \cos(3\omega t)$$

$$m_c = m'_c + m_0 = M_1 \cdot \cos\left(\omega t + \frac{2\pi}{3}\right) + M_3 \cdot \cos(3\omega t)$$

$$M_1 = \frac{\hat{U}}{\frac{1}{2}U} \quad M_3 = \frac{\hat{U}_0}{\frac{1}{2}U}$$

$$\alpha_a = 1 - m_a \quad \text{(relative on-time of } T_{a+}\text{)}$$

$$\alpha_b = 1 - m_b \quad \text{(relative on-time of } T_{b+}\text{)}$$

$$\alpha_c = 1 - m_c \quad \text{(relative on-time of } T_{c+}\text{)}$$

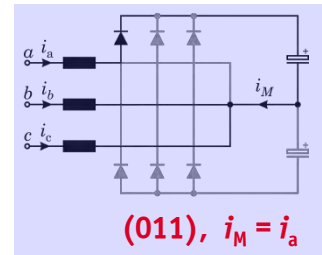
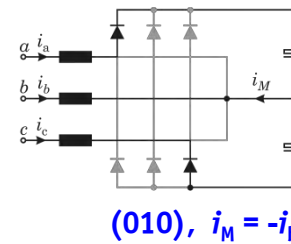
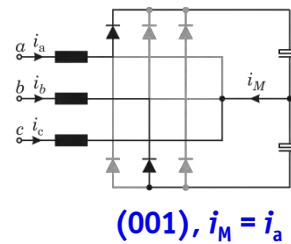
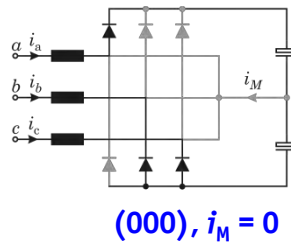
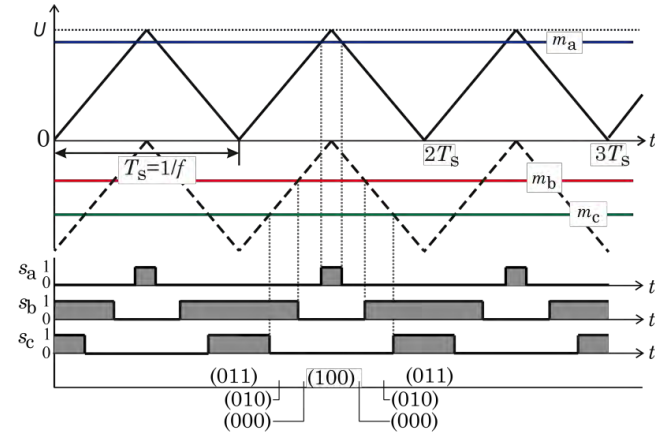
$$\begin{aligned} \bar{i}_M &= \alpha_a \cdot i_a + \alpha_b \cdot i_b + \alpha_c \cdot i_c \\ &= (1 - m_a) \cdot i_a + (1 - m_b) \cdot i_b + (1 - m_c) \cdot i_c \end{aligned}$$

$$\text{RMS of } \bar{i}_M \text{ minimal for } \frac{M_3}{M_1} \approx \frac{1}{4}$$

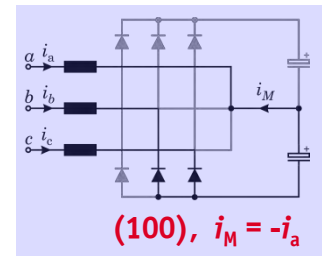
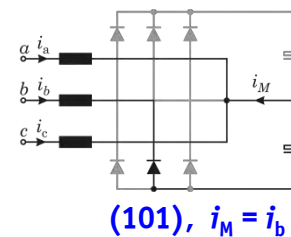
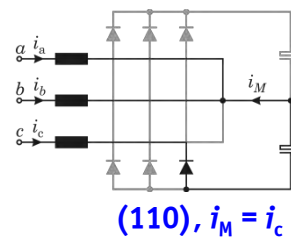
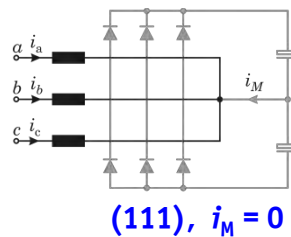
- m_0 , i.e. PWM incl. 3rd Harm., Reduces \bar{i}_M and Extends the Modulation Range

► Cond. States within a Pulse Period / Center Point Current Formation

- Consider e.g. $i_a > 0, i_b < 0, i_c < 0$
- Switching States (100), (011) are Forming Identical Voltages u'_a, u'_b, u'_c but Inverse Centre Point Currents i_M
- Control of i_M by Changing the Partitioning of Total On-Times of (100) and (011)



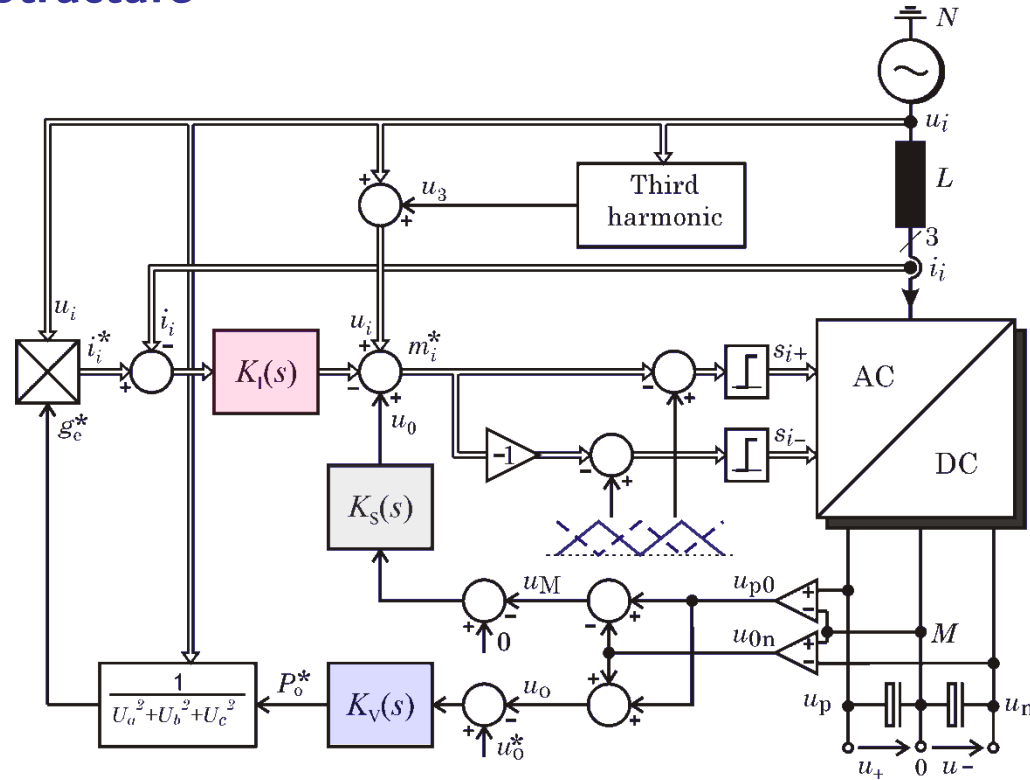
- Corresponding Switching States and Resulting Currents Paths



System Control

- *Control Structure*
- *Balancing of the Partial Output Voltages*

► Control Structure

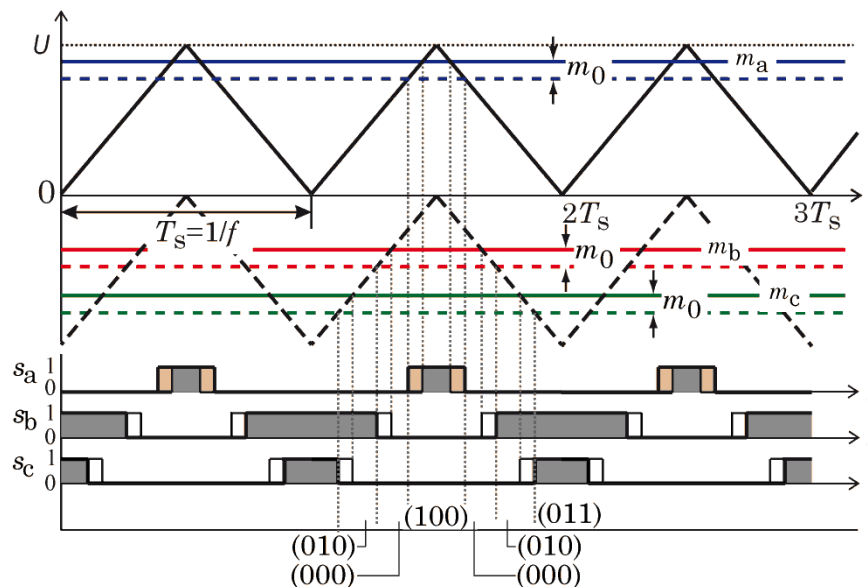


- Output Voltage Control
- Mains Phase Current Control
- Control of Output Center Point Potential (Balancing of U_+ , U_-)

- Control of i_a , i_b , i_c Relies on $u_{\bar{a}}$, $u_{\bar{b}}$, $u_{\bar{c}}$
- Control of u_M Relies on \bar{u}_0 (DC Component)
- No Cross Coupling of both Control Loops

► Control of Potential u_M of Output Voltage Center Point

- Assumption: $i_a > 0, i_b < 0, i_c < 0$

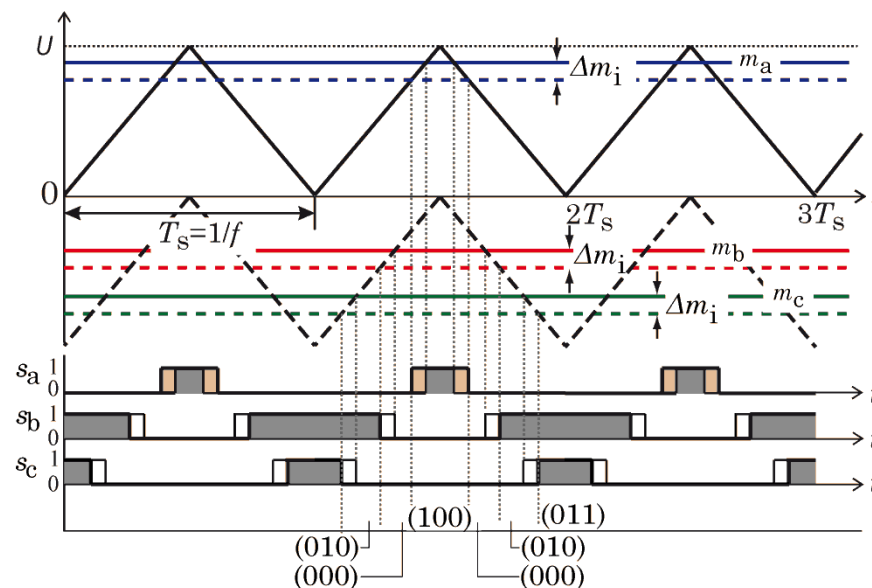
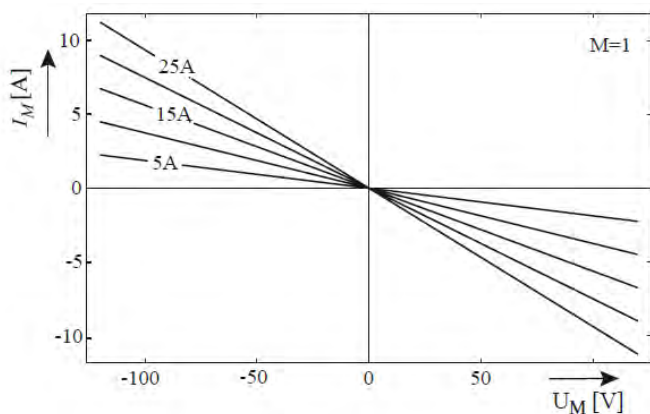


- Control via DC Component of u_0 , i.e. by Adding m_0 to the Phase Modulation Signals
i.e. by Inversely Changing the Rel. On-Times of (100) and (011), $\delta_{(100)}$ and $\delta_{(011)}$, without taking Influence on the Total On-Time $\delta_{(100)} + \delta_{(011)}$.

► Control of Output Voltage Center Point Potential u_M

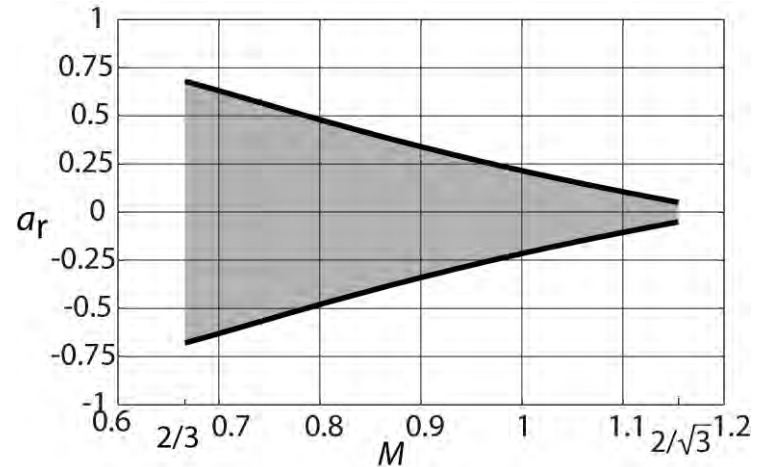
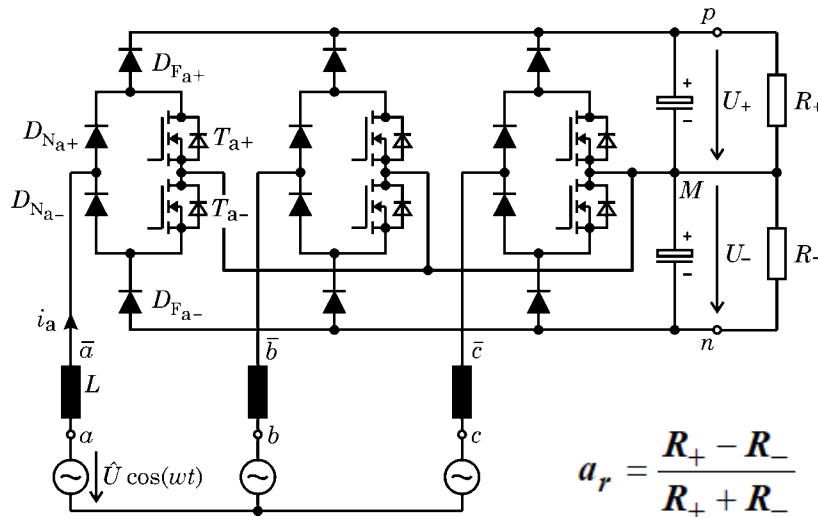
- Assumption:
$$U_+ = \frac{1}{2}U + \Delta U$$

$$U_- = \frac{1}{2}U - \Delta U$$



- Output Voltage Unbalance Results in Increasing On-Time of T_{a+} and Decreasing Off-Times of T_{b-} and T_{c-} so that the Voltages \bar{u}'_a , \bar{u}'_b , \bar{u}'_c are Formed as in the Symmetric Case ($\Delta U = 0$) and/or the Mains Phase Currents Remain at Sinusoidal Shape
- Resulting \bar{i}_M Reduces ΔU , i.e. Self Stability Guaranteed ✓

► Admissible Unbalance of Loading of U_+ and U_-



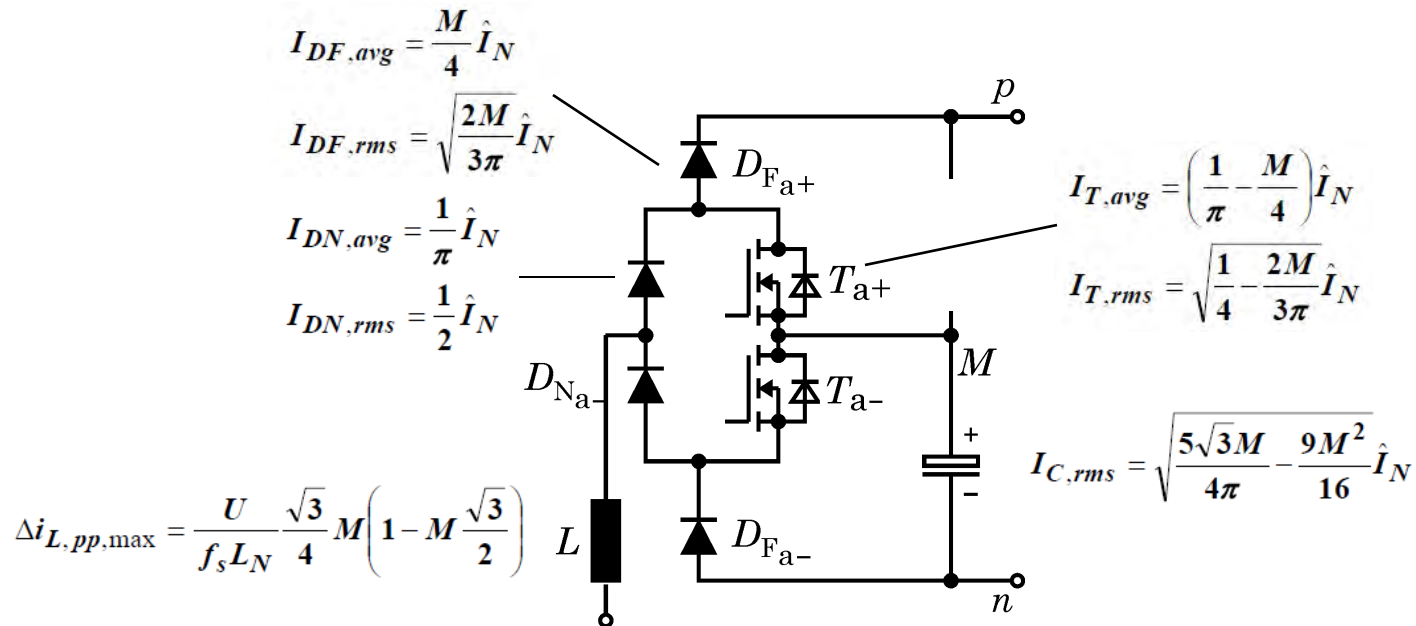
- System Tolerates Load Unbalance Dependent on the Voltage Transfer Ratio $(U_+ + U_-)/\hat{U}$ and/or the Value of The Modulation Index M

Design Guidelines

- *Current Stress on the Components*
- *Transistor Selection*
- *Output Pre-Charging at Start-up*

► Current Stress on Power Semiconductors

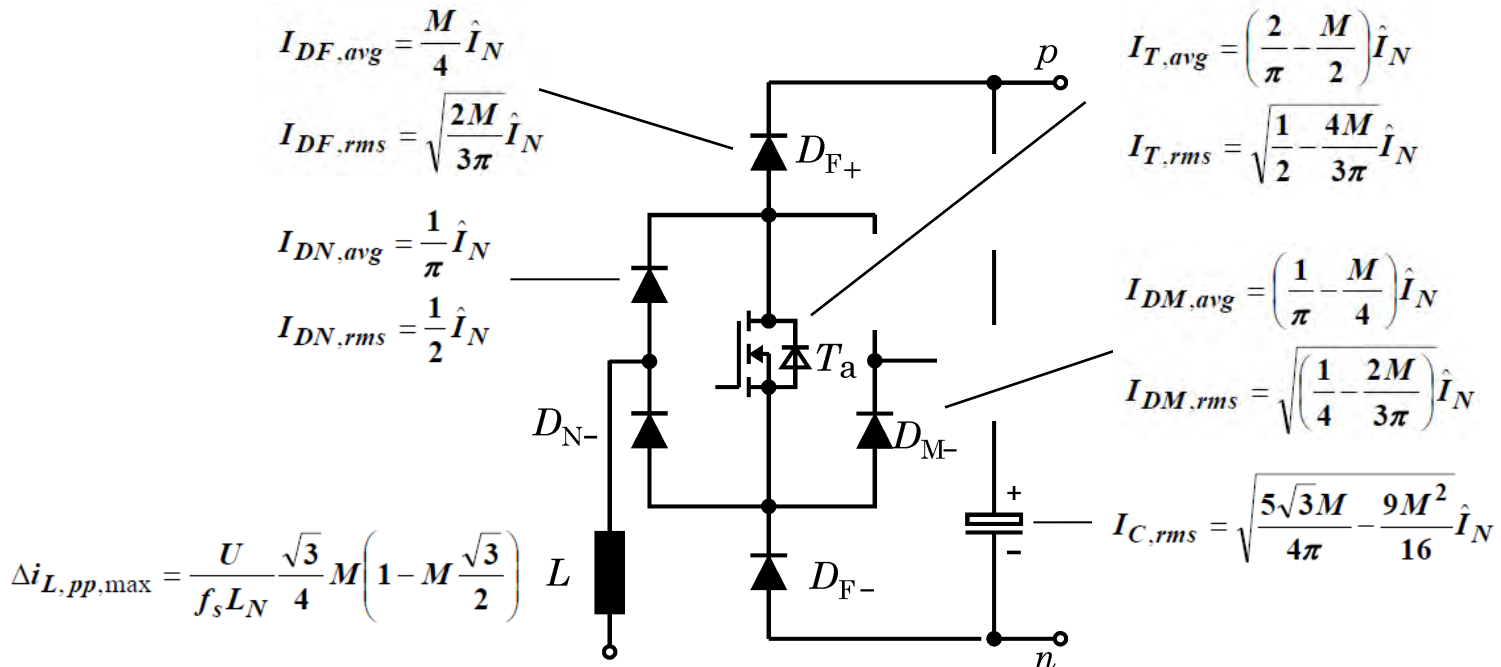
■ 6-Switch Circuit Topology



- Output Voltage $> \sqrt{3} \hat{U}_{max}$ (typ. $1.2 \sqrt{3} \hat{U}_{max}$); \hat{U}_{max} : Ampl. of Max. Mains Phase Voltage
- Required Blocking Capability of All Semiconductors: $\frac{1}{2} U$

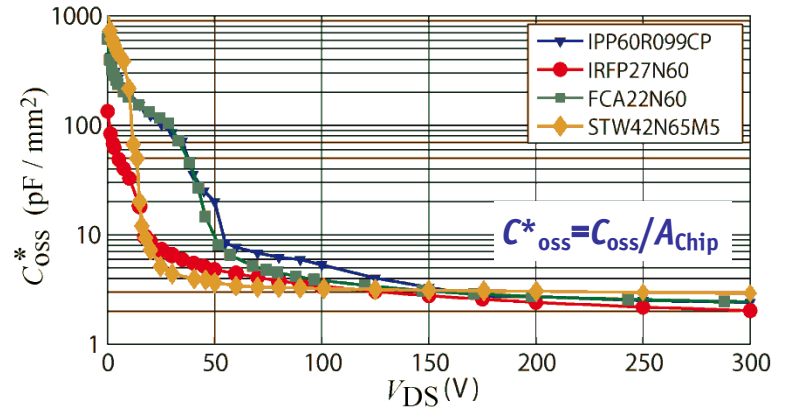
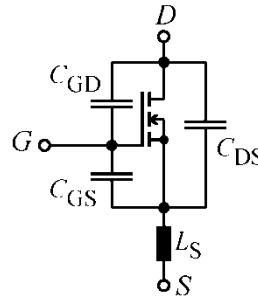
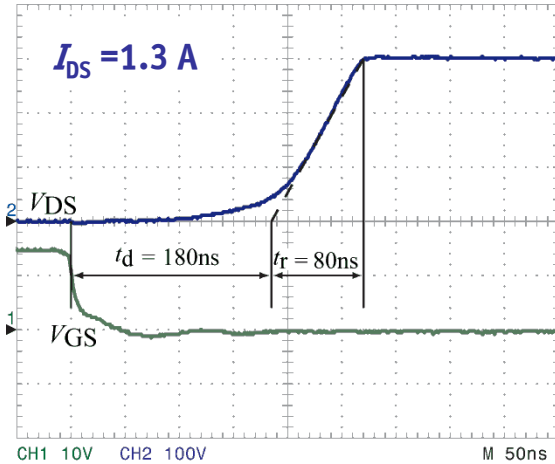
► Current Stress on Power Semiconductors

■ 3-Switch Circuit Topology



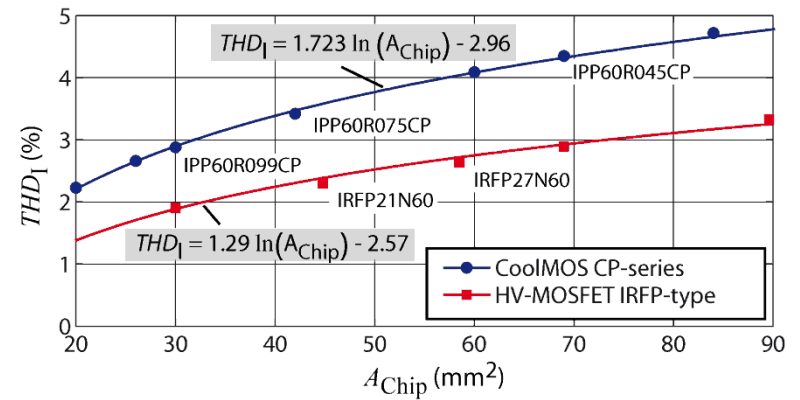
- Output Voltage $> \sqrt{3} \hat{U}_{max}$ (typ. $1.2 \sqrt{3} \hat{U}_{max}$); \hat{U}_{max} : Ampl. of Max. Mains Phase Voltage
- Required Blocking Capability of All Semiconductors: $\frac{1}{2} U$

► Nonlin. C_{oss} of Superjunct. MOSFETs Causes Input Curr. Distortion



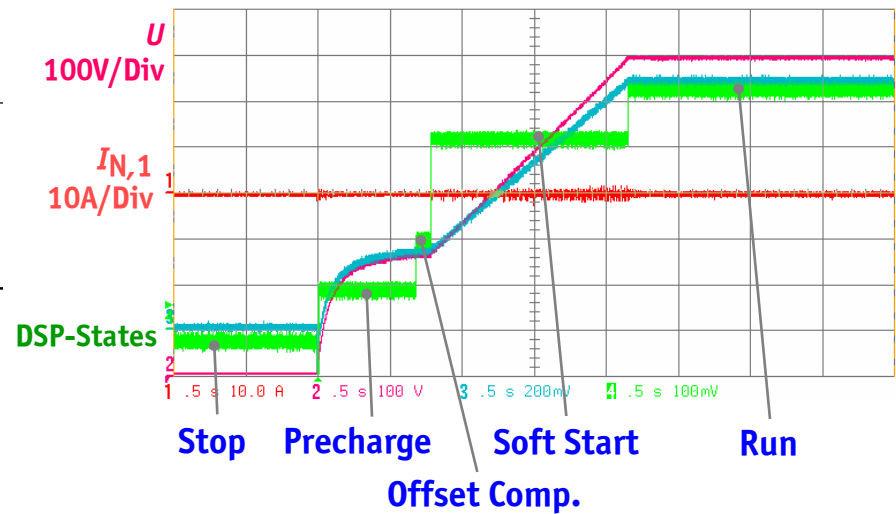
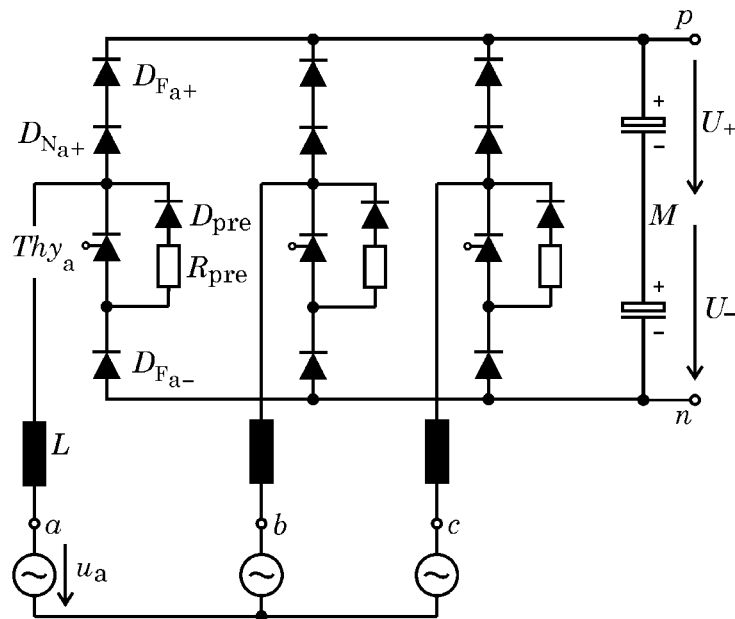
- Nonlinear Output Capacitance C_{oss} of MOSFET (CoolMOS) has to be Charged at Turn-off
- Large Turn-Off Delay for Low Currents (e.g. Delay of CoolMOS IPP60R099 (@ $I_{DS} = 1.3 \text{ A}$): 11% of Switching Cycle @ $f_s = 500 \text{ kHz}$)
- Results in PWM Volt. and/or Input Curr. Distortion

$U_{LL} = 3 \times 400 \text{ V (50 Hz)}, f_s = 1 \text{ MHz}, P_o = 10 \text{ kW}$



► Pre-Charging of Output Capacitors / Start-Up Sequence

- Lower Mains Diode D_{N-} is Replaced by Thyristor
- Inrush Current is Limited by R_{pre}
- Switches are not Gated During Start-Up
- Start-up Sequence is Required

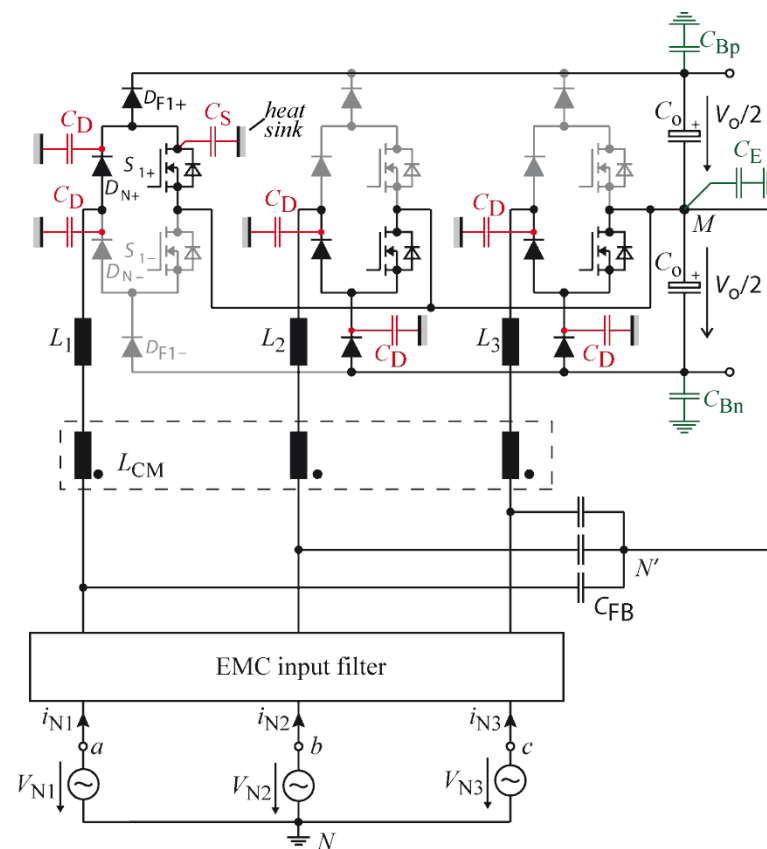
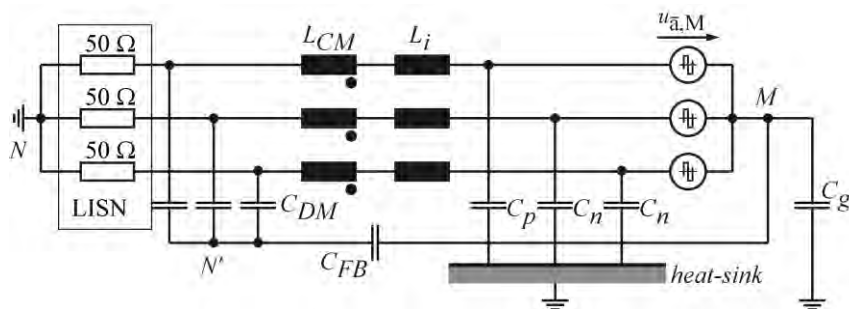


EMI Filtering

- *DM Filtering*
- *CM Filtering*

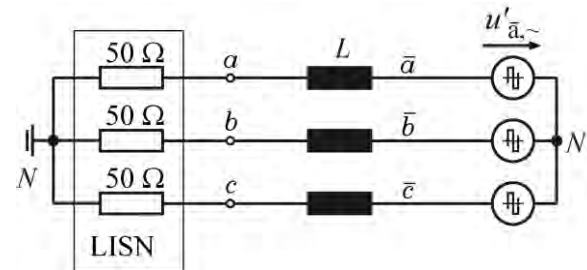
EMI Filtering Concept

- DM and CM Filter Stages
- Connection of Output Voltage Midpoint M to Artificial Mains Star-Point N'
 - No High-Frequency CM-Voltage at M
 - Capacitance of C_{FB} Not Limited by Safety Standards
- Parasitic Capacitances have to be Considered for CM-Filter Design

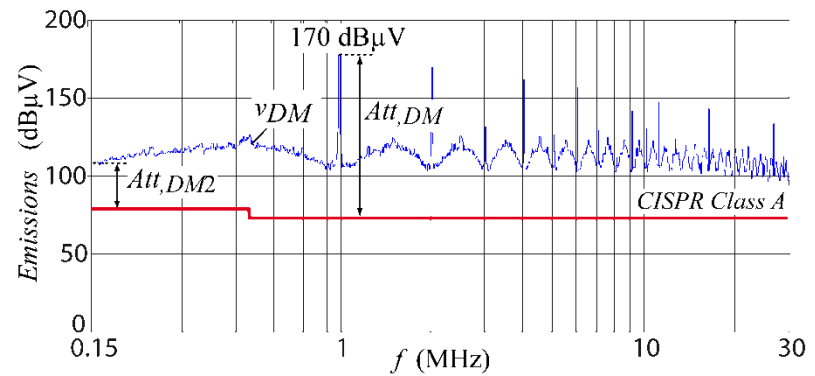


► DM Filter Design

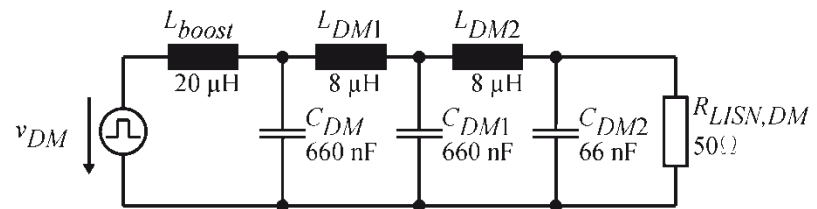
- DM Equivalent Circuit



- Required DM Attenuation, e.g. for $f_s = 1\ \text{MHz}$ (VR1000)

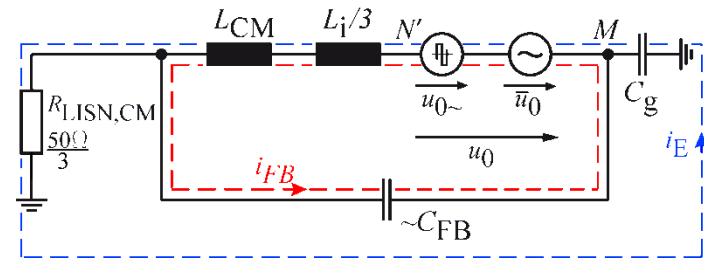


- DM Filter Structure



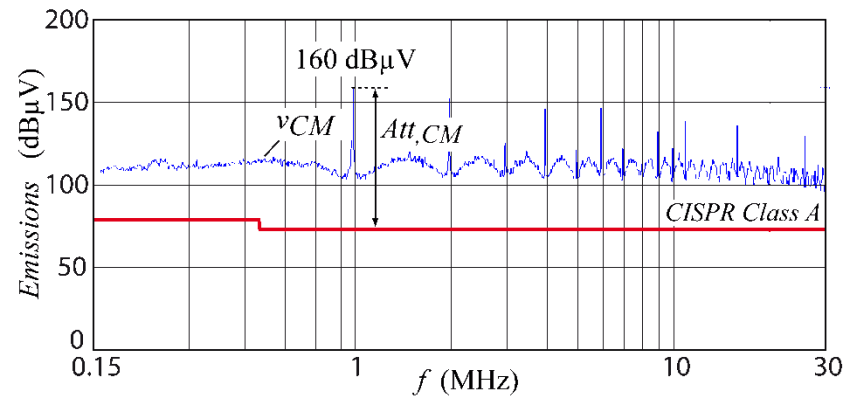
► CM Filter Design

- CM Equivalent Circuit



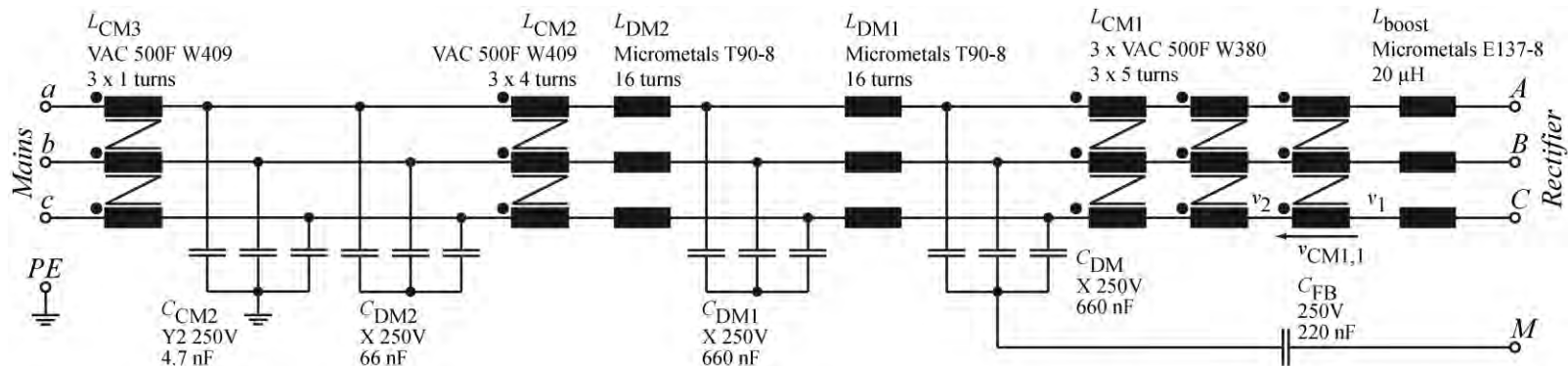
$C_{FB} = 220 \text{ nF}$

- Required CM Attenuation



► EMI Filter Structure for VR1000 Rectifier System

- 3 Stage DM Filter
- 2 Filter Stages for CM Filter

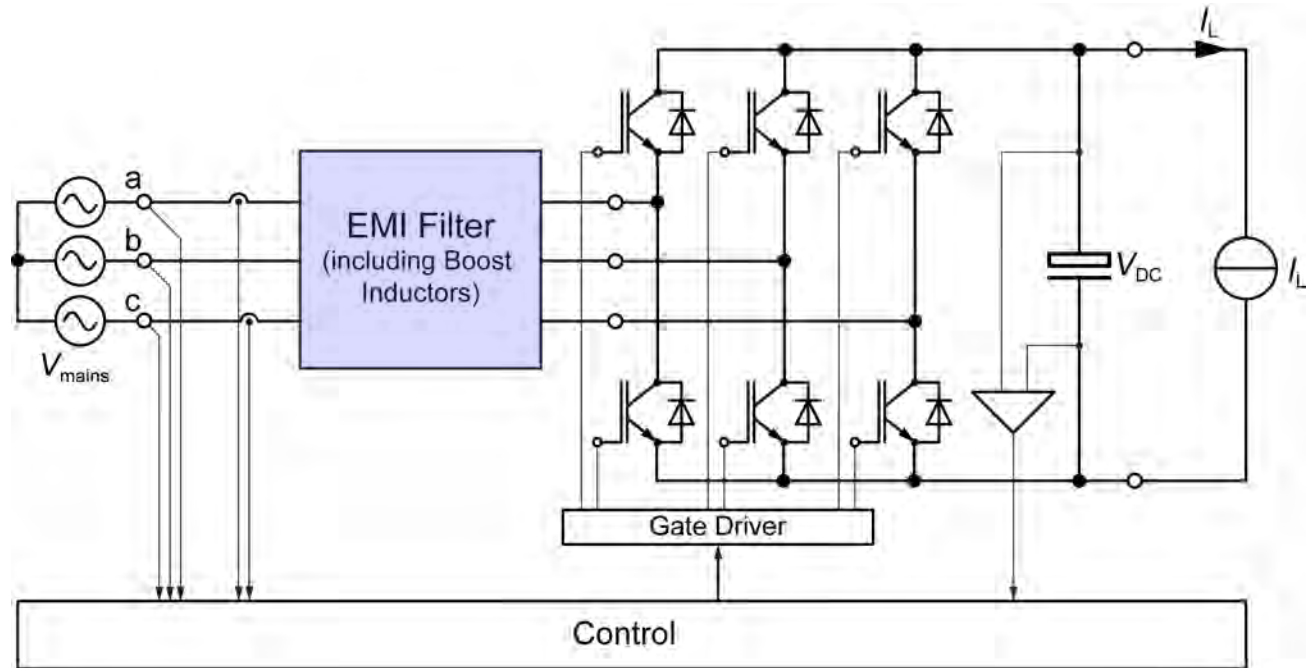


- 3 x CM Inductors in Series to Implement Proposed Filter Concept
- Additional CM Filter Stage Required Due to Parasitic Capacitances

EMI Filter Design

- *Analytical Approximation*
- *Volume / Efficiency Optimization*

Considered System



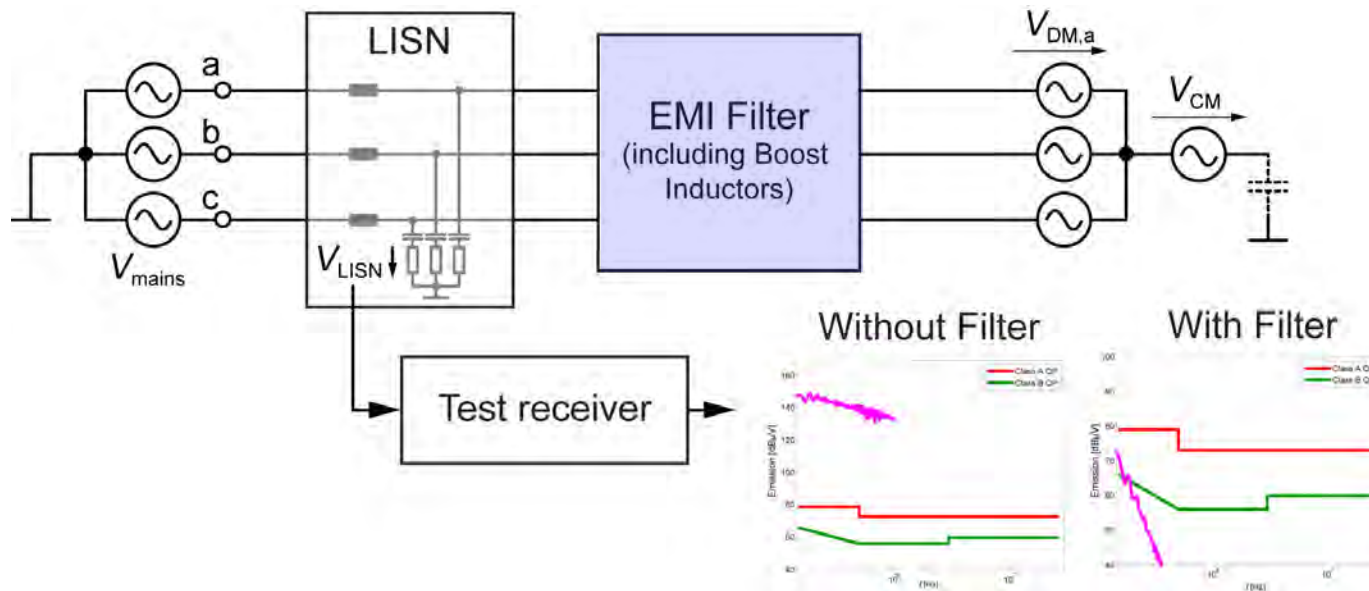
Goal

→ Meet Conducted EMI Standards (e.g. CISPR 11, Class A or Class B)

Tasks

- 1) Find Needed Filter Attenuation
- 2) Design Filter Accordingly

Calculate Required Filter Attenuation



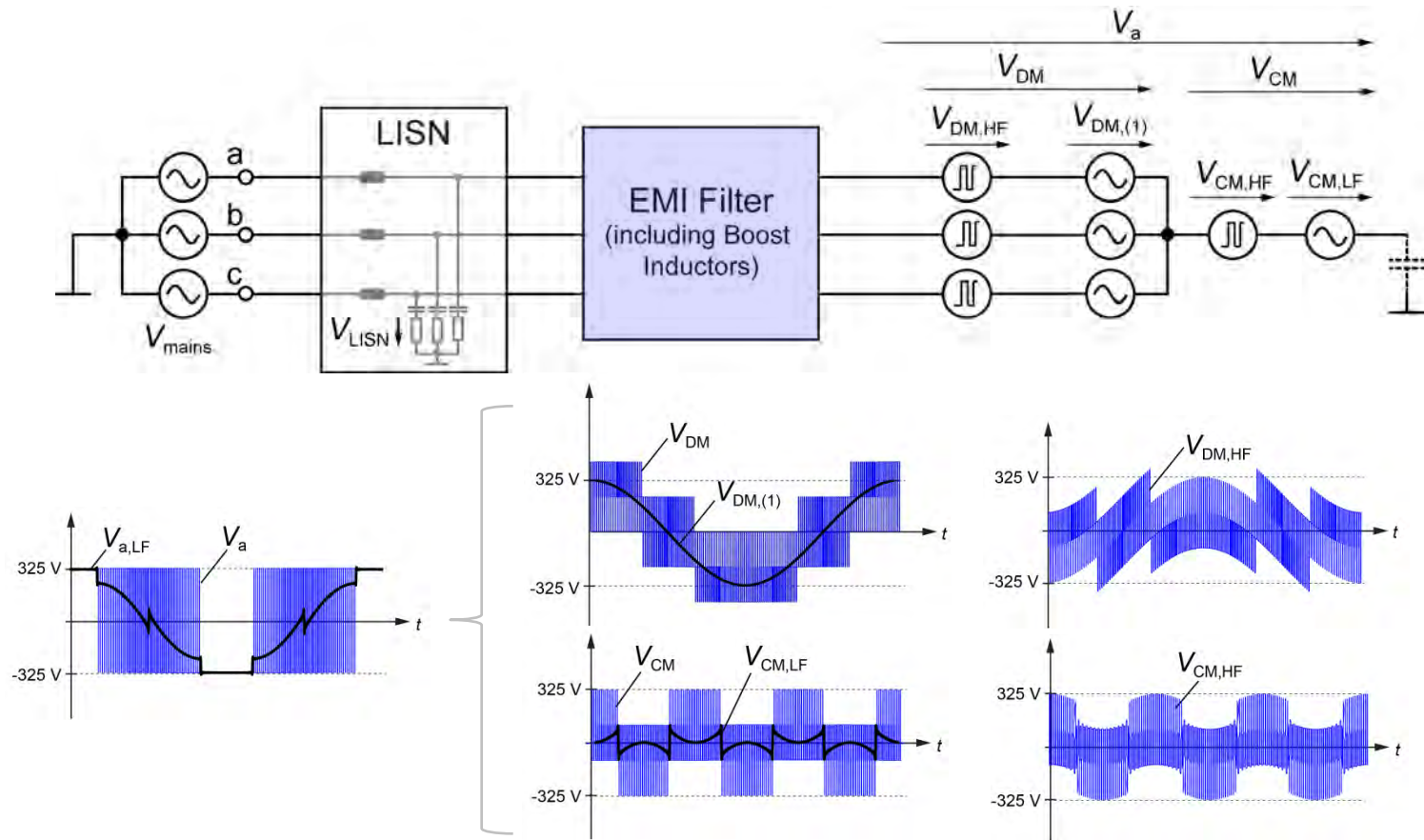
DM Attenuation

→ Determine Filter Attenuation such that Test Receiver Output is Below EMI Limits at all Frequencies

Challenges

→ Determine Spectrum of VDM and VCM
→ Computationally Intensive Test Receiver Modeling

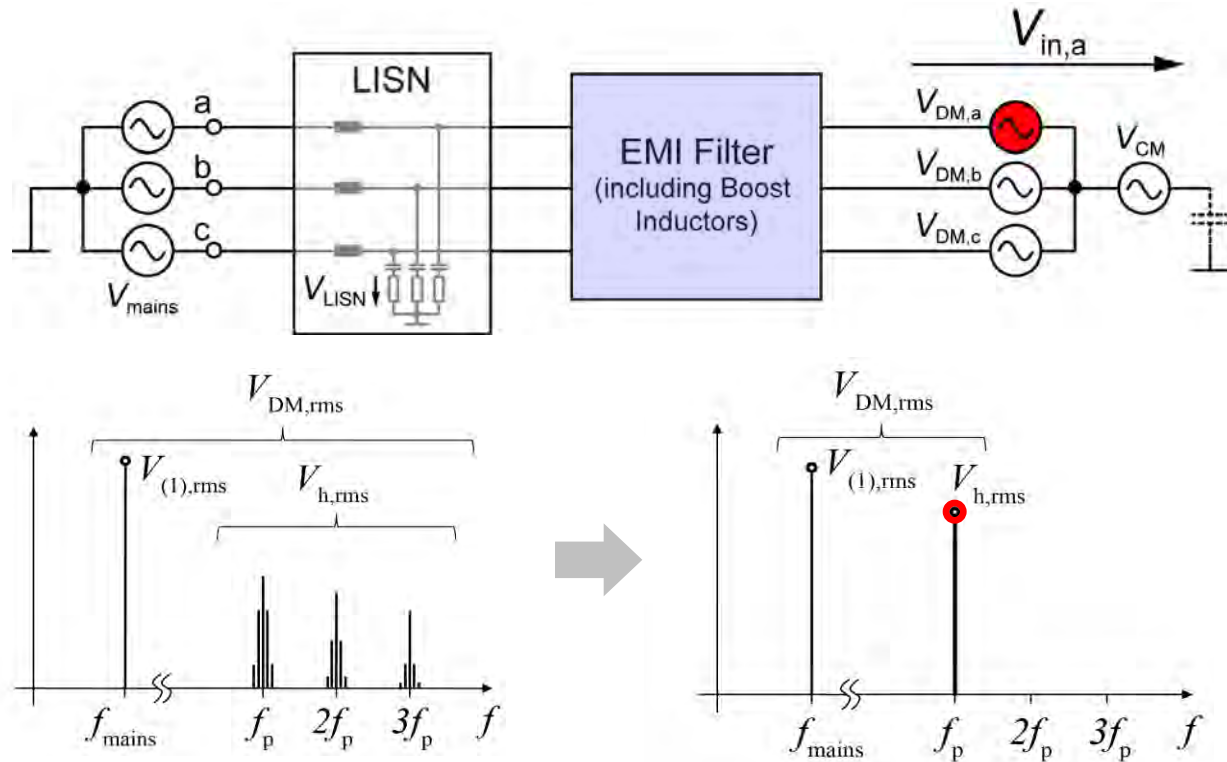
CM and DM Voltage Formation / Time Behavior



► Voltage V_a splitted into LF and High Frequency Components

Simplified Calculation of Required Filter Attenuation

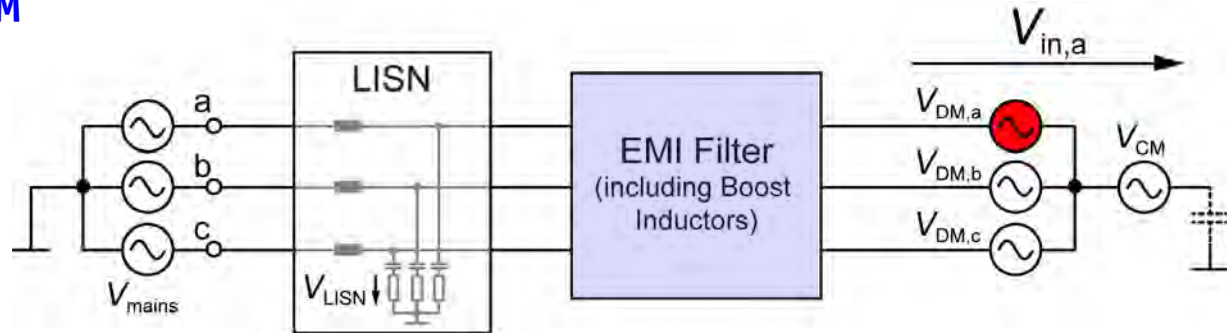
► Shown for DM Attenuation



- Model of Test Receiver is Omitted
- Harmonic Power Concentrated only @ Switching Frequency
- $V_{DM,rms}$ can be Calculated in Time Domain

Simplified Calculation of Required Filter Attenuation

► Shown for DM Attenuation

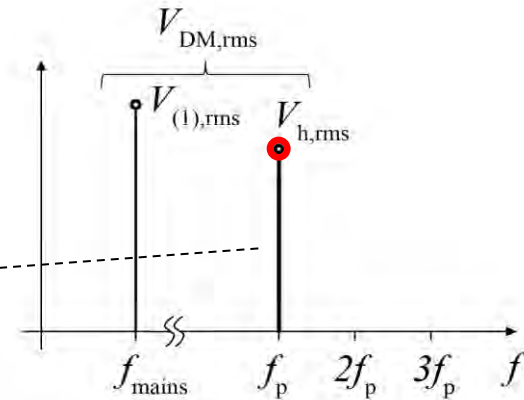


For Space Vector Modulation:

$$V_{CM,rms}^2 = \frac{1}{12} \frac{V_{DC}^2 (3\pi - 4\sqrt{3}M)}{\pi}$$

$$V_{DM,h,rms} = \sqrt{V_{in,rms}^2 - V_{(1),rms}^2 - V_{CM,rms}^2}$$

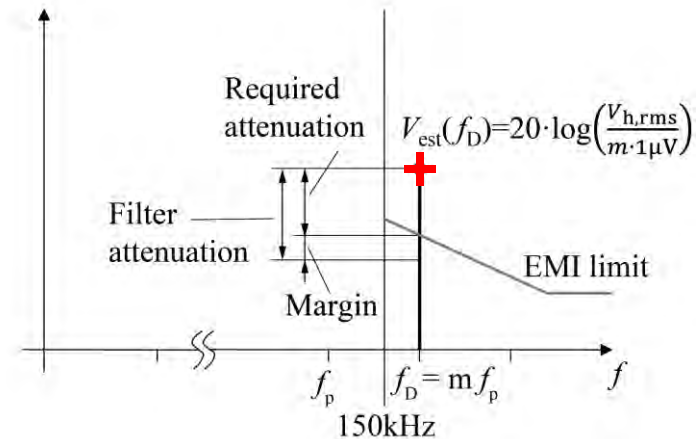
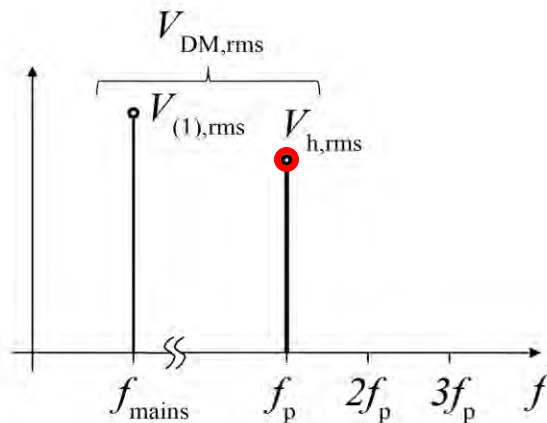
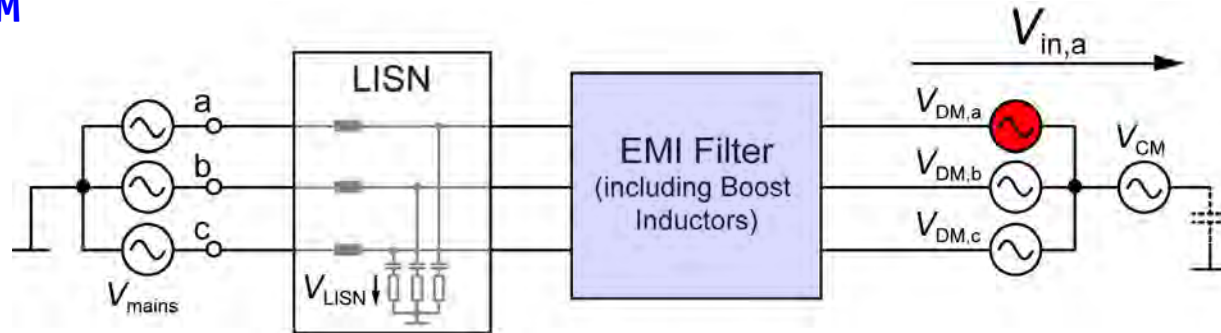
$$= \sqrt{\frac{1}{24} \frac{V_{DC}^2 M (8\sqrt{3} - 3M\pi)}{\pi}}$$



- Model of Test Receiver is Omitted
- Harmonic Power Concentrated only @ Switching Frequency f_p
- $V_{DM,rms}$ can be Calculated in Time Domain

Simplified Calculation of Required Filter Attenuation

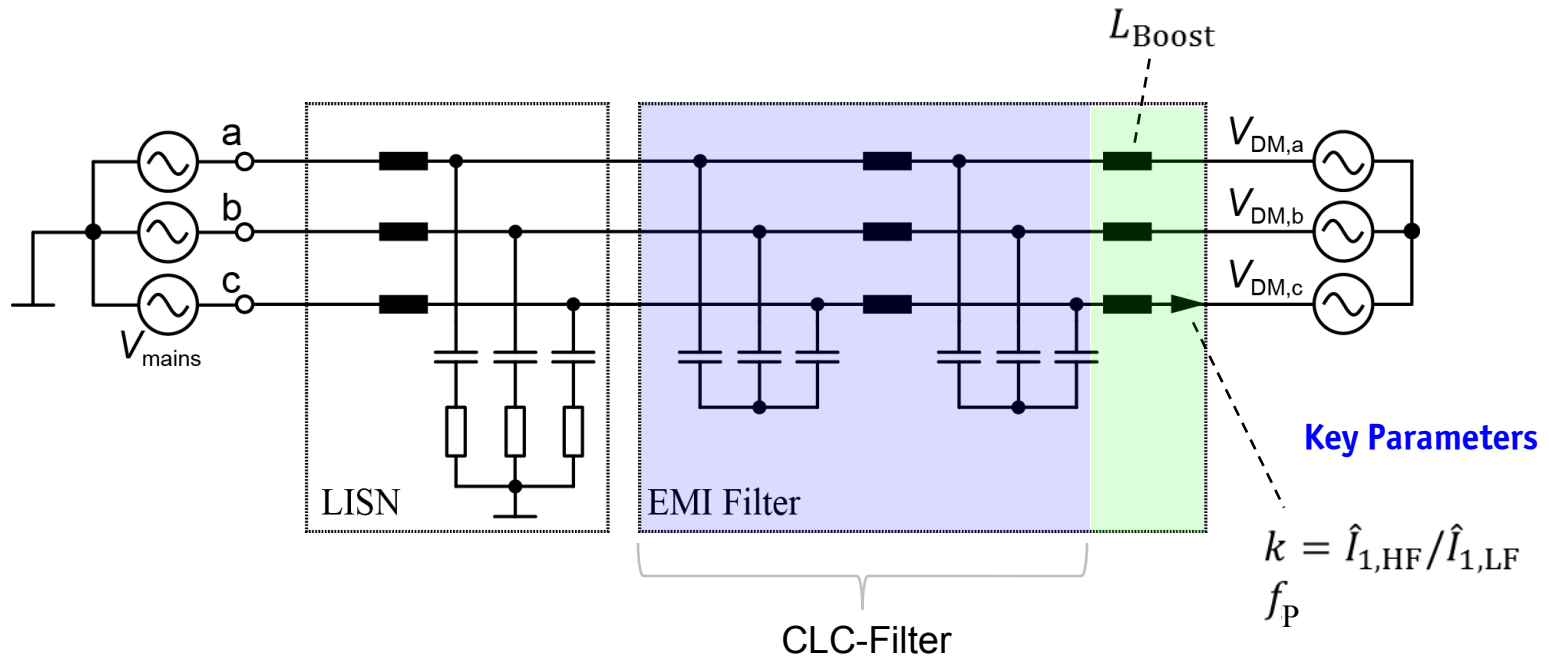
► Shown for DM Attenuation



$$A_{\text{filter}}(f_D) [\text{dB}\mu\text{V}] = V_{\text{est}}(f_D) [\text{dB}\mu\text{V}] - \text{Limit}(f_D) [\text{dB}\mu\text{V}] + \text{Margin}(f_D) [\text{dB}\mu\text{V}]$$

EMI Filter Optimization

► Shown for DM Filter

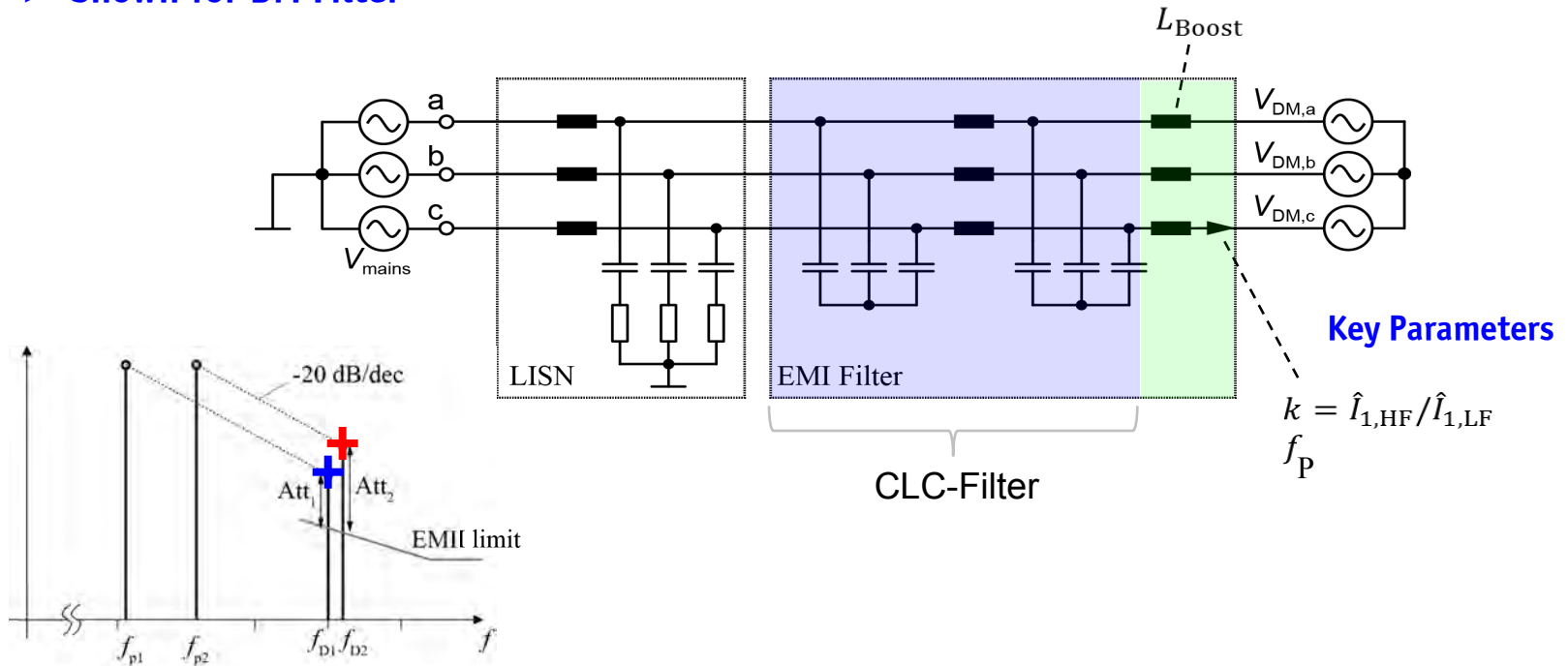


► Optimal Selection of Current Ripple Ratio k ($f_p = const.$)

- High Ripple Current in L_{Boost} (→ high k) requires Large CLC-filter; in Return the L_{boost} is Small
- Small Ripple Current in L_{Boost} (→ small k) requires Large L_{boost} ; in Return the CLC-filter is Small

EMI Filter Optimization

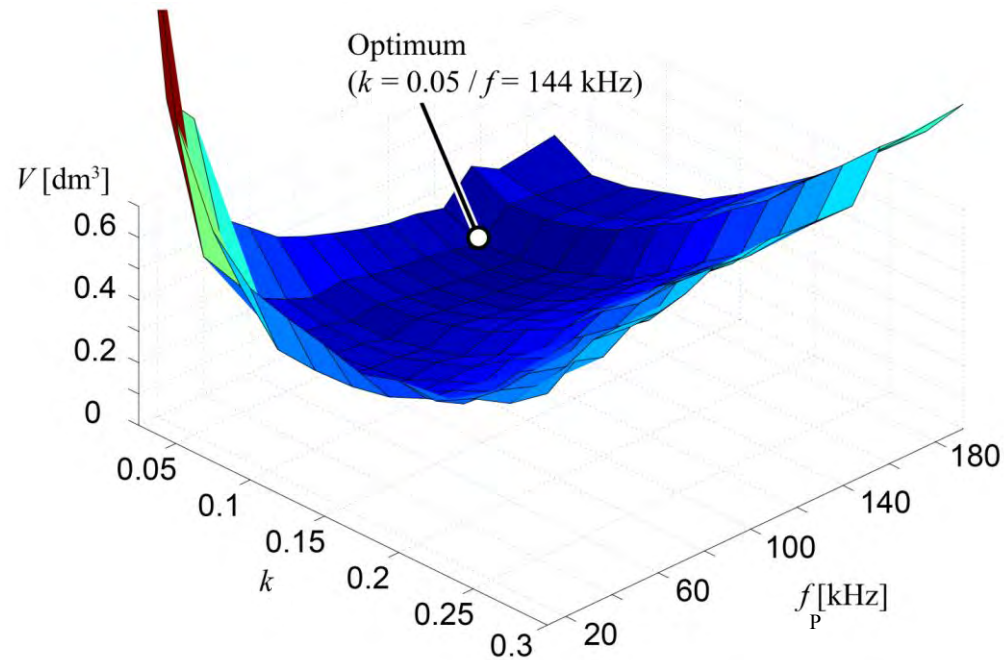
► Shown for DM Filter



► Optimal Selection of Switching Frequency f_p ($k = const.$)

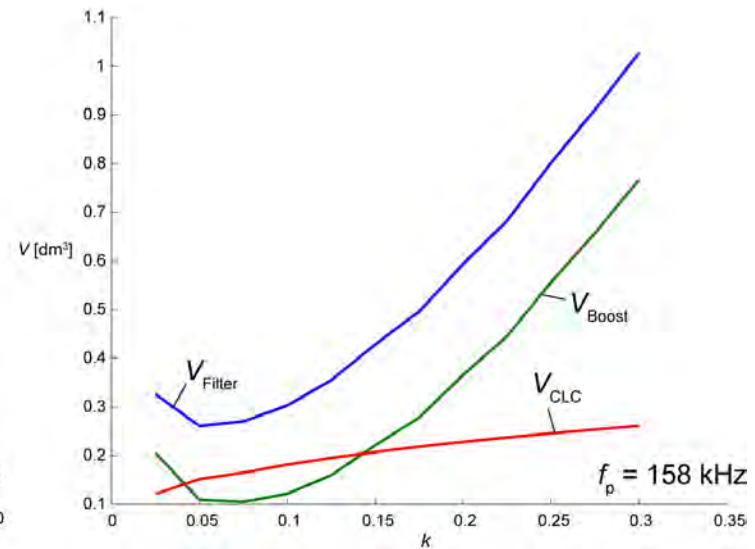
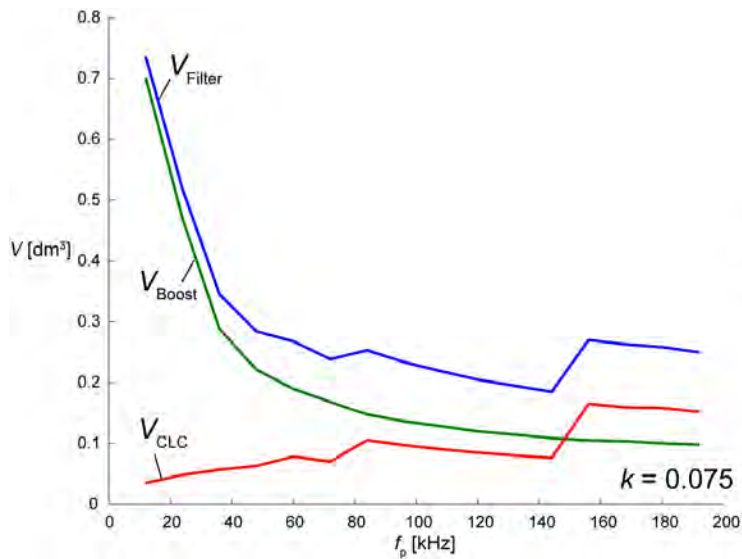
- High Switching Frequency requires Large CLC-filter; in Return the L_{boost} is Small
- Low Switching Frequency requires Large L_{boost} ; in Return the CLC-filter is Small

EMI Filter Optimization



► Optimization Result for DM Filter of a Single-Phase Boost-Type PFC Rectifier

EMI Filter Optimization



► Optimization Result for DM Filter of a Single-Phase Boost-Type PFC Rectifier

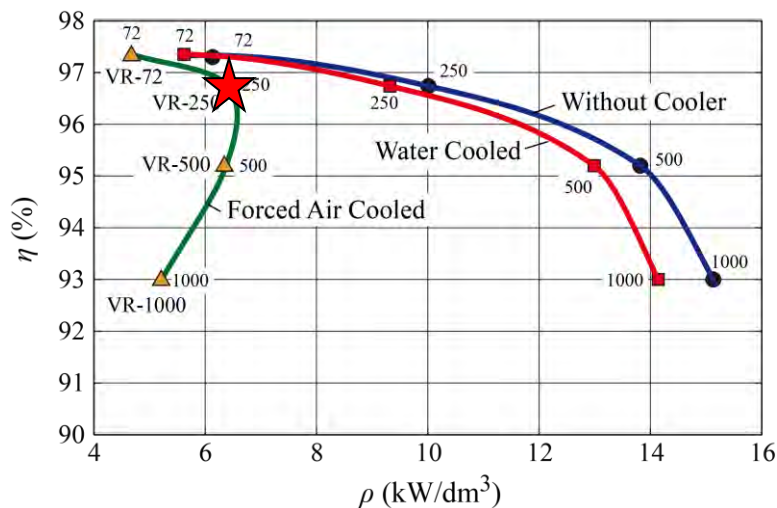
Experimental Analysis

- *Power Density / Efficiency Pareto Limit*
- *Experimental Analysis – VR250*

► Experimental Analysis

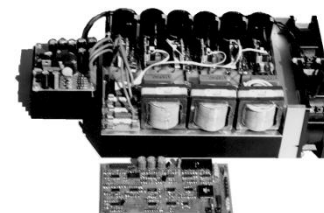
■ Generation 1 – 4 of VIENNA Rectifier Systems

- Switching Frequency of $f_s = 250$ kHz Offers Good Compromise Concerning Power Density / Weight per Unit Power, Efficiency and Input Current Quality THD_i



$$f_s = 50 \text{ kHz}$$

$$\rho = 3 \text{ kW/dm}^3$$



$$f_s = 72 \text{ kHz}$$

$$\rho = 4.6 \text{ kW/dm}^3$$



$$f_s = 250 \text{ kHz}$$

$$\rho = 10 \text{ kW/dm}^3$$

$$(164 \text{ W/in}^3)$$

$$\text{Weight} = 3.4 \text{ kg}$$



$$f_s = 1 \text{ MHz}$$

$$\rho = 14.1 \text{ kW/dm}^3$$

$$\text{Weight} = 1.1 \text{ kg}$$



► Demonstrator – VR250 (1)

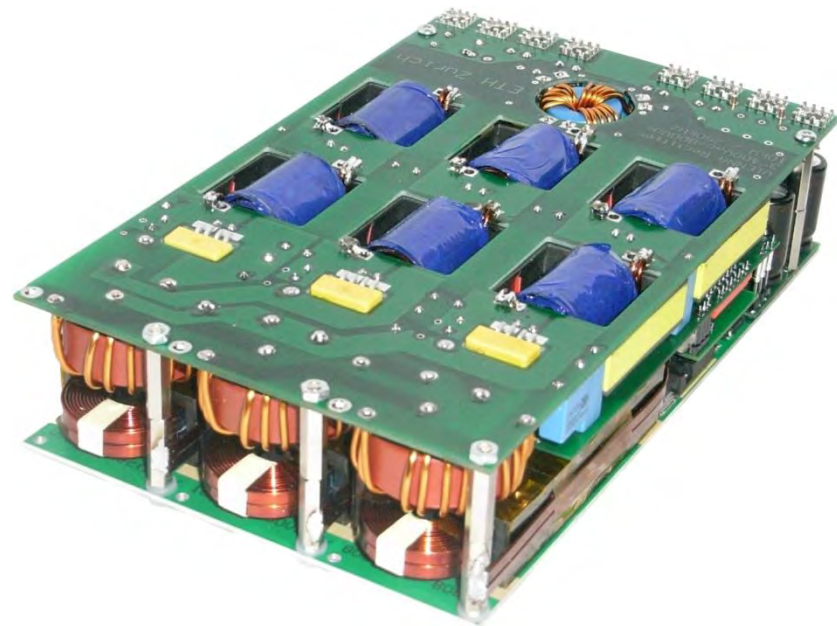
● Specifications

$$\begin{aligned}
 U_{LL} &= 3 \times 400 \text{ V} \\
 f_N &= 50 \text{ Hz} \dots 60 \text{ Hz} \text{ or } 360 \text{ Hz} \dots 800 \text{ Hz} \\
 P_o &= 10 \text{ kW} \\
 U_o &= 2 \times 400 \text{ V} \\
 f_s &= 250 \text{ kHz}
 \end{aligned}$$

● Characteristics

$$\begin{aligned}
 \eta &= 96.8 \% \\
 \text{THD}_i &= 1.6 \% @ 800 \text{ Hz} \\
 &10 \text{ kW/dm}^3 \\
 &3.3 \text{ kg} (\approx 3 \text{ kW/kg})
 \end{aligned}$$

Dimensions: 195 x 120 x 42.7 mm³



► Demonstrator – VR250 (2)

- Specifications

$$\begin{aligned}
 U_{LL} &= 3 \times 400 \text{ V} \\
 f_N &= 50 \text{ Hz ... 60 Hz or 360 Hz ... 800 Hz} \\
 P_o &= 10 \text{ kW} \\
 U_o &= 2 \times 400 \text{ V} \\
 f_s &= 250 \text{ kHz}
 \end{aligned}$$

- Characteristics

$$\begin{aligned}
 \eta &= 96.8 \% \\
 \text{THD}_i &= 1.6 \% @ 800 \text{ Hz} \\
 &10 \text{ kW/dm}^3 \\
 &3.3 \text{ kg } (\approx 3 \text{ kW/kg})
 \end{aligned}$$

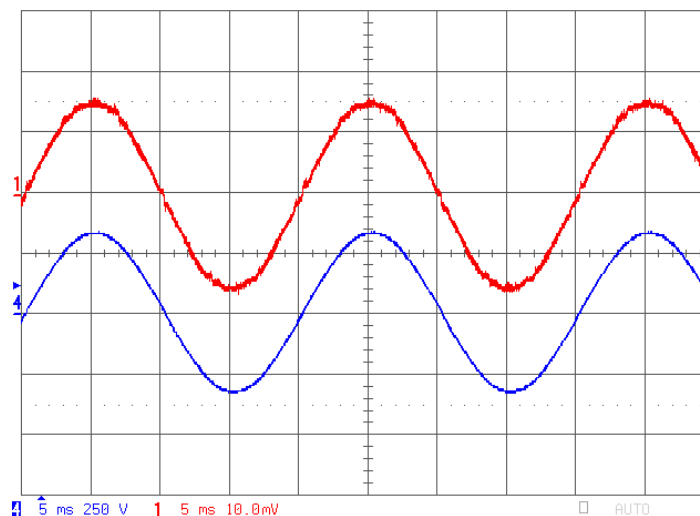
Dimensions: 195 x 120 x 42.7 mm³



► Mains Behavior @ $f_N = 50$ Hz

5A/Div
200V/Div
5ms/Div

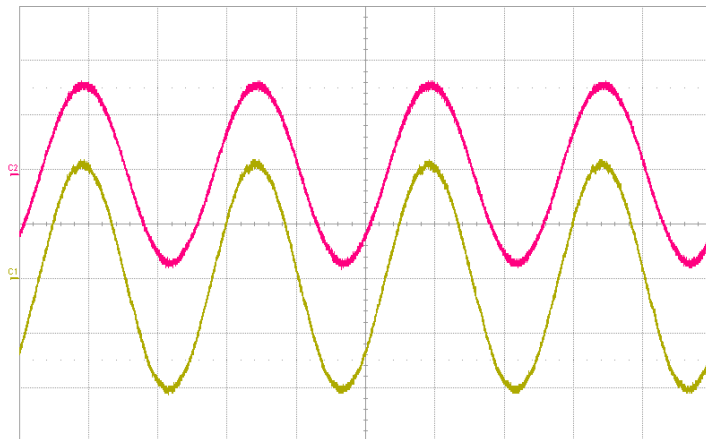
$P_o = 4\text{kW}$
 $U_N = 230\text{V}$
 $f_N = 50\text{Hz}$
 $U_o = 800\text{V}$
 $THD_i = 1.1\%$



► Mains Behavior @ $f_N = 400\text{Hz} / 800\text{Hz}$

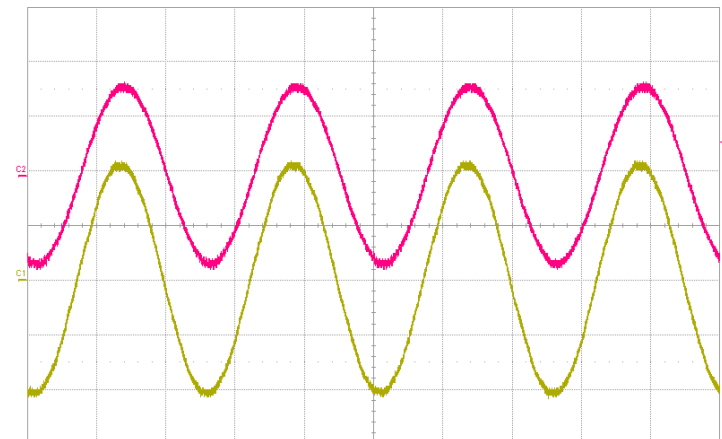
$P_O = 10\text{kW}$
 $U_N = 230\text{V}$
 $f_N = 400\text{Hz}$
 $U_O = 800\text{V}$
 $THD_i = 1.4\%$

10A/Div
 200V/Div
 1ms/Div



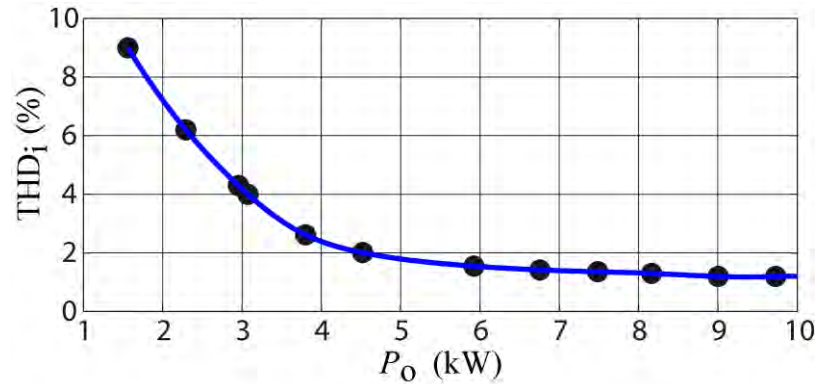
$P_O = 10\text{kW}$
 $U_N = 230\text{V}$
 $f_N = 800\text{Hz}$
 $U_O = 800\text{V}$
 $THD_i = 1.6\%$

10A/Div
 200V/Div
 0.5ms/Div

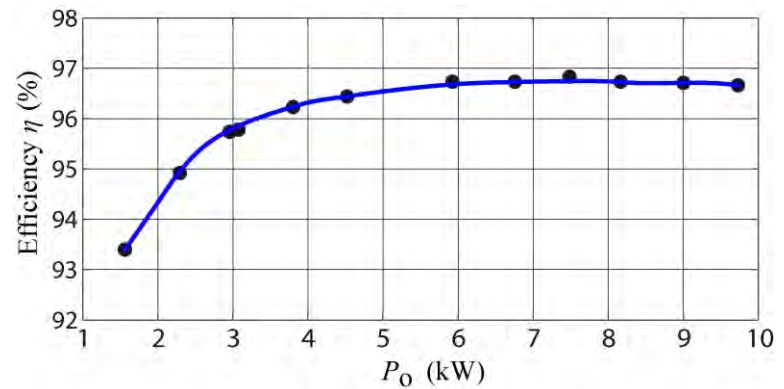


► Demonstrator Performance (VR250)

- Input Current Quality @ $f_N = 800$ Hz

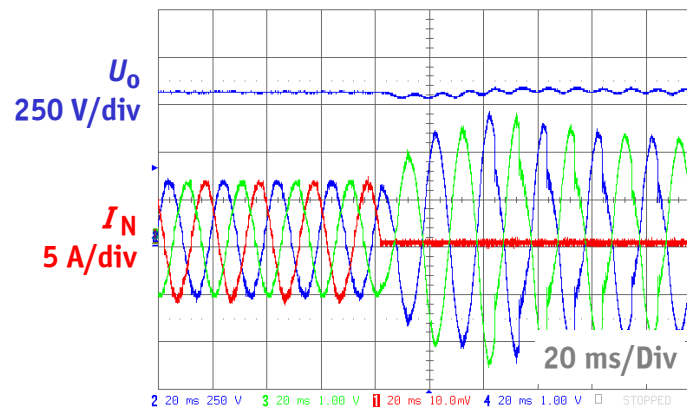


- Efficiency @ $f_N = 800$ Hz

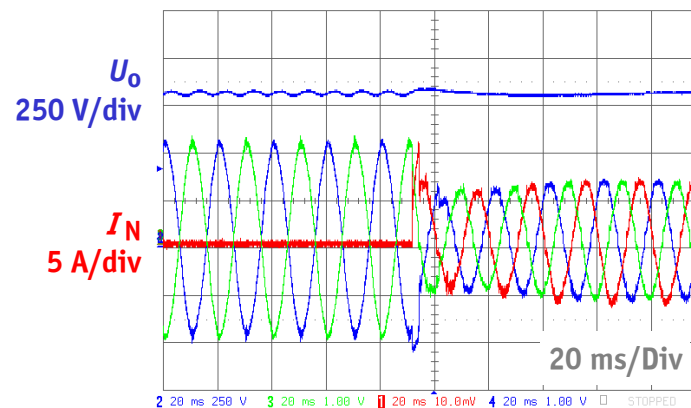


► Demonstrator (VR250) Control Behavior

- Mains Phase Loss

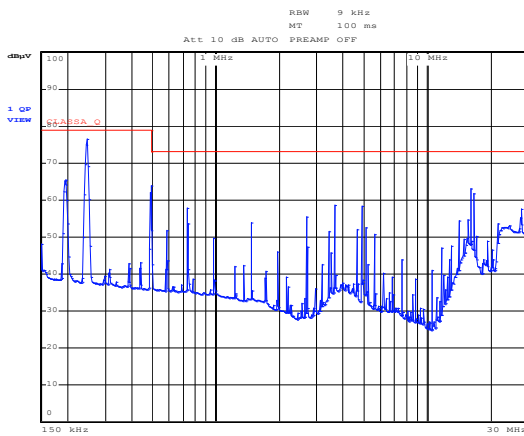


- Mains Phase Return



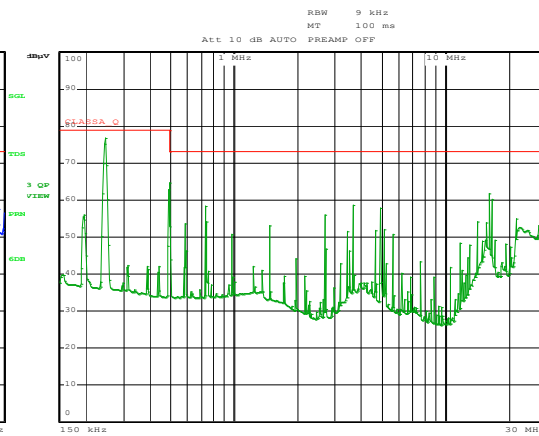
► Demonstrator (VR250) EMI Analysis

● Total Emissions



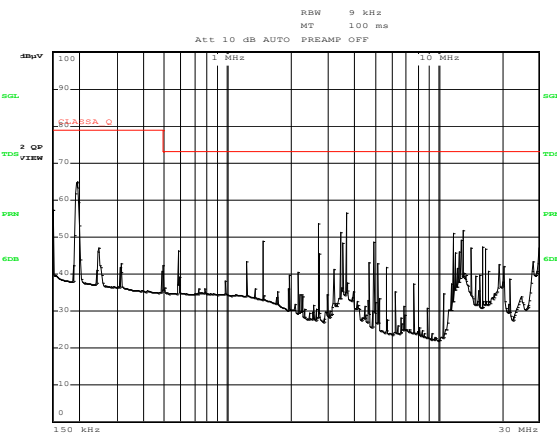
Date: 23.DEC.2009 14:18:39

● DM Emissions



Date: 23.DEC.2009 14:17:40

● CM Emissions



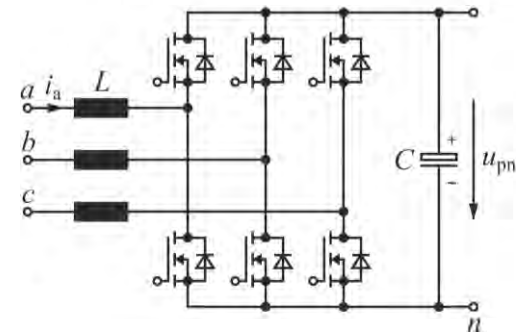
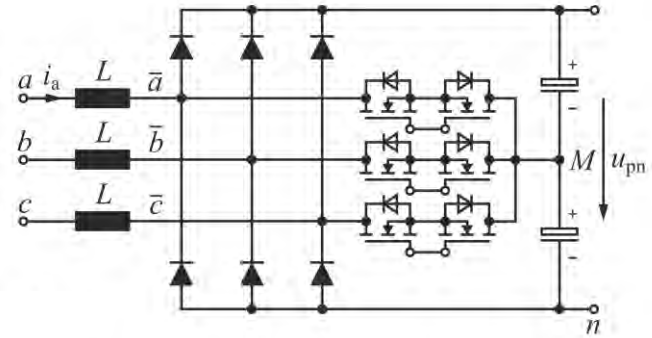
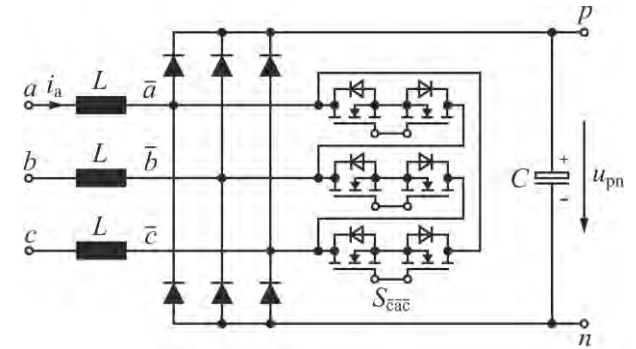
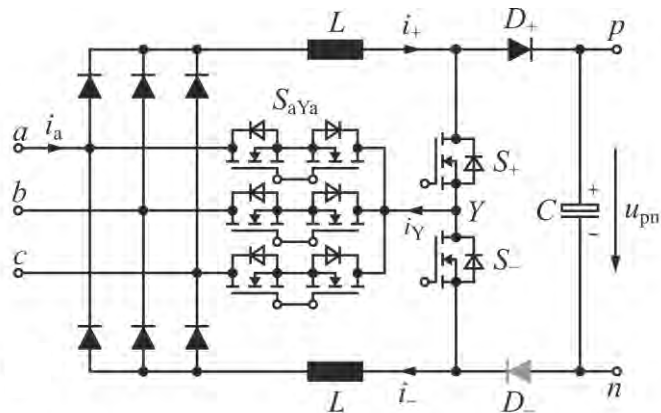
Date: 23.DEC.2009 14:18:11

Evaluation of Boost-Type Systems

3rd Harmonic Inj. Rectifier
Δ-Switch Rectifier
Vienna-Rectifier
Six-Switch Rectifier

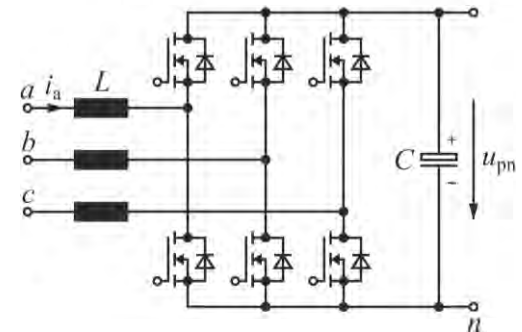
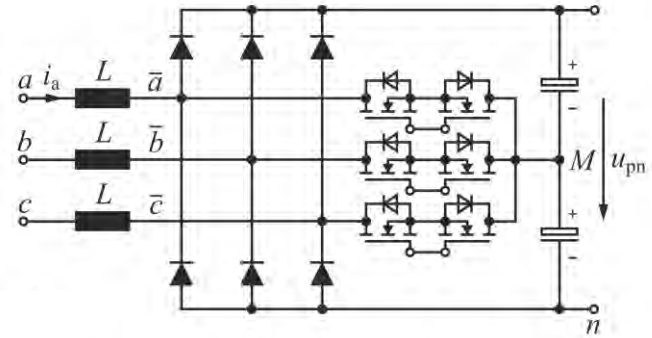
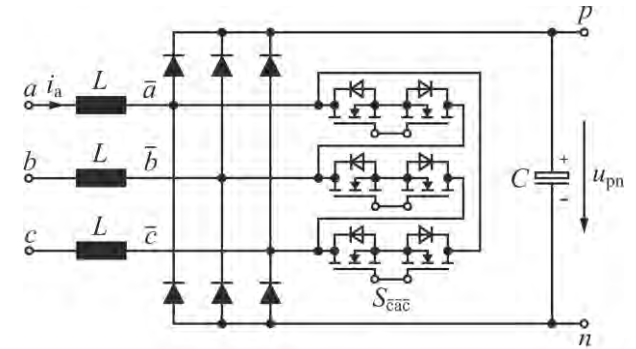
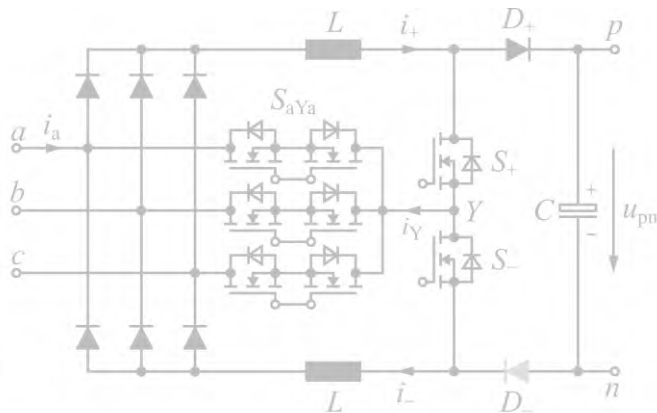
Boost-Type PFC Rectifiers

- 3rd Harmonic Inj. Type
- Diode Bridge Conduction Modulation



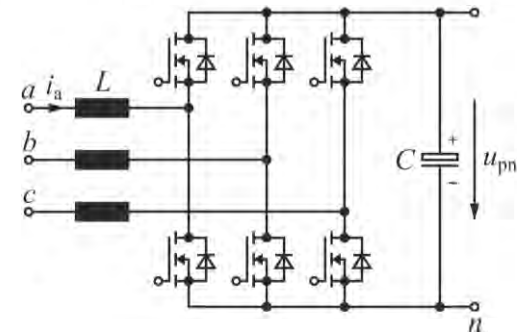
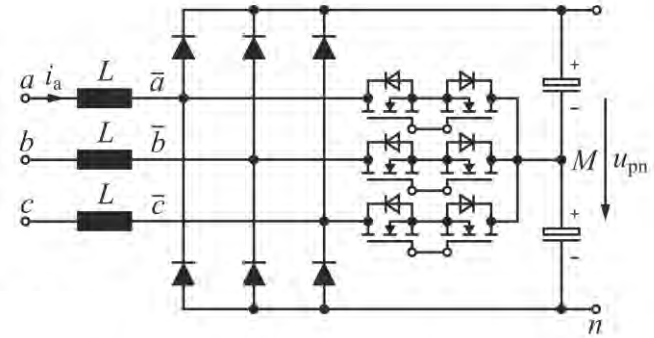
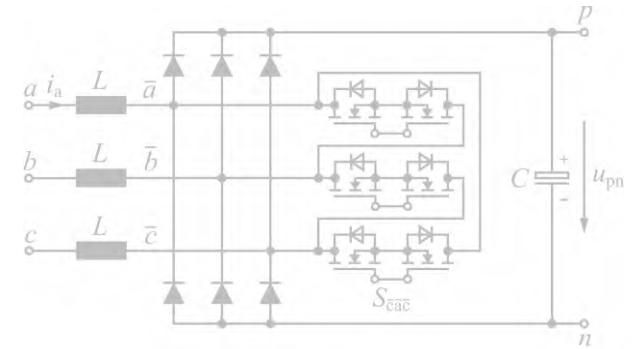
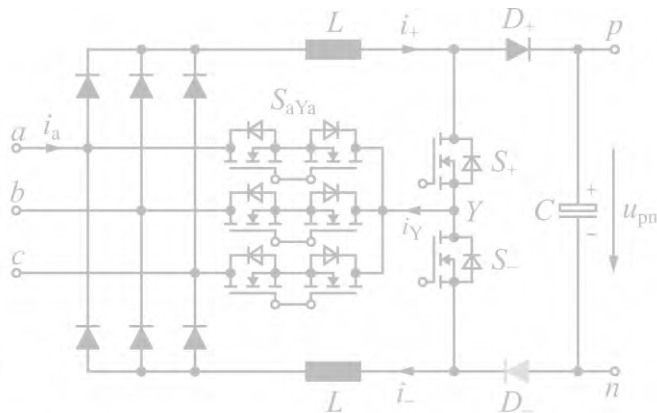
Boost-Type PFC Rectifiers

- 3rd Harmonic Inj. Type
→ Limited Operating Range

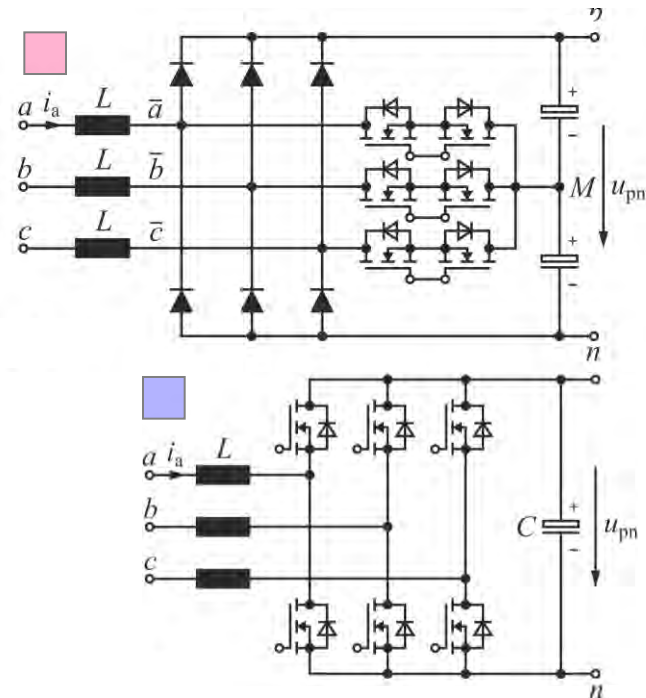
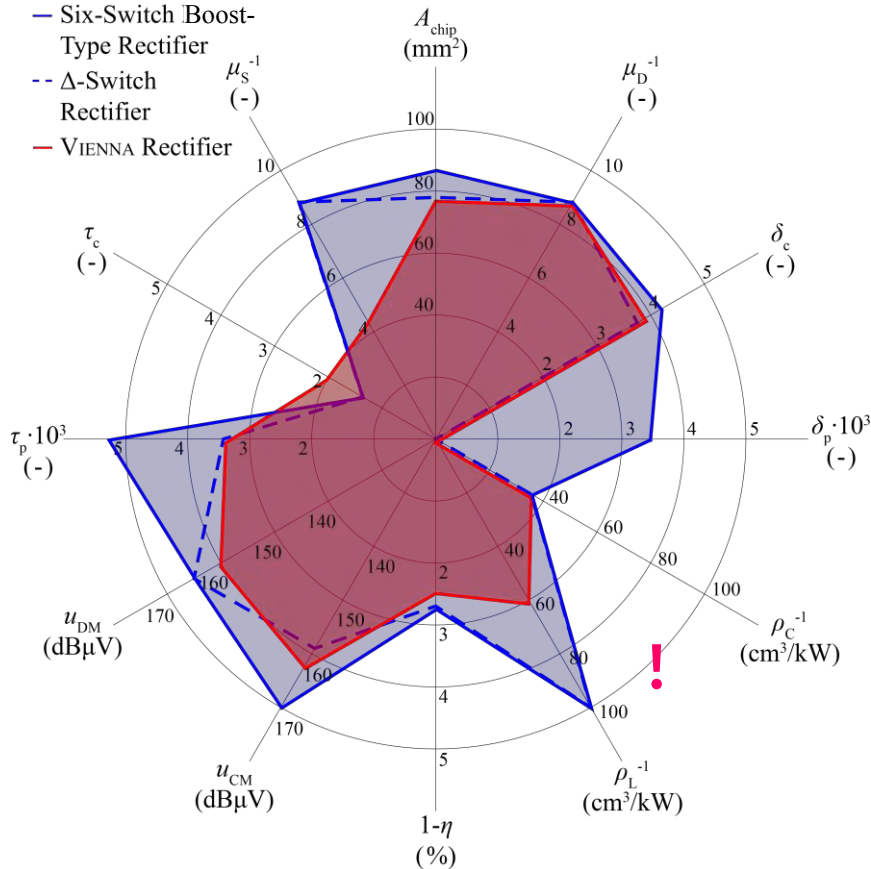


Boost-Type PFC Rectifiers

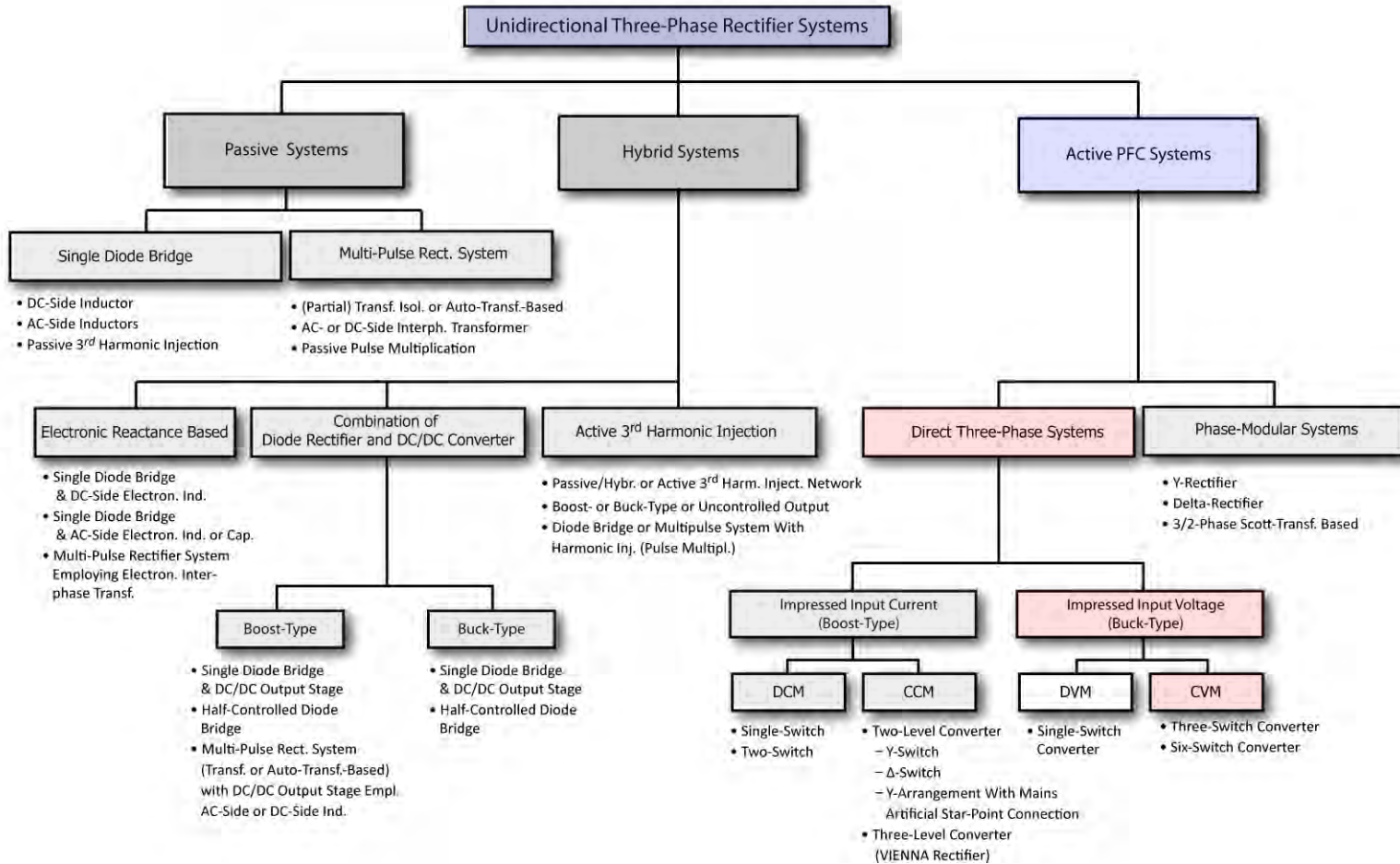
- Δ -Switch Rectifier
→ System Complexity



Vienna Rectifier vs. Six-Switch Rectifier



► Classification of Unidirectional Rectifier Systems

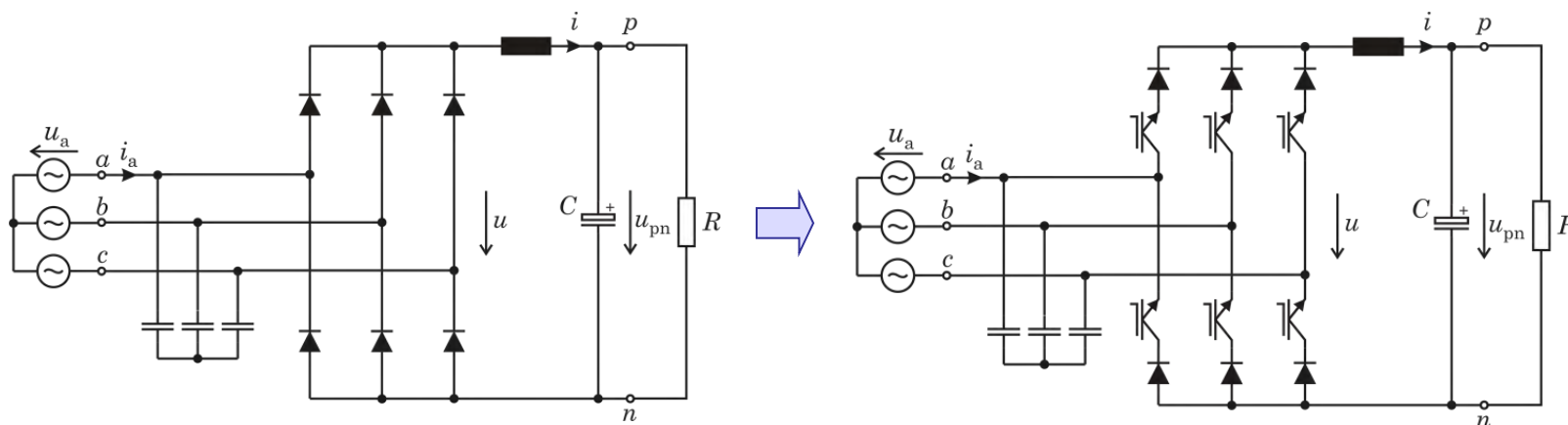


Buck-Type CVM PFC Rectifier System

- *Derivation of Circuit Topologies*

► Derivation of the Circuit Topology (1)

■ Insertion of Switches in Series to the Diodes

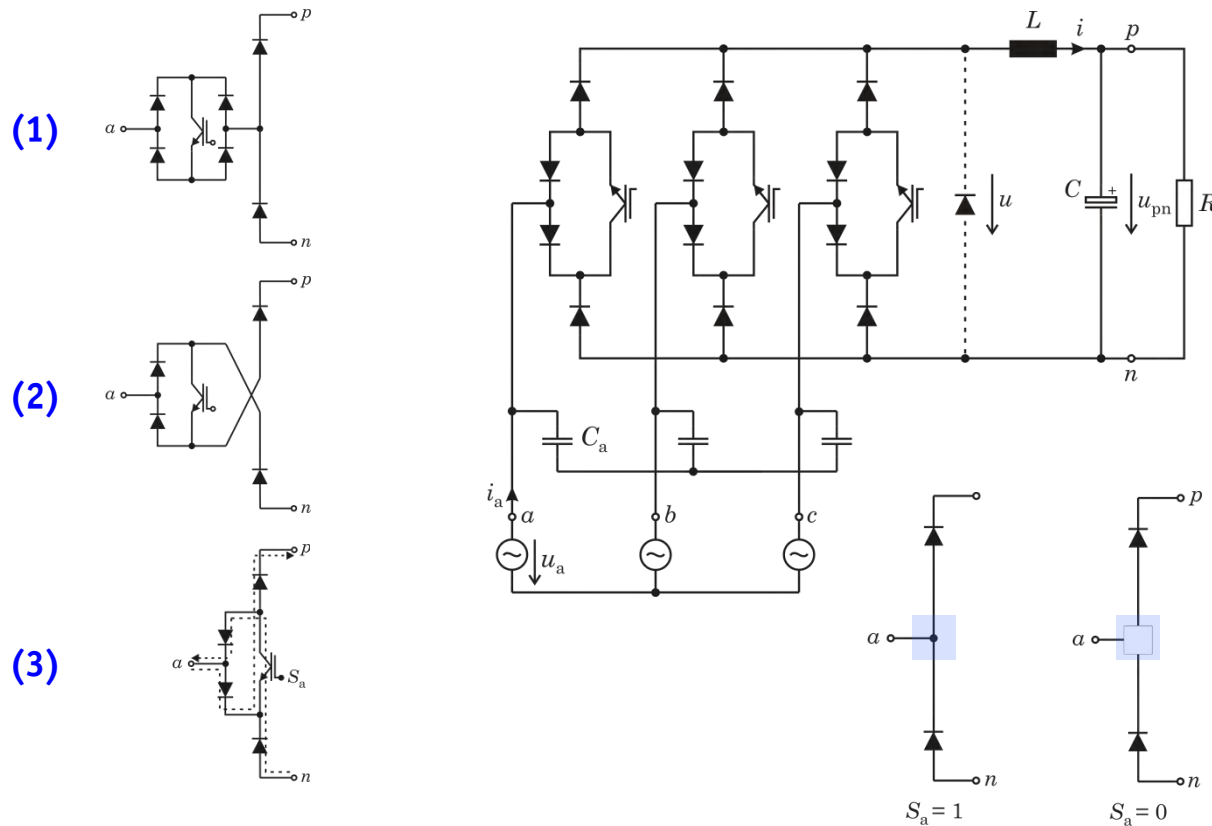


+ DC Current Distribution to Phases *a, b, c*
can be Controlled

+ Control of Output Voltage $0 \leq u \leq \frac{3}{2} \hat{U}$

- Pulsating Input Currents / EMI Filtering Requ.
- Relatively High Conduction Losses

► Derivation of the Circuit Topology (2)

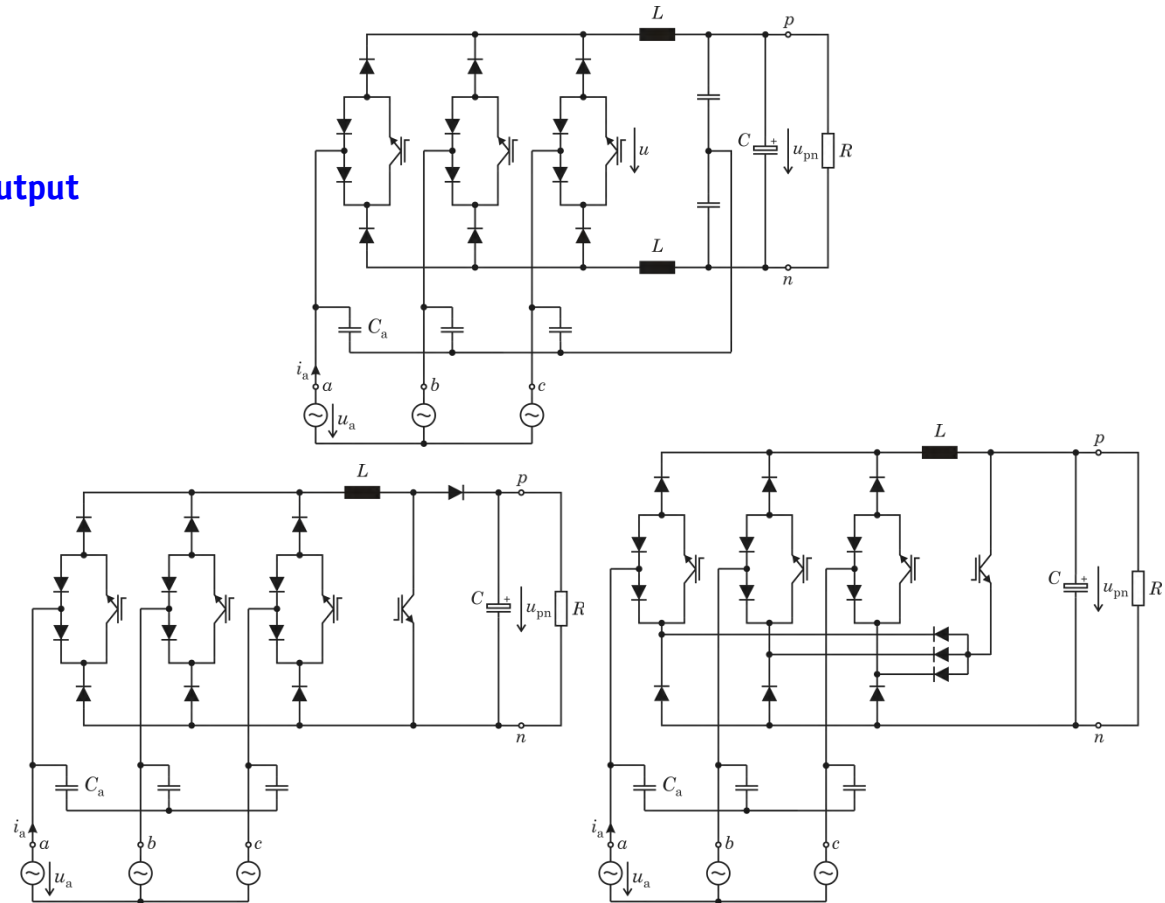


- Insertion of 4Q-Switches on the AC-Side in Order to Enable Control of the DC Current Distribution to Phases a , b , c

► Derivation of the Circuit Topology (3)

■ Circuit Extensions

- Internal Filtering of CM Output Voltage Component
- Integration of Boost-Type Output Stage
- Wide Output Voltage Range, i.e. also $U > \frac{3}{2} \hat{U}$
- Sinusoidal Mains Current also in Case of Phase Loss



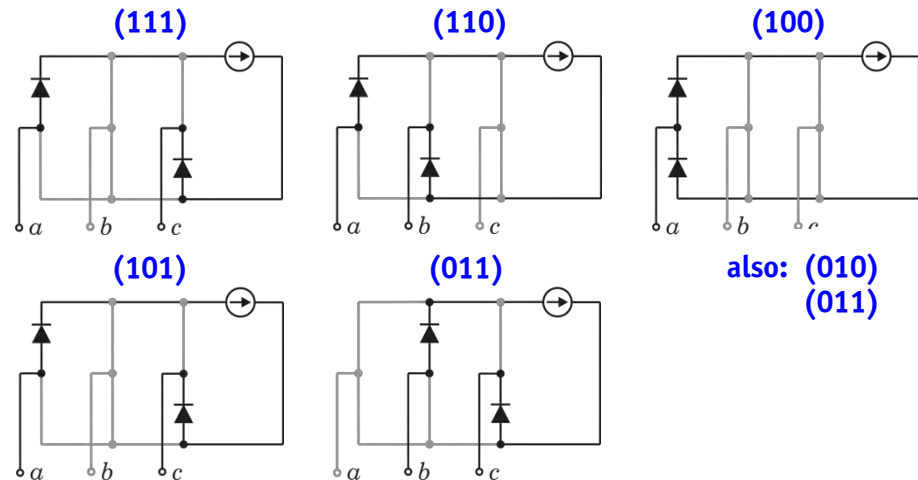
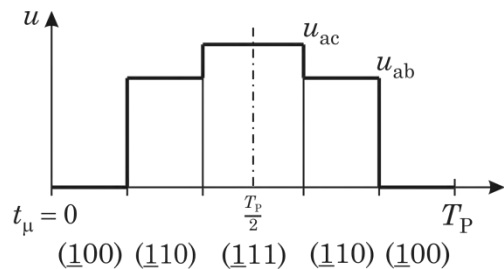
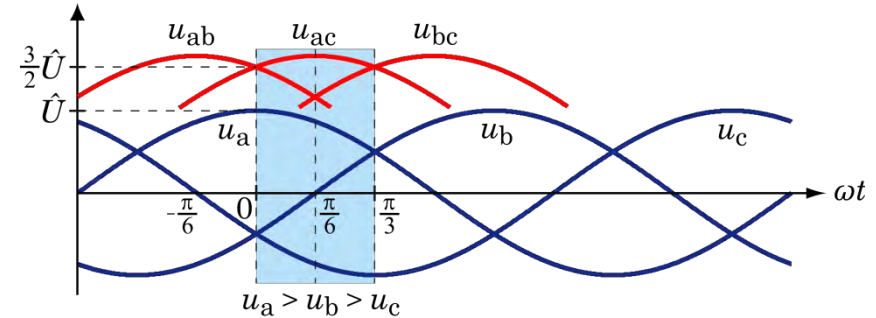
■ Circuit Extensions Shown for 3-Switch Topology, but is also Applicable to 6-Switch Topology

Buck-Type PFC Rectifier Analysis

- *Modulation*
- *Input Current Formation*
- *Output Voltage Formation*
- *Experimental Analysis*

► Modulation Scheme

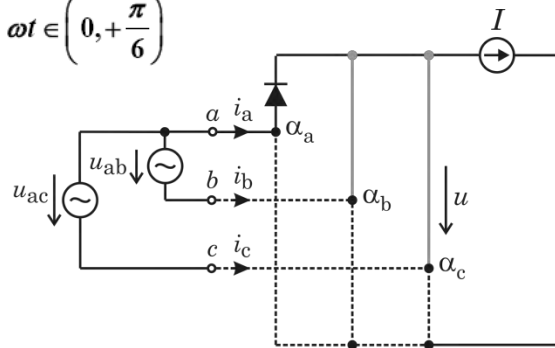
- Consider 60°-Wide Segment of the Mains Period; Suitable Switching States Denominated by (s_a, s_b, s_c)
- Clamping to Phase with Highest Absolute Voltage Value, i.e.
 - Phase a for $\omega t \in \left(-\frac{\pi}{6}, +\frac{\pi}{6}\right)$,
 - Phase c for $\omega t \in \left(+\frac{\pi}{6}, +\frac{\pi}{2}\right)$ etc.
- Assumption: $\omega t \in \left(0, +\frac{\pi}{6}\right)$



- Clamping and “Staircase-Shaped” Link Voltage in Order to Minimize the Switching Losses

► Input Current and Output Voltage Formation (1)

- Assumption: $\omega t \in \left(0, +\frac{\pi}{6}\right)$



- Ohmic Mains Behavior:

$$i_a = G^* u_a = (\alpha_b + \alpha_c) \cdot I$$

$$i_b = G^* u_b = -\alpha_b \cdot I$$

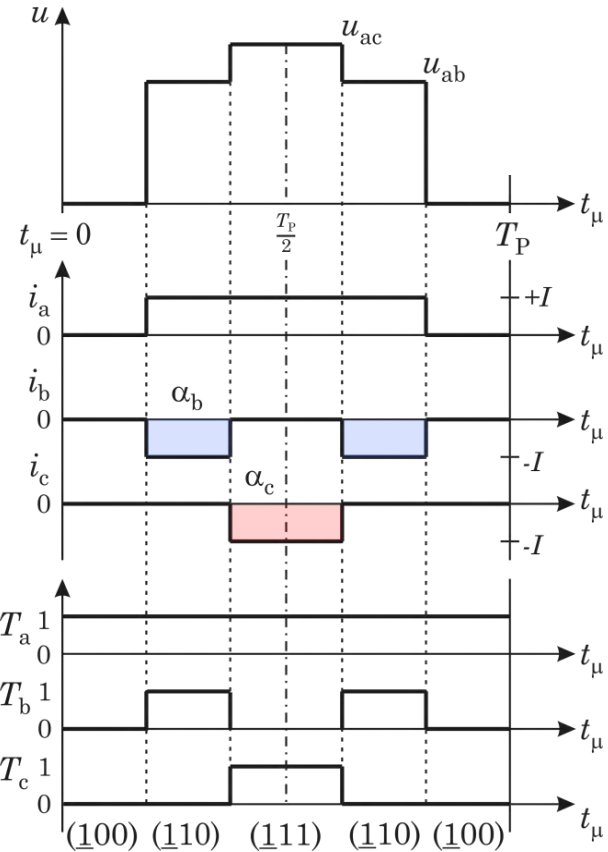
$$i_c = G^* u_c = -\alpha_c \cdot I$$

- Example:

$$\alpha_b + \alpha_c = \frac{G^* u_a}{I} = \frac{G^* \hat{U}}{I} \cdot \cos(\omega t) = M \cdot \cos(\omega t)$$

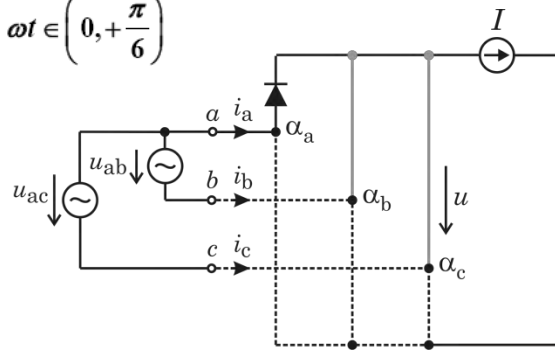
$$\alpha_b = -\frac{G^* u_b}{I} = M \cdot \cos\left(\omega t - \frac{2\pi}{3}\right)$$

$$M \in (0 \dots 1), I \geq \hat{I}^* \quad \alpha_c = -\frac{G^* u_c}{I} = M \cdot \cos\left(\omega t + \frac{2\pi}{3}\right)$$



► Input Current and Output Voltage Formation (2)

- Assumption: $\omega t \in \left(0, +\frac{\pi}{6}\right)$



- Output Voltage Formation:

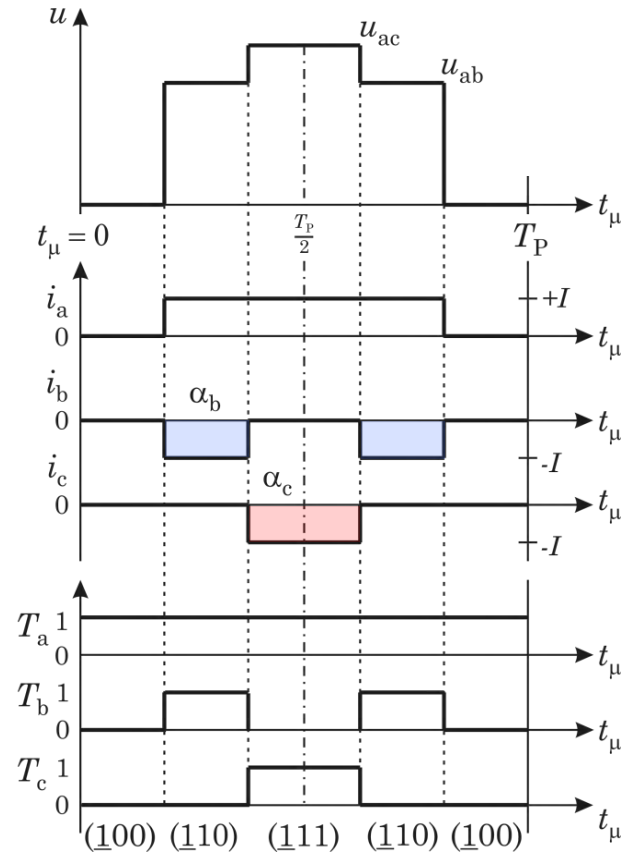
$$\bar{u} = u_{ab} \cdot \alpha_b + u_{ac} \cdot \alpha_c$$

$$P_{\text{link}} = P_{\text{input}}$$

$$\bar{u} \cdot I = \frac{3}{2} \cdot \hat{U} \cdot \hat{I}^*$$

$$\bar{u} = \frac{3}{2} \cdot \hat{U} \cdot \frac{\hat{I}^*}{I} = \frac{3}{2} \cdot \hat{U} \cdot M$$

- Output Voltage is Formed by Segments of the Input Line-to-Line Voltages
- Output Voltage Shows Const. Local Average Value



► Experimental Results

■ Ultra-Efficient Demonstrator System

$$U_{LL} = 3 \times 400 \text{ V (50 Hz)}$$

$$P_o = 5 \text{ kW}$$

$$U_o = 400 \text{ V}$$

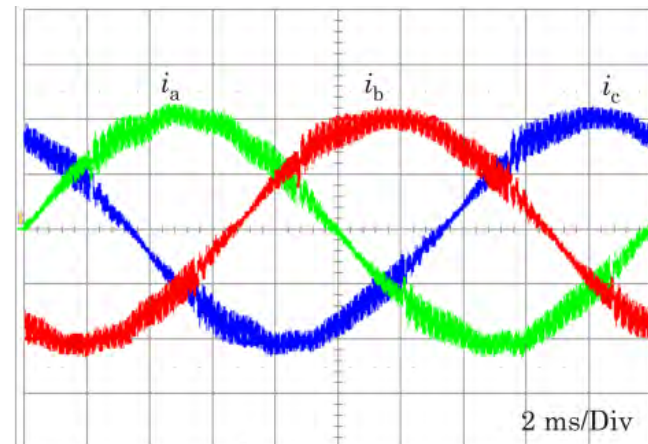
$$f_s = 18 \text{ kHz}$$

$$L = 2 \times 0.65 \text{ mH}$$

$$\eta = 98.8\% \text{ (Calorimetric Measurement)}$$



Input Phase Currents (5 A/Div)



► Experimental Results

■ Ultra-Efficient Demonstrator System

$U_{LL} = 3 \times 400 \text{ V (50 Hz)}$

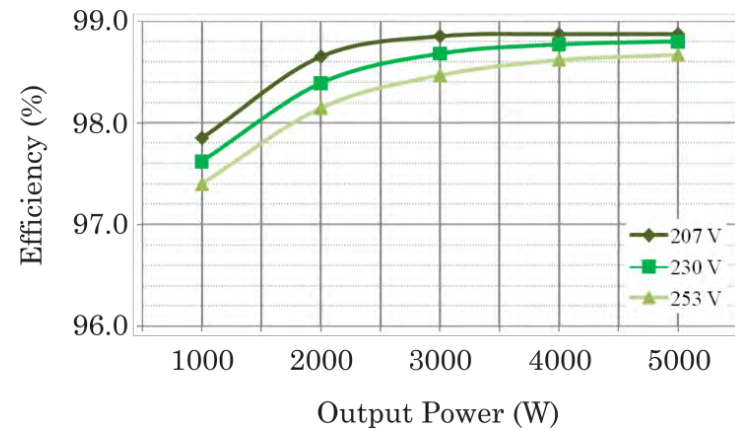
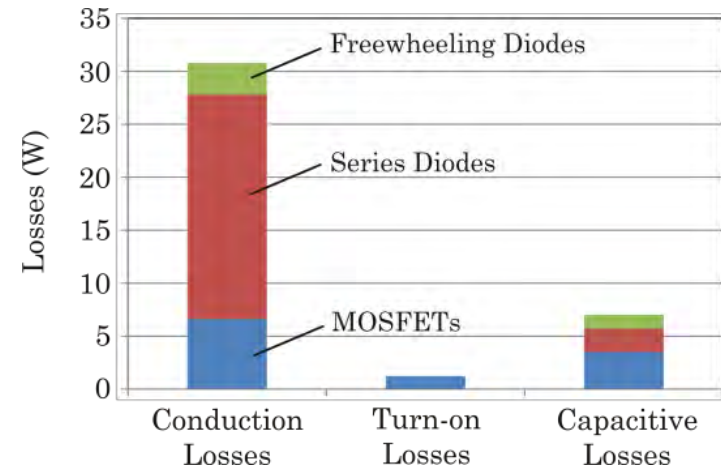
$P_o = 5 \text{ kW}$

$U_o = 400 \text{ V}$

$f_s = 18 \text{ kHz}$

$L = 2 \times 0.65 \text{ mH}$

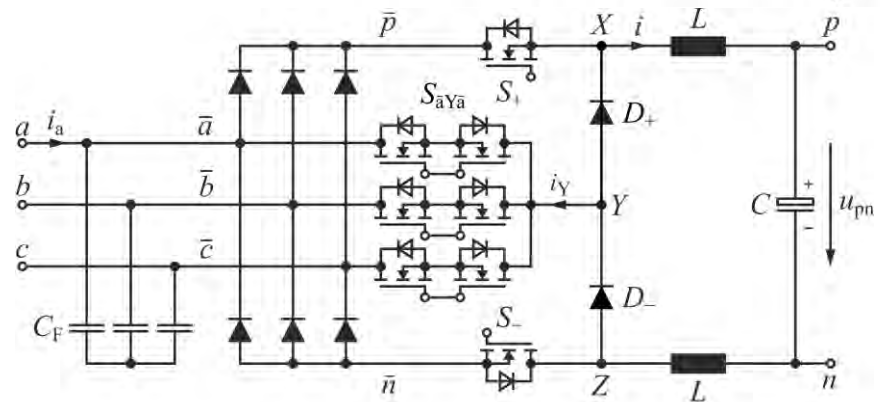
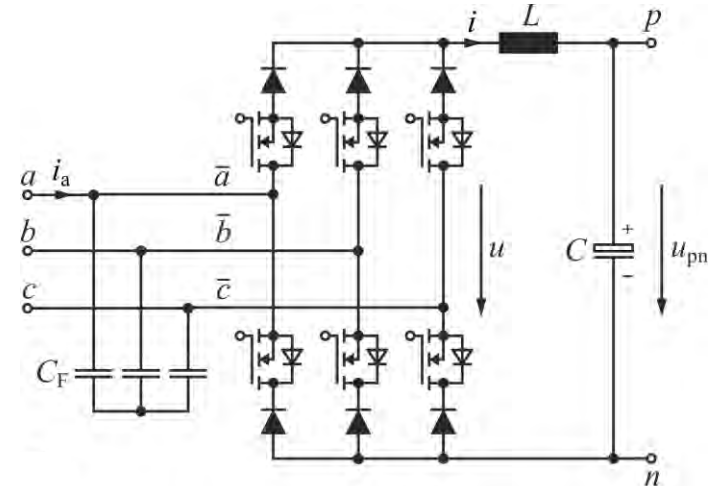
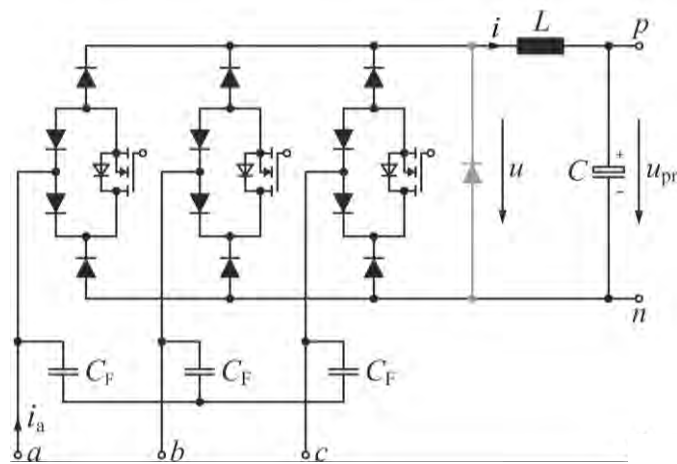
$\eta = 98.8\%$ (Calorimetric Measurement)



Comparison of Buck-Type Systems

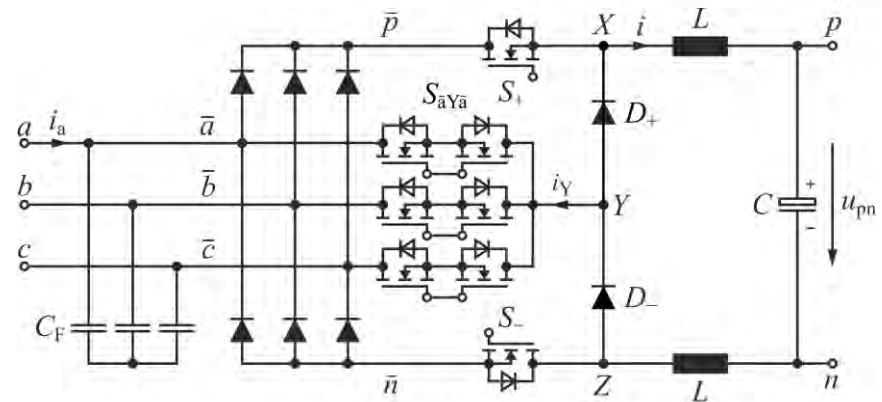
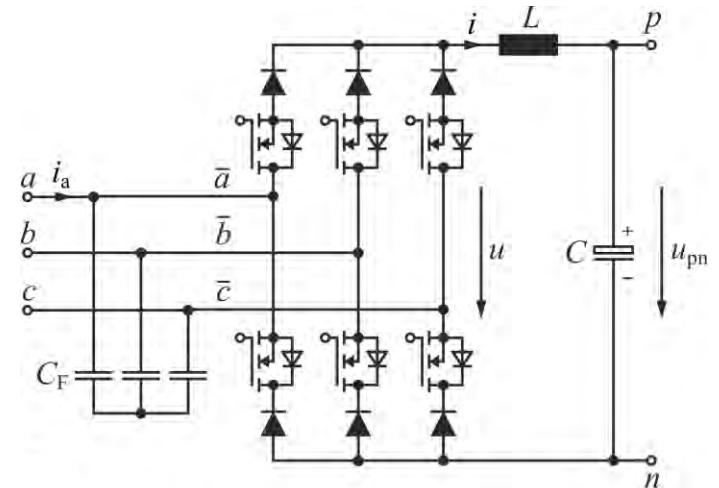
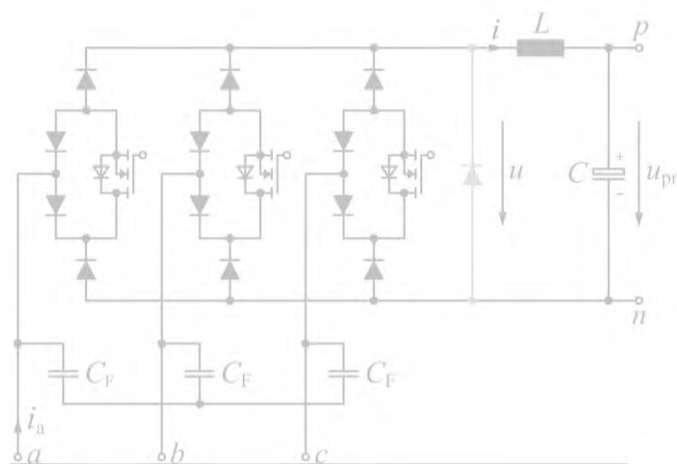
Six-Switch Rectifier
SWISS-Rectifier

Buck-Type PFC Rectifiers



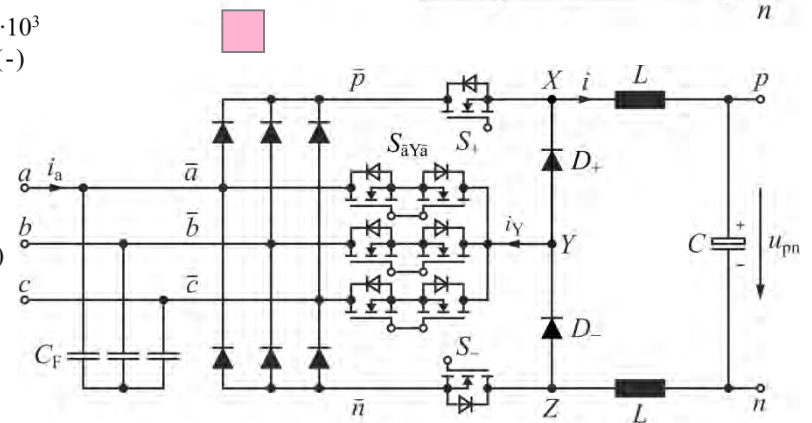
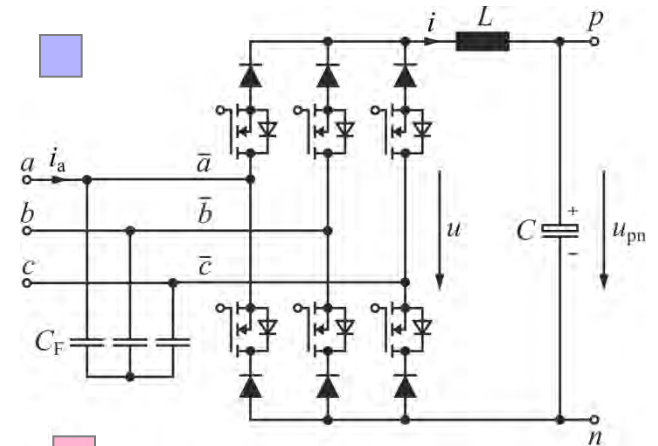
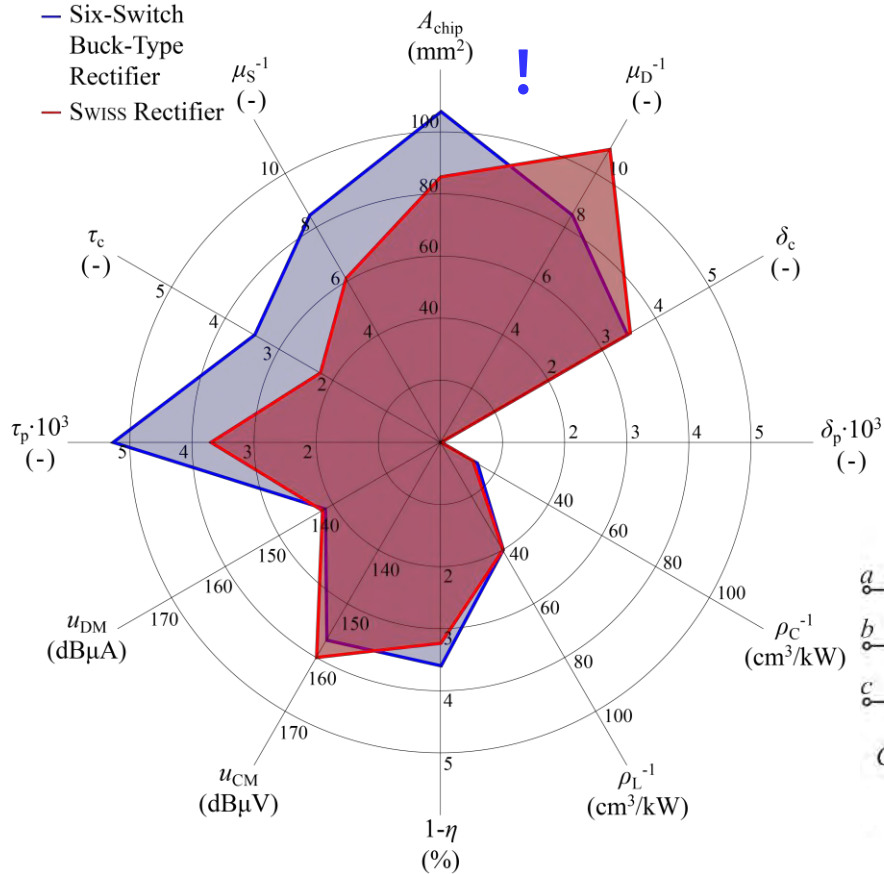
- 3rd Harmonic Inj. Type
- Diode Bridge Cond. Modulation

Buck-Type PFC Rectifiers



- Three-Switch Rectifier
 → Conduction Losses

SWISS Rectifier vs. Six-Switch Rectifier



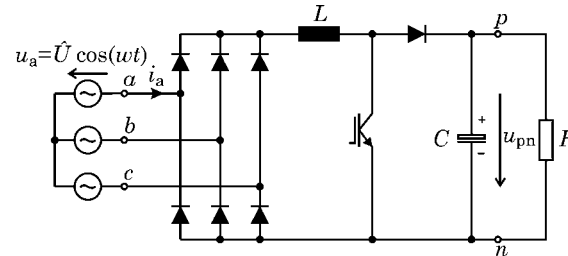
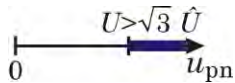
Summary of Unidirectional PFC Rectifier Systems

- *Block Shaped Input Current Systems*
- *Sinusoidal Input Current Systems*

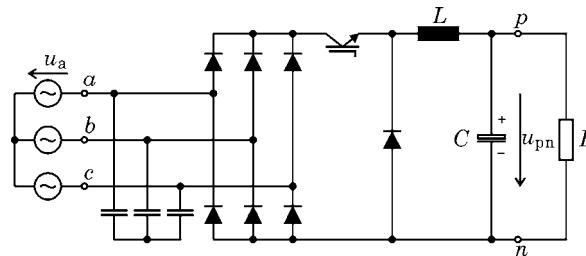
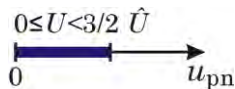
► Block Shaped Input Current Rectifier Systems

- + Controlled Output Voltage
- + Low Complexity
- + High Semicond. Utilization
- + Total Power Factor $\lambda \approx 0.95$
- THD_I $\approx 30\%$

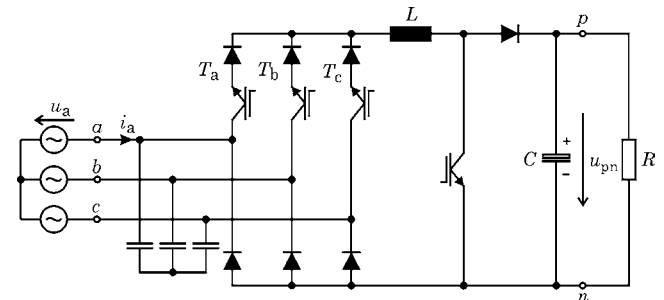
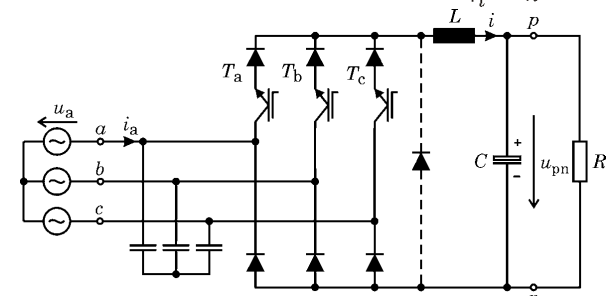
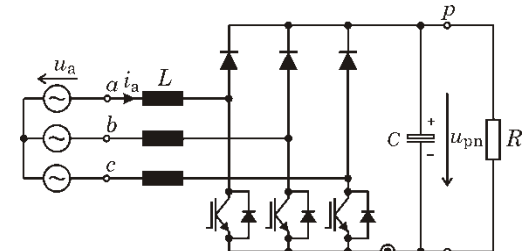
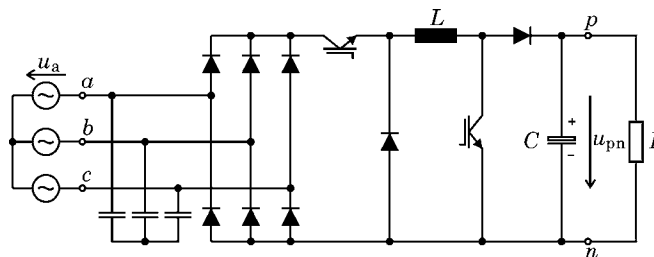
Boost-Type



Buck-Type



Buck+Boost-Type

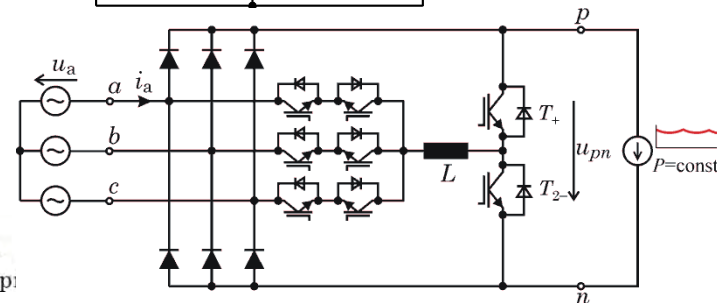
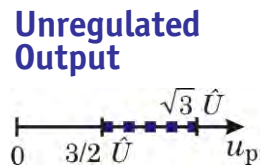
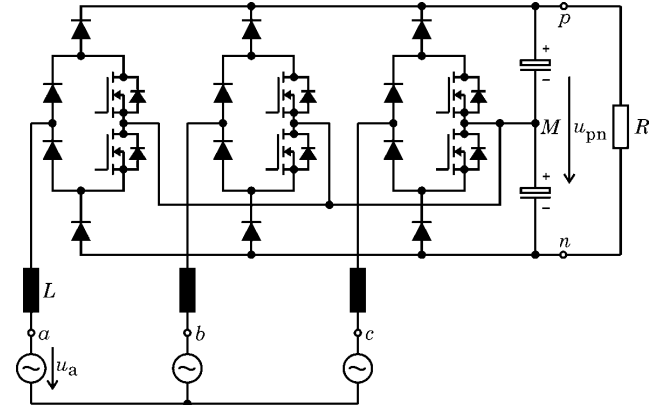
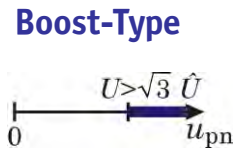
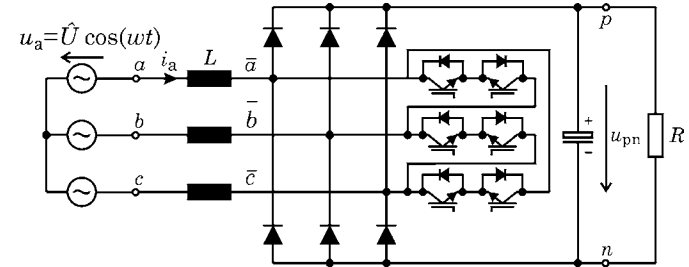
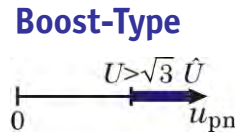


Sinusoidal Input Current Rectifier Systems (1)

- + Controlled Output Voltage
- + Relatively Low Control Complexity
- + Tolerates Mains Phase Loss
- 2-Level Characteristic
- Power Semiconductors Stressed with Full Output Voltage

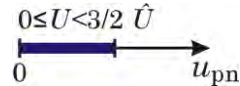
- + Controlled Output Voltage
- + 3-Level Characteristic
- + Tolerates Mains Phase Loss
- + Power Semicond. Stressed with Half Output Voltage
- Higher Control Complexity

- + Low Current Stress on Power Semicond.
- + In Principal No DC-Link Cap. Required
- + Control Shows Low Complexity
- Sinusoidal Mains Current Only for Const. Power Load
- Power Semicond. Stressed with Full Output Voltage
- Does Not Tolerate Loss of a Mains Phase

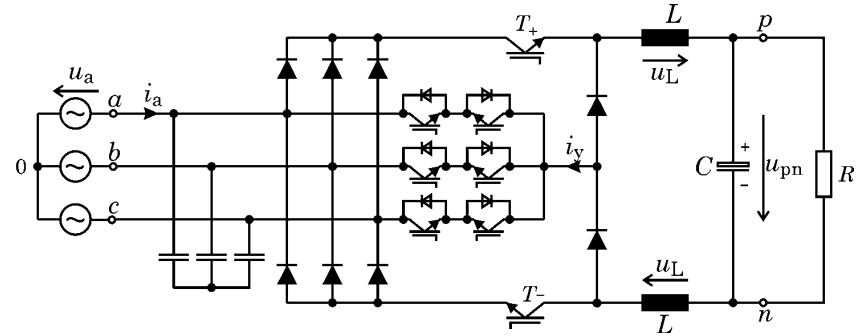


► Sinusoidal Input Current Rectifier Systems (2)

Buck-Type



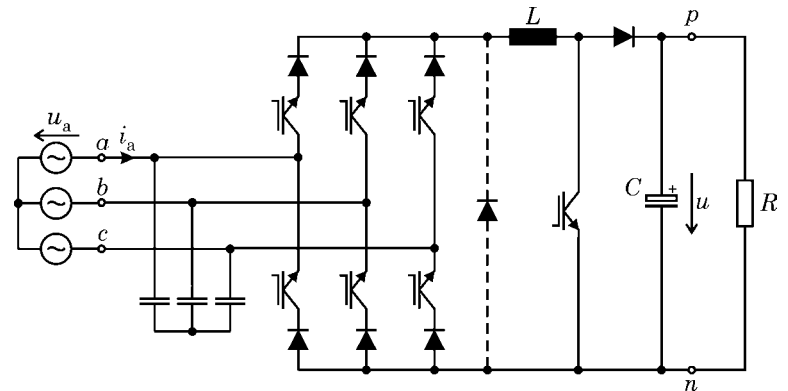
- + Allows to Generate Low Output Voltages
- + Short Circuit Current Limiting Capability
- Power Semicond. Stressed with LL-Voltages
- AC-Side Filter Capacitors / Fundamental Reactive Power Consumption



Buck+Boost-Type



- + See Buck-Type Converter
- + Wide Output Voltage Range
- + Tolerates Mains Phase Loss, i.e. Sinusoidal Mains Current also for 2-Phase Operation
- See Buck-Type Converter (6-Switch Version of Buck Stage Enables Compensation of AC-Side Filter Cap. Reactive Power)

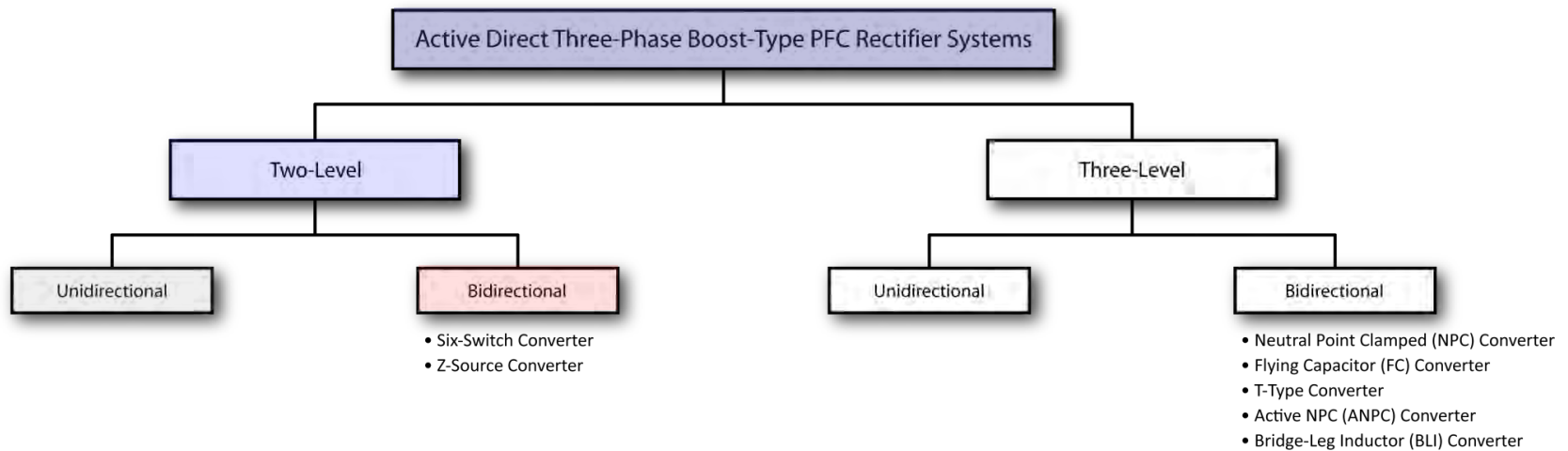


Bidirectional PFC Rectifier Systems

- *Boost-Type Topologies*
- *Buck-Type Topologies*

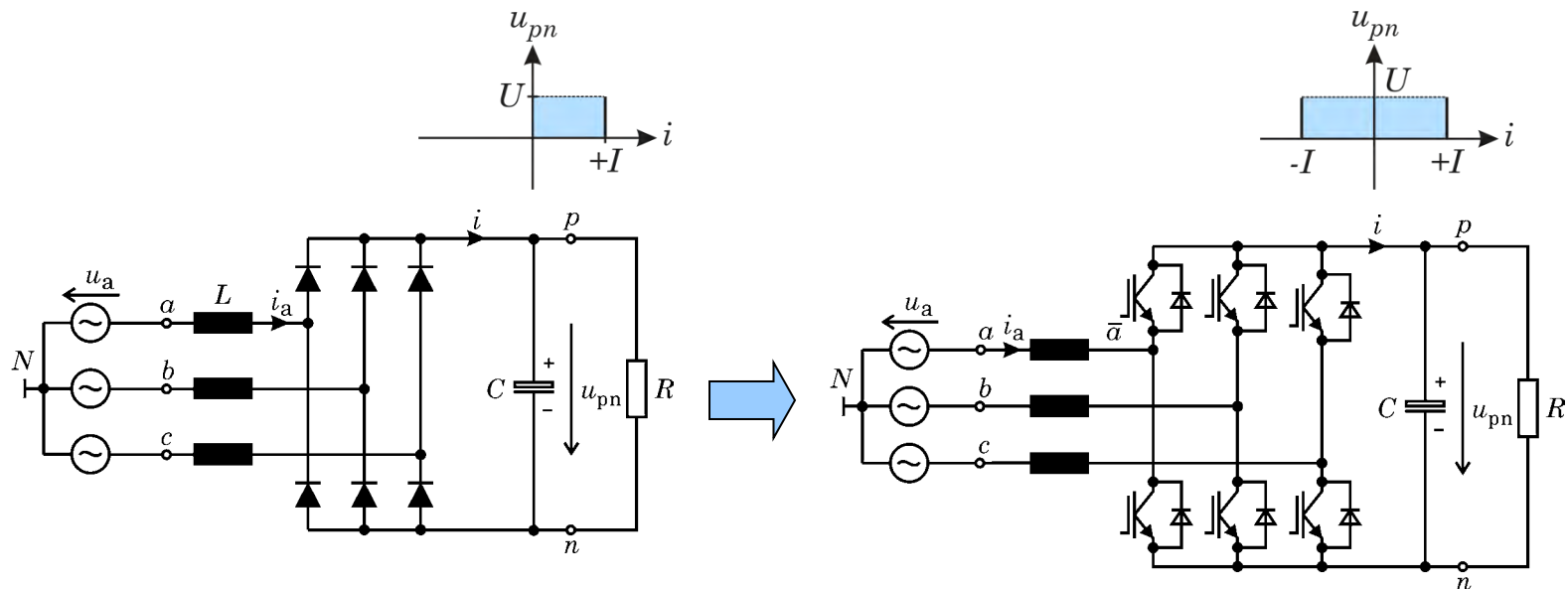
Boost-Type Topologies

► Classification of Bidirectional Boost-Type Rectifier Systems

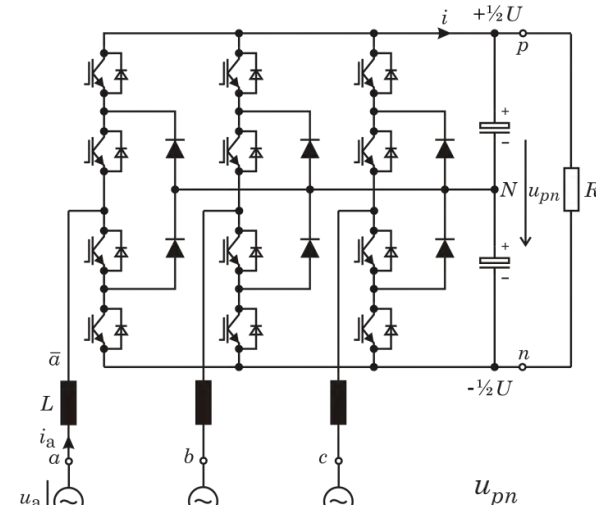
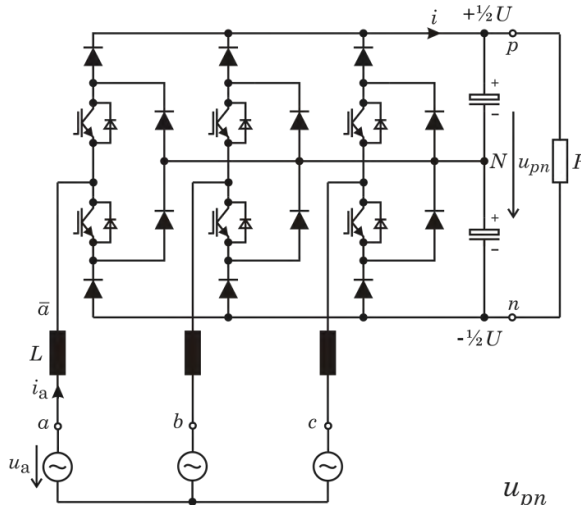
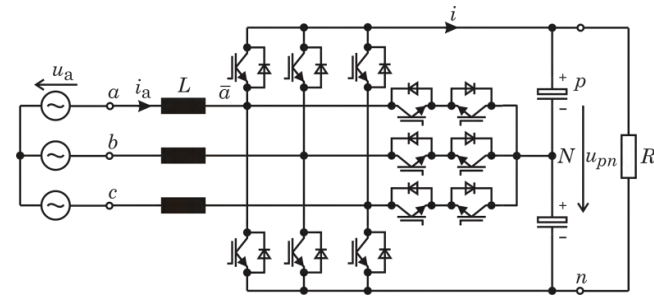
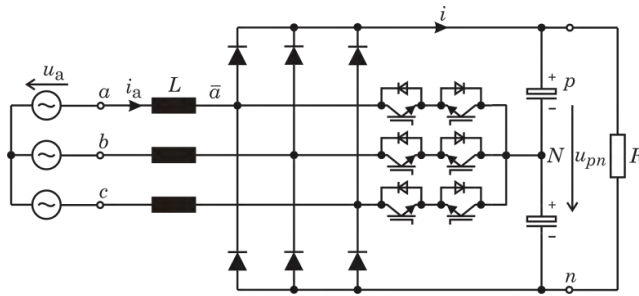


► Derivation of Two-Level Boost-Type Topologies

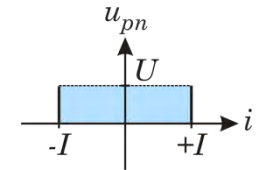
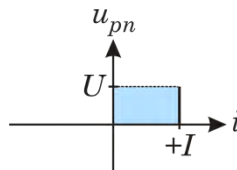
- Output Operating Range



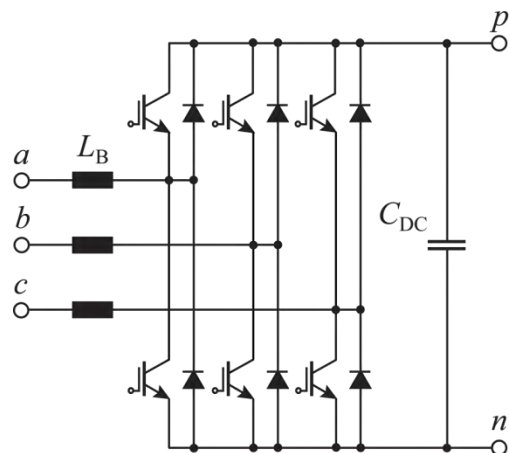
► Derivation of Three-Level Boost-Type Topologies



- Output Operating Range

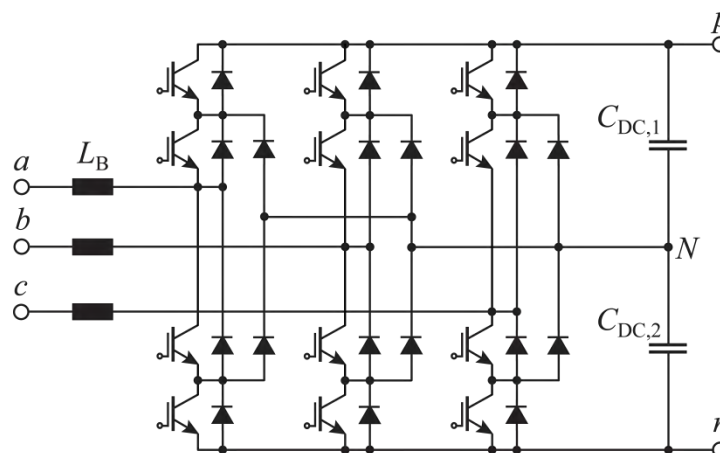


► Comparison of Two-Level/Three-Level NPC Boost-Type Rectifier Systems



• Two-Level Converter Systems

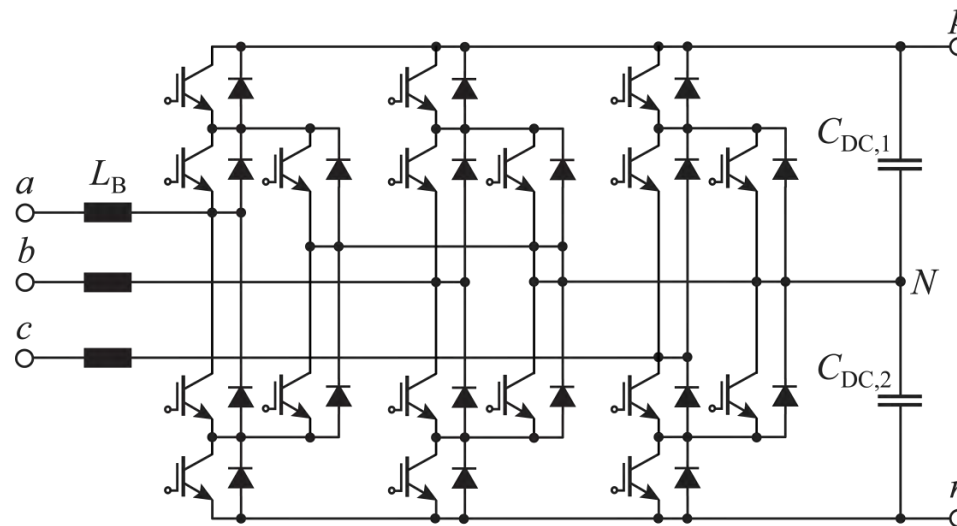
- + State-of-the-Art Topology for LV Appl.
- + Simple, Robust, and Well-Known
- + Power Modules and Auxiliary Components Available from Several Manufacturers
- Limited Maximum Switching Frequency
- Large Volume of Input Inductors



• Two-Level → Three-Level Converter Systems

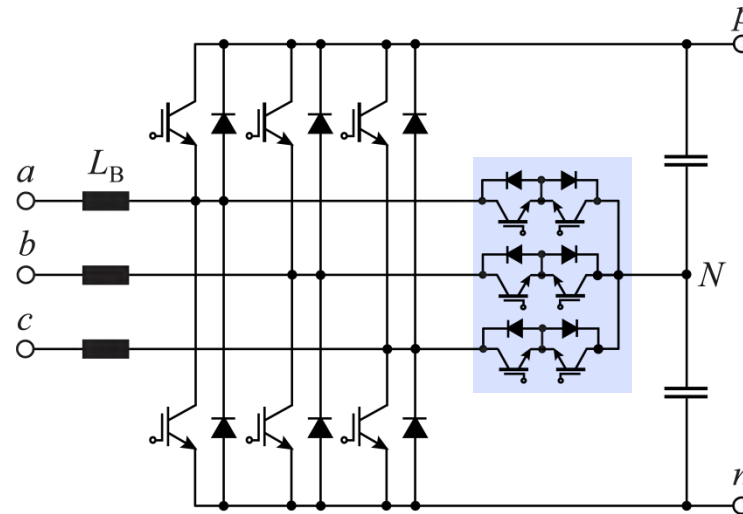
- + Reduction of Device Blocking Voltage Stress
- + Lower Switching Losses
- + Reduction of Passive Component Volume
- Higher Conduction Losses
- Increased Complexity and Implementation Effort

► Active Neutral Point Clamped (ANPC) Three-Level Boost-Type System



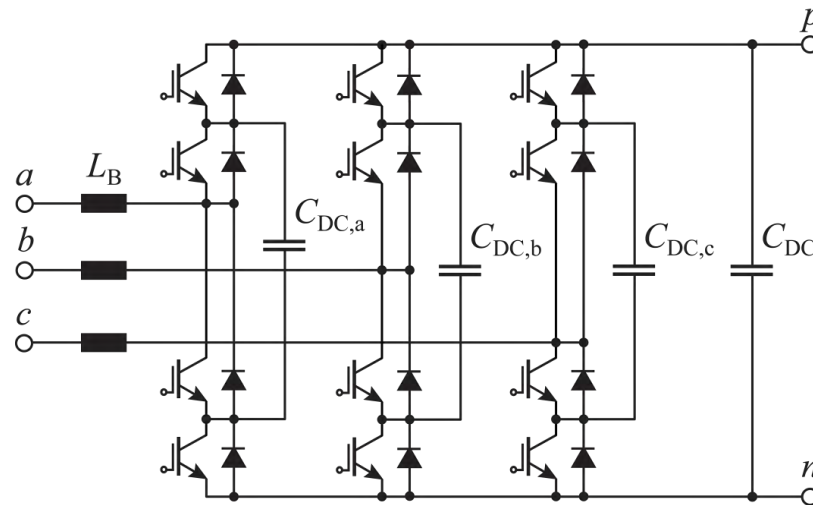
- + Active Distribution of the Switching Losses Possible
- + Better Utilization of the Installed Switching Power Devices
- Higher Implementation Effort Compared to NPC Topology

► T-Type Three-Level Boost-Type Rectifier System



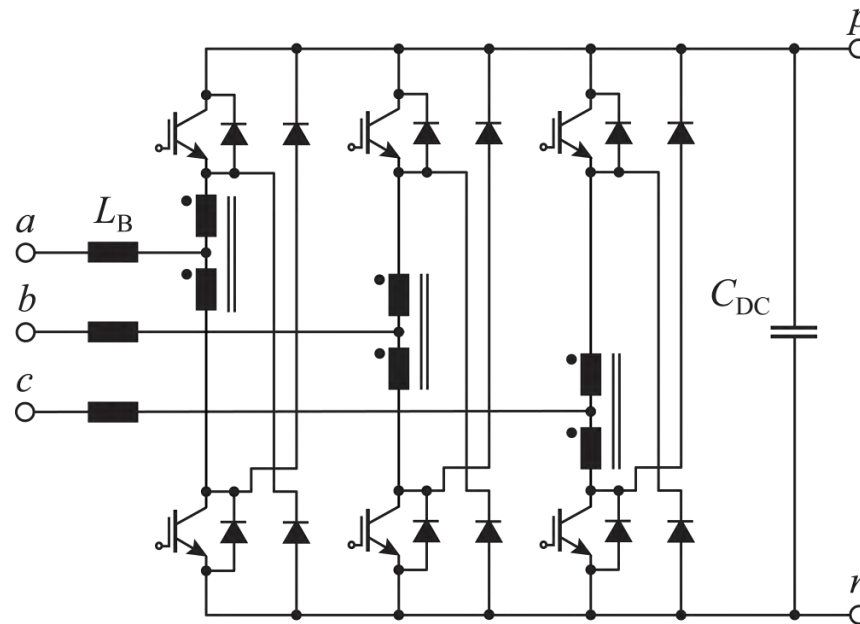
- + Semiconductor Losses for Low Switching Frequencies
Lower than for NPC Topologies
- + Can be Implemented with Standard Six-Pack Module
- Requires Switches for 2 Different Blocking Voltage Levels

► Three-Level Flying Capacitor (FC) Boost-Type Rectifier System



- + Lower Number of Components (per Voltage Level)
- + For Three-Level Topology only Two Output Terminals
- Volume of Flying Capacitors
- No Standard Industrial Topology

► Three-Level Bridge-Leg Inductor (BLI) Boost-Type Rectifier System



- + Lower Number of Components (per Voltage Level)
- + For Three-Level Topology only Two Output Terminals
- Additional Volume due to Coupled Inductors
- Semiconductor Blocking Voltage Equal to DC Link Voltage

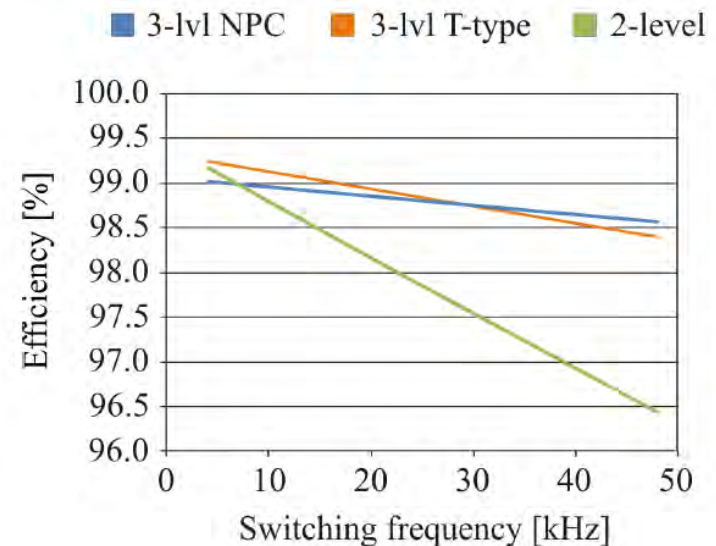
► Pros and Cons of Three-Level vs. Two-Level Boost-Type Rectifier Systems

- + Losses are Distributed over Many Semicond. Devices; More Even Loading of the Chips → Potential for Chip Area Optimization for Pure Rectifier Operation
- + High Efficiency at High Switching Frequency
- + Lower Volume of Passive Components

- More Semiconductors
- More Gate Drive Units
- Increased Complexity
- Capacitor Voltage Balancing Required
- Increased Cost

- Moderate Increase of the Component Count with the T-Type Topology

► Multi-Level Topologies are Commonly Used for Medium Voltage Applications but Gain Steadily in Importance also for Low-Voltage Renewable Energy Applications

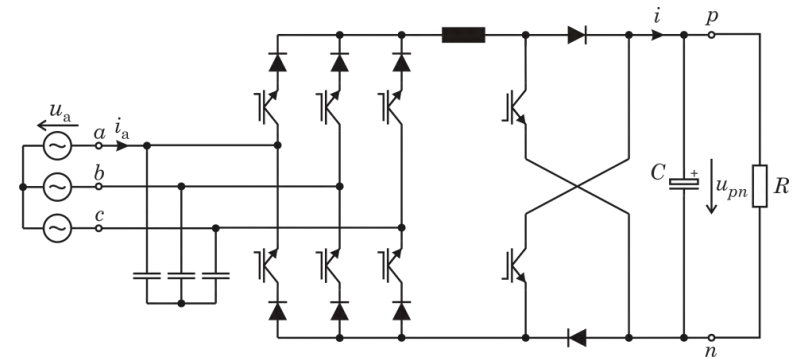
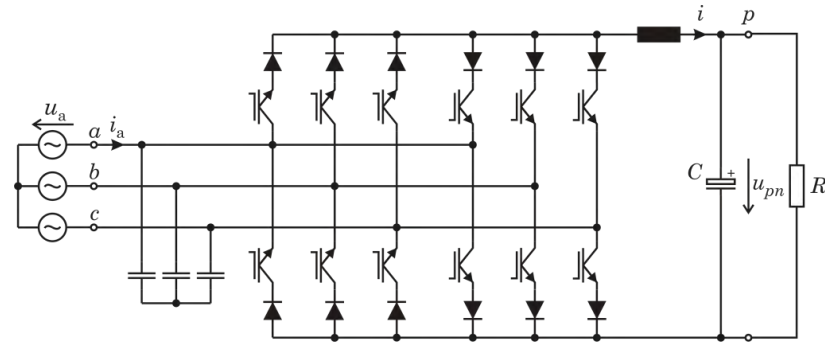
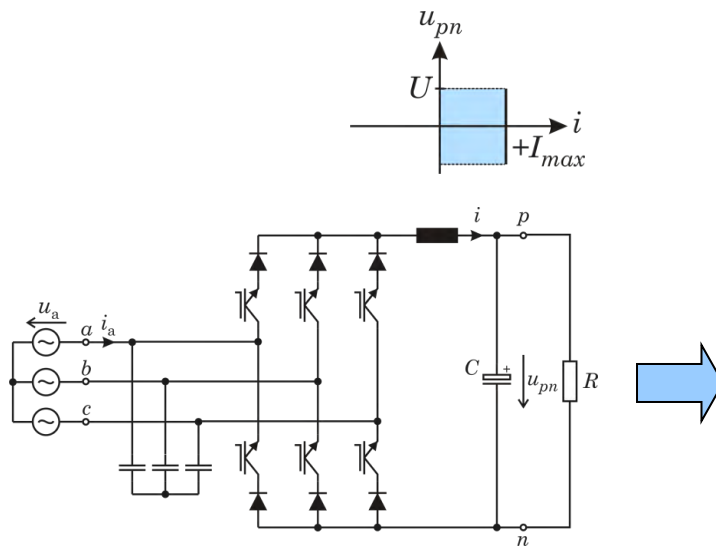
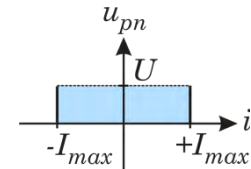


Consideration for 10kVA/400V_{AC} Rectifier Operation; Min. Chip Area, $T_{j,max} = 125^{\circ}\text{C}$

Buck-Type Topologies

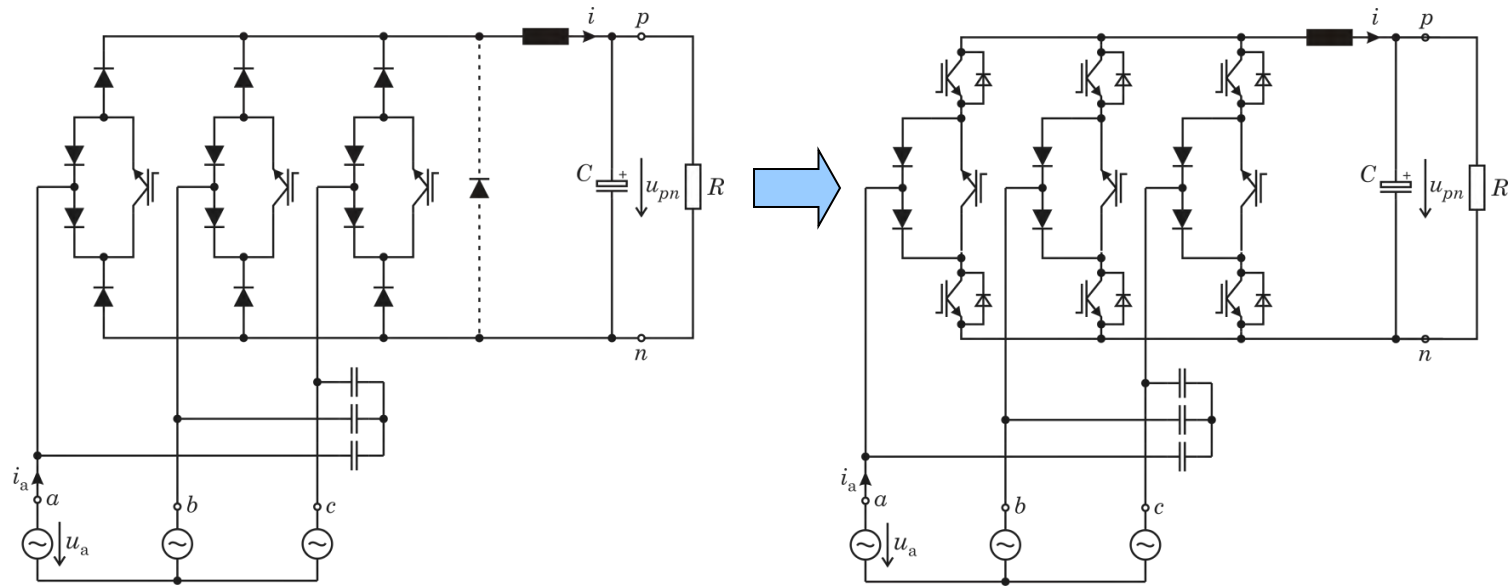
► Derivation of Unipolar Output Bidirectional Buck-Type Topologies

- Output Operating Range

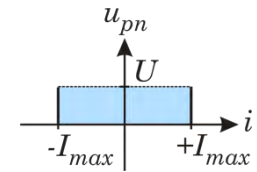
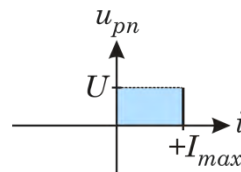


- System also Features Boost-Type Operation

► Derivation of Unipolar Output Bidirectional Buck-Type Topologies



- Output Operating Range



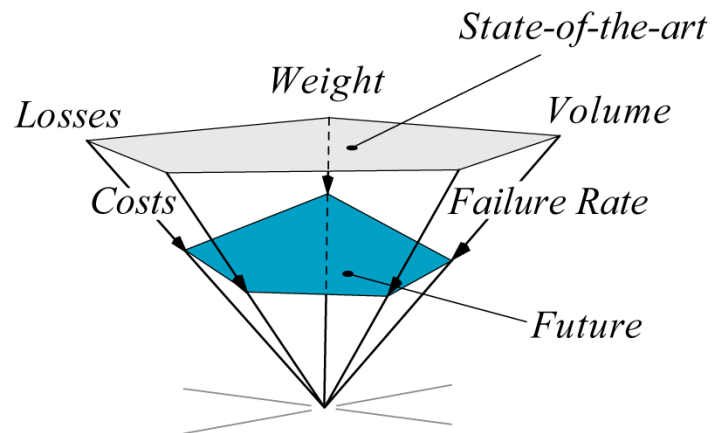
Final Remarks

Performance Trends
Multi-Objective Optimization

Power Electronics Performance Trends

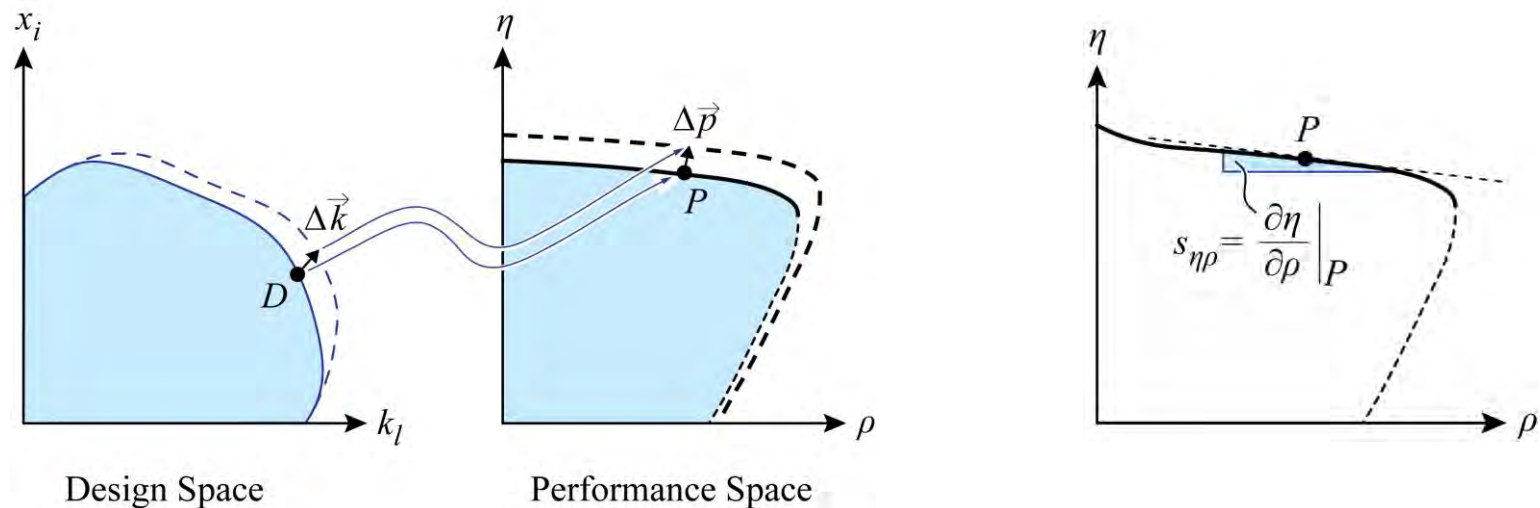
■ Performance Indices

- Power Density [kW/dm³]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/\$]
- Relative Losses [%]
- Failure Rate [h⁻¹]



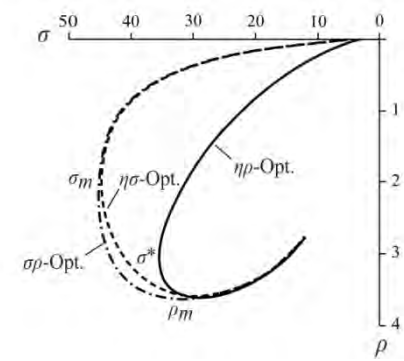
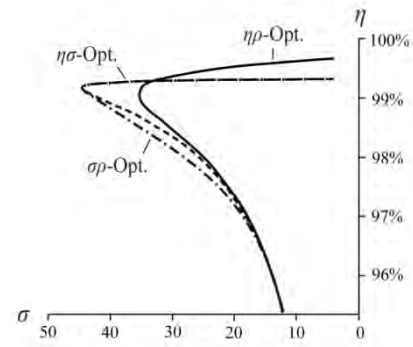
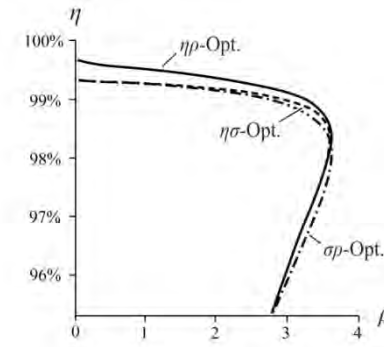
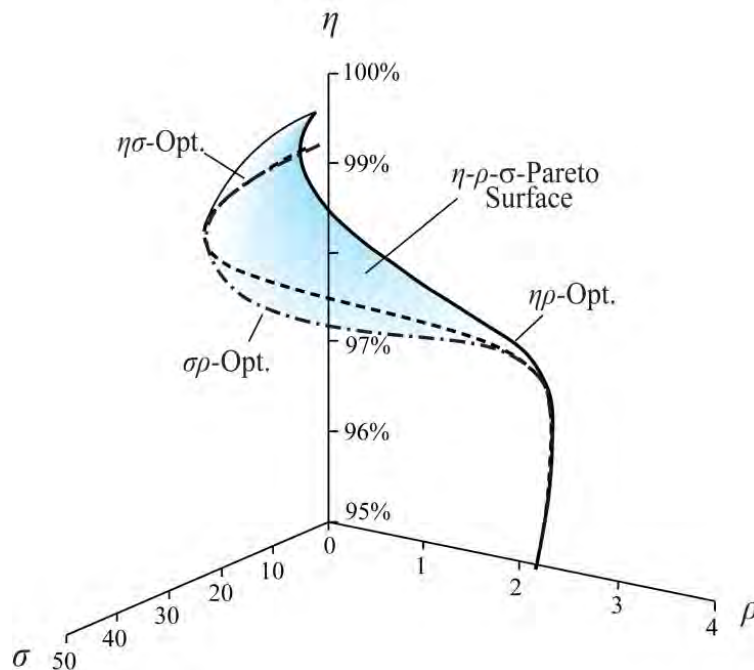
Technology Sensitivity Analysis Based on η - ρ -Pareto Front

- ▶ Sensitivity to Technology Advancements
- ▶ Trade-off Analysis



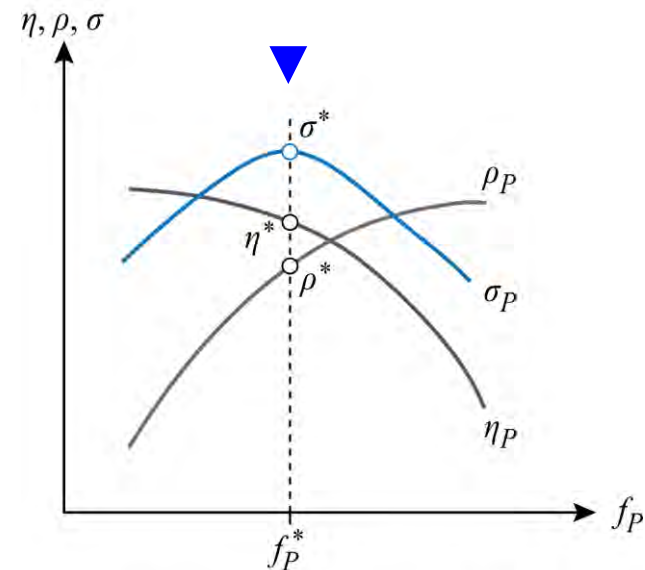
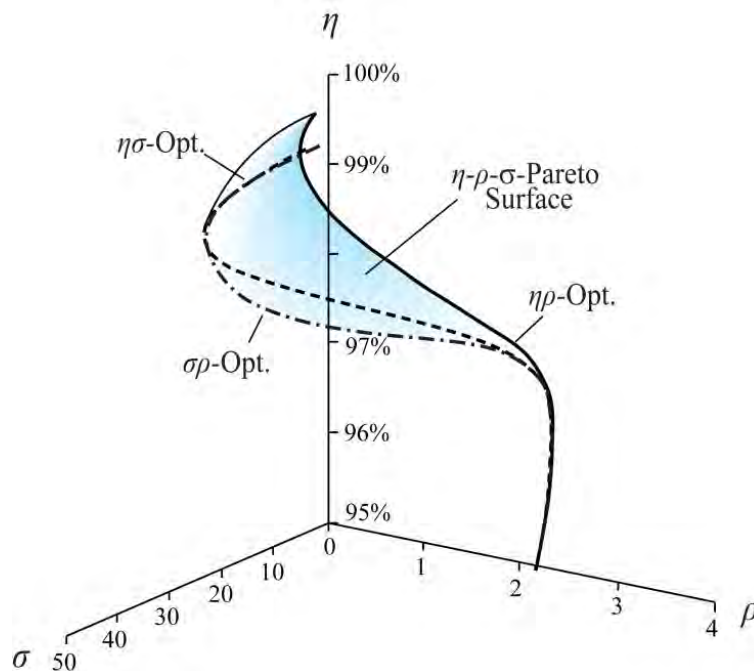
Converter Performance Evaluation Based on η - ρ - σ -Pareto Surface

► σ : kW/\$



Converter Performance Evaluation Based on η - ρ - σ -Pareto Surface

► 'Technology Node'



Technology Node: $(\sigma^*, \eta^*, \rho^*, f_P^*)$

Thank You!

Questions ?



Passive Rectifier Systems

- [1.1] **P. Pejovic**, "A Novel Low-Harmonic Three-Phase Rectifier," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol.49, no.7, pp.955-965, Jul 2002.
- [1.2] **P. Pejovic, P. Bozovic, D. Shmilovitz**, "Low-Harmonic, Three-Phase Rectifier That Applies Current Injection and a Passive Resistance Emulator," IEEE Power Electronics Letters, vol.3, no.3, pp. 96- 100, Sept. 2005.
- [1.3] **P. Pejovic, Z. Janda**, "Optimal Current Programming in Three-Phase High-Power-Factor Rectifier Based on Two Boost Converters," IEEE Transactions on Power Electronics, vol.13, no.6, pp.1152-1163, Nov 1998.
- [1.4] **S. Kim, P. Enjeti, P. Packebush, and I. Pitel**, "A New Approach to Improve Power Factor and Reduce Harmonics in a Three Phase Diode Rectifier Type Utility Interface," Record of the IEEE Industry Applications Society Annual Meeting, Pt. II, pp. 993-1000, 1993.
- [1.5] **P. Pejovic Z. Janda**, "Low Harmonic Three-Phase Rectifiers Applying Current Injection," Proc. of the Internat. Conf. on Power Electronics and Motion Control, Prague, 1998.
- [1.6] **P. Pejovic and Z. Janda**, "A Novel Harmonic-Free Three-Phase Diode Bridge Rectifier Applying Current Injection," Proc. of the 14th IEEE Appl. Power Electron. Conf. APEC'99, Dallas, USA, March 14-18, Vol. 1, pp. 241-247, 1999.
- [1.7] **P. Pejovic, and Z. Janda**, "An Improved Current Injection Network for Three-Phase High-Power-Factor Rectifiers that Apply Third Harmonic Current Injection," Letter to the Editor, IEEE Transactions on Industrial Electronics, Vol. 47, No. 2, pp. 497-499, 2000.
- [1.8] **T. Sakkos and V. Sarv**, "New Unity Power Factor Diode Rectifiers Using Ripple-Power Re-Rectification," in. Proc. of the 8th Internat. Conf. on Power Electron. and Variable Speed Drives, London, Sept. 18-19, pp. 378-381, 2000.
- [1.9] **T. Sakkos, V. Sarv, and J. Soojärvi**, "Optimum Diode-Switched Active Filters for Power Factor Correction of Single- and Three- Phase Diode Rectifiers with Capacitive Smoothing," in Proc. of the 7th European Conf. on Power Electron. and Appl., Trondheim, Norway, Vol. 2, pp. 870-875, 1997.

Hybrid Rectifier Systems (Electronic Reactance Based)

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About the Instructors



Johann W. Kolar (F' 10) received his M.Sc. and Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria. Since 1984 he has been working as an independent international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel converter topologies and modulation/control concepts, e.g., the VIENNA Rectifier, the Swiss Rectifier, and the three-phase AC-AC Sparse Matrix Converter. Dr. Kolar has published over 450 scientific papers in international journals and conference proceedings and has filed more than 85 patents. He was appointed Professor and Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich on Feb. 1, 2001.

The focus of his current research is on AC-AC and AC-DC converter topologies with low effects on the mains, e.g. for data centers, More-Electric-Aircraft and distributed renewable energy systems, and on Solid-State Transformers for Smart Microgrid Systems. Further main research areas are the realization of ultra-compact and ultra-efficient converter modules employing latest power semiconductor technology (SiC and GaN), micro power electronics and/or Power Supplies on Chip, multi-domain/scale modeling/simulation and multi-objective optimization, physical model-based lifetime prediction, pulsed power, and ultra-high speed and bearingless motors. He has been appointed an IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2011.

He received the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005, the Best Paper Award of the ICPE in 2007, the 1st Prize Paper Award of the IEEE IAS IPCC in 2008, the IEEE IECON Best Paper Award of the IES PETC in 2009, the IEEE PELS Transaction Prize Paper Award 2009, the Best Paper Award of the IEEE/ASME Transactions on Mechatronics 2010, the IEEE PELS Transactions Prize Paper Award 2010, the Best Paper 1st Prize Award at the IEEE ECCE Asia 2011, and the 1st Place IEEE IAS Society Prize Paper Award 2011 and the IEEE IAS EMC Paper Award 2012. Furthermore, he received the ETH Zurich Golden Owl Award 2011 for Excellence in Teaching. He also received an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003.

He initiated and/or is the founder/co-founder of 4 spin-off companies targeting ultra-high speed drives, multi-domain/level simulation, ultra-compact/efficient converter systems and pulsed power/electronic energy processing. In 2006, the European Power Supplies Manufacturers Association (EPSMA) awarded the Power Electronics Systems Laboratory of ETH Zurich as the leading academic research institution in Power Electronics in Europe.

Dr. Kolar is a Fellow of the IEEE and a Member of the IEEEJ and of International Steering Committees and Technical Program Committees of numerous international conferences in the field (e.g. Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). He is the founding Chairman of the IEEE PELS Austria and Switzerland Chapter and Chairman of the Education Chapter of the EPE Association. From 1997 through 2000 he has been serving as an Associate Editor of the IEEE Transactions on Industrial Electronics and since 2001 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEEJ Transactions on Electrical and Electronic Engineering.

About the Instructors (Cont'd)



Jonas Mühlethaler (M'09) received his M.Sc. in 2008 and the Ph.D. degree in 2012, both in electrical engineering and both from the Swiss Federal Institute of Technology Zurich (ETHZ), Switzerland. During his master studies, he focused on power electronics and electrical machines. In his M.Sc. thesis, which he wrote at ABB Corporate Research in Sweden, he worked on compensating torque pulsation in Permanent Magnet Motors. In 2008 he joined the Power Electronic Systems Laboratory (PES), ETHZ, to work towards his Ph.D. degree. During the Ph.D. studies, which he finished in 2012, he worked on modeling and multi-objective optimization of inductive power components. Currently, he is working as a Postdoctoral Fellow at PES. Dr. Mühlethaler is the author of 13 conference and Transactions papers and a Member of the IEEE.