Chapter 5
Modelling for the Lifetime Prediction of Power Semiconductor Modules

Ivana F. Kovačević-Badstuebner*, Johann W. Kolar*, and Uwe Schilling**

Reliability engineering has emerged as a relatively new branch of Power Electronics (PE) supporting the fast progress towards advanced Power Electronic Converter Systems (PECS) with significantly improved reliability ratings. PECS operate under increasingly severe temperature profiles, i.e., fast temperature cycling between extreme temperature levels. Accordingly, the reliability requirements for power semiconductor modules as fundamental components of PECS are significantly increased. Power module manufacturers have been working on new power module designs and packaging technologies in order to increase endurance and prolong the lifetime of power modules in the future, and subsequently enable high performance of the PECS also concerning reliability [1]. In the future, the reliability aspects have to be included into novel multi-domain optimization tools that will further improve the design of PECS. The first step towards this goal is to allow the integration of lifetime models of the system components into the design process.

The reliability of power modules represents a highly interdisciplinary topic as it requires a deeper knowledge in different areas: 1) mechanical design and thermal capabilities of power modules, 2) physics of failure explained by material science, and 3) power electronics as its application field. The prediction techniques and sophisticated models for lifetime estimation of power modules have been studied and received more and more attention. Major investigations have been carried out by the manufacturers of power modules as they possess detailed product data, the expertise and resources necessary for developing and verifying lifetime models of power modules. Most of these models are empirical lifetime models used for the characterization of power cycling capabilities of power modules, e.g., the lifetime models presented in [2, 3]. They are practically based only on experience and statistical analysis of the large databases gained in long-running accelerated cycling tests. The existing

*Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, 8092 Zurich, Switzerland

**SEMIKRON Elektronik GmbH & Co. KG, Sigmundstrasse 200, 90431 Nuernberg, Germany

empirical models are often used in practice by PE engineers as the only means for an End-of-Life (EOL) estimation of power modules and, further then for the prediction of PECS reliability under specified mission profiles. However, these lifetime models must be carefully applied, as normally, an extrapolation is conducted when applying the models gained from accelerated testing to field conditions. The validity of this extrapolation is sometimes doubtful.

Accelerated power and temperature cycling tests are used to emulate the actual operation conditions in the field with the aim to collect relevant data for building the lifetime models of power modules. A lifetime model can be defined as a tool for the EOL estimation of a power module exposed to cyclic thermal loading. By carefully controlling test conditions, it can be assumed that failures are only due to wear-out effects. Interconnection failures are reported to be the most common causes of failure of power modules operated in these cycling tests. Usually, the critical parts of standard power modules in power and/or temperature cycling experiments are three interconnections: wire bonds, the chip solder joint, and the substrate-baseplate solder layer. In the study presented in [4], it was shown that the bond wire lift-off failure mode and solder fatigue have different physical behaviour and thus, have to be separately analysed and treated differently. In the sense of the empirical lifetime modelling approach, this requires developing a specific model for each failure mode separately. This, in turn, implies performing the separation of failure modes in the first place and then an extensive number of power cycling experiments that typically take considerable time.

The main drawback of the empirical models is that they are purely statistical and do not directly describe and assess the deformation mechanisms of power modules invoked under complex thermal loadings. Therefore, with new concepts of power module packages, and ever-increasing lifetime expectations for power semiconductor devices operating under very challenging environmental conditions, many research groups have started investigating physics-based lifetime models [5–9]. The physical modelling of failure includes the analysis and modelling of actual failure mechanisms, i.e., the stress and strain development under thermal loading. The calibration of physics-based lifetime models typically requires only several power cycling tests. The physics-based lifetime models provide a better insight in the physical process leading to a failure, and furthermore, they can be integrated in multi-domain modelling tools for the virtual design of PECS. In addition, they can contribute to the validation of the extrapolation of existing empirical models. As a result, the Physics-of-Failure (PoF) approach has emerged as a new methodology in power electronics that can potentially improve the lifetime estimation and enable the reliability engineering to be integrated into the development and research cycles of the overall design process of PECS. However, today, physics-based lifetime modelling is still missing in common engineering practice with respect to the design for reliability in PE.

This chapter reviews the basic ideas and difficulties with the physics-based lifetime modelling of power semiconductor modules, demonstrating the capa-

bilities of a developed physics-based lifetime model for solder interconnections. The chapter is organized as follows. In Section 5.1, accelerated power and temperature cycling tests are briefly described. The power (active) and temperature (passive) cycling tests are used by manufacturers to verify the required functionality of the power module during the total field lifetime. Power cycling tests are important for the lifetime calculation of power modules operating in the actual applications. Section 5.2 presents the standard power module package and its intrinsic failure modes. The main focus is put on the most-stressed parts of the power module assembly that define the dominant failure mechanisms occurring during the power cycling experiments. An overview of existing empirical and physics-based lifetime models for power modules is given in Section 5.3. These lifetime models represent the state-of-the-art of the lifetime modelling of power modules. The necessary steps for further investigations and improvements are presented, which should improve the design for reliability of PECS. In Section 5.4, the theoretical background of the physics-based lifetime modelling of solder joints is given. Subsequently, in Section 5.5, a proposed physics-based lifetime model for the power module's solder joints is introduced. Finally, the theoretical considerations are verified based on a set of power cycling test data provided by SEMIKRON Elektronik GmbH & Co. KG [10].

5.1 Accelerated cycling tests

PECS, like those used in cars, locomotives, and airplanes, require long-ranging lifetime guarantees of five up to 30 years [11]. Collecting the system information for the reliability assessment under real application conditions even over a mid-term period of several years is not feasible since the technology changes very fast and the manufacturers of power modules must provide certain warranties for new products. Therefore, accelerated Power Cycling (PC) and Temperature Cycling (TC) tests are performed and well established among the manufacturers of power modules as the means for a lifetime estimation of products. PC and TC tests are designed to accelerate the failure modes occurring in the real applications due to thermo-mechanically induced wear-out. The IEC International Standards for semiconductor devices such as IEC 60747-34 and IEC 60747-9 [12, 13] define endurance and reliability test setups; however, the exact procedures for PC and TC tests, e.g., setting the level of load current and the heating-cooling times, are mostly product-oriented, and, hence, defined independently by manufacturers [14].

TC tests are performed using temperature-controlled chambers to evaluate the influence of ambient temperature variations on power modules and are mainly aimed at the lifetime testing of large area solder interconnections such as the solder joint between the baseplate and substrate of the power module [15]. In the PC tests, a power module is actively heated by switching on and off the current, resulting in defined heating and cooling phases. Accordingly, the semiconductor chip represents the source of heat dissipation and, hence,

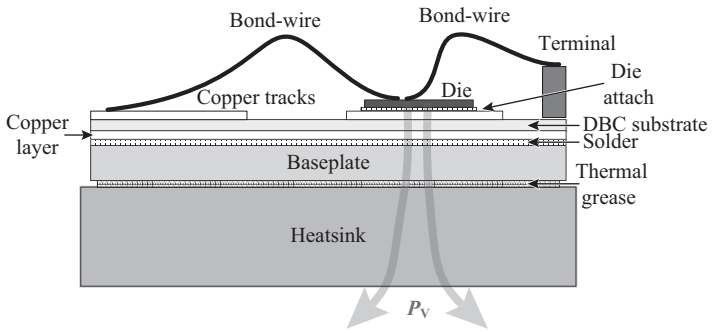

Figure 5.1: Multi-layer structure of a standard power module design.

the interconnections in close vicinity to the chip, i.e., bond wires and chip solder, are more stressed and likely to fail. PC tests are commonly used by manufacturers to trigger wear-out mechanisms of power modules in use in a shorter time period and gain useful data for the lifetime modelling.

5.2 Dominant failure mechanisms

Power modules represent main functional elements of power electronic converters and typically contain several semiconductor devices, e.g. MOSFETs, IGBTs, and diodes. The package of power modules has a very important function as an interface between the semiconductor devices and the circuit application.

Standard power modules are designed in a multi-layer structure, as shown in Fig. 5.1. The heat dissipated inside a power semiconductor chip, illustrated by the power flow P_V in Fig. 5.1, is conducted through the multi-layer structure into a heatsink, and is then transferred by convection to the ambient. The chip (silicon layer) is soldered to a Direct-Bonded-Copper (DBC) ceramic substrate and then, at the bottom side, the substrate is soldered to a metal baseplate. The baseplate and heatsink are interfaced via a layer of thermal grease to achieve a better thermal contact. The layers silicon(Si)-copper(Cu)-ceramic(AlN, Al_2O_3), characterized by different thermal properties, have great influence on the heating and cooling rates of the module and determine its overall thermal performance. The thermo-mechanical stress appearing within a power module can be directly related to the temperature gradients formed across the layers and the difference between their thermal properties, such as the Coefficients of Thermal Expansion (CTE). Consequently, fatigue failures of power modules are directly related to the power modules assembly structure and packaging technology.

There are different failure mechanisms of power modules, such as bond wire fatigue, reconstruction of chip metallization, solder fatigue, fatigue crack propagation within the ceramic substrate, corrosion of aluminium bond wires,

and burn-out failures, which can occur within the power module when it operates in the field and fatally affect its functionality [16]. Particularly, the failures can be a result of wear-out, a poorly designed and optimized manufacturing process, some external sources, e.g., comsic rays, a usage out of specifications, etc. The reliability of a power module can be then defined as a probability that the power module performs its required function for a specified time interval under certain operating conditions. Typically, the failure rate over time is described by the so-called bathtub-curve, consisting of early-life failures, random failures, and EOL failures. Lifetime models, e.g., described in [2, 3, 17], serve to describe EOL failures due to wear-out, i.e., aging of material. They are used to gain a better understanding of the useful functional period of a component operating in the field. Moreover, lifetime models play an important role in the thermal and electrical design of a PECS as they describe the power and temperature cycling capabilities of power modules, the influence of the cycling parameters on the number of cycles to failure, N_f, which in turn determines the EOL of the power module under the assumed conditions. Accordingly, the lifetime modelling represents a valuable step for a general reliability analysis of power modules.

The root cause of wear-out is the thermo-mechanical stress that is invoked in the materials of the layers of the power module structure operating under intrinsic cyclic temperature profiles. It was shown that during accelerated power/temperature cycling tests, the inner interconnections of the power module, such as bond wires, the chip solder layer, and the substrate-baseplate solder joint (see Fig. 5.1), determine the lifetime of the whole assembly. In practice it is hard to distinguish the dominant failure mode as there is a close interaction between different failure mechanisms. For example, solder fatigue results in a higher thermal resistance of the power module $R_{\mathrm{th(j-s)}}$ ($= \Delta T_{\mathrm{j-s}}/P_\mathrm{V}$, where $\Delta T_{\mathrm{j-s}}$ is the temperature difference measured between the chip and the heatsink), that leads to higher junction temperatures T_j and thus, to higher stress levels at the place of the bond wires, which results eventually in a lift-off of bond wires. Similarly, bond wire lift-off causes uneven current distribution that produces higher power losses and/or higher T_j and, hence, more thermal stress at the solder interconnections.

Carefully specified accelerated cycling tests are performed to decouple different failure modes, and failure criteria must be defined in order to acquire useful data for the generation of lifetime models. Typically, the bond-wire lift-off failure mechanism is detected by an increase of the forward voltage drop of 5 % to 20 %. An indicator of solder fatigue is an increase of 20 % to 50 % of the thermal resistance, $R_{\mathrm{th(j-s)}}$, of the power module measured between the chip and the heatsink, which is caused by crack propagation within the solder interconnecting layer [14, 18].

Driven by the automotive industry and improvements in traction systems, the main requirement for new generations of power modules is to allow an operation at higher temperature levels, e.g. above 150 °C. The reliability of power module's interconnections is a factor that limits the increase of the

allowed junction (chip) temperature. Accordingly, the idea for novel design concepts of power modules has been to eliminate and/or reinforce the most-stressed interconnections, i.e., wire bonds and solder interconnecting layers. The first solder-free IGBT power module, the SEMIKRON SKiM module, became commercially available in 2008 and has demonstrated significantly enhanced power cycling capability, as reported in [19]. In this novel power module concept, the baseplate is removed and the DBC substrate is pressed onto the heatsink, i.e., pressure is induced by a pressure part on top which is screwed to the heatsink. Additionally, a silver sintering technology is applied for die-attach, and spring contacts are used instead of soldering for the interconnections between the substrate and the terminals for the load current, the gate control circuit, and auxiliary contacts such as the auxiliary emitter and temperature sensor. The main advantage of this novel concept is the capability to operate at much higher temperatures due to the significantly higher melting temperature of the silver sinter layer in comparison to the melting temperature of solder alloys.

5.3 Lifetime modelling

The power modules of PECS are rated for high switching current and blocking voltage levels. The power losses generated under the field/test operation conditions lead to high temperature variations, which in turn produce thermo-mechanical stresses within the power modules that gradually degrade their functionality and lead to wear-out. As the first step of the lifetime modelling, the power losses of the PECS must be calculated for a characteristic load profile by means of electrical circuit simulations and translated via thermal modelling into corresponding temperature profiles, to which the power module's layers are exposed. Specifically, thermal modelling and simulation is performed to gain knowledge and information of the temperature distribution within the power module's structure, since the direct temperature measurements of the power module's layers are practically not possible. As the electrical properties of switching devices, i.e., power modules, are temperature-dependent, the thermo-electric modelling might be necessary for the accurate determination of the actual temperature behaviour. Accordingly, thermal (and/or thermo-electric) modelling can be seen as a constitutive part of the lifetime prediction approach.

The main principle of the lifetime modelling is based on the correlation of the number of cycles to failure, N_{f}, directly gained in the PC and/or TC tests to the corresponding temperature profiles. This further allows a quantitative evaluation of the response of the power module to the temperature changes in the application field. Lifetime modelling of power modules therefore strongly depends on the cycling test results. Two lifetime modelling approaches can be distinguished: empirical lifetime models and physics-based lifetime models.

This section presents the main steps of the lifetime modelling procedure for power semiconductor modules. First, the principles of thermal modelling

of power modules are described, and then, the existing empirical and physics-based lifetime models are briefly summarized, pointing out the main differences of the physics-based modelling approach in comparison to the well-established empirical lifetime models.

5.3.1 Thermal modelling

Thermal problems in power electronics can be solved in a simplified way by means of one-dimensional thermal networks, defined by the so-called Cauer and Foster models [20]. These thermal networks are built of thermal circuit elements, i.e., thermal resistances R_{th} and thermal capacitances C_{th}. Similar to an electric circuit, C_{th} are included to model the transient response, while only R_{th} can be used to model the steady-state thermal behaviour. The Cauer model has a physical interpretation as the internal nodes of the Cauer network can be directly associated with the layers of the power module, which is not the case for the Foster model. In the Foster model, only the input node with respect to the power source corresponds to an actual physical point of the power module. Both thermal models return the same transient behaviour of this input node, i.e., the same overall thermal system impedance, Z_{th}. In particular, the same thermal behaviour is obtained for different sets of R_{th} and C_{th}, which define the Cauer model and the Foster model respectively. The main advantage of the Foster model is that it provides a straightforward analytical expression for Z_{th}, which can be used to numerically calculate the thermal response of the overall power module structure to an application given mission profile. Under the real operation conditions, the power module's layers experience different temperature distributions, both in the lateral and vertical directions. The layers below the chip typically exhibit a similar temperature pattern as the chip (silicon), and their maximum temperature is lower than the maximum temperature of the chip. Having non-constant temperature over the surface area, the main question that arises with the physics-based lifetime modelling is which temperature value should be applied in the corresponding lifetime models, i.e., the average, the maximum, or the minimum temperature. In particular, when modelling the thermo-mechanical stress inside a power module's interconnecting layer, its lateral temperature gradients have to be taken into account. Accordingly, three-dimensional (3D) thermal solvers allowing finer discretization of the power module's structure have to be employed. This allows a more comprehensive and detailed calculation of the temperature evolution, which is required for the physics-based lifetime modelling.

Thermal solvers are typically based on a Finite Difference Method (FDM), and they use a 3D network of equivalent thermal resistances, R_{th}, and capacitances, C_{th}, for the modelling of the power flow inside the power module package. 3D thermal modelling provides both lateral and vertical temperature gradients of the power module's layers. This lateral and vertical temperature distribution is used for a comprehensive thermal characterization of the power

module package. On the other hand, thermal characterization based on measurements provides only the so-called virtual junction (chip) temperature T_{vj}, since the inner points of the power module's structure are not accessible for direct temperature measurements without alterations of the structure. Accordingly, thermal modelling represents a necessary step for a valid lifetime estimation process, which specifically provides information about the temperature distribution in the observed solder layer for lifetime modelling of the solder intersections.

What distinguishes power modules from other physical systems is the ability to accommodate very fast temperature changes. The fast temperature transients make the temperature measurements non-trivial and thus standard thermocouples cannot be applied. The virtual junction temperature, T_{vj}, is therefore typically derived from measurements of the temperature-dependent electrical parameters of the power semiconductor devices, e.g., the on-state saturation voltage $V_{\mathrm{ce}}(T)$ between the collector and emitter contacts at low (sense) current levels. In [21], the physical meaning of this single temperature value T_{vj} is related to the temperature distribution across the active surface of the chip. Specifically, it was shown that T_{vj} corresponds to the area-weighted average temperature over the active chip area.

5.3.2 Empirical lifetime models

Empirical models are deduced from experience and large databases of PC test results collected over many years for different module technologies; they express lifetime in terms of the number of cycles to failure, N_{f}. Specifically, empirical models describe the N_{f}-dependence on the parameters of PC tests, such as maximum, mean, or minimum temperature, cycle frequency, heating and cooling times, load current, and furthermore the power module's properties such as blocking voltage class, and the geometry of bond wires. PC tests are conducted to investigate the influence of PC test parameters on the N_{f}-results. It was observed that the dominant failure mechanisms under PC experiments are the failures of bond wires and solder interconnecting layers, i.e., the EOL of power modules is typically limited by the lifetime of these interconnections.

The first well-established empirical model, which resulted from the so-called LESIT project [2], did not distinguish between different failure mechanisms, i.e., a single analytical model was used to describe the N_{f}-lifetime of power modules. The main reason was the difficulty to set the PC experimental conditions to control dominant failure modes in order to make the database of PC N_{f}-results correspond to a single failure mechanism, i.e., either wire-bond lift-off or solder failure. These two failure mechanisms cannot be explained by the same dependencies on PC test parameters, as the natures of these failures are different. This implies that a separation of failure modes has to be performed in the first place, and then two analytical models have to be derived from PC experiments. Advanced interconnection technologies

that became available in last couple of years have allowed making a clear distinction between these two failure modes under PC test conditions [22], and hence, enable power module manufacturers to develop different empirical models for each failure mode, which was not possible for the early lifetime models.

Examples of empirical lifetime models

As power modules are exposed to periodic thermo-mechanical stress, the well-known Coffin-Manson law can be used to relate the number of cycles to failure, N_f, and the temperature change ΔT (= T_max - T_min) reached in the applied power cycles,

$$N_\mathrm{f} = a \cdot (\Delta T)^{-n}, \tag{5.1}$$

where the model constants a and n are the empirical parameters depending on the module design. The experience gained in PC experiments indicated that the other PC parameters besides ΔT also have a strong influence on the number of cycles to failure. In the 1990s, the LESIT project [2] was conducted for standard power modules with Al_2O_3 ceramic substrate and copper baseplate from different manufacturers. As a result, the influence of the average junction temperature, $T_\mathrm{j,m}$, was included into the Coffin-Manson N_f-model via the Arrhenius approach as

$$N_\mathrm{f} = a \cdot (\Delta T_\mathrm{j})^{-n} \cdot \mathrm{e}^{\frac{E_\mathrm{a}}{k_\mathrm{b} \cdot T_\mathrm{j,m}}}, \tag{5.2}$$

where ΔT_j is the peak-to-peak variation of the junction temperature cycle ($T_\mathrm{j,max}$ - $T_\mathrm{j,min}$), $T_\mathrm{j,m}$ is the mean temperature value $(T_\mathrm{j,max} + T_\mathrm{j,min})/2$, and k_b is the Boltzmann's constant; a, n, and E_a are the model parameters, which are determined by fitting (5.2) to the experimental PC data. E_a represents the activation energy that characterizes the deformation process. This analytical lifetime model corresponds to linear functions in a log-log, i.e. $\log(N_\mathrm{f})$ - $\log(\Delta T_\mathrm{j})$, plane for different average junction temperatures, $T_\mathrm{j,m}$.

As a next step, the N_f-lifetime dependency on the other PC parameters, such as the heating time and the power density, was examined.

ABB (Hamidi et al. [23]) conducted PC tests to characterize the influence of the heating time t_on on the thermal fatigue of High-Voltage (HV) IGBT power modules. Two dominant failure mechanisms were taken into account: bond wires lift-off and baseplate solder failure. It was shown that longer t_on has a severe impact on the lifetime of power modules and represents an important ageing accelerator.

INFINEON (Bayerer et al. [3]) proposed a lifetime model,

$$N_\mathrm{f} = K \cdot (\Delta T_\mathrm{j})^{\beta_1} \cdot e^{\frac{\beta_2}{T_\mathrm{j}+273}} \cdot t_\mathrm{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6}, \tag{5.3}$$

which includes, in addition to (5.2), the influence of the heating time t_on, the current per wire bond stitch I, the diameter of bond wires D, and the chip

voltage class V (defined by blocking voltage of chip) on the power-cycling capabilities. The impact of these parameters is assumed to have power law nature and, thus, the dependency of N_f on t_on, I, V, and D can be described by a linear log-log characteristic. This empirical lifetime model, referred to in the literature as CIPS2008 model, is based on a purely statistical analysis of a large number of PC test results from different module technologies. Additionally, the CIPS2008 lifetime model does not cover the lifetime limitation due to substrate-baseplate solder failures and it is not applicable for the power modules used in traction applications, as the assumed relation between the blocking voltage and chip thickness does not apply to modules for traction application [3]. The second limitation is that the model parameters cannot be set independently during the PC experiment, e.g., the heating time and a certain maximum temperature are correlated by the nature of power module and PC tests. The authors suggested therefore that the model should be carefully used and only in the range where the PC tests were performed.

Similarly, SEMIKRON (Scheuermann et al. [17]) has recently proposed a new lifetime model for the advanced power modules with sintered chips, e.g., SKiM modules. These modules exhibit significantly improved lifetime as the classical solder process for the die attach, is replaced by Ag diffusion sintering technology, and the Al wire bond geometry is optimized. In this way, the bond wire lift-off and heel cracking were the only observed failure modes, so that the developed lifetime model corresponds only to the failure mechanisms due to thermo-mechanical stress of bond wires. The proposed lifetime model also includes the impact of the aspect ratio of Al bond wire (ar) as significantly higher lifetime was observed by increasing the height of the bond wire loops,

$$N_\mathrm{f} = A \cdot (\Delta T_\mathrm{j})^{\alpha} \cdot ar^{\beta_1 \cdot \Delta T_\mathrm{j} + \beta_0} \cdot \left(\frac{C + t_\mathrm{on}^{\gamma}}{C+1}\right) \cdot e^{\frac{E_\mathrm{a}}{k_\mathrm{b} \cdot T_\mathrm{jm}}} \cdot f_\mathrm{Diode}, \tag{5.4}$$

where A is a general scaling factor, ΔT_j is the junction temperature swing given in Kelvin, t_on is the load puls duration, T_jm is the absolute medium junction temperature in Kelvin, k_b is the Boltzmann's constant, E_a is an activation energy in eV, and f_Diode is a de-rating factor applied for the test on free-wheeling diodes; β_0 are β_1 are the model coefficients determined together with the other model parameters A, α, C, γ, E_a, and f_Diode, using a least square fitting procedure. The parameterization of this analytical model was based on a set of 97 PC tests, gained in the experiments that took approximately five years. According to the authors, more PC tests are still required to gain better understanding of the influence of the model parameters on the lifetime. Furthermore, the Ag-diffusion sintered modules and the standard modules with baseplate were compared in [4,22] that allowed distinguishing and analysing dominant failure mechanisms under different PC test conditions. The comparison has shown that: (a) wire bond lifetime is less affected by the medium junction temperature than the lifetime of the chip solder, which is reflected by lower activation energy, E_a; (b) the chip solder degradation is dominant for high temperatures; and c) for an intermediate temperature range both failure mechanisms, i.e., solder failure and bond wire

lift-off occur and lead gradually to the module's EOL. This referenced study represents an approach for separating failure modes that allowed building empirical lifetime models for each failure mode alone, with the aim to develop more accurate lifetime prediction methods.

5.3.3 Physics-based lifetime models

Physical modelling requires failure and deformation mechanisms to be known so that the stress and strain development within the power module assembly is modelled and directly correlated to the number of cycles to failure. Physical modelling represents the basis for the Physics-of-Failure (PoF) analysis. PoF provides a deeper physical description of the observed failure mechanism, and hence, represents a promising alternative to empirical lifetime models.

Direct measurements of stress and strain in electronic packages demand the usage of high resolution measuring methods, e.g. infrared and scanning electron microscopy. The other way to determine the stress and strain deformations within a power module is by means of a stress-strain simulation via computational mechanics, e.g. Finite Element Analysis (FEA). However, the physics-based modelling by FEA requires detailed knowledge of the material and geometry properties of the power module assembly, which is often not available in the power module datasheets and only accessible by the manufacturers. An alternative to FEA for the stress-strain modelling is based on a numerical approach for calculating the stress-strain response under a given temperature profile and using a parameterization procedure based on the PC experimental data, as it is described in the following. The existing physics-based lifetime models of power modules published in the literature are briefly summarized in this section with the aim of highlighting the state-of-the-art for the PoF analysis in power electronics with regard to power modules as reliability-critical components of PECS.

Model 1 - ETHZ-PES lifetime model

One of the first physics-based models in power electronics [5, 24, 25], referred to as the ETHZ-PES lifetime model in this book, is dedicated to the planar solder joints within power semiconductor modules. It is based on a numerical algorithm for calculating the stress-strain evolution under a cyclic thermal load applied to the solder interconnecting layer and the thermo-mechanical model described in [26]. The applied numerical algorithm was originally developed for the solder joints of Surface Mount Devices (SMD). The basic idea is that the solder response to a cyclic thermal load can be described by means of a hysteresis loop [27]. The number of cycles to failure N_f can be then calculated by Morrow's type of fatigue law as,

$$N_\mathrm{f} = W_\mathrm{crit} \cdot (\Delta w_\mathrm{hys})^{-n}, \tag{5.5}$$

where the constant n ($n > 0$) depends on the solder type and varies from less than 1 up to 2.2 [25], W_crit is the energy leading to the failure, and

Δw_{hys} represents the accumulated deformation energy per cycle, i.e., inelastic strain energy density calculated as the area enclosed by the hysteresis loop. As a result, the stress-strain solder response, i.e., hysteresis behaviour, can be employed as a tool for lifetime estimation of solder joints in electronic devices [28]. The material and geometry properties of the power module have to be known in order to calculate Δw_{hys}. Similarly to (5.5), the plastic strain range per cycle $\Delta \varepsilon_{\mathrm{hys}}$ can also be used to calculate N_{f} using a Coffin-Manson's type of fatigue law,

$$N_{\mathrm{f}} = \varepsilon_{\mathrm{crit}} \cdot (\Delta \varepsilon_{\mathrm{hys}})^{-n_1}, \tag{5.6}$$

which can be applied for many metals subjected to repetitive plastic deformation. The hysteresis solder behaviour is calculated from the constitutive equations for the specific type of eutectic solder alloy describing the elastic and (visco)plastic strain deformation of the solder joint under the applied stress. The material-dependent constants of the constitutive solder equations for various solder alloys are available in the literature. The main problem, as reported by Clech [29], is that constitutive solder equations were fitted to data-sets of various sources corresponding to different solder joints so that the material parameters found in the literature show a significant scatter. Specifically, the solder deformation is typically measured on solder joints of SMD electronic assemblies, e.g., Ball-Grid Arrays (BGA), Flip-Chip (FC), and Ceramic Chip Carriers (CCC). The geometry of the solder joint has an influence on the stress distribution and, thus, the solder deformation is expected to differ for bulk solder specimen and large area planar solder joints of power modules from SMD solder joints. Due to a lack of available data, the material parameters corresponding to SMD electronic assemblies found in the literature were applied for the lifetime modelling based on the ETHZ-PES model in [5,24,25]. It should be emphasized that there is a strong requirement to verify the employed constitutive model for the solder interconnections in power modules in order to be able to correctly and accurately calculate the lifetime expectations.

Besides the material parameters, the constitutive solder equations include other parameters depending on the geometry of the assembly, such as the effective assembly stiffness K and the imposed strain per degree temperature change D_1. These parameters have to be determined for the specific power module structure.

In [5,24], a parameterization procedure that takes a set of the experimental PC tests as input was suggested for the calculation of the unknown parameters K and D_1.

In [25], the authors used an FE method simulation of the power module's structure to find K and D_1 based on the approach suggested by Darveaux [30]. They proved a good agreement between the PC experiments and the developed physics-based lifetime model. The exponent n in (5.5) was the only parameter fitted to the experimental data.

Furthermore, using this energy-based model, the influence of different arbitrary temperature profiles on the lifetime of a power module can be estimated

by means of W_{crit}, e.g. as illustrated in [24]. However, for accurate lifetime estimation, it is necessary to extract the actual temperature profile of the solder layer under investigation for the given operational conditions. Therefore, in comparison to empirical models, which are mostly based on the virtual junction temperature value, the described energy-based model requires the knowledge of local maximum solder temperature values. This potentially leads to computationally expensive calculations and modelling techiques in practice, e.g., 3D thermal modelling performed to gain the solder temperature from the measured junction temperature. Accordingly, mission profile evaluation based on this physics-based lifetime model has to be further analysed and investigated in the future, including also the extraction of stress-strain hysteresis loops from complex stress-strain curves that can be defined as response of the solder material to arbitrary temperature profiles.

The theory of the ETH-PES lifetime model is described in more detail in Section 5.4, and the verification of this proposed approach by means of results of PC tests is presented in Section 5.5.

Model 2 - O. Schilling et al.

A second physics-based lifetime modelling approach was presented by O. Schilling et al. in [7]. This lifetime model is dedicated for the power module structure with the EOL determined by the failure of Al bond wires. The developed lifetime model is also based on a Morrow's type of fatigue law,

$$N_{\mathrm{f}} = c_1 \cdot (\Delta w_{\mathrm{hys}})^{c_2}, c_2 < 0. \tag{5.7}$$

The integrated deformation energy per cycle, Δw_{hys}, within Al bond wires was calculated from the stress-strain hysteresis loop using a 2D FEM simulation. Al bond wires are described by tensile strength, Young's modulus and yield strength in the 2D FEM simulation, while the solder layers are described by the viscoplastic ANAND model implemented in the commercial ANSYS FEM software tool [31]. The authors assumed $c_2 = -1.83$ taken from previous investigations presented in [32] that addressed the failure of power modules due to heel cracking of Al bond wires. However, the authors in [32] used the Coffin-Manson type of fatigue law based on the inelastic strain range defined by (5.6).

As the constant c_1 has no universal value and depends on geometry, the proposed approach returns only normalized N_{f} values. The lifetime modelling approach was compared with the normalized N_{f} vs. ΔT_{j} curve gained from empirical PC data assuming the power law $N_{\mathrm{f}}(\Delta T_{\mathrm{j}})$ dependency. The authors stated that the 2D FEM simulation data and the empirical data agreed well within the uncertainty of measurements.

Model 3 - Steinhorst et al.

A third physics-based modelling idea was recently presented by Steinhorst et al. in [6]. The proposed model calculates the crack initiation and propagation

in the solder layers due to fatigue, on the basis of the Darveaux's energy-based model [30],

$$N_0 = K_1 \cdot (\Delta W)^{K_2}, \tag{5.8}$$

$$\frac{\mathrm{d}a}{\mathrm{d}N} = K_3 \cdot (\Delta W)^{K_4}, \tag{5.9}$$

where N_0 is the number of cycles to crack initiation calculated based on the plastic energy density, ΔW, integrated during one temperature cycle, a is the crack length, and $\mathrm{d}a/\mathrm{d}N$ is the crack propagation. K_j, $j = 1 \ldots 4$ are the model parameters, which have to be fitted to the experimental curves. The academic FEM package SPC-Pm2Ad [33] is used to simulate the stress-strain hysteresis loops of the solder layers. From the integrated deformation energy, the crack length can be obtained. Simultaneously with the crack development, a thermal simulation of the power module is performed, and an increase of more than 20 % of the thermal resistance, R_{th}, is used as the failure criterion. The model is still in the development phase. The parameters of the model are arbitrarily selected, and also more comprehensive constitutive solder equations have to be implemented. The physics of crack propagation under thermal loading is complex in nature, as the crack propagation changes the structure of the solder layer. Additionally, the change of solder material properties with temperature should be also taken into account. The Darveaux's energy-based model given by (5.8) and (5.9) was also used in [34] to investigate the crack behaviour within the baseplate solder layer under different TC tests.

Model 4 - Déplanque et al.

Another lifetime prediction method for the solder joints in power modules was presented by Deplanque et al. in [35,36]. It is based on the crack propagation within the assembly of a chip soldered on a copper substrate. Damage of the solder joint was characterized by three methods: Scanning Acoustic Microscopy (SAM), measurements of the thermal resistance, and an FE method used to predict the crack initiation and propagation using the Paris law,

$$N_0 = C_1 \cdot (\varepsilon_{\mathrm{acc,int}})^{C_2}, \tag{5.10}$$

$$\frac{\mathrm{d}a}{\mathrm{d}N} = C_3 \cdot (\varepsilon_{\mathrm{acc,int}})^{C_4}, \tag{5.11}$$

where $\varepsilon_{\mathrm{acc,int}}$ is the mean value of the integrated accumulated creep strain along the lines coinciding with the direction of the crack propagation, N_0 is the number of cycles until crack initiation, $\frac{\mathrm{d}a}{\mathrm{d}N}$ is the crack propagation rate, and the constant parameters C_i, $i = 1 \ldots 4$, are the material-dependent coefficients, which are determined by means of FEM simulations. The authors calculated the values of C_i, $i = 1 \ldots 4$, for two examined solder alloys, SnPb and SnAgCu (SAC305). The crack length L after N cycles can be then calculated as

$$L = \frac{\mathrm{d}a}{\mathrm{d}N} \cdot (N - N_0). \tag{5.12}$$

It was shown in [35] that the damage surface can be used as a damage indicator instead of using the crack length, i.e., the equivalent accumulated creep strain integrated along the damage surface of the solder layer using the commercial FEM tool ANSYS. The implemented solder model includes both the primary and secondary creep, which makes the model more accurate. As the authors emphasized, the developed lifetime model is not fully tested, and more investigations are required in order to be able to apply it universally for every planar solder joint.

Based on (5.10)-(5.11), Newcombe et al. suggested in [37] a PoF approach for the substrate-baseplate solder interconnection, i.e., the solder layer between the DBC substrate and the baseplate,

$$\frac{\mathrm{d}L}{\mathrm{d}N} = C_3 \cdot (\Delta\varepsilon_\mathrm{p})^{C_4}, \tag{5.13}$$

where L is the crack length, and $\Delta\varepsilon_\mathrm{p}$ is the accumulated plastic strain per cycle. The coefficients C_3 and C_4 were taken from [36] for SnPb solder alloy. Using this lifetime model, an increase in lifetime for higher solder thickness was observed. A similar work was performed in [9], calculating C_3 and C_4 coefficients by FEA computer simulation for SnAg solder.

Furthermore, in [37], the main idea was to show that a PoF method using (5.13) integrated in a design optimization tool has a tremendous advantage over the standard Coffin-Manson approach. The parameters of a Coffin-Manson model (5.1) always correspond to a specific power module structure that has to be fully characterized in advance. On the other hand, the physics-based lifetime model defined by (5.13) enables an efficient lifetime prediction when some of the design paremeters are altered, e.g., the thickness of the solder layer.

Based on Model 4, a PoF approach for reliability prediction of IGBT modules, including four failure modes/locations — chip solder joint (die attach), substrate solder joint, the busbar solder joint and Al wire bonds — was presented in [38]. Two physics-based lifetime models were used: the model (5.13) was used for the lifetime estimation of solder interconnecting layers, and the $N_\mathrm{f}(\Delta\varepsilon_\mathrm{p})$ relation given by (5.6) was employed for the lifetime prediction of the bond wires. The advantages of such physics-based reliability design tools were pointed out by the authors.

Model 5 - Yang et al.

The damage-based crack propagation model in the time domain described in [8, 39] represents a very comprehensive physics-based model for wire bonds in power electronics modules. It takes into account both, the damage accumulation and the damage removal processes. It was shown that both mechanisms have an important impact during thermo-mechanical cycling. Specifically, the measurements of the bond shear force showed that the bonds subjected to temperature cycles with higher maximum value, T_max, had slower wear-out rates even though they were exposed to larger temperature swings, ΔT. This

behaviour was explained by the diffusion-driven damage removal mechanism and it was stated that neglecting this mechanism can lead to wrong lifetime predictions. Similarly to the ETHZ-PES lifetime model, the main idea of the damage-based crack propagation model is to avoid extensive accelerated testing, and additonally, to enable a more accurate lifetime estimation for arbitrary mission profiles.

The proposed damage-based lifetime model was evaluated against several TC tests only and the parameterization procedure was not explained in a comprehensive way. Additionally, a detailed verification that would allow for the usage of this lifetime estimation approach in typical PC test applications is needed in order to prove its functionality and accuracy.

The authors also summarized in [8] the state-of-the-art lifetime prediction models for wire bonds analysing their limitations and necessary investigations that have to be performed to gain better understanding of the real deformation mechanisms occurring in the bond wires under thermal loading, e.g. grain coarsening and softening.

5.3.4 Lifetime prediction based on PC lifetime models

The lifetime prediction of power modules using a PC test lifetime model, i.e., N_f-based model, is performed based on Miner's rule for damage accumulation [26]. According to Minor's rule, each temperature swing, ΔT_k, contributes independently to the decrease of the power module's lifetime with an extent defined by the corresponding number of cycles to failure, $N_\mathrm{f}|_{\Delta T_k}$, $Q(\Delta T) = \frac{N|_{\Delta T_k}}{N_\mathrm{f}|_{\Delta T_k}}$, where $Q(\Delta T_k)$ is the total damage produced by N cycles at the temperature swing of ΔT_k. EOL is reached when Q equals unity, $Q = 1$. The lifetime of a power module operating under n different temperature conditions, $k = 1 \ldots n$, is then defined by superposition of all individual damages $Q(\Delta T_k)$, and the EOL is reached for $\sum_{k=1}^{n} Q(\Delta T_k) = 1$.

In a real operating environment, power modules are exposed to rather non-uniform temperature variations, and thus, a proper definition of a temperature cycle within a given mission profile is required for the N_f-based lifetime modelling. Typically, the Rainflow algorithm is used to extract the temperature cycles from an arbitrary temperature profile. The Rainflow-counting algorithm was originally developed to define cycles as closed stress/strain hysteresis loops within a complex stress-strain curve in order to asses the fatigue life of material exposed to complex loading [40]. If it is assumed that the junction temperature is proportional to the stress in a given design, the Rainflow algorithm can be applied to count and measure temperature cycles contained within an arbitrary temperature profile. Generally, a cycle-counting algorithm cannot easily describe the impact of time-dependent effects and non-linear damage accumulation on the wear-out behaviour of power module interconnections. Thus, the transformation of a mission-profile into a sequence

of temperature cycles of certain duration remains a problem that introduces some uncertainties into the lifetime prediction especially for highly irregular temperature profiles, such as those experienced in automotive applications.

5.4 Physics-based lifetime estimation of solder joints within power semiconductor modules

The physics-based lifetime modelling of the solder joints used in power semiconductor modules is based on the stress-analysis of the module's assembly. The stress levels are used as indicators for the activation of different failure modes. Firstly, the nature of the stresses has to be examined, i.e., how stress appears and acts within materials, and secondly, the calculated or measured stress levels have to be correlated with the observed failures. The wear-out failures typically result from the thermally induced stresses, which in turn originate from the mismatch in thermal expansion of the adjoining layers. Specifically, mechanical and physical properties of the interconnecting interfaces determine the nature of stresses that the power module is able to survive. Furthermore, the time parameter has to be also included as a relevant variable in the stress analysis as the damage mechanisms within power modules are time-, geometry- and material-dependent.

The deformation occuring in a solder interconnecting layer can be numerically described by the constitutive solder equations. These constitutive equations are based on two state variables represented by two physical measures: stress and strain.

The thermo-mechanical deformation is often described by the equivalent von-Misses stress σ^{e} and strain ε^{e} in the three dimensional space, using three principle planes [41]. The equivalent von-Misses stress and strain can be expressed in terms of the actual normal (σ, ε) and shear (τ, γ) stress and strain components that are developed when the solder interconnecting layer is exposed to a cyclic thermal load. For the planar solder joints within power modules, the shear stress and strain components are important due to the geometry and material properties of the power module's assembly. The effective shear stress τ and strain γ can be derived from the equivalent von-Misses stress σ^{e} and strain ε^{e} as [41]

$$\tau^* = \frac{1}{\sqrt{3}} \cdot \sigma^{\mathrm{e}}, \tag{5.14}$$

$$\gamma^* = \sqrt{3} \cdot \varepsilon^{\mathrm{e}}. \tag{5.15}$$

In the literature, the consitutive solder equations are either given in the form of shear or tensile solder data. The transformations given by (5.14) and (5.15) are then used to convert the normal stress τ and strain ε components into the shear components τ and γ and vice-versa [42].

Two different deformation mechanisms of solder material can be distinguished: fatigue and creep/stress relaxation. Fatigue occurs in solder due

to the constant accumulation of damage when the solder material is exposed to cyclic thermo-mechanical loading. On the other hand, at sufficiently high stresses and temperatures, the solder material shows the tendency to move or deform permanently to relieve stress. These phenomena are referred to as creep and stress relaxation. Compared to fatigue, i.e., time-independent deformation caused usually by the initiation and propagation of cracks, creep and stress relaxation are types of time- and rate-dependent damage mechanisms and are usually caused by the formation and growth of voids within the solder material [43]. The term "creep" is more specifically used for straining under a constant stress, while stress relaxation corresponds to the deformation under a constant strain.

At the temperatures developed under PC and TC test conditions or in the field defined by the mission profile, both the creep and fatigue damaging processes can be activated in the power module. Instead of pure creep or pure fatigue, the regime of creep-fatigue interaction is more often present [43]. It is very hard to say which of these two mechanisms will predominate and finally cause the failure of the weakest solder interconnecting layer.

The next sections (Section 5.4.1-Section 5.4.4) address the theory of the stress and strain deformations of solder material exposed to cyclic thermal loading. The constitutive solder equations relevant for the physics-based lifetime models of solder joints in power semiconductor modules are summarized.

5.4.1 Stress-strain (hysteresis) solder behaviour

Due to the difference of thermo-mechanical properties of the adjacent components connected by solder, shear force acts across the solder interconnecting layer and produce simultaneous bending and stretching of the whole assembly. Analysing deformation mechanisms of the solder joint layer between ceramic chip-carriers (CCC) and printed wiring boards in the Leadless CCC assemblies, Hall found that the shear stress-strain response of the solder joint to periodical temperature cycling has the shape of a hysteresis loop [27]. The accumulation of damage in the solder material is reflected by the area enclosed by the hysteresis loop. A hysteresis loop describes the complex stress-strain history of the solder layer exposed to repetitive cyclic loading, and the shape of the hysteresis can be explained by the behavioural model of solder material. Furthermore, it was observed that the points on the hysteresis curve corresponding to the same temperatures form a set of parallel lines called the stress reduction lines.

A resulting stress-strain loop that is not closed means that the stress-strain response may change with successive load cycles. In the simulation, the hysteresis loop usually tends to stabilize after several load cycles. With respect to the thermo-mechanical deformations occurring in power modules, a load cycle corresponds to a temperature cycle that is either generated under the accelerated cycling tests or in the application field. The parameters that determine the shape of a stabilized hysteresis loop are presented schematically in Fig. 5.2.

The minimum and maximum shear stress and strain values, $\tau_{\min}$,$\tau_{\max}$, $\gamma_{\min}$ and $\gamma_{\max}$, correspond to the extreme values of the temperature cycle, $T_{\min}$ and $T_{\max}$.

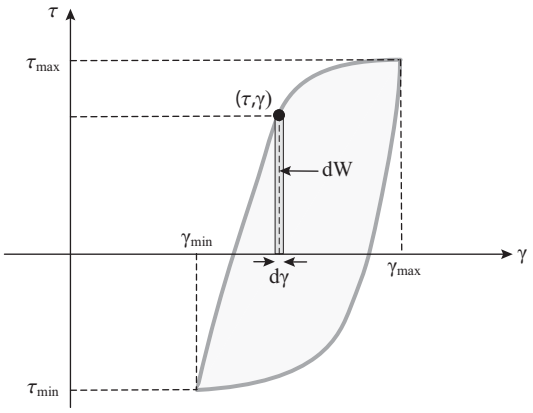

Figure 5.2: The response of solder to a periodic temperature cycle between $T_{\min}$ and $T_{\max}$ temperature values: a stabilized hysteresis loop. The minimum and maximum shear stress and strain values, $\tau_{\min}$, $\tau_{\max}$, $\gamma_{\min}$, and $\gamma_{\max}$, are defined by $T_{\min}$ and $T_{\max}$ and the material and geometrical properties of solder.

At different stress levels and temperatures, the solder material experiences different physical deformations that gradually contribute to damage accumulation and finally to the failure of the solder interconnection. As a result, the stress-strain plot can be employed as a tool for lifetime estimation of solder joints in electronic devices, which was also described by the proposed thermo-mechanical model in [26]. Solder constitutive equations numerically describe time-independent elastic and plastic deformations, i.e., fatigue, and time-dependent plasticity (viscoplasticity), i.e., creep. Specifically, for each temperature change, the total increase of strain can be described by three components: γ_{elastic}, γ_{plastic}, and γ_{creep}. All three components are incorporated in a general equation for total strain,

$$\gamma_{\text{TOT}} = \gamma_{\text{eleastic}} + \gamma_{\text{plastic}} + \gamma_{\text{creep}}. \tag{5.16}$$

Furthermore, the strain components can be defined as a function of stress τ, temperature T, and time t. As elasticity and plasticity are time- and rate-independent, the elastic and plastic strain components, γ_{elastic} and γ_{plastic}, are only functions of stress and temperature. On the other hand, creep represents the time-dependent plasticity, and it is a function of all three variables. The elastic, plastic, and creep solder behaviour are derived based on the methods of classical mechanics and physics. The corresponding constitutive solder equations are summarized in the following subsection.

5.4.2 Constitutive solder equations

The elastic behaviour is described by Hooke's law,

$$\gamma_{\text{eleastic}} = \frac{\tau}{G(T)}, \tag{5.17}$$

where $G(T)$ is the shear modulus. The temperature-sensitivity of the shear modulus is given by the shear modulus constants G_0 and G_1,

$$G(T) = G_0 - G_1 \cdot (T - 273\text{K}), \tag{5.18}$$

which depend only on the type of material.

Several models for time- and rate-independent plasticity of eutectic solder alloy were published in the literature [44–46]. The commonly used model was proposed by Darveaux [45, 47],

$$\gamma_{\text{plastic}} = C_{\text{p}} \cdot \left(\frac{\tau}{G}\right)^{m_{\text{p}}}, \tag{5.19}$$

where C_{p} and m_{p} are the material-dependent parameters.

Typically, creep becomes relevant at temperatures of about $0.3T_{\text{M}}$ for pure metals and about $0.4T_{\text{M}}$ for alloys and most ceramics, where T_{M} is the melting point of material. Three typical stages of creep can be identified: primary, secondary, and steady-state creep. Primary creep is a transient regime of deformation in which the strain rate decreases over time until it reaches the minimal value defined by the steady-state creep rate. The tertiary creep is an unstable regime with very fast increasing strain-rate, which precedes the final rapture of the material. The steady state creep has been mainly investigated by engineers in the past, as it was assumed to be the dominant creep over time. The majority of strain-rate equations in the literature correspond therefore to the steady-state regime. For most of the existing physics-based lifetime models of solder interconnections in electronic devices, often only the steady-state is taken into account. Moreover, the creep mechanisms are mainly investigated for the steady-state creep regime. Under these investigations of steady-state creep, different atomistic processes responsible for creep development are analysed, such as the gliding and climbing motions of dislocations in the crystal structure, and the diffusion of atoms (or vacancies) through the lattice of a crystal or along the grain boundaries. These two mechanisms refer to the dislocation-controlled and diffusion-controlled creep mechanisms, respectively. They become dominant at different stress and temperature levels. Specifically, the dislocation creep occurs and becomes dominant for higher levels of applied stress, while the diffusion-controlled creep appears at lower stress levels and higher temperatures, which is roughly at about $0.3T_{\text{M}}$ for metals. A schematic representation of a deformation mechanism map can be used to identify the dominant damage mechanism [43].

Different types of models based on, e.g., a power law approach, a hyperbolic sine (sinh) law, a two-cell model, or an obstacle-controlled model, as

summarized in [42], have been used for modelling the steady-state creep behaviour. These equations can be directly applied if all equation parameters are given for the specific solder type of interest. Here, the Darveaux's constitutive solder model is presented as a comprehensive model that includes both the equations for the primary and the steady state creep:

$$\frac{\mathrm{d}\gamma_\mathrm{s}}{\mathrm{d}t} = C_1 \cdot \frac{G(T)}{T} \cdot \left[\sinh\left(\alpha \frac{\tau}{G(T)}\right)\right]^n \cdot e^{-\frac{Q}{k \cdot T}}, \tag{5.20a}$$

$$\gamma_\mathrm{prim} = \gamma_\mathrm{T} \cdot (1 - e^{-B \cdot t \cdot \frac{\mathrm{d}\gamma_\mathrm{s}}{\mathrm{d}t}}), \tag{5.20b}$$

$$\gamma_\mathrm{tot} = \gamma_\mathrm{prim} + \frac{\mathrm{d}\gamma_\mathrm{s}}{\mathrm{d}t} \cdot t, \tag{5.20c}$$

where $G(T)$ is the temperature-dependent shear modulus (5.18), γ_s is steady-state creep strain component, γ_prim is the strain component due to primary creep, α, B, Q, γ_T, C_1, G_0 and G_1 are material constants dependent on solder type and τ is the value of shear stress in MPa. Additionally, the material-dependent model constants for several solder types can be found in the literature.

Another stress-strain relation describing the thermo-mechanical solder behaviour is defined by the isothermal stress reduction lines,

$$\gamma + \frac{\tau}{K} = D_1 \cdot (T - T_0), \tag{5.21}$$

where T_0 is a fixed temperature reference, K is the effective assembly stiffness, and D_1 is the imposed strain per degree temperature change. The parameters K and D_1 depend both on solder type and on the geometry of the power module. In the special cases when the slope of the stress reduction lines, K, tends to a very high or very low value, i.e. $K \to \infty$ or $K \to 0$, it reduces to the stress relaxation line and pure creep line, respectively. This relationship is derived from a simplified spring model of an assembly of two materials connected by solder [48].

The constitutive solder equations (5.17)-(5.21) are used to model the hysteresis behaviour of the solder material exposed to an arbitrary temperature profile. Clech derived the algorithm for calculating the stress-strain response of the solder joints exposed to temperature changes. As a numerical approach, the Clech's algorithm can be implemented as a computer application that further allows building a computer-based design-for-reliability tool [49]. Clech's algorithm is therefore introduced in the next subsection.

5.4.3 Clech's algorithm

Clech's idea was to find a way to accurately simulate the response of the solder joints of Surface-Mount Devices (SMDs) exposed to cyclic thermal loading. Clech's algorithm can be explained by Fig. 5.3.

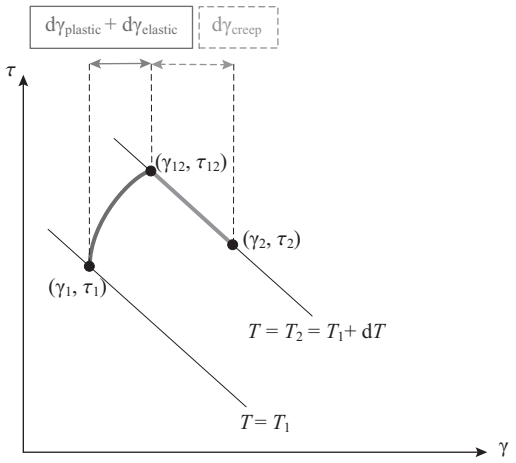

Figure 5.3: Calculation of stress-strain (hysteresis) response according to Clech's algorithm.

Knowing the stress-strain state (γ_1, τ_1) at time t, the stress-strain state (γ_2, τ_2) at time $t+\Delta t$ can be calculated using the constitutive solder equations. It is assumed that:

(a) Δt is a relatively small time step ($\Delta t \rightarrow \mathrm{d}t$). (b) The stress is built up instantaneously for the temperature increase from $T = T_1$ to $T_2 = T_1 + \mathrm{d}T$. For this instantaneous stress change it is assumed that dominant strain components are time-independent elastic and plastic components $\mathrm{d}\gamma_{\mathrm{elastic}}$ and $\mathrm{d}\gamma_{\mathrm{plastic}}$. (c) At temperature T_2, the change of stress follows the T_2-stress reduction line building the total strain component, which is in turn mainly defined by the creep component, $\mathrm{d}\gamma_{\mathrm{creep}}$.

Clech's algorithm allows the numerical calculation of the stress-strain hysteresis loops of solder interconnecting layers exposed to a given temperature profile (mission profile) with an arbitrary shape. Accordingly, Clech's algorithm represents the computational core of a Computer-Aided-Design (CAD) lifetime estimation tool.

5.4.4 Energy-based lifetime modelling

Physical lifetime modelling of solder joints in chip packages is based on models that can be classified in four groups: stress-based, strain-based, damage-based, and energy-based models [50]. All these models require the stress and strain data to be known in order to predict service life. In comparison to the other methods, energy-based models are seen to be the most convenient, as they have the ability to capture test conditions with more accuracy.

The energy-based lifetime models use the information of the energy enclosed by the stress-strain hysteresis loop to predict the EOL of an electronic

device. Most of the energy-based models are derived based on studies that investigated the lifetime of solder joints in high-density electronics packages mostly used in telecommunication and consumer electronics, such as surface-mount packages, e.g. Chip Size Packages (CSP), Chip Carrier (CC), and Ball Grid Arrays (BGA). The developed lifetime models account for the geometry of the solder joint and, thus, cannot be straightforwardly applied to an arbitrary type of solder joint.

Energy-based modelling is based on the assumption that the EOL of a device is determined by the total deformation energy accumulated within the solder joint during the operation of a device. A device fails when the deformation work reaches the critical value, W_{tot}. Specifically, the energy-based models correlate the hysteresis energy density, i.e., the deformation energy per cycle, and the number of cycles to failure, N_{f},

$$N_{\mathrm{f}} = C \cdot (\Delta w_{\mathrm{hys}})^{-n}, \tag{5.22}$$

where C and n are the model constants that often depend on the material and geometrical properties of the chip package, and Δw_{hys} is the accumulated energy per cycle or inelastic strain energy density. The value of Δw_{hys} is calculated by integrating the stress along strain in the strain range $(\gamma_{\mathrm{min}}, \gamma_{\mathrm{max}})$ defined by the hysteresis loop, see Fig. 5.2,

$$\Delta w_{\mathrm{hys}} = \oint_{\mathrm{HysLoop}} \tau \, \mathrm{d}\gamma \, . \tag{5.23}$$

The energy-based lifetime modelling using Clech's algorithm can then be summarized by the following steps: (1) the stress-strain response of a solder joint is generated by means of Clech's algorithm, (2) the parameters C and n are derived from experiments, and (3) the parameterized energy-based N_{f}-model is applied to calculate EOL for different temperature profiles.

The other type of energy-based models involves the crack initiation and propagation inside the solder layer, based on the Darveaux's energy-based model (5.8)-(5.9), which links the number of cycles to the crack initiation, N_0, and the crack propagation rate to the accumulated energy density per cycle. The EOL is then defined by a critical crack length.

5.5 Example of physics-based lifetime modeling for solder joints

The ETHZ-PES lifetime model for the solder joints inside of power semiconductor modules described in Section 5.3.3 was tested using experimental PC results, conducted by SEMIKRON Elektronik GmbH & Co. KG [10]. The aim was to verify the proposed lifetime prediction approach for its application to PC test conditions. Nine samples of standard baseplate modules in half-bridge configuration, SKM200GB12T4 [22], were used for the verification. The specifications of the corresponding PC experiments are given in Table 5.2 and Table 5.4. In the SKM200GB12T4 module, the chips are soldered to the

DBC substrate using Sn3.5Ag solder. Under all PC tests, the chip solder fatigue was the dominant failure mechanism that justifies the selection of the employed set of PC cycles for the model verification.

The modelling steps using the proposed algorithm are schematically presented by a flowchart in Fig. 5.4 and described in the following. Additionally, the solder material- and geometry-dependent parameters used in the model are specified in Table 5.1.

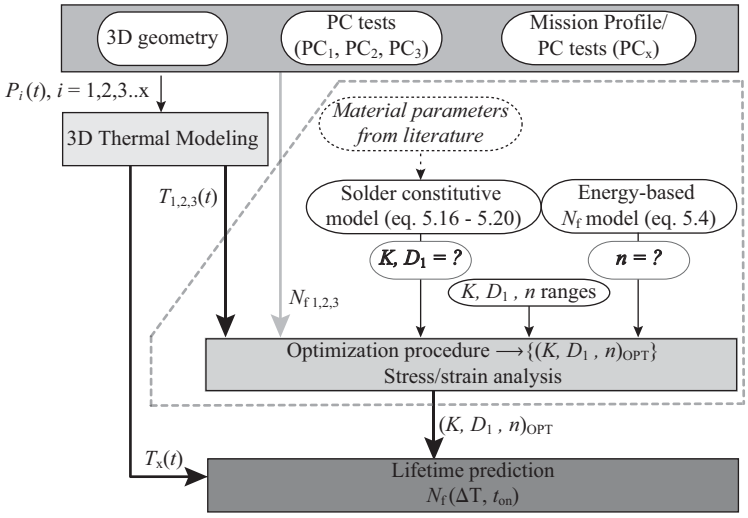

Figure 5.4: Flowchart describing the main modelling steps of the ETHZ-PES physics-based lifetime model for the solder joints of power semiconductor modules. The block marked by a dashed line includes the procedure for finding the unkown material and geometry-dependent solder parameters.

5.5.1 Thermal simulation

As a first step, 3D thermal simulations of the power module were conducted in order to calculate the temperature evolution in the module during a power cycle of each experimental PC test. In order to perform a physical simulation of the solder aging in which both creep and time-independent elasticity and plasticity are considered, it is necessary to know not only the maximum and minimum temperature of the junction, but also the total time-dependence of the solder temperature $T(t)$.

In the experimental setup, the devices were mounted on a water-cooled heatsink. During the heating phase of a power cycle, the water flow through the heatsink was stopped in order to obtain a sharp temperature increase. By contrast, the water flow was turned on during the cool-down time of each power cycle, so that the lower temperature limit was reached more quickly.

Table 5.1: Material- and geometry-dependent Sn3.5Ag solder parameters.

Time-independent elastic strain (5.17) [47]	
G_0 [MPa]	19310
G_1 [MPa/K]	68.9
Time-independent plastic strain (5.19) [47]	
C_p	$2 \cdot 10^{11}$
m_p	4.4
Steady-state creep strain (5.20)(a) [47]	
C_1 [K/s/MPa]	0.454
α	1500
n	5.5
Q [eV]	0.5
Primary creep strain (5.20)(b) [47]	
γ_T	0.086
B	147
Range of the unkown geometry-dependent parameters (5.21)	
K [MPa]	$(5 \cdot 10^2\ ,\ 10^4)$
D_1 [1/K]	$(10^{-4}\ ,\ 10^{-3})$

Because of this design of the experiment, a simulation is not straight-forward: Foster models cannot be used, since two different models describe the system with and without water flow, and it is impossible to switch the models during simulation (since there is no way of determining the state of charge of the equivalent capacitors). At the same time, a full-fledged thermo-hydrodynamic simulation of the complete system, including the water flow, is very time-consuming, especially because multiple power cycles have to be simulated, before the system reaches thermal equilibrium. Therefore, a physical approach has been chosen based on a simplified 3D-Cauer-based model (see Section 5.3.1). Experience has shown that the simulation of the junction temperature evolution of a power module on a heatsink can be well approximated if a solid heatsink is used and a (non-physical) transition layer with negligible thermal capacitance is inserted beneath it. The thermal resistivity of this transition layer is then adapted such that the measured total thermal resistance from junction to ambient is reproduced. This approach can be applied to both systems with and without water flow, resulting in two different values for the thermal resistivity of the transition layer. Specifically, in an electric equivalent circuit of the thermal system of the power module, the transition layer is replaced by two sets of thermal resistors. The switches, which are placed in

front of the resistors, connect the corresponding set of the resistors to the rest of the electric equivalent circuit. These switches are then operated in accordance with the heating and cooling cycles.

Using this approach, a 3D thermal simulation model was built using the program MAKENET [51], as illustrated in [21], which generates an electrical equivalent circuit of resistors and capacitors from the 3D geometry that can consequently be simulated with PSPICE. The simulation results of the junction temperature change during a power cycle are found to be in good accordance with the temperature monitoring during the PC test. In order to reach even higher accuracy for the simulation of the solder aging, the power cycle is then rescaled linearly in order to describe the measured temperature change exactly. The solder temperature is read from these rescaled simulation results. The maximum temperature points of the solder layer under the chip center obtained from the thermal modelling are used further as the input for the lifetime modelling.

5.5.2 Stress-strain modeling

The second step was to calculate the stress-strain response to the simulated temperature profiles according to the procedure described in Section 5.4.3. The required inputs of the algorithm for calculating hysteresis solder behaviour are the constitutive solder equations (5.17)-(5.20), the geometry-dependent parameters that define the stress-reduction lines (5.21) and the exponent parameter n of the energy-based N_f-model, cf. (5.22).

The complete constitutive equations including creep and plastic time-independent deformations of Sn3.5Ag solder alloy have not been published. A majority of publications concentrates on the ultimate strength and steady-state creep [29]; however, it was shown in [45] that Sn3.5Ag undergoes more primary creep and, hence, the primary creep should not be neglected for this type of solder material. Dareveaux's solder constitutive relations were found to provide the most comprehensive solder model of Sn3.5Ag solder alloy available, and, thus, they were implemented in the proposed lifetime model [47], cf. Table 5.1.

The parameters K and D_1 in (5.21) define the stress-reduction lines, and both depend on the solder type and the module geometry. These model parameters are determined in a parameterization procedure implemented as MATLAB optimization routine using the N_f results from three PC experiments, PC_{1-3}. The properties of the tests PC_{1-3} are defined in Table 5.2, and the corresponding Temperature Profiles (TP) gained from the thermal modelling decribed above are shown in Fig. 5.5.

The optimal parameters K, D_1, and n should minimize the difference of three deformation energies, $W_{\mathrm{crit}i}$, $i = 1, 2, 3$, calculated by (5.5) for the corresponding simulated temperature profiles, T_i,

$$W_{\mathrm{crit}i} = N_{\mathrm{f}i} \cdot (\Delta w_{\mathrm{hys}i})^n, i = 1, 2, 3. \tag{5.24}$$

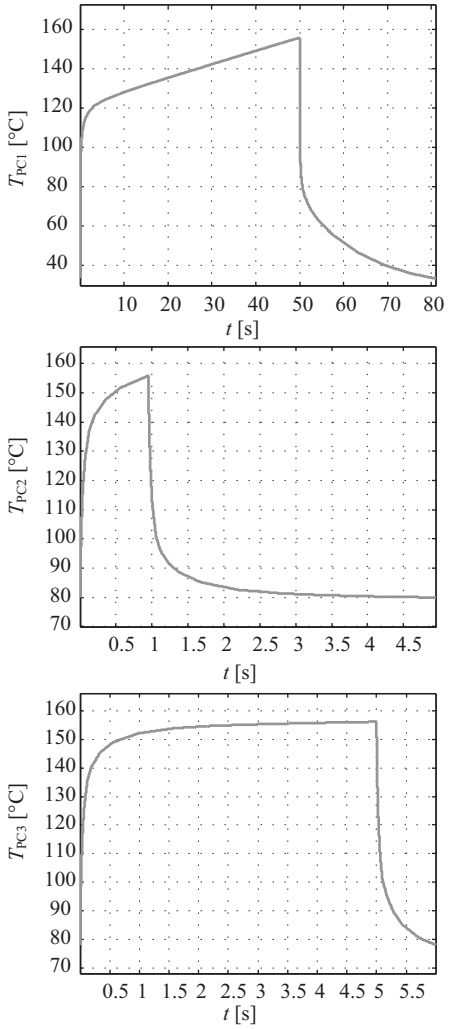

Figure 5.5: Temperature profiles T_{PC1}, T_{PC2}, and T_{PC3} developed under PC_1, PC_2, and PC_3 tests, respectively.

Table 5.2: Specifications of PC Tests used for the Parameterization.

PC test	$T_{\min}$ [°C]	$T_{\max}$ [°C]	ΔT [°C]	$t_{on}, t_{off}[s]$	P_{loss} [W]	N_{f} [cycles]
PC_1	40	155	115	50, 31	925.9	31332
PC_2	80	148	68	0.95, 4	900	220279
PC_3	78	148	70	5, 1	480	168390

Table 5.3: N_{f} prediction for $PC_{1,2,3}$ tests.

PC test	N_{fmin}, N_{favg}, N_{fmax} (5.25)	$N_{\text{f,estim}}$	Rel. error [%]	$\frac{\text{d}T}{\text{d}t}$ (at $T_{\max}$)
1	31302, 38762, 53654	(N_{fmin}, N_{favg})	$(-0.09, 23.7)$	0.66 K/s
2	128514, 159142, 220279	(N_{favg}, N_{fmax})	(27.7, 0)	10.67 K/s
3	168390, 208521, 288627	(N_{fmin}, N_{favg})	(0, 23.8)	0.37 K/s

The free parameters of the optimization algorithm are K, D_1, and the exponent n. The values of other model parameters are the solder constants taken from the literature, cf. Table 5.1. The error r of parameterization is defined as the maximum ratio between the calculated critical energies, $r = \max(W_{\text{crit}i}/W_{\text{crit}j})$, $i, j = 1, 2, 3$, $i \neq j$. In an ideal case, r would be unity, i.e., $W_{\text{crit1}} = W_{\text{crit2}} = W_{\text{crit3}}$. In practice, there is an optimal r-value higher than unity. Accordingly, the estimated number of cycles to failure, $N_{\text{f,estim}}$, can be defined as a N_{f}-range, (N_{fmin}, N_{favg}, N_{fmax}), which corresponds to the minimum $W_{\text{crit}min}$, average $W_{\text{crit}avg}$, and maximum $W_{\text{crit}max}$ of the calculated critical energies for three PC tests resulting from the optimization procedure (5.25).

$$W_{\text{critFunc}} = \text{Func}(W_{\text{crit1}}, W_{\text{crit2}}, W_{\text{crit3}}) \tag{5.25a}$$

$$N_{\text{fFunc}} = \frac{W_{\text{critFunc}}}{(\Delta w_{\text{hys}})^n}, \text{Func} = \text{avg}, \max, \min. \tag{5.25b}$$

The error, r, of the parameterization for the PC tests specified in Table 5.2 is $r = 1.714$. Namely, for the PC_1 test, the actual N_{f1} value is closer to the minimum of the estimated N_{f}-range, for the PC_2 test the actual N_{f2} value coincides with the maximum, and for the PC_3 test the actual N_{f3} coincides with the minimum of the estimated N_{f}-range, as shown in Table 5.3.

The exponent, n, is set to 2.2 as the best fit to the experimental data. The range of the parameters as input of the optimization procedure is selected such

that the stress-strain behaviour of solder alloy is correctly modeled, i.e., creep is higher at high maximum temperatures and low temperature rates, e.g., for the PC_1 and PC_3 tests, and time-independent plasticity is dominant for fast temperature changes, e.g., the PC_2 test. Specifically, the order of 10^3 and of 10^{-4} is selected for K and D_1, respectively, as specified in Table 5.1, which returns a good agreement with the simulated stress-strain response of the solder joint to the expected physical behaviour of solder, see Section 5.5.6. It was shown in [25] that the unknown parameters K and D_1 are correlated, i.e., a higher D_1 corresponds to a lower value of K and vice versa. An optimal parameter set is calculated to be $(K,\, D_1) = (1403.03,\, 9.9 \cdot 10^{-4})$.

5.5.3 Stress-strain analysis

The N_f prediction is performed based on the analysis of the simulated stress-strain curves. The parameters of interest are the temperature swing amplitude, ΔT, the maximum temperature level, T_max, and the temperature rate, $\mathrm{d}T/\mathrm{d}t|_{T_\mathrm{max}}$. The values of ΔT, T_max, and $\mathrm{d}T/\mathrm{d}t|_{T_\mathrm{max}}$ for PC_{1-3} are given in Tables 5.2 and 5.3.

The temperature profiles generated in PC_i experiments can be analysed to gain a better understanding of the expected stress-strain response. For example, both the PC_3 test and the PC_2 test have a lower temperature amplitude of 70K, but the PC_3 test is characterized by slower temperature change at the maximum temperature level in comparison to the PC_2 test. Accordingly, the chip solder layer experiences more creep deformation for the PC_3 test and, thus, shorter lifetime. On the other hand, the PC_1 experiment is characterized by a higher temperature swing of 115K and a longer heating time, which explains the resulting shorter lifetime.

The share of creep strain component in the total strain deformation can be used as a quantitative measure of creep deformation. Specifically, by observing the stress-strain deformation under a temperature cycle, it can be concluded that the temperature evolution at T_max is relatively slow for PC_3, and thus it can be expected that the creep strain component has a similar or higher share in the total strain deformation than the elastic/plastic time-independent strain component. After the simulation, with the optimal parameter set, the creep component at T_max was calculated for the PC_3 test to be approx. 50 %. Similarly, for the PC_1 experiment, the creep component reaches 40 % of the total strain deformation, while for the PC_2 test, the time-independent elastic-plastic strain component is dominant, i.e., more than $\approx$ 80 % of the total strain.

Due to longer heating times, the stationary state is reached for the PC_1 and PC_3 experiments, and not reached for the PC_2 test with a shorter t_on. As an example, for the described stress-strain analysis, the hysteresis loops for the tests PC_1, PC_2 and PC_3, are presented in Fig. 5.6, where also the fast temperature change occurring in power modules under typical power cycling test conditions and the strain components for test PC_1 are depicted.

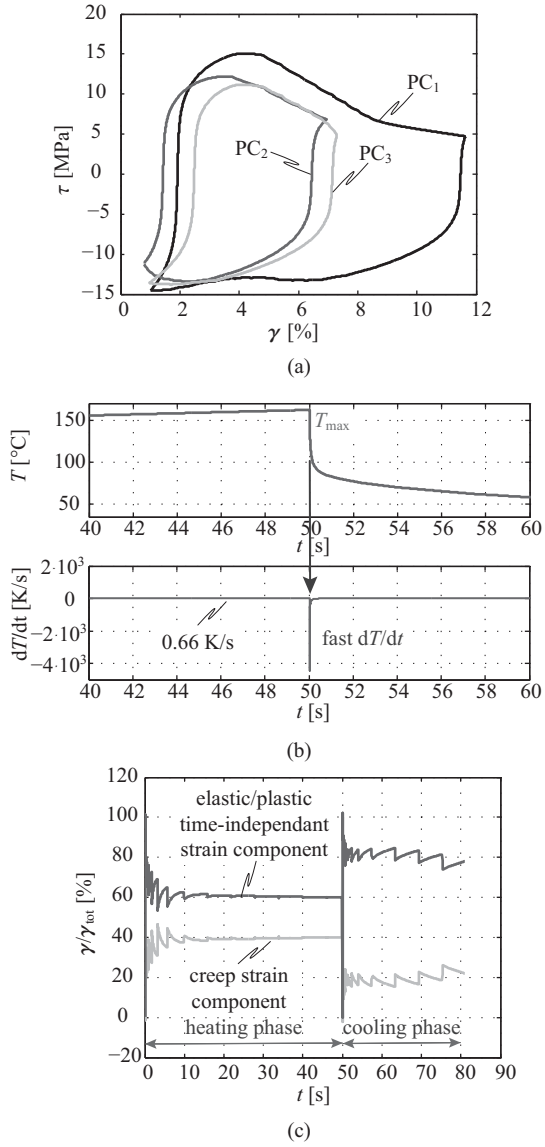

Figure 5.6: Stress-strain analysis: (a) stress-strain response, i.e., hysteresis loops, under PC_1, PC_2 and PC_3 tests; (b) zoomed part of the temperature profile T_{PC1} of the PC_1 test at the transition between the heating and cooling phases illustrating a fast temperature change; (c) strain components developed for the PC_1 test.

Table 5.4: Specifications of PC tests used for the model verification.

PC test	$T_{\min}$ [°C]	$T_{\max}$ [°C]	ΔT [°C]	$t_{\text{on}}, t_{\text{off}}[s]$	P_{loss} [W]	N_{f}
A	40	155	174	64.5, 48.7	921.9	28780
B	79	146	67	0.95 , 4	912	248710
C	80	150	70	1.2, 4	920	234632
D	77	150	73	2.9, 0.9	944	149125
E	39	148	109	13.6, 10.3	1122	38441
X	40	176	136	2, 3	1569.4	21956

Table 5.5: N_{f} prediction for $\text{PC}_{\text{A-X}}$ tests.

PC test	N_{fmin}, N_{favg}, N_{fmax} (5.25)	$N_{\text{f,estim}}$	Rel. error [%]	$\frac{\text{d}T}{\text{d}t}$ (at $T_{\max}$)
A	23216, 28749, 39793	(N_{fmin}, N_{favg})	(19.3,-0.1)	0.7 K/s
B	140949 174541, 241594	(N_{favg}, N_{fmax})	(-29.9, -2.8)	10.4 K/s
C	122054, 151142 209205	(N_{favg}, N_{fmax})	(-35.6, -10.8)	10.1 K/s
D	164966, 204281, 282758	(N_{fmin}, N_{favg})	(10.6, 36.9)	1.2 K/s
E	31393, 38875, 53809	(N_{fmin}, N_{favg})	(-18.3, 1.1)	0.9 K/s
X	21853, 27061, 37457	(N_{fmin}, N_{favg})	(-0.5, 23.2)	5.2 K/s

5.5.4 Model verification

By observing the properties of the calculated stress-strain curves at the simulated temperature profiles T_{1-3}, the N_{f}-lifetime is estimated within the calculated N_{f}-range. For PC tests, which resemble the tests PC_1 or PC_3, N_{f} is predicted in the lower N_{f}-range, (N_{fmin}, N_{favg}); and for PC tests which are similar to the PC_2 test, the N_{f} predictions are located in the upper part of the N_{f}-range, (N_{favg}, N_{fmax}).

Following the proposed procedure, the prediction of the number of cycles to failure for other power cycle experiments, PC_{A}, PC_{B}, PC_{C}, PC_{D}, PC_{E}, PC_{X}, specified in Table 5.4, was performed. The estimated N_{f}-ranges and relative errors are shown in Table 5.5.

The temperature profiles of the power cycles PC_B and PC_C are very close to the temperature profile of PC_2, so that N_f is evaluated as the maximum of the calculated N_f-range with relative errors of less than 11 %.

Tests PC_D and PC_3 exhibit similar ΔT and T_{max}. Analysing the stress-strain curves, it was observed that the creep strain component has a similar share in the total strain for both PC tests, i.e., tending to 50%. Accordingly, the estimated N_f value is set in the lower N_f-range, as for test PC_3.

Tests PC_A and PC_E exhibit higher temperature amplitudes, similar to the PC_1 test, the stationary state is reached in test PC_A and nearly reached in test PC_E. The share of the creep strain component is approximately 40 %, as for test PC_1, so that the estimation of the lifetime belongs to the lower N_f-range, according to the parameterization of the PC_1 test.

Test PC_X represents a more specific case. It exhibits a shorter heating time but a very high maximum temperature of 176°C and a high temperature amplitude of 134°C. The creep component was calculated to be less than 40 % of total strain, as for test PC_2. As the high temperature amplitude and high maximum temperature are shown to have a direct influence on the lifetime and the creep strain component is a derived factor, the decision making is performed based on the parameterization of test PC_1, which is characterized by a high ΔT.

The relative estimation errors are summarized in Table 5.5. A maximum estimation error of less than 24 % indicates a good agreement between the lifetime prediction based on the ETHZ-PES model and the PC N_f-test results.

5.5.5 Lifetime curves extraction

The presented lifetime modeling enables extracting the lifetime curves of the SKM200GB12T4 power module. A lifetime curve represents the N_f dependency on the temperature swing amplitude ΔT for a defined heating time t_{on}, i.e., $N_f(\Delta T)|_{t_{on}}$.

Temperature profiles for different values of ΔT are calculated by keeping the average temperature, the heating time, and the cooling time constant, and scaling the simulated temperature profile of the power module to obtain the desired temperature change. This corresponds to power cycles which differ only in the amount of dissipated power and the cooling medium temperature. Using the calculated temperature profiles for lower and higher temperature swings, the lifetime prediction, i.e., N_f, in both low and high stress regimes can be calculated by applying the proposed procedure described by the flowchart in Fig. 5.4. The $N_f(\Delta T)$ curve corresponding to the medium temperature T_{avg}, heating time t_{on}, and cooling time t_{off} of test PC_2 is shown in Fig. 5.7.

As can be seen in Fig. 5.7, the calculated N_f values show two asymptotic linear dependencies in a log-log plot, i.e., $N_f \propto \Delta T^{-\alpha}$, for low and high temperature swings, with exponents of $\alpha \approx 3$ and $\alpha \approx 13$, respectively. The lifetime curves extracted for the tests PC_1 and PC_3 show similar behaviour, i.e., the exponent α varies around 3 for higher ΔT and around 13 for lower

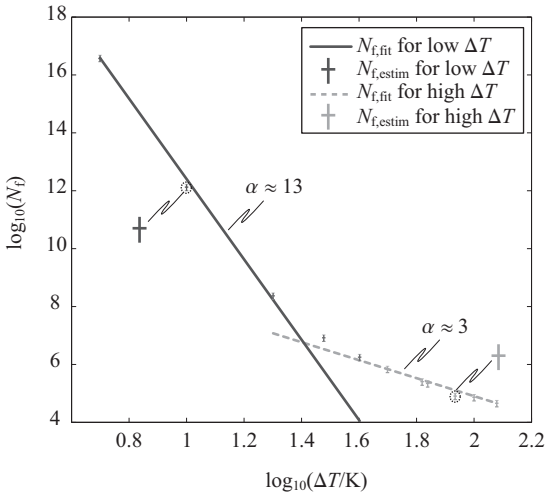

Figure 5.7: Lifetime curves $N_f(\Delta T)$ extracted for the average temperature T_{avg}, heating time t_{on}, and cooling time t_{off} of test PC_2; the cross symbols indicate the estimated N_f values with an estimation error of less than 25% in the low and high ΔT ranges; the full lines represent the linear asymptotic curves fitted to the estimated N_f values with the calculated slopes of $\alpha = 13$ and $\alpha = 3$ for lower and higher values of ΔT, respectively.

values of ΔT. A high exponent of $\alpha = 13$ indicates that the common extrapolation of the power cycling results towards lower temperatures is much too conservative, at least for solder failures. This can be also ascribed to the constitutive model used, i.e., Darveaux's solder model. The parameters of Darveaux's model for Sn3.5Ag solder were derived from tensile and shear loading experiments employed in the temperature range between 25 °C and 135 °C [47]. Accordingly, it must be considered that Darveaux's solder model must be further evaluated and verified for lower and/or higher temperatures for accurate lifetime prediction in a wide temperature range.

5.5.6 Model accuracy and parameter sensitivity

It should be pointed out that the scattering of cycles to failure by ≈ 20% around the mean value is common for PC tests even if the tests are conducted under as far as possible equal conditions. Specifically, the PC tests PC_2, PC_B, and PC_C can be considered as nearly same; however, a deviation of the number of cycles to failure between these PC tests can be observed. Similar to tests PC_D and PC_3, even though the power module under test PC_3 is expected to fail faster than under test PC_D due to longer heating time [17], a shorter lifetime was observed for test PC_D. Accordingly, an estimation error in the range of about 20% can be characterized as a good N_f prediction.

As previously mentioned, a reliable constitutive model for the solder alloy employed in the power module has to be implemented first in order to correctly model the lifetime assuming the wear-out of the solder layer as the dominant failure mechanism. The elastic deformation is described by the Young's modulus, and the strain-hardening power law is typically used to describe time-independent plastic strain deformation, but there is no unique relation describing the creep deformation mechanism of solder. In order to simplify creep modelling, the steady-state (secondary) creep is commonly the only creep mechanism considered in the thermo-mechanical modelling of solder joints in microelectronics packaging. Different types of creep models, e.g., a power law model, a hyperbolic sine (sinh) law, a two-cell model, and an obstacle-controlled model [42], have been developed to describe the steady-state creep behaviour. However, it was shown that primary creep cannot be neglected for lead-free solder alloys [52]. The parameters of the constitutive relations are determined by curve fitting using data gained in monotonic and creep test experiments of the solder material under investigation [53]. Therefore, the model parameters depend on solder material and solder joint configuration. To collect data for building an accurate constitutive model, the solder joint used in the experiment setup should closely resemble the real solder joint design to be modeled [54]. These types of experiments actually are missing for the solder joints of power modules. The data of Sn3.5Ag solder alloy used in the tested SKM200GB12T4 modules are not well covered in the literature. Darveaux's model for Sn3.5Ag solder was implemented in the ETHZ-PES lifetime model as all model parameters of the solder constitutive model can be found in the literature, including primary and secondary creep strain deformation and elastic/plastic time-independent deformation [47].

The sensitivity of N_f estimation to the change of K, D_1, and n, which are fitted to the experimental PC test data in the parameterization procedure, is performed to gain a better insight into the physical meaning of the unknown parameters. The parameter K represents the effective assembly stiffness, and D_1 is the imposed strain per degree temperature change, which reflects the geometry and the difference of the CTEs between the layers connected by soldering. As can be observed by increasing the stiffness K and/or decreasing D_1 by an order of magnitude, the creep strain component becomes smaller than the elastic/plastic time-independent strain component for all PC temperature profiles and vice versa; by decreasing the stiffness K and/or increasing D_1 by an order of magnitude, the creep component becomes dominant over the elastic/plastic time-independent strain component even for the PC_2 test, characterized by a fast temperature change and a short heating time. This behaviour agrees to the isothermal stress reduction curve, which tends to a stress relaxation line and a pure creep line, for two extremes, $K = \infty$ and $K = 0$, respectively [48]. Even though a similar error of parameterization can be achieved by values of K and D_1 of different magnitude, the stress-strain curves obtained with these parameters do not describe the expected physical solder behaviour.

By finding an optimal parameter set (K, D_1) in the same parameters ranges for different values of n, it was observed that the relative error of the N_f estimation is significantly higher for lower values of n, which is best visible for the test PC_X, e.g., the relative error is about 64 % for $n = 1$. Accordingly, the best estimation is achieved for a value of $n = 2.2$, which is also the result of the optimization procedure with three variables (K, D_1, n).

By changing the value of the parameters (K, D_1) by 10 % around their nominal (calculated) values, the error of the parameterization r is changing up to 1.76, which does not have a significant influence on the lifetime prediction, i.e., less than 10 %. Higher D_1 shifts the hysteresis loop in the area of higher strain, and higher K increases the hysteresis loop area, which implies higher damage.

5.5.7 Lifetime estimation tool

The ETHZ-PES lifetime model is implemented in a MATLAB software tool, which has been partially developed in the course of the ECPE research project "Reliability and Lifetime Modeling and Simulation of Power Modules and Power Electronic Building Blocks" [55]. Through an easy-to-use GUI (Fig. 5.8), users can specify the temperature profiles of power cycling tests, run a parameterization for the defined range of model parameters, analyse the calculated stress-strain response, and estimate the relative lifetime of power module for two arbitrary temperature profiles. The constitutive solder models for different solder types found in the literature [42,45,56] have also been implemented. This software tool still needs further improvements, but nevertheless represents a useful basis for developing a universal physics-based lifetime modeling tool for power modules.

5.6 Conclusions

Physics-of-Failure (PoF) lifetime modeling approaches can be seen as a new methodology in power electronics that potentially can improve the lifetime estimation and enable reliability engineering to be integrated into the development and research cycles of the overall design process of power electronics systems. As illustrated in Fig. 5.9, the coupling of different domains within a virtual prototyping platform, e.g., electrical circuit simulations, thermal modeling and lifetime prediction, will allow egineers to develop reliable PECSs in a time- and cost-efficient way in future. The developed MATLAB software with the implemented ETH-PES lifetime model can be seen as a first step towards a virtual prototyping platform.

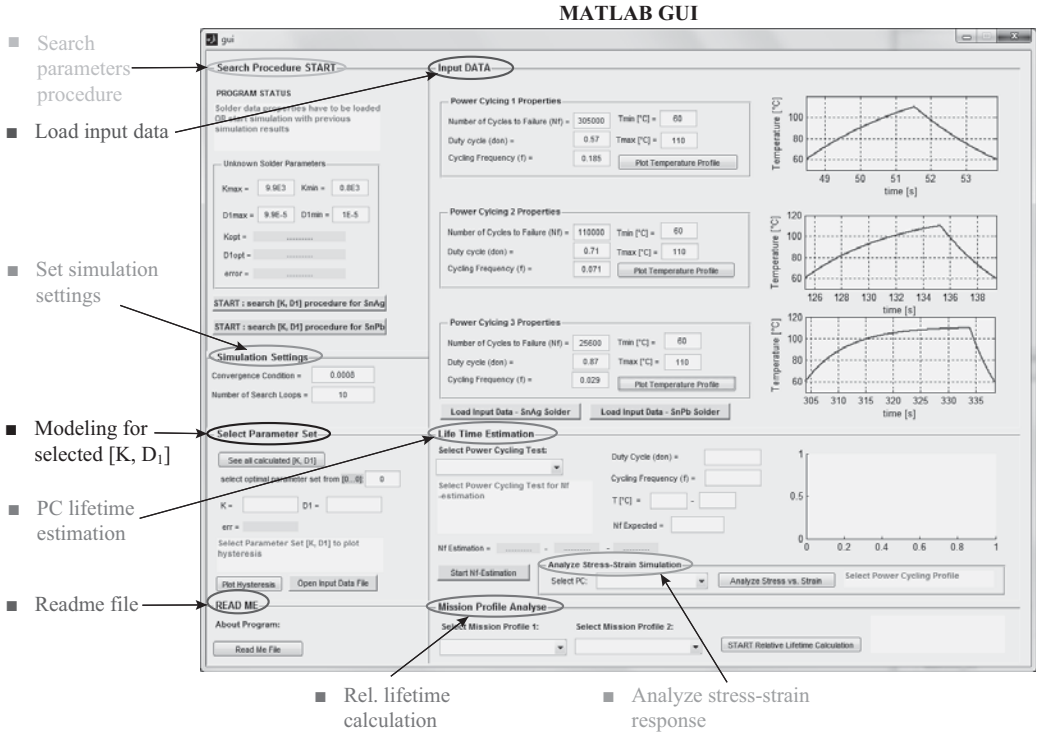

Figure 5.8: GUI of the MATLAB software tool for lifetime estimation of solder layers of power modules based on the ETHZ-PES model.

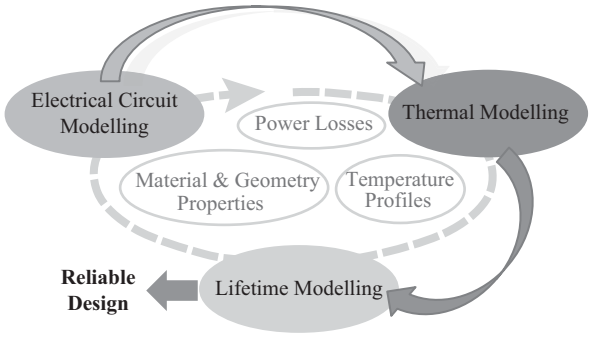

Figure 5.9: Concept for a virtual prototyping platform for reliability analysis of power modules and/or PECS.

5.7 Acknowledgements

The authors would like to thank Prof. Dr. Uwe Scheuermann and Dr. Ralf Schmidt from SEMIKRON for providing experimental data, helpful suggestions, and inspiring discussions based on their long-term experience in lifetime modeling. Furthermore, the authors are very much indebted to the European Center for Power Electronics (ECPE) for financing the research project "Reliability and Lifetime Modeling and Simulation of Power Modules and Power Electronic Building Blocks" [55], which significantly contributed to the development of the presented approach.

Bibliography

[1] J. Lutz, "Packaging and reliability of power modules," in Proc of 8^{th} Int. Conf. on Integrated Power Systems (CIPS), 2014, pp. 17–24.

[2] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of IGBT modules in traction application," Int. Journal of Electronics, vol. 86, no. 10, pp. 1193–1204, 1999.

[3] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of IGBT modules - various factors influencing lifetime," in Proc of 5^{th} Int. Conf. on Integrated Power Systems (CIPS), 2008, pp. 37–42.

[4] R. Schmidt, F. Zeyss, and U. Scheuermann, "Impact of absolute junction temperature on power cycling lifetime," in Proc. of 15^{th} European Conf. on Power Electronics and Applications (EPE), 2013, pp. 1–10.

[5] I. Kovacevic, U. Drofenik, and J. W. Kolar, "New physical model for lifetime estimation of power modules," in Proc. of the Int. Power Electronics Conf. (ECCE Asia), 2010, pp. 2106–2114.

[6] P. Steinhorst, T. Poller, and J. Lutz, "Approach of a physically based lifetime model for solder layers in power modules," Microelectronics Reliability, vol. 53, no. 8-10, pp. 1199–1202, 2013.

[7] O. Schilling, M. Schaefer, K. Mainka, M. Thoben, and F. Sauerland, "Power cycling testing and FE modelling focussed on Al wire bond fatigue in high power IGBT modules," Microelectronics Reliability, vol. 52, no. 9-10, pp. 2347–2352, 2012.

[8] L. Yang, P. A. Agyakwa, and C. M. Johnson, "Physics-of-failure lifetime prediction models for wire bond interconnects in power electronic modules," IEEE Trans. Device Mater. Rel., vol. 13, no. 1, pp. 9–17, 2013.

[9] H. Lu, T. Tilford, and D. Newcombe, "Lifetime prediction for power electronics module substrate mount-down solder interconnect," in Proc. of Int. Symp. on High Density Packaging and Microsystem Integration (HDP), 2007, pp. 1–10.

[10] (2015). [Online]. Available: http://www.semikron.com/

[11] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. Jacobson, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 1, pp. 97–114, 2014.

[12] Semiconductor devices-Mechanical and climatic test methods-Part 34: Power cycling (IEC 60747-34), Int. Electrotechnical Commission (IEC) Std.

[13] Semiconductor devices-Discrete devices-Part 9: Insulated-gate bipolar transistors (IGBTs) (IEC 60747-9), Int. Electrotechnical Commission (IEC) Std.

[14] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. DeDoncker, Semiconductor Power Devices Physics, Characteristics, Reliability. Springer, 2011.

[15] T. Herrmann, M. Feller, J. Lutz, R. Bayerer, and T. Licht, "Power cycling induced failure mechanisms in solder layers," in Proc. of the European Conf. on Power Electronics and Applications, 2007, pp. 1–7.

[16] M. Ciappa, "Selected failure mechanisms of modern power modules," Microelectronics Reliability, vol. 42, no. 4, pp. 653–667, 2002.

[17] U. Scheuermann and R. Schmidt, "A new lifetime model for advanced power modules with sintered chips and optimized Al wire bonds," in Proc. of Int. Exhibition and Conf. for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), 2013, pp. 810–817.

[18] H. Huang and P. A. Mawby, "A lifetime estimation technique for voltage source inverters," IEEE Transactions on Power Electronics, vol. 28, no. 8, pp. 4113–4119, 2013.

[19] U. Scheuermann and P. Beckedahl, "The road to the next generation power module - 100% solder free design," in Proc. of 5^{th} Int. Conf. on Integrated Power Systems (CIPS), 2008, pp. 111–120.

[20] U. Drofenik and J. Kolar, "Teaching thermal design of power electronic systems with web-based interactive educational software," in Proc. of 18^{th} Annual IEEE Applied Power Electronics Conf. and Exposition (APEC), vol. 2, 2003, pp. 1029–1036.

[21] R. Schmidt and U. Scheuermann, "Using the chip as a temperature sensor - The influence of steep lateral temperature gradients on the $V_{ce}(T)$-measurement," in Proc. of 13^{th} European Conf. on Power Electronics and Applications (EPE), 2009, pp. 1–9.

[22] U. Scheuermann and R. Schmidt, "Impact of solder fatigue on module lifetime in power cycling tests," in Proc. of 14^{th} European Conf. on Power Electronics and Applications (EPE), 2011, pp. 1–10.

[23] A. Hamidi, A. Stuck, N. Beck, and R. Zehringer, "Time dependent thermal faitgue of HV-IGBT-modules," in Proc. of 27^{th} Kolloquium Halbleiter-Leistungsbauelemente und Materialgüte von Silizium, Freiburg/Breisgau, Oct. 1998.

[24] U. Drofenik, I. Kovacevic, R. Schmidt, and J. W. Kolar, "Multi-domain simulation of transient junction temperatures and resulting stress-strain behavior of power switches for long term mission profiles," in Proc. of the 11^{th} IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), 2008, pp. 1–7.

[25] G. Riedel, R. Schmidt, C. Liu, H. Beyer, and I. Alapera, "Reliability of large area solder joints within IGBT modules: Numerical modeling and experimental results," in Proc. of 7^{th} Int. Conf. on Integrated Power Systems (CIPS), 2012, pp. 288–298.

[26] M. Ciappa, "Lifetime modeling and prediction of power devices," in Proc. of 5^{th} Int. Conf. on Integrated Power Systems (CIPS), 2008, pp. 1–9.

[27] P. M. Hall, "Forces, moments, and displacements during thermal chamber cycling of leadless ceramic carriers soldered to printed boards," IEEE Trans. Compon., Hybrids, Manuf. Technol., vol. 7, no. 4, pp. 314–327, 1984.

[28] R. Darveaux, "Effect of assembly stiffness and solder properties on thermal cycle acceleration factors," in Proc. of 11^{th} Int. Workshop on Thermal Investigations of ICs and Systems (THERMINC), 2005, pp. 192–203.

[29] J.-P. Clech, Lead-Free Electronics: iNEMI Projects Lead to Successful Manufacturing. Wiley-IEEE Press, 2007.

[30] R. Darveaux, "Effect of simulation methodology on solder joint crack growth correlation," in Proc. of 50^{th} Electronic Components and Technology Conf., 2000, pp. 1048–1058.

[31] G. Z. Wang, K. Becker, J. Wilde, and Z. N. Cheng, "Applying ANAND model to represent the viscoplastic deformation behavior of solder alloys," J. Electron. Packag., vol. 123(3), pp. 247–253, 1998.

[32] S. Ramminger, N. Seliger, and G. Wachutka, "Reliability model for Al wire bonds subjected to heel crack failures," Microelectronics Reliability, vol. 40, no. 8-10, pp. 1521–1525, 2000.

[33] A. Meyer, Programmer's Manual for Adaptive Finite Element Code SPC-PM 2Ad, Preprint SFB393 01-18 TU Chemnitz, 2001.

[34] T.-Y. Hung, C.-J. Huanga, C.-C. Leed, C.-C. Wange, K.-C. Lue, and K.-N. Chiang, "Investigation of solder crack behavior and fatigue life of the power module on different thermal cycling period," Microelectronic Engineering, vol. 107, pp. 125–129, 2013.

[35] S. Déplanque, "Lifetime prediction for solder die-attach in power applications by means of primary and secondary creep," Ph.D. dissertation, The Brandenburg University of Technology Cottbus-Senftenberg, 2007.

[36] S. Déplanque, W. Nuchter, B. Wunderle, R. Schacht, and B. Michel, "Lifetime prediction of SnPb and SnAgCu solder joints of chips on copper substrate based on crack propagation FE-analysis," in Proc. of 7^{th} Int. Conf. on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems (EuroSime), 2006, pp. 1 – 8.

[37] D. Newcombe and C. Bailey, "Rapid solutions for application specific IGBT module design," in Proc. of Int. Exhibition and Conf. for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM), 2007.

[38] H. Lu, C. Bailey, and C. Yin, "Design for reliability of power electronic modules," Microelectronics Reliability, vol. 49, pp. 1250–1255, 2009.

[39] L. Yang, P. A. Agyakwa, and C. M. Johnson, "A time-domain physics-of-failure model for the lifetime prediction of wire bond interconnects," Microelectronics Reliability, vol. 51, no. 9-11, pp. 1882–1886, 2011.

[40] S. D. Downing and D. F. Socie, "Simple rainflow counting algorithms," International Journal of Fatigue, vol. 4, no. 1, pp. 31–40, 1982.

[41] J. H. L. Pang, Lead Free Solder. Springer, 2012.

[42] J.-P. Clech, "An obstacle-controlled creep model for Sn-Pb and Sn-based-lead-free solders," in Proc. of SMTA Int. Conference (SMTAI), 2004.

[43] D. Rubesa, Lifetime prediction and constitutive modeling for creep-fatigue interaction. Gebrueder Borntraeger Berlin, 1991.

[44] W. Ramberg and W. R. Osgood, "Description of stress-strain curves by three parameters," National Advisory Committee for Aeronautics, Washington DC, Tech. Rep., 1943.

[45] R. Darveaux and K. Banerji, "Constitutive relations for tin-based solder joints," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. 15, no. 6, pp. 1013–1024, 1992.

[46] S. Knecht and L. R. Fox, "Constitutive relation and creep-fatigue life model for eutectic tin-lead solder," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. 13, no. 2, pp. 424–433, 1990.

[47] R. Darveaux, K. Banerji, A. Mawer, and G. Dody, Reliability of plastic ball grid array assemblies (Chapter 13), J. H. Lau, Ed. McGraw-Hill, 1995.

[48] C. H. Raeder, L. E. Felton, R. W. Messier, and L. F. Coffin, "Thermomechanical stress-strain hysteresis of Sn-Bi eutectic solder alloy," in Proc. of 17^{th} IEEE/CPMT Int. Electronics Manufacturing Technology Symp., 1995, pp. 263–268.

[49] J.-P. Clech, "Solder reliability solutions: A PC-based design-for-reliability tool," Soldering & Surface Mount Technology, vol. 9, pp. 45 – 54, 1997.

[50] W. Lee, L. Nguyen, and G. Selvaduray, "Solder joint fatigue models: Review and applicability to chip scale packages," Microelectronics Reliability, vol. 40, no. 2, pp. 231–244, 2000.

[51] U. Scheuermann and J. Lutz, "High voltage power module with extended reliability," in Proc. of 8^{th} European Conference on Power Electronics and Applications (EPE), 1999.

[52] D. Shirley, "Transient and steady-state creep in Sn-Ag-Cu lead free solder alloys: Experiments and modeling," Ph.D. dissertation, University of Toronto, 2009.

[53] K. Mysore, G. Subbarayan, V. Gupta, and R. Zhang, "Constitutive and aging behavior of Sn3.0Ag0.5Cu solder alloy," IEEE Trans. Electron. Packag. Manuf., vol. 32, no. 4, pp. 221–232, 2009.

[54] H. Yang, P. Deane, P. Magill, and K. Murty, "Creep deformation of 96.5Sn-3.5Ag solder joints in a flip chip package," in Proc. of Electronic Components and Technology Conf., 1996, pp. 1136–1142.

[55] (2015) The European Center for Power Electronics (ECPE). [Online]. Available: http://www.ecpe.org/home/

[56] S. Wiese and K.-J. Wolter, "Microstructure and creep behaviour of eutectic SnAg and SnAgCu solders," Microelectronics Reliability, vol. 44, pp. 1923–1931, 2004.