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Opportunities and challenges for spintronics in the microelectronics industry

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Spintronic devices exploit the spin, as well as the charge, of electrons and could bring new capabilities to the microelectronics industry. However, in order for spintronic devices to meet the ever-increasing demands of the industry, innovation in terms of materials, processes and circuits are required. Here, we review recent developments in spintronics that could soon have an impact on the microelectronics and information technology industry. We highlight and explore four key areas: magnetic memories, magnetic sensors, radio-frequency and microwave devices, and logic and non-Boolean devices. We also discuss the challenges—at both the device and the system level—that need be addressed in order to integrate spintronic materials and functionalities into mainstream microelectronic platforms.

Conventional electronic devices are based on nonmagnetic semiconductors and use the controlled flow of electric charges to achieve information processing and communication. Spintronic devices, on the other hand, exploit the spin of electrons to generate and control charge currents, and to interconvert electrical and magnetic signals. By combining processing, storage, sensing, and logic within a single integrated platform, spintronics could complement and, in some cases, outperform semiconductor-based electronics, offering advantages in terms of scaling, power consumption, and data processing speed[1].

The discovery of giant magnetoresistance[2,3] (GMR) in 1988, a result for which Albert Fert and Peter Grünberg would later be awarded the Nobel Prize in Physics, kick-started the field of spintronics. Since then, a range of phenomena have been studied, including the behaviour of nanostructured magnetic systems under electric currents[4–6], the interplay of charge and spin transport[7,8], and spin dynamics in magnetic[9–11] and nonmagnetic[12,13] systems. The field has also already delivered large-scale commercial applications: GMR-based spin valves and magnetic tunnel junctions (MTJs) have been used as magnetic field sensors in tape and hard disk drive read heads, as position or proximity sensors in cars, automated industrial tools, and biomedical devices. Furthermore, the discovery of spin-transfer torque[14,15] (STT) and spin–orbit torque (SOT)[16], of giant tunnelling magnetoresistance (TMR)[17,18] in MgO-based MTJs and of large interfacial magnetic anisotropy at magnetic metal/oxide interfaces[19], has led to the development of scalable nonvolatile magnetic random-access memories[20–23] (MRAMs). Commercial STT-MRAMs are now used as a replacement for embedded flash (eFlash) memory or static RAM (SRAM) in embedded cache memories due to advantages such as easy integration with complementary metal oxide semiconductor (CMOS) technology, low energy consumption, fast switching, and superior endurance[22].

However, in order for spintronic devices to meet the ever-increasing demands for high-speed, high-density, and low power electronic components, further innovations in the design of materials, processes, and circuits are required. Recent developments include the generation and interconversion of charge, spin, heat and optical signals, based on non-equilibrium spin–orbit interaction effects, such as the spin Hall and Rashba–Edelstein effects[8,24] or their thermal[25] and optical[26,27] analogues. SOT can, in particular, excite any type of magnetic material, including metals, semiconductors and insulators, whether ferromagnetic, ferrimagnetic or antiferromagnetic[6]. This versatility means that SOT can be used to switch the spin configuration of single magnetic layers, as well as to

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Box 1 | The TRL scale

TRL 1 – Basic principles observed
TRL 2 – Technology concept formulated
TRL 3 – Experimental proof of concept
TRL 4 – Technology validated in lab
TRL 5 – Technology validated in relevant environment (industrially relevant environment in the case of key enabling technologies)
TRL 6 – Technology demonstrated in relevant environment (industrially relevant environment in the case of key enabling technologies)
TRL 7 – System prototype demonstration in operational environment
TRL 8 – System complete and qualified
TRL 9 – Actual system proven in operational environment (competitive manufacturing in the case of key enabling technologies; or in space)

excite spin waves and auto-oscillations in both planar and vertical device geometries[10,11]. Furthermore, charge–spin conversion effects could potentially be used for information processing with Boolean logic, as well as unconventional computing schemes such as neuromorphic[28–30] and probabilistic[31] computing. Spintronic devices also cover a broad frequency spectrum from direct current (d.c.) to THz[32,33], which could be useful for the on-chip generation and detection of high-frequency signals.

In this Review Article, we examine spintronic phenomena and the specific applications that have the potential for medium-term implementation in integrated or embedded electronic systems: that is, applications that have been validated by proof-of-concept devices, corresponding to a technology readiness level (TRL)[34] of three and above (Box 1). Our aim is to highlight the current and future capabilities of spintronics to the broader electronics community and to encourage the spintronics community to focus on, and think about, applications; the ultimate goal being to help translate basic research into industrial technologies and economic gains. We discuss four key areas (http://www.spintronicfactory.eu/): magnetic memories, magnetic sensors, radio frequency and microwave devices, and logic and non-Boolean devices. We also discuss two key research areas needed to support these applications: the development of advanced materials, fabrication methods and tests; and modelling and design.

Magnetic memories

The demand for on-chip memories is increasing due the exponential growth of data storage requirements and the gap between processor and off-chip memory speeds. The increase in volatile memory components, which require power to maintain stored data, has also increased the energy consumption at the chip level, reaching the power limits for safe operation of devices. One approach to overcome these issues is to adopt a modified memory hierarchy by integrating nonvolatile memories at various levels. This approach would minimize the static power consumption and also enable normally-off/instant-on computing: that is, computing that is off when not in use and instantly switches on when needed.

Current status. Perpendicularly magnetized STT-MRAM (Fig. 1b), offers low power consumption, fast switching, small cell size, high endurance and scalability[22,23], and leading semiconductor companies and tool suppliers have launched STT-MRAM development programs[35–38]. For example, Intel recently announced that the company has successfully integrated embedded MRAM into its 22 nm FinFET CMOS technology on full 300mm wafers[39], whereas Samsung and Everspin/Global Foundries have announced the release of a 1GB embedded MRAM on their 28 nm (ref. [40]) and 22 nm technology nodes[41] respectively. STT-MRAMs have entered commercialization as a replacement for eFlash in embedded cache memories, with strong potential applications as L3/L4 SRAM replacement[42] and also possibly as a persistent dynamic RAM (DRAM) technology. Table 1 compares the properties of various memory technologies, including DRAM, different types of SRAM volatile memory, perpendicular STT-MRAM (pSTT-MRAM) and SOT-MRAM. Note that the MTJ pillar diameter (35 nm) in MRAM technologies is significantly larger than the CMOS node.

Future challenges. To make MRAM competitive with DRAM, improvements in density via downscaling are required. Several solutions for patterning MTJ at very narrow pitch have been proposed, which typically either use improved etching chemistries[43] or use unconventional strategies such as depositing the MTJ on pre-patterned pillars[44]. Improvements in the power consumption of STT-MRAM (by reducing the STT current below 2 MA cm^{-2}) and its operation speed (by increasing the TMR), while maintaining long retention times, will also be required. In this regard, an optimized stack design based on two tunnel barriers with antiparallel polarizing layers has recently been shown to maximize anisotropy, retention and STT efficiency[45]. One approach to improve downsize scalability is to introduce perpendicular shape anisotropy[46] (PSA-STT-MRAM)[46], by significantly increasing the thickness of the storage layer in order to induce a perpendicular shape anisotropy that reinforces the interfacial anisotropy. As a result, large thermal stability factors can be achieved down to sub-10-nm diameters.

Magnetic memories based on SOT (SOT-MRAM)[16,47] (Fig. 1c,d) offer high speed and improved endurance, but require larger writing currents, a static magnetic field in some configurations[48], and have a higher footprint. To reduce the write current, and therefore the size of the selection transistor of these devices, charge–spin conversion materials with low resistivity and large SOT efficiency need to be developed. Wafer-scale SOT-MRAM architectures based on CMOS-compatible processes have been demonstrated[47,48], as well as cell configurations not requiring an external magnetic field. Such configurations may use an antiferromagnetic heavy metal line that provides an in-plane exchange bias via the spin Hall effect[49,50], a combination of STT with SOT[51,52], or a magnetic in-plane magnetized hard mask[47], to achieve field-free SOT switching.

To reduce the power dissipation due to Ohmic conduction, the control of magnetism by an electric field (voltage-controlled MRAM) has been explored as a new MRAM write mechanism[53,54]. Such devices require a current only during the read operation for charging/discharging the MTJ, which results in a very low switching energy for the write operation. However, the practical use of voltage-controlled MRAM is still challenging. First, the application of moderate voltages (of around 1 V) cannot achieve a sufficient voltage-induced change of magnetic anisotropy (VCMA) to induce magnetization switching, while ensuring the magnetic thermal stability of the device in standby. Second, the write time window in these devices is small and size-dependent, resulting in reliability issues. Similar to SOT-based technologies, voltage-controlled MRAM also requires an in-plane field. Promising approaches to mitigate these issues include hybrid VCMA-STT combinations in two-terminal devices, and VCMA-SOT combinations in three-terminal MTJ devices, which can offer an acceleration in the write speed, lower current thresholds, as well as the selective SOT switching of several MTJs sharing a single write line[55].

Other proposed types of memory are storage shift registers, termed race track memories[56]. In these devices, the information is stored in the form of tracks of polarized spin textures (that is, domain walls or skyrmions[57]), which can be moved by an electrical

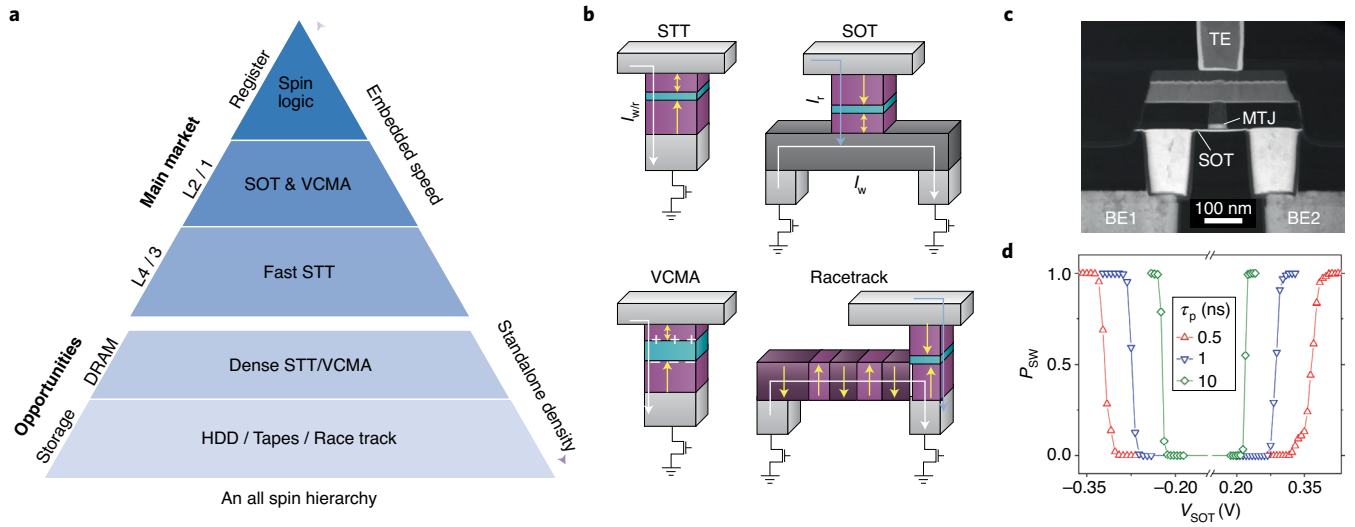

Fig. 1 | Nonvolatile magnetic memories. a, Modification of the memory hierarchy by spintronic solutions where main markets are embedded cache memories (L1–4) and possibly extending to in-memory computing and logic applications, and standalone memories opportunities markets for intermediate memory layers (DRAM, storage class) and storage applications requiring high density and low power. **b**, MRAM architectures considered. Two terminal spin transfer torque (STT), fast and dense but limited to 5–10 ns write latencies. It is actively developed by major actors of semiconductor industry and in production. Voltage control of magnetic anisotropy (VCMA) that is foreseen as a future of STT as it combines low energy and ns write latencies. Three terminal spin-orbit torque (SOT) that operates at sub-ns regimes with high endurance. Racetrack memory concept that relies on fast domain wall motions under SOT current for high density memories or spin logic applications. **c**, Transmission electron microscopy (TEM) cross section of a field-free SOT memory cell where write current is injected from BE1 to BE2 and read from TE to BE2. **d**, probability of switching as a function of the injected voltage for a 50 nm SOT-MRAM memory cell. I_w, write current; I_r, read current. Credit: **c**,**d**, IMEC.

Table 1 | Comparison of the properties of volatile memory technologies and perpendicular STT-MRAM and SOT-MRAM at advanced CMOS technology nodes (7 nm and 5 nm)

	DRAM 10× (ref. [151])	HP-SRAM 5 nm (ref. [152])	HD-SRAM 5nm (ref. [152])	HD-SRAM 7 nm (ref. [152])	pSTT 35 nm WER 1e9 / 1e6 (ref. [47])	SOT 35 nm (ref. [47])
Techn./node	10x	5 nm	5 nm	7 nm	5 nm	5 nm
Write energy/bit (fJ)	89	19	76	70	<500 / 375	75
Read energy/bit (fJ)	58	17	55	50	60 /52	15
Write latency (ns)	10	>1	2.75	2.5	<10 / 7.5	1.2
Read latency (ns)	10	>1	2.5	2.2	3.5 / 3.5	1
Cell size (μm²)	0.0026	0.034	0.0267	0.0422	0.014 / 0.009	0.0282

current along the tracks (Fig. 1b), achieving high storage densities without mechanical motion. In this field, the technical challenges are the control of coherent motion of the spin textures along the track without pinning, at high speed and low current.

Magnetic sensors

In the past 10–15 years, spintronic magnetic field sensors based on the TMR effect have been gradually replacing technologies based on giant magnetoresistance (GMR), anisotropic magnetoresistance (AMR), and conventional Hall effect, offering higher output and signal-to-noise ratio (SNR), good thermal stability, compatibility with CMOS integration, reduced cost, and small feature sizes (< 1 mm²; refs. [58–63]). These sensors have applications in areas such as the automotive sector (for example, angular, speed, current and position sensors), industry 4.0 (for example, current and power sensors, linear and angular encoders, and scanners), and consumer electronics (for example, three-dimensional (3D) magnetometers and digital compasses). Novel low-power, reliable devices on silicon or flexible substrates[58,60] have also found application in the emerging Internet of Things (IoT) and biomedical sectors.

A typical TMR stack consists of several layers (buffer/AF/SAF/MgO/FL/cap)[59,60]. In particular, the antiferromagnetic (AF) layer is coupled to the pinned layer in the synthetic antiferromagnet (SAF) via exchange bias. The free layer (FL) on MgO is the sensing layer that responds to an external magnetic field, which can range from few mT to hundreds of mT. These sensors have TMR values up to 200%, resistance-area (RA) products from few hundred Ω μm² to several kΩ μm², temperature coefficients from 500 ppm °C⁻¹ to few thousand ppm °C⁻¹, operation frequencies from d.c. to hundreds of MHz, and detectivities of a few hundred pT in d.c. (ref. [62]). Hybrid architectures (for example, magnetic flux guides) can achieve detectivities around 10–20 pT at 10 Hz, and below 1 pT under white noise[63]. For applications, the MTJ sensor needs to be integrated in a Wheatstone bridge, to ensure a null output in the absence of external excitation. Figure 2 shows an example of a TMR-based probe system that can detect defects in metal surfaces (non-destructive testing (NDT)).

In the automotive industry, magnetic sensors are used in anti-lock braking systems (ABS), drive by wire, engine management, and electronic stability programs (ESP). Although devices

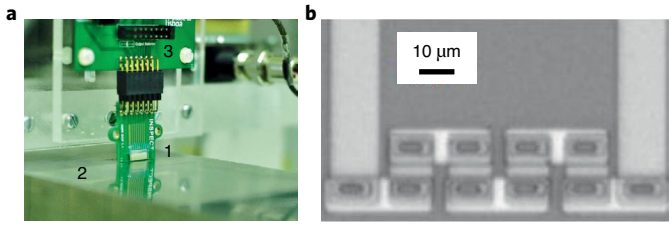

Fig. 2 | Magnetic sensors. a, Magnetoresistive sensor based multichannel scanning head for non-destructive testing of defects in metal parts. 1, the multichannel MR sensor mounted on a PCB holder including an excitation current line; 2, the test metal mock-up; 3, the discrete electronics for MR signal amplification and excitation current line drive. **b**, MTJ sensor array (10 MTJ sensors in series) used as MR sensor in one of the channels of the multichannel scanning head for surface defect detection. Credit: **a**, INESC ID, INESC MN, and IST; **b**, INESC MN, and INL.

based on Hall effects are still dominant today, magnetoresistive sensors based on GMR, and recently TMR, are becoming more popular because of their higher accuracy and sensitivity, which are required for advanced driver assistance systems and autonomous driving solutions. For these high-volume applications, TMR sensors can be monolithically integrated onto CMOS (as in MRAM). In a broader industrial environment (industry 4.0), spintronic sensors are being used in a variety of applications, such as low-volume, highly specialized measurement systems (scanners), as well as medium-volume, standard applications (linear or angular encoders, and electrical current sensors). Today, AMR and GMR sensors for industrial application provide high resolution and robustness in adverse conditions in comparison to competing optical or Hall effect based encoders. TMR devices have advantages in resolution, temperature and lifetime drift. In terms of packaging, the current standard in high-volume applications is to integrate magnetoresistive sensors with signal conditioning and higher-level electronics in discrete packages on printed circuit boards (PCBs). For medium-volume scenarios, the sensors can be integrated with application specific integrated circuits (ASICs) side-by-side.

Magnetoresistive sensors (mostly GMR-based) can also be used for protein or DNA recognition in emerging biomedical applications, such as spintronic biochip platforms where bioanalytes are labelled with magnetic nanoparticles[58–60]. Another type of magnetoresistance (MR)-based biochip is the integrated cytometer where labelled cells/bacteria are detected on the fly as they pass on microfluidic channels with incorporated MR sensors[58–60].

Future challenges. Material optimization will, in the future, be required to improve the TMR values and thus the SNR of the magnetic sensor devices. In particular, improved control over material growth will be needed to achieve good lattice matching between the different active layers using standard substrates with appropriate buffers and industry-compatible sputter deposition methods. Perpendicular magnetized materials could also be used to improve the dynamic ranges of the sensors[64] or for integrated 3D magnetometers. Besides, new vortex-based sensors[65] based on topologically protected magnetic states offer a high linear range compared to sensors based on single-domain states. Further research about the effect of magnetic properties (for example, easy axis dispersion and magnetization fluctuations) on $1/f$ noise, where f represents the frequency, is though still needed[66,67], since $1/f$ noise limits the sensor detectivity.

In the automotive market, developments will be needed to make vehicles cleaner, safer and smarter. In the near term, spintronic sensors can be of use in combustion engine control systems. However, their accuracy needs to be guaranteed over the vehicle's lifetime under demanding environmental conditions and at a competitive cost at the system level. In the longer term, the full electrification of vehicles and other transportation systems will increase the demand for magnetic sensors in all automotive applications. Higher sensor accuracy will be required to control the drivetrain or powertrain of hybrid or fully electrified vehicles, a task that is challenging because of magnetic disturbances originating from the electric motor and its periphery. Despite their high sensitivity and small size, spintronic sensors are not yet competitive compared to shunt sensors for electrical current measurements in such applications. As examples, challenging goals for open loop TMR sensors (that is, with no feedback) will be to reach below 0.1° accuracy over full 360° range for angular sensors, and 0.05% accuracy of full scale for electrical current sensors.

Radio-frequency and microwave devices

Besides the sensing, storing, and processing of information, information and communication technologies (ICT) require the transmitting of data. Common wireless communication systems operate in the GHz range, where major markets are IoT (with bands in the 0.3–5.5 GHz range) and public mobile networks (2G–4G; using bands in the 0.7–3 GHz range). For fifth-generation (5G) networks and beyond, very high frequencies (on the order of hundreds of GHz towards THz) will be needed[68]. As a result, the typical components for wireless communication (antennas, amplifiers, filters, delay lines, mixers, modulators, demodulators, and frequency synthesizers) will have to be adapted to new frequency bands and communication protocols. In addition, energy-efficient, compact and low-cost components will have to be developed to address the energy requirements of the IoT.

RF spintronics device configurations. Spintronics radio-frequency (RF) technologies make use of two basic device classes: MTJ nanopillars exploiting the spin momentum transfer from a spin-polarized charge current[14,15,69,70] (Fig. 3a), and 2D bilayer structures (Fig. 3b,c) exploiting the inter-conversion between charge and spin currents[71–73] or the propagation of magnetic excitations (spin-waves or magnons). From these device classes, different RF functionalities can be realized (Fig. 3d–g) that result from the combination of the oscillatory precession of magnetic moments due to spin torques and magnetoresistance phenomena. The two basic functionalities are the d.c. to RF conversion for RF signal generation (Fig. 3d) and RF to d.c. conversion for RF signal detection (Fig. 3e). Adding additional time varying control signals $i(t)$ (Fig. 3d), it is also possible to modulate (Fig. 3f) and to sweep (Fig. 3g) the oscillator frequency on short time scales[74–77].

RF signal generation for wireless communication. The nanoscale size of MTJ nanopillars (Fig. 3a), combined with the frequency tuning (Fig. 3d) makes the d.c.-to-RF conversion of interest for implementation in broadband transmitter (Tx)–receiver (Rx) radio links[69]. In addition, for MTJ nanopillars (typical diameters of 50–500 nm; Fig. 3a) different complementary frequency ranges can be easily achieved by adjusting the device configuration: 0.1–1 GHz using vortex MTJs[70] and 1–20 GHz with quasi-uniform magnetized MTJs[69,74,78]. Using these configurations, system level phase-locked loops[70] (PLL) were developed in a hybrid CMOS/PCB technology, demonstrating the capability of frequency synthesis at reduced phase noise (−90 dBm; Fig. 3c). Future work will use advanced designs and concepts to improve the phase noise and to demonstrate frequency shift keying protocols at data rates close to the PLL bandwidth (1–10 MHz).

For data rates above 100 Mbs (ref. [74]), spintronic devices offer compact solutions for amplitude[78], frequency[74] and phase shift keying[75] (respectively ASK, FSK, PSK) protocols that are of interest for communication within sensor networks for the 1–10 m range.

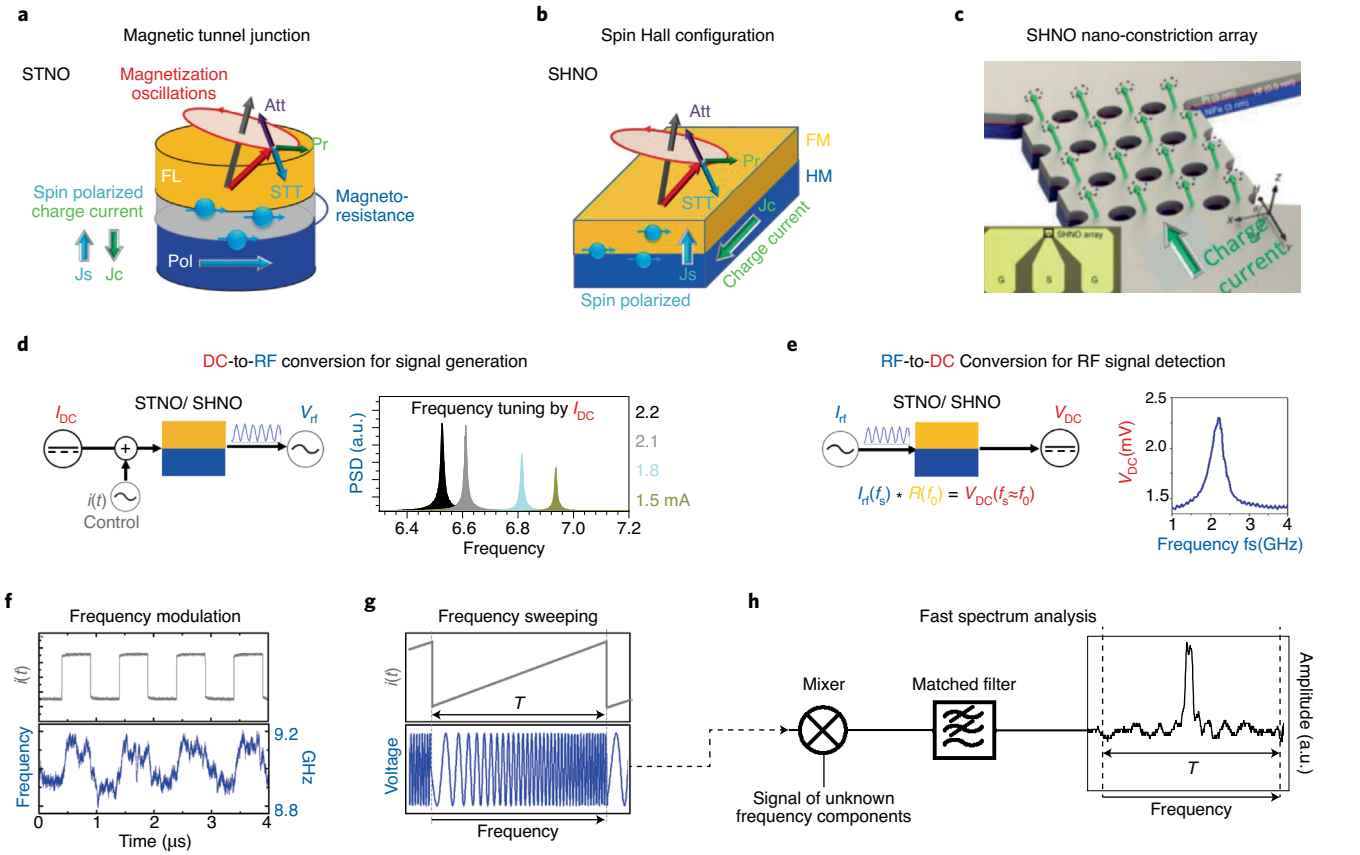

Fig. 3 | Radiofrequency and microwaves devices. a–**c**, Illustration of basic RF spintronics device configurations. **a**, Magnetic tunnel junction nanopillars, also called spin-torque nano-oscillators (STNO). A charge current J_c is spin polarized by the polarizer Pol and transfers a spin-torque (STT) to the magnetization of the free layer FL. J_s is the spin current. In case of a d.c. current I_{DC}, the compensation of the damping torque (Att) by the STT will lead to steady state magnetization oscillations whose frequency is determined by the precession torque (Pr). The magnetoresistance converts the oscillations into a voltage signal. **b**, Two dimensional ferromagnetic/heavy-metal (FM/HM) spin Hall bilayer structure, also called Spin Hall nano-oscillator (SHNO). A charge current J_c within HM leads to an upward directed spin current that can transfer spintorque (STT) to the magnetization of the FM layer and set up steady state magnetization oscillations as in **a**, that can be detected via the anisotropic magneto-resistance. **c**, Typical device configuration for a SHNO where a constriction or an array of constrictions is contacted using a coplanar waveguide (see inset). Within an array of constrictions, the oscillations of different constriction areas (green arrows) can mutually synchronise. **d**,**e**, Illustration of the two basic RF functionalities. In **d**, the conversion of a d.c. current I_{DC} into an RF voltage signal V_{rf} can be used to generate RF or microwave signals, whose frequency is tuned via I_{DC}, as shown in the graph to the right by the power spectral density (PSD) of V_{rf} for four different values of I_{DC}. An additional time varying control signal $i(t)$ can be used to modulate the output signal frequency as explained in **f** and **g**. **e**, The conversion of an RF input signal I_{rf} into a d.c. voltage signal V_{DC} can be used for frequency-selective RF signal detection. The conversion is due to the rectification effect that leads to a DC component in the voltage when the frequency of the external signal f_s is equal to the frequency of the STNO or SHNO device f_o, as illustrated by the graph to the right. **f**, Digital modulation of the STNO or SHNO output frequency (lower panel) when the control signal $i(t)$ (upper panel) varies between two discrete signal levels. This can be used to implement frequency shift keying[74] or phase shift keying[75] protocols within wireless communication schemes. **g**, When the control signal $i(t)$ is linearly increasing (sawtooth signal of period T, upper panel), the frequency of the STNO or SHNO device is continuously increasing (or decreasing) where each point in time will correspond to a given frequency (lower panel). This can be used to develop ultra-fast spectrum analyzers[76] as illustrated in **h**. **h**, The frequency swept signal from **g** is mixed with a signal of unknown frequency components, that can vary in time. Passing the mixed signal through a matched filter will generate a peak at the point in time where the frequency of the STNO/SHNO device equals the one of the signal. Using vortex type STNOs, fast frequency detection was demonstrated for sweep times of 1 μs (ref. [77]), with prospect of reaching ultra-fast time scales of 1–10 ns. It was also demonstrated that fast changes in frequencies can be tracked. Credit: **a**,**b**,**d**–**h**: SPINTEC. Panel **c** adapted with permission from ref. [73], Springer Nature.

For ASK, FSK, modulation can be achieved without external mixers because of the non-linear coupling of amplitude and frequency (see Fig. 3f). Future efforts need to push the technology beyond TRL 3 by achieving: (1) a full integration within CMOS technology to demonstrate, for instance, RxTx modules, PSK communication and fast spectrum analysis (Fig. 3g,h) and (2) competitive performance by improving the signal stability (phase noise), the output power and achieving multifrequency operation. A major strategy towards these targets is the implementation of networks of mutually synchronized devices[79,80].

RF signal generation for neuromorphic computing. These networks of mutually synchronized MTJ devices can also provide novel solutions for neuromorphic computing[28]. Neuromorphic computing is inspired by the neurons of the brain, which form a network of coupled oscillators that can self-synchronize in frequency or phase. Initial experiments have demonstrated that a network of MTJ signal generators can be used to achieve recognition and classification operations based on the rich synchronization dynamics of the oscillators[28] (Fig. 4g). But much is still to be understood about the physics of networks of mutual synchronized oscillating MTJ nanodevices.

RF signal detection and power harvesting. RF to d.c. signal conversion in MTJ nanopillars can be used for signal detection (Fig. 3e). Spintronic detectors with DC output voltage levels in the μV to mV range have been demonstrated for input power levels as low as 60 dBm (ref. [81]), making them competitive with Schottky diodes, which have limited sensitivity at low input power levels. Furthermore, spintronic RF detectors are compact, frequency-selective, and can be operated in two modes: passive (without d.c. current bias and therefore with zero power consumption in the off-state) and active (under d.c. bias resulting in d.c. voltage levels that are 10–100 times higher than in the passive mode). These properties create a range of potential applications. For example, spintronic broadband microwave detectors have also been used as power harvesters to power nanodevices[82]. Alternatively, frequency filtering based on spintronic microwave detectors are proposed for ultra-low power and compact demodulators to be used within multi-frequency protocols in wireless sensor networks[83,84]. To push the technology beyond TRL 3, future efforts need to focus on integration with CMOS, increasing the conversion efficiencies for energy harvesting, improving the SNR for signal demodulation, and defining suitable multi-frequency protocols.

Planar Spin Hall architectures. The above-mentioned schemes rely mostly on the MTJ nanopillar configuration (Fig. 3a), while charge-to-spin current conversion due to spin–orbit interactions in 2D ferromagnetic/heavy-metal (FM/HM) bilayer systems (Fig. 3b) offer additional functionalities such as localized generation of spin waves. This property could potentially be used to develop filters and delay lines. On the other hand, signal generation in the GHz range, with well-defined steady state oscillations using single FM/HM nano-constrictions has recently been demonstrated[72]. Compared to nanopillar-based setups, this configuration has the advantages of easier nanofabrication and the possibility of synchronization of a large number of oscillators. For instance, an array of up to 8 × 8 synchronized nano-constrictions (see Fig. 3c) was used for microwave signal generation with narrow linewidth (60 kHz) and increased output power (linewidth scaling as $1/N$ and power as N^2 up to $N \approx 25$; N, number of synchronized oscillators)[73]. The future challenge will be to combine the FM/HM bilayer devices with MTJs to enable the efficient conversion of the magnetization dynamics into large electrical signals. This property will find application in novel schemes for microwave signal generators and neuromorphic computing, but also for electrically controlled spin-wave emitters for magnonics where spin-waves could be used for low-power information transport. Replacing the ferromagnetic material with insulating ferrimagnets or antiferromagnets could push the corresponding frequencies for emission and detection into the THz range[85] because of the strong exchange coupling between sublattices in these systems.

RF signal processing with spin-waves. Ferromagnetic insulating materials such as yttrium iron garnet (YIG)[86], which has the lowest damping of known materials, could be useful for the development of various RF components based on spin-waves (also called magnons). Magnons are elementary collective excitations of magnetic moments in magnetic materials that can be treated as quasiparticles and have recently been shown to be of potential use in the development of nanoelectronics[10,11]. Magnonics offer functionalities for RF applications that are currently unavailable in conventional electronic devices or devices based on surface acoustic waves (SAW), including reconfigurability, scalability down to sub-100-nm sizes, a wide operational frequency range from 1 GHz up to hundreds of THz, and nonlinearity. These properties are relevant to the ICT industry. In terms of applications, concepts of RF devices have been proposed, including reconfigurable filters (based on, for example, magnonic crystals), delay lines, phase shifters, frequency separators, Y-circulators and isolators, phase and amplitude multiplexers, wake-up receivers, spectrum analysers, power limiters, signal-to-noise enhancers, and wave front reversers[10,87,88]. Most of these concepts have only been investigated at a basic research level, TRL 2 to 3. One of the main challenges in developing magnonic technologies is the relatively low efficiency of the current converters of RF electric signals to spin waves and back. As a result, insertion losses for micron-scale devices do not yet meet industry standards.

Logic and non-Boolean devices

To switch a nanomagnet the energy required is of the order of 0.1 aJ, two to three orders of magnitude lower than the energy per bit required for computation using conventional CMOS devices. There is therefore strong interest in using the magnetic degrees of freedom for ultralow power nonvolatile logic circuits[89] (Table 2 summarizes the various approaches being investigated). However, spintronic logic and computation are still at a rather conceptual level, with only few demonstrations reported beyond TRL 3. Initial research has

Fig. 4 | Spintronic approaches for logic. a,**b**, Binary logic based on switching of nanometric magnetic structures. **a**, Scanning electron micrographs of a majority gate based on magnetic quantum-dot cellular automata using dipolar coupling between nanomagnets. The nanomagnets are either ferromagnetically (vertically) or antiferromagnetically (horizontally) coupled. The majority of the three horizontal input nanomagnets determines the direction of the output magnet in the centre of the device. **b**, Magneto-electric spin–orbit (MESO) logic combining a magnetoelectric capacitor to switch a nanomagnet (charge-to-spin conversion) with spin-to-charge conversion by the spin Hall effect. The devices can be cascaded by a charge-based interconnect to form circuits, as shown in the top figure. $I_{c(input)}$ and $I_{c(out)}$ are the charge currents, respectively, for input and output of each block. I_{supply} is the current injected for the power supply (that is, energy gain). The threshold function of the nanomagnet switching can be used for computation. On the left side of **b**, the operating mechanism for spin-to-charge conversion is presented: a high spin–orbit (SOC) material is used to generate a charge current (I_c) by injecting spins (I_s) from a ferromagnet (FM) via a spin injection layer (SIL). On the right side of **b**, the operating mechanism for a magnetoelectric (ME) material is presented. A ferromagnet (FM) is coupled via exchange/strain to the magnetoelectric material. The charge current I_c triggers the switch of the magnetization in the FM layer. H_{EB} and H_{EC} are the exchange bias and the exchange coupling from the magnetoelectric material to the ferromagnet, respectively, as a function of the voltage (V) and **m** is the magnetization of the ferromagnet. **c**, Photograph of a prototype of a three-input majority gate based on linear spin-wave superposition. Interference of spin waves with phases of 0 or π (logic 0 or 1) leads to a spin wave with the phase corresponding to the majority of the inputs. **d**, Scanning electron micrographs of a magnonic directional coupler superimposed with colour maps that represent the spin wave intensity measured by Brillouin Light Scattering. Depending on the frequency, the spin wave is routed into different outputs. Different directional couplers can be combined into logic circuits, such as magnonic half adders. **e**, Neuromorphic computing using nonlinear spin-torque nano-oscillators. Top panel: Schematic of the experimental setup including the nano-oscillator. A d.c. current (I_{DC}) and a rapidly varying waveform that encodes the input (V_{in}) are injected into the spin-torque nano-oscillator. The emitted V_{osc} (bottom panel) and its envelope $\tilde{V}$ can be used for tasks such as pattern recognition. **f**, Reservoir computing scheme using a magnetic skyrmion network as nonlinear magnetoresistive element. In both cases a portion of the material ($y \times x$, 250 nm × 500 nm) is simulated Top panel: contour plot of the magnetic configuration. The blue and red droplets correspond to Skyrmions. Bottom panel: Current profile. Figure adapted with permission from: **a**, ref. [94], AAAS; **b**, ref. [96], Springer Nature; **c**, ref. [104], APS; **d**, ref. [102]; **e**, ref. [28], Springer Nature **f**, ref. [114], APS.

focused on implementing the spin degrees of freedoms in analogues to conventional semiconductor devices[90]. Such devices, however, are based on dilute magnetic semiconductors with Curie temperatures below room temperature, which limits their practical potential.

Current status. Numerous spintronic concepts for digital Boolean logic have been reported based on spin currents[91,92], nanomagnets (Fig. 4a)[93–95], magneto-electric spin–orbit (MESO) logic (Fig. 4b)[96], exchange-driven magnetic logic (Fig. 4c)[95], domain walls,[97–99] skyrmions,[100] and spin waves (Fig. 4c,d)[101–104]. Spin currents can replace charge currents in logic switches and gates,[91,92] and information can be encoded in the polarization of the spin current. Decoupling spin currents from charge currents could potentially result in a large reduction of the energy dissipation. Materials with weak spin–orbit interaction, such as graphene, provide sufficiently long spin lifetimes at room temperature to make these devices practical[105], though an experimental demonstration of logic operation is still lacking.

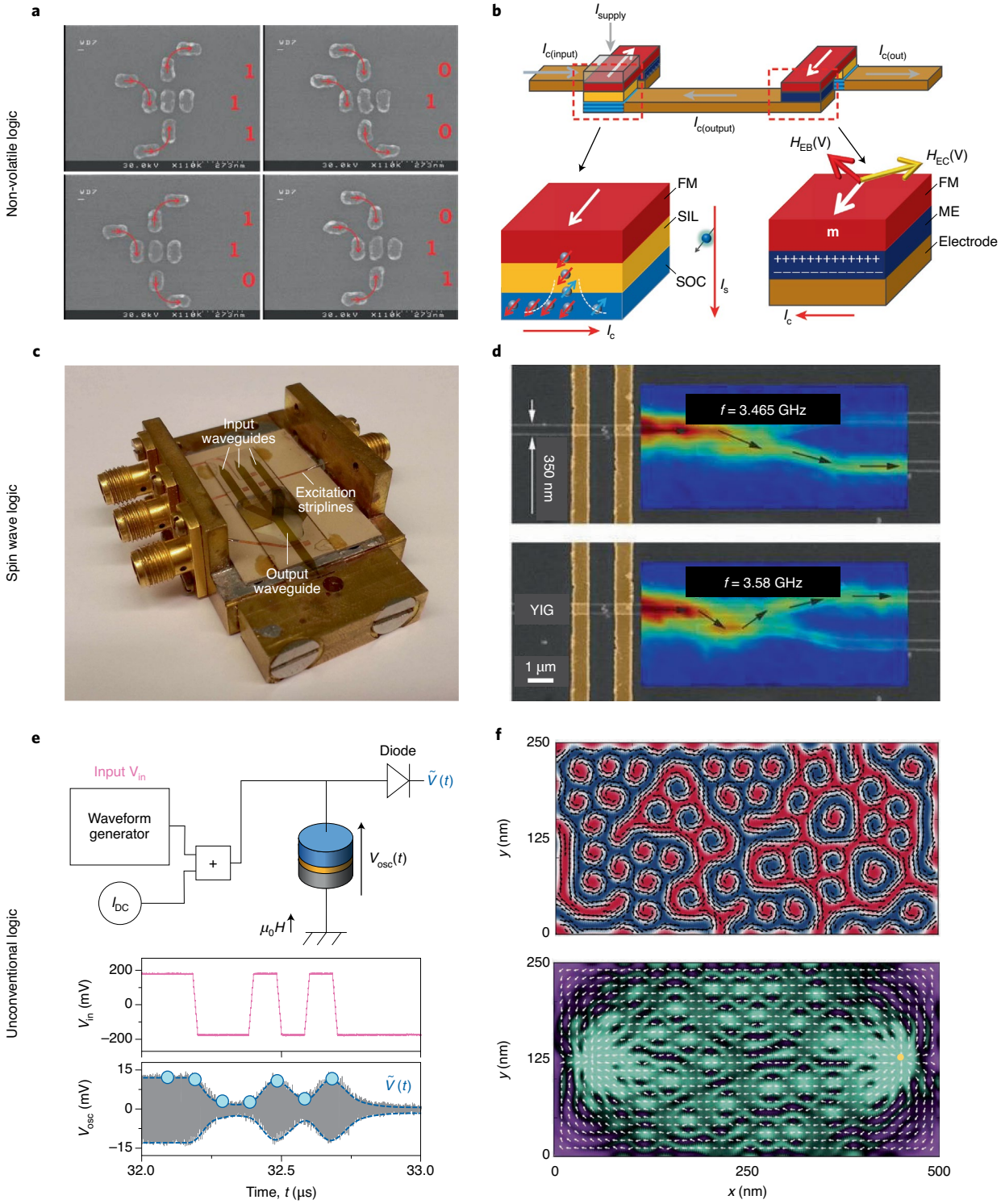

Table 2 | Different types of magnetic logic principles

	Reference(s)	Input/output state	Compute mechanism	State retention	Interconnect
Nanomagnet logic	93,94	Magnetization orientation	Dipolar interactions	Magnetization orientation	Magnetic
Magnonic logic	101–104	Amplitude and/or phase of spin wave	Interference, waveguiding, non-linear spin wave interactions	Volatile unless coupled with nanomagnet	Spin wave, electric, hybrid
Spin field-effect transistors	91	Magnetization orientation	Spin precession	Magnetization orientation	Spin current, electric, hybrid
Spin-based semiconductor logic	92	Magnetization orientation	Spin accumulation	Magnetization orientation	Electric
MESO logic	96	Magnetization orientation	Magnetoelectric and spin-orbit interactions	Magnetization orientation	Electric
Exchange-driven magnetic logic	95	Magnetization orientation	Exchange interaction	Magnetization orientation	Magnetic, electric, hybrid
Domain wall logic	97–99	Magnetization orientation	Domain wall motion and interaction	Magnetization orientation	Magnetic
Skyrmion logic	100	Skyrmion chirality	Skyrmion interaction	Skyrmion chirality	Magnetic, electric, hybrid

Several other concepts are based on encoding information in the magnetization state of a nanomagnet, providing a pathway to nonvolatile logic[93–95]. Computation can then be achieved using spin currents[92], or dipolar[93,95] or exchange[95] coupling between nanomagnets. While robust room-temperature operation has been demonstrated, the scalability as well as the energy-delay product of these approaches still need to be assessed on a circuit level. Recently, a nanomagnetic logic concept based on magnetoelectric control of a nanomagnet in combination with a readout scheme using the inverse spin–orbit effect was proposed[96] (Fig. 4b). This concept promises ultralow power operation of circuits if the magnetoelectric coupling and the inverse spin-Hall effect are sufficiently large. However, the experimental demonstration of such a device is still lacking. Domain wall logic is a related concept that replaces individual nanomagnets by domains in extended ferromagnetic conduits[98], similar to the magnetic racetrack memory concept[56,106]. Here, the main challenge is the control of and fast domain wall propagation in nanoscale magnetic conduits at low power.

Magnonics offers a different approach to spintronic logic and uses the amplitude or phase of spin waves to encode information[10]. Spin waves can have wavelengths down to the nm range and frequencies from GHz to THz, which makes them interesting for nanoscale fast logic technologies. In particular, spin wave interference can be used for computation via the construction of majority gates[101]. Recently, a prototype of such spin wave majority gate has been experimentally demonstrated (Fig. 4c)[104,107]. While spin waves are intrinsically low power, the lack of energy-efficient converters from spin waves to electric current and vice versa limits the implementation of such concepts. All-magnon data processing using directional couplers requires a smaller number of converters, but relies on non-linear magnonic effects[102,108]. Although integrated magnonic circuits[108] have been proposed, experimental demonstrations, as well as analysis at the circuit level, are still lacking.

Another important concept is the three-terminal device proposed by Supriyo Datta and Biswajit Das[91] and termed spin field-effect transistor (spin-FET)[109]. Spin-FETs are composed of two ferromagnetic contacts which act as a polarizer and analyser (or, spin-polarized source and drain) and are separated by a gated semiconductor channel. Because of the non-zero spin–orbit interaction, the spin polarization at the drain is controlled by the voltage applied to the gate. As a result, electrons with their spin aligned to the drain magnetization have higher probability to leave the channel than those with their spin anti-aligned, thus realizing an on/off functionality[91,109]. This device was initially predicted to have a faster and more efficient operation than conventional FETs with additional advantages, such as nonvolatility and lower heat losses. Though a large number of material combinations have been tested[105,110], this concept has not shown efficient room temperature operation. A key limitation is that the spin splitting of the electrochemical potential in the semiconductor due to injected spin currents is rather small and therefore logic signal levels at the ferromagnetic output contact are well below levels of about 50 to 100 mV required for robust electronic circuits[109]. A notable breakthrough has though been achieved with the development of an all-electric and all-semiconductor spin-FET with two quantum point contacts as spin injectors and detectors (at low temperature)[111].

Beyond Boolean logic, spintronics could be used to explore unconventional computing schemes. The integration of analogue-like low-power computation and memory devices (nonvolatile memory or memory with adapted retention), could be relevant for neuromorphic computation using spin waves[112], spin-torque oscillators (Fig. 4e)[28] and MTJ-based memristors[29]. Recently, reservoir computing schemes—a machine-learning scheme based on large non-linear dynamical systems (Fig. 4f)—have been introduced. In such a system, the input signals are mapped into the dynamical system (the reservoir) and the resulting developing pattern is analysed to provide the output signal without the need to train the reservoir itself[113]. Spintronic-based reservoir computing proposals are based on skyrmion networks[114] or spin-torque oscillators.[28]

Future challenges. Most spintronic concepts described here are fundamental building blocks of logic circuits that are equivalent to conventional electronics components or logic gates. For practical computing applications, such fundamental building blocks need to fulfil a set of criteria, including cascading, fan-out, logic level restoration, immunity to noise and losses, and input–output isolation. Only few concepts currently fulfil all these criteria[96] and can thus be used to design more complex logic circuits. Moreover, there is currently no concept for a full spintronic computer, which incorporates logic and memory, and interconnects using exclusively magnetic signals without the need for intermediate conversion to charge signals.

A potential solution would be a hybrid system that combines spintronic subsystems with CMOS electronics, where signal interconversion takes place. The overall performance of such a system, in terms of energy consumption and computing throughput, will depend on the conversion mechanisms and the number

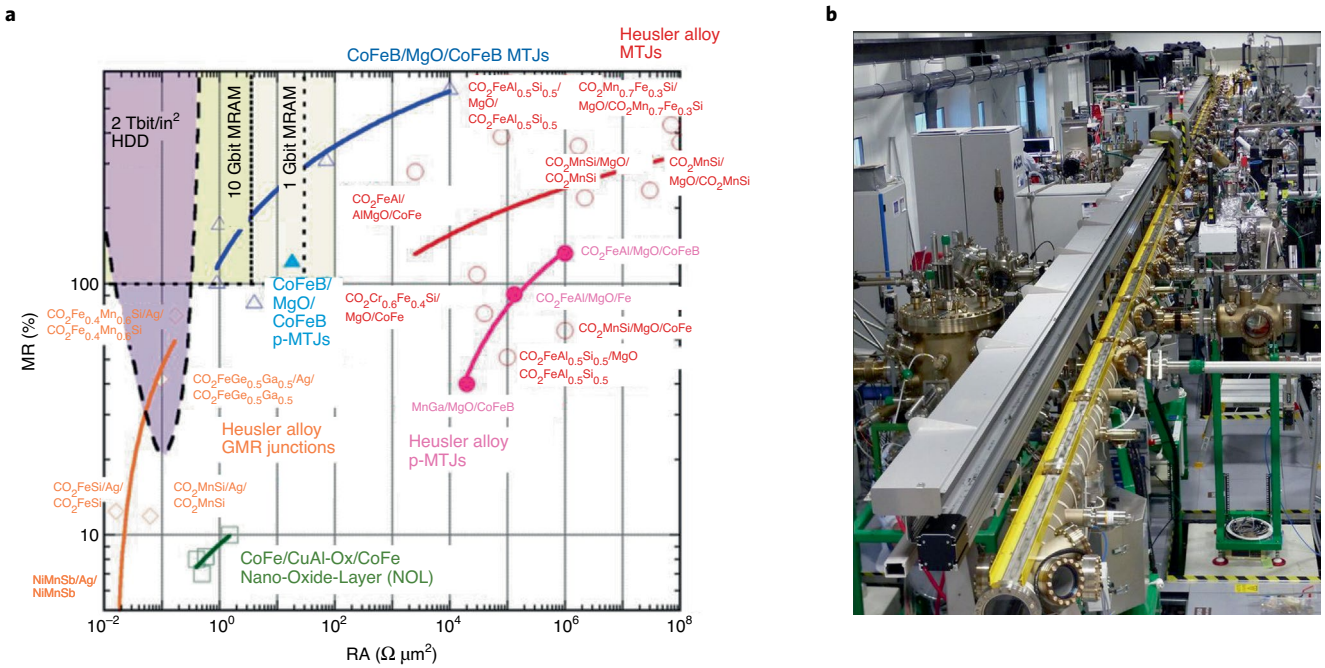

Fig. 5 | Spintronics materials. a, Relationship between magnetoresistance (MR) and resistance-area product (RA) for various series of junctions. The target requirements for the next-generation storage and memory is also indicated in the figure: 2 Tbit in^{-2} for hard disk drive (HDD) read heads, 1 and 10 Gbit for magnetic random-access memory (MRAM). **b**, Tube Daμm: 30 pieces of equipment for growth and characterization are connected under ultra-high vacuum along a 70 meter long tube at Institut Jean Lamour (Université de Lorraine-France). Figure adapted with permission from: **a**, ref. [123], PMID; **b**, Institut Jean Lamour.

of interconversions needed to perform the computation. Various physical phenomena, including magnetoresistance, STT or SOT, spin-Hall-effect, and inductive conversion can be used. However, their energy conversion efficiencies in nanoscale devices are rather low and severely reduce the computing throughput. Moreover, the energy consumed in the CMOS interfaces typically outweighs the energy savings from using a magnetic subsystem, increasing the total energy consumption of the hybrid circuit. The MESO approach, in which electric fields couple to magnetization via strain or other mechanisms, promises a potential solution with much higher energy efficiency and output signal[89,96,115]. Larger effect amplitudes and the scalability of the approach to the nm–GHz range are key challenges for practical implementations of such concepts.

Advanced materials, fabrication and tests

Progress in our four highlighted areas of application will require functional materials exhibiting high spin polarization, spin filtering, large spin–orbit coupling, high (perpendicular) magnetic anisotropy, and low magnetic damping[116,117]. Moreover, the implementation of novel approaches to manipulate the magnetic state of a device without magnetic fields[116–120] relies on the growth and characterization of materials with atomic precision, and on the fabrication of complex multilayered structures combining metallic, semiconductor, insulating, magnetic (ferro-, ferri- and antiferromagnetic) and non-magnetic materials.

Current status. Spintronic sensors and MRAM are based on interface and spin-filtering effects. Standard materials for MTJs are ferromagnetic transition metals (FM), their alloys and the insulator MgO (Fig. 5a). However, obtaining large magnetoresistance values and reliable switching as the MgO-barrier thickness scales down is challenging. The largest TMR at room temperature (604%) was actually reported for a CoFeB/MgO/CoFeB junction back in 2008[121]. In addition, the TMR amplitude in perpendicular MTJs is not sufficiently high for dense MRAM applications, and requires amplification at the reading stage, which results in penalties in terms of read speed, ancillary components, and space. Industry is therefore looking to replace MgO, even reverting back to using GMR for some applications (sensors, RF). Van der Waals heterostructures based on 2D materials have atomically thin interfaces and could potentially replace MgO. Few-layer graphene, in particular, has been predicted to act as a spin filter with low resistance[122]. Hexagonal boron nitride (hBN) has also shown potential in Co/hBN/Fe structures, achieving a TMR over 50% (ref. [122]). Another approach to increase the TMR involves the use of half-metallic ferromagnets, for example, Heusler alloys, perovskites, rutiles, ferrites and dilute magnetic semiconductors. Heusler alloys, in particular, have demonstrated 100% spin polarization at room temperature[123]. Their crystallization temperature has been recently reduced from >400 °C down to <235 °C (ref. [124]), allowing their use in spintronic devices because interfacial mixing during fabrication is avoided.

To enhance the writing efficiency of STT-MRAM and decrease its energy consumption, PMA can be introduced. Graphene can further enhance the PMA in FMs such as Co (ref. [125]). An alternative write approach is to use the spin Hall effect or the inverse spin-galvanic effect in materials with large spin–orbit coupling. In particular, the charge-spin conversion in topological insulators (TI) has been used for SOT switching in FM/TI bilayers[126]. For devices with PMA, the symmetry of SOT can be engineered by introducing materials with low crystalline symmetry, as reported for transition-metal dichalcogenides (TMDC)/FM bilayers[127].

Heterostructures combining magnetic effects such as the Dzyaloshinskii–Moriya interaction (DMI) with magnetic 2D materials have shown remarkably large magnetoresistances, albeit at low temperature[128,129]. In particular, a record TMR amplitude of 19,000% has been achieved in spin-filter van der Waals heterostructures[130]. In terms of spin-based computing, graphene can transfer spin information over tens of micrometres for spin-interconnects or

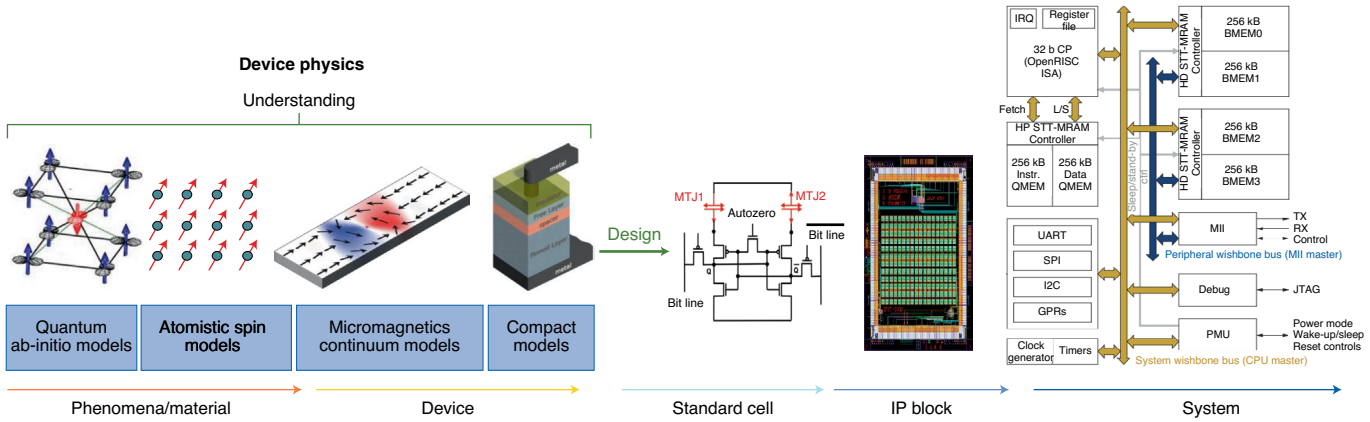

Fig. 6 | Modelling approaches used in spintronics. Various steps which must be covered from basic understanding of spintronic phenomena to system design. On the left are the tools specific to spintronics developments (phenomena, material and device levels). These tools are intended on one hand to better understand the device physics and thereby guide the device optimization and on the other hand, provide the inputs for the higher levels of design (standard cell, IP block and system). The tools used at the higher levels of design are standard in microelectronic design flow. JTAG, Joint Test Action Group (industry standard for verifying designs and testing printed circuit boards after manufacture); BMEM, bus memory reference (a signal issued among devices for memory access); CPU, central processing unit; IRQ, interrupt request; HP, high power; L/S, load/store (memory instructions); I2C, inter-integrated circuit (a synchronous, multi-master, multi-slave, packet switched, single-ended, serial communication bus); UART, universal asynchronous receiver–transmitter (a computer hardware device for asynchronous serial communication); GPRs, general purpose registers; SPI, serial peripheral interface; PMU, power management unit; MII, media-independent interface.

reprogrammable magneto-logics[116]. Combining TMDCs with graphene can be used for room-temperature spin filters and switches[131–133]. Magnetic proximity effects in graphene from magnetic EuS and yttrium iron garnet (YIG) have also been observed[134] and are promising for spin generation.

It is also worth noting that crystalline spintronic materials, such as garnets, can be integrated with silicon CMOS using epitaxy or wafer bonding in order to achieve nonreciprocal CMOS photonics[135] and high-frequency signal processing[136].

Future challenges. Improvements in scaling, sensitivity and SNR are needed for sensor and memory applications. A specific target is the fabrication of 10 Gbit MRAM (Fig. 5a)[123] but several challenges must be addressed. Current MTJ stacks are complex and relatively thick (around 20 nm), hindering the ion-beam etching process and setting a lower limit for the memory-cell pitch. For energy-efficient SOT writing, improved spin-charge interconversion is needed; for STT writing, reduced switching currents and larger TMR are needed. A crucial challenge is engineering the interface properties, for example, between new FMs and insulators, between TIs and FMs, and between 2D materials.

To move to high TRLs, high-quality nanostructured materials must be obtained on large surfaces. Common spintronic materials such as Co and Cu are already used in microelectronics, simplifying their integration. In contrast, embedding Heusler alloys, TIs or 2D materials into spintronic technologies requires the development of large-scale production tools, in order to transfer or directly grow these materials onto 300 mm wafers. Specific tools for growing of complex spintronics heterostructures have though been assembled (Fig. 5b).

For testing and characterization, tools and facilities must be developed to collect specific information associated with spintronic devices for large-volume production and quality control. These include techniques to assess the quality of tunnel barriers and device reliability.

Modelling and design

Fundamental models aim to describe the interplay between structural, magnetic, and electron transport properties in order to predict device performance. At the technological level, these models support the optimization of devices against industrial specifications and provide tools for circuit designers.

Current status. The design of spintronic devices is a multiscale problem (Fig. 6); there is no single model capable of describing all underlying physical processes at all spatial and temporal scales. Instead, an ensemble of complementary theories and models operating at different levels are used.

Starting from the atomic scale, quantum-mechanical ab-initio models using density functional theory[92] have been very successful at, for example, predicting intrinsic magnetic properties central to spintronic functionalities. Together with the non-equilibrium Green's function formalism, they are able to predict the transport properties of complex structures. However, these calculations remain idealized and lack many important features significantly influencing spintronic applications, including defects, finite temperature, and realistic magnetization dynamics.

Finite size effects and disorder require discrete classical spin models[137]. These models correctly describe thermal spin waves and can account for local disorder. They are used to study dynamical magnetic properties in different systems. Coupled to spin transport models, they are suitable for calculating spin currents and spin accumulation at interfaces at the nanometre scale, and the dynamic response of the magnetic material, in particular, the switching time in STT-MRAM[138].

Micrometre scale objects can be studied by micromagnetics[139], a mesoscopic theory that has proven helpful because it can reproduce experimental data quantitatively. It is based on the Landau–Lifshitz–Gilbert equation for the magnetization dynamics, and can include phenomena such as spin-transfer, and spin–orbit or Rashba torques. These additional terms introduce unknown parameters, which are sometimes measured experimentally, or calculated by ab-initio models. A more appropriate description for temperature effects is based on the Landau–Lifshitz– Bloch equation[140].

Finally, designing hybrid CMOS/magnetic logic circuits requires integrating the magnetic devices into the standard design suites of microelectronics. Consequently, compact models of magnetic devices have been developed[141,142]. Here, the physical behaviour of

the device can be described by an electrical equivalent circuit with operational characteristics that are integrated with the appropriate electrical simulator. Compact models of MTJs are widely used. Some compute the magnetization dynamics[143], giving high accuracy and particular suitability for analogue functionalities, such as sensing or RF communication. Others consider MTJs as bi-stable magnetization states and calculate switching times triggered by current pulses[144]. This much faster approach allows the simulation of larger circuits, such as memory arrays.

Future challenges. Despite continuous advances in modelling, key aspects need to be accelerated to match the fast progress of experiments and to meet industrial demands. First, because no single model can describe all physical effects in a complete picture, a hierarchical, multi-scale description is required[143]. In such an approach, atomistic on-site parameters (anisotropy, exchange, Dzyaloshinkii–Moriya interactions) are evaluated with ab-initio theories. Atomistic models then evaluate the temperature dependence of macroscopic parameters, which serve as input for large-scale micromagnetic simulations. This atomistic/micromagnetic interface should be thoroughly investigated, including proper characterization of cell-size effects. Finally, micromagnetic simulations are used to test the accuracy of compact models.

A second target is improving the current models. In particular, ab-initio models need to move towards larger-scale simulations with thousands of atoms and novel approaches beyond the local density approximation, also considering disordered magnetic states at finite temperatures. With respect to discrete atomistic spin models, the main challenge is to introduce quantum effects and correlations in the classical description. The development of mesoscopic approaches, such as micromagnetics, must include coupling to other models of physical phenomena that affect magnetization. For example, a model coupling both charge and spin transport self-consistently with magnetization dynamics is required[144,145]. Indeed, spin-currents are often inhomogeneous in spintronics devices[146,147] and consequently exert a non-uniform influence on the magnetization dynamics. Finally, the integration of compact and efficient electrical circuit models of spintronic devices into the standard design suites of CMOS-integrated electronics using a process design kit (PDK) is essential.

In addition, models need to be developed to describe new phenomena that have been observed experimentally. We highlight five key examples here. First, ultrafast all-optical switching[148], where dynamic magnetization processes are triggered by ultrafast laser excitation; this involves complex interactions of various subsystems (electrons, phonons, magnons) with the laser pulse. Second, terahertz spintronics[32], where interaction of the THz electric pulse with a magnetic medium efficiently excites magnetization dynamics and is far from understood. Third, spin caloritronics[25], which requires models to describe the interplay between heat, charge and spin currents. Fourth, electric field switching[149], which requires models capable of predicting the complicated dynamical influence of electric fields on ferromagnets. Finally, antiferromagnetic spintronics[150], which requires a large-scale model description for simulation of nanodevices, something that is only at an early stage of development.

A common strategic view is to work towards the standardization of modelling approaches. For instance, compact models can be associated with a 'model card', which provides the technology parameters and their typical variations. The next step will be to evolve the cards along with developing technology, possibly using automatic characterization tools and fitting algorithms. This process is expected, similarly to that developed by the Compact Model Coalition for CMOS electronics, to boost interconnectivity among different sources, and to increase the efficiency of feedback between industrial modelling and device design.

Conclusions

Spintronics has the potential to play a major role in the future of the microelectronics industry, and we have highlighted here four key areas of impact, which are associated with medium-term technological developments.

MRAMs have a proven potential to replace existing memory technologies for applications where a combination of nonvolatility, speed and endurance is key. STT-MRAM is a high density and scalable technology that is well suited to high performance computing applications at the last level caches. STT-MRAM may not be suitable for faster caches, for which SOT-RAM could be a solution. Electric field control of the magnetization, possibly in combination with spin–charge interconversion, as well as optical switching of the magnetization, could extend the range of spintronic memories beyond CMOS technologies.

Magnetoresistive-based sensing is increasingly being used in applications where high output and SNR, good thermal stability, compatibility with CMOS integration, low cost and small footprints ($< 1\ mm^2$) are required. With the transition to electric vehicles, the increasing use of renewable energy sources, and the development of industry 4.0 and IoT concepts, the need for smarter and more advanced magnetic sensors is expected to grow.

RF spintronics is reaching maturity, in terms of materials, nanofabrication, and control of the dynamical modes. CMOS-integrated demonstrations are expected in the next three-to-five years.

Spintronic logic is promising for ultra-low-power electronics due to the low intrinsic energy needed to manipulate nanomagnets and magnetic excitations such as magnons at the nanoscale. A large number of different logic concepts have been proposed, but currently very few of them can be used for complex circuits. Hybrid systems combining spintronics and CMOS are required to validate these concepts at system level and benchmark them against traditional CMOS approaches.

As has been the case for the industrialization of devices based on GMR, TMR, and STT, progress is achieved by developing novel materials, functional heterostructures, and device architectures. Simulations tools that bridge the gap between the atomistic, device, and system levels could significantly speed up the translation of basic research into microelectronic technologies.

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Author contributions

B.D. and P.B. have coordinated the writing of this review. I.L.P., K.G. and P.G. wrote the section "Magnetic memories". P.F., R.L. and W.R. wrote the section "Magnetic sensors"; U.E., S.O.D., J.A., P.B. and A.D. wrote the section "Radio-frequency and microwave devices". P.P., C.A., A.A. and A.V.C. wrote the section "Logic and non-Boolean devices". A.H., S.M., S.V. and M.C.O. wrote the section "Advanced materials, fabrication and tests". M.d'A., G.P., G.F., L.L.D., R.C. and O.C.F. wrote the section "Modelling and design".

Competing interests

The authors declare no competing financial interests.

Additional information

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