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SUPPLEMENTARY INFORMATION

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Single-shot dynamics of spin–orbit torque and spin transfer torque switching in three-terminal magnetic tunnel junctions

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Supplementary Note 1. Figures of merit for SOT-MRAM devices

Commercial deployment of SOT switching in MRAMs relies on meeting requirements that are specific to a given technology (CMOS node, memory array size, associated cell design and peripheral electronics) and end-user application. SOT-MRAM applications are primarily oriented towards replacing high-performance and high-density SRAM (8T and 6T families) at register, L1 and L2 level in CPUs and GPUs. The overall performances should not be considered only at the single cell level, but also at the array size level, which includes the dissipation and capacitances of the access lines as well as the control and sensing periphery. Therefore, proper benchmarking of a memory technology requires compact device models built from experimental data, bit-cell design optimization, and system-design power-performance-area-cost analysis. This analysis goes beyond the scope of this work. Nonetheless, we can discuss relevant aspects at the device level, which include: size, operation speed, endurance, power consumption, and CMOS compatibility.

Cell size (cost). The main difficulty today is that the work carried out on design is still limited, compared, e.g., to STT-MRAM. Preliminary analysis carried out at imec shows that standard SOT-MRAM designs are moderately competitive because of the too large number of controlling terminals. However, it is possible to reduce the number of terminals in an SOT bit cell by sharing some of them through smart designs, leading to a cell that can be 40% denser than SRAM cells. Below we compare cell size predictions for two different technology nodes based on imec's internal data:

- Node = 16 nm / 5 nm
- 8T-SRAM cell dimension: 0.1334 / 0.034 μm^2
- 6T-SRAM (1:3:3) cell dimension: 0.124 / 0.26775 μm^2
- SOT-MRAM simplest regular design: 0.162 / 0.028253 μm^2
- SOT-MRAM optimized high density design: 0.0324 / 0.0162 μm^2

Operation speed. The read and write latencies (including delay time in access lines) should be < 1 ns for the typical target applications. We demonstrate here that the writing latency is largely matched. The reading latency is mostly dependent on the TMR (target >150%), reading current, resistance area product (RA~10 $\Omega\mu m^2$), and cell design (capacitance of the read bit line).

Endurance. Typical specification values are > 10^{14} read/write cycles. This is an area where SOT has clearly an advantage over STT, particularly at high speed. Various studies showed already endurance being tested > 10^{12} without cell degradation.

Power consumption. Write energy < 100 fJ per bit, ideally 25 fJ/bit. In the present devices, we have already reached 400 fJ by SOT (see Fig. S1a and Fig. 2f in the main manuscript). Reducing the device size and improving the VCMA and/or the SOT efficiency can bring very substantial reductions of the write energy. Read energy ~ 10 fJ per bit. The read energy is directly linked to the minimum current detectable by the periphery sense amplifiers and stand-by power. For fast reading with 100-150% TMR, the typical read current should be ~50 µA in the low level state. Here SOT has a clear advantage over STT in that unintentional writing by the read current can be avoided. Further, compared to SRAM, the stand-by power of an SOT-MRAM is minimal.

CMOS compatibility. The compatibility with CMOS back-end-of-line processes is similar to STT-MRAM and already established[1]. Additionally, the size of the CMOS control transistors should be equal or smaller than the size of an SOT-MRAM cell in order to minimize footprint and be competitive with other technologies in terms of areal density. Therefore, a 3-terminal MTJ cell should match the power performances of a single CMOS transistor in terms of voltage and current delivery. Typically, a transistor in sub-28 nm nodes can deliver from 0.7 to 1.1 V and ~100 µA/fin. While the voltage is already within the specifications of the devices presented in this work, the writing current remains too large. Larger current values can be matched but would require more fins or larger planar transistors, increasing the cell size and cost.

Given the above, the main challenge in implementing commercial SOT-MRAMs lies in reducing the critical switching current while preserving the device functionality and speed. Strategies that allow for a reduction of

the critical current are presented below.

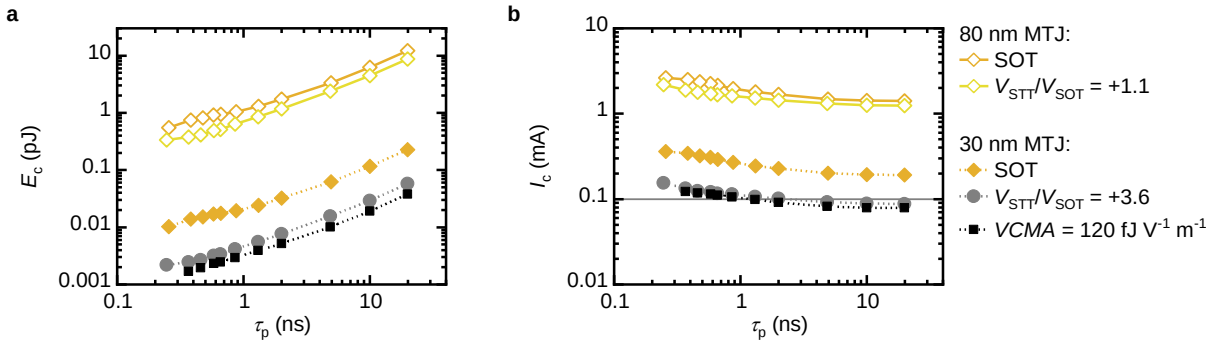
The most straightforward approach is *downscaling*. Assuming a constant critical current density, an MTJ with a diameter of 30 nm placed on top of a 30 nm wide SOT-line would allow a critical current reduction from about 2 mA to 300 µA for 0.5 ns long pulses for SOT alone, that is, more than 80% with respect to the MTJs with 80 nm diameter and 220 nm wide SOT-line studied in this work (Fig. S1b, orange diamonds).

A second approach is to increase the *STT bias*. In this work, the bias range was restricted to $V_{\mathrm{STT}}/V_{\mathrm{SOT}} \leq +1.1$, which results in a decrease of the critical current of about 20% (Fig. S1b, open yellow diamonds). A stronger STT bias would lead to an even larger reduction of the critical current. Above a certain limit, the STT bias would lead to the emergence of STT-dominated field-free switching[2], which is observed around $V_{\mathrm{STT}}/V_{\mathrm{SOT}} = +4$ in our devices. At this point, however, the advantages of SOT-switching in terms of speed and endurance would be likely lost. For the scaled device, we estimate that a ratio of $V_{\mathrm{STT}}/V_{\mathrm{SOT}} = +3.6$ would be sufficient to reduce the critical current below 100 µA in the SOT-dominated regime (Fig. S1b, gray circles).

The third approach is to exploit the *VCMA effect*. Here we distinguish this effect from STT by averaging the critical current for P-AP and AP-P switching (see main text), which allows us to obtain the reduction of critical parameters due to VCMA alone. Based on our measurements (see, e.g., Fig. 5e), we estimate that the critical current would scale as $I_{\mathrm{c}} = I_{\mathrm{c0}} \times 45/(VCMA\ [\mathrm{fJ\ V^{-1}\ m^{-1}}])$, where I_{c0} is the critical current at zero bias. Therefore, a VCMA coefficient of 120 fJ V^{-1} m^{-1} would be sufficient to achieve a critical current of 100 µA in the scaled device at 1 ns (Fig. S1b, black squares). Note that typical VCMA values reported in MgO-based MTJs reach up to 400 fJ V^{-1} m^{-1} (Refs. 3,4).

The fourth possibility is to increase the *SOT efficiency*, i.e., the effective spin Hall angle of the SOT line. In our devices, the SOT efficieny is about -0.32. Recent work has demonstrated values of 1 and above in transition-metal alloys, topological insulators, and oxide interfaces[4]. The critical current density is supposed to scale linearly with the SOT efficiency. However, further work needs to be done in order to assess the compatibility of these systems with device requirements (e.g., perpendicular magnetic anisotropy) and compatibility with CMOS and back-end-of-line processes.

We emphasize that measurements on real devices are needed in order to validate the strategies and extrapolations presented above. In particular when reducing the MTJ size, several factors can play a role in either decreasing the critical current (geometry, thermal stability, Oersted field) or increasing it (heat dissipation, transition to macrospin behavior). Notably, the flexibility of SOT enables to test and combine different strategies in order to meet the specifications for different memory classes.



Supplementary Figure S1 | Comparison of the critical switching energy and current in different conditions. a, Critical energy E_{c} and **b**, Critical current I_{c} as a function of τ_{p}. Open symbols correspond to P-AP reversal measured with $\mu_0 H_x$ = -23 mT for SOT switching (orange) and switching with $V_{\mathrm{STT}}/V_{\mathrm{SOT}} = +1.1$ (yellow). The full symbols represent an extrapolation of the experimental data to an MTJ with a diameter of 30 nm under various experimental conditions: pure SOT switching (orange diamonds), STT bias $V_{\mathrm{STT}}/V_{\mathrm{SOT}} = +3.6$ (gray circles), and VCMA of 120 fJ V^{-1} m^{-1} at $V_{\mathrm{STT}}/V_{\mathrm{SOT}} = +1.1$ (black squares). The 100 µA current limit is shown as a gray line in **b**.

Supplementary Note 2. Relationship between VCMA and critical switching voltage

The VCMA effect was recently measured in MTJs[5] and results in an electric field dependent free layer effective anisotropy field ($H_{\mathrm{K,eff}}$), characterized by the VCMA coefficient

$$VCMA = \frac{\mu_0 M_S t}{2} \frac{\partial H_{\mathrm{K,eff}}}{\partial E}, \tag{1}$$

where μ_0 is the permeability of vacuum, M_S the free layer saturation magnetization, t the free layer thickness, and E the applied electric field.

In general, the effective anisotropy field at a given E can be linearized as

$$H_{\mathrm{K,eff}}(E) = H_{\mathrm{K,eff}}(0) + \frac{\partial H_{\mathrm{K,eff}}}{\partial E} E. \tag{2}$$

Due to the large resistance area product of the MgO layer with respect to the other metallic layers, we have $E \approx V_{\mathrm{STT}}/t_{\mathrm{MgO}}$, where t_{MgO} is the thickness of the MgO barrier. We can thus write

$$H_{\mathrm{K,eff}}(V_{\mathrm{STT}}) = H_{\mathrm{K,eff}}(0\ \mathrm{V}) + \frac{\partial H_{\mathrm{K,eff}}}{\partial E} \frac{V_{\mathrm{STT}}}{t_{\mathrm{MgO}}}. \tag{3}$$

By combining (1) and (3) we have

$$VCMA = \frac{\mu_0 M_S t}{2} \frac{t_{\mathrm{MgO}}}{V_{\mathrm{STT}}} \left(\frac{H_{\mathrm{K,eff}}(V_{\mathrm{STT}})}{H_{\mathrm{K,eff}}(0)} - 1 \right) H_{\mathrm{K,eff}}(0). \tag{4}$$

Assuming that the critical voltage is proportional to the effective anisotropy field of the free layer,

$$V_c \propto \frac{e \mu_0 M_S t}{\hbar \theta_{\mathrm{SHE}}} H_{\mathrm{K,eff}}, \tag{5}$$

where e is the charge of the electron, μ_0 the magnetic permeability of vacuum, $\hbar$ the reduced Planck constant, and θ_{SHE} the effective spin Hall angle of the W layer. Thus, assuming that the changes of the average of the normalized critical voltage are due to the VCMA effect, we have:

$$\bar{v}_c(V_{\mathrm{STT}}) = \frac{V_c(V_{\mathrm{STT}})}{V_c(V_{\mathrm{STT}} = 0)} = \frac{H_{\mathrm{K,eff}}(V_{\mathrm{STT}})}{H_{\mathrm{K,eff}}(V_{\mathrm{STT}} = 0)}. \tag{6}$$

From (4) and (6) we get

$$VCMA = \frac{\mu_0\ M_S\ t\ t_{\mathrm{MgO}}\ H_{\mathrm{K,eff}}(0)}{2} \frac{\bar{v}_c(V_{\mathrm{STT}}) - 1}{V_{\mathrm{STT}}}. \tag{7}$$

From the characterization of our sample we have $M_S = 900 \times 10^3 \mathrm{A\ m^{-1}}$, $t = 1$ nm, $H_{\mathrm{K,eff}}(0) = 2.78 \times 10^5 \mathrm{A\ m^{-1}}$, and $t_{\mathrm{MgO}} = 1$ nm. For $V_{\mathrm{STT}} = 550$ mV, we have $\bar{v}_c(V_{\mathrm{STT}}) = 0.8$, which gives a VCMA coefficient of 57 fJ $\mathrm{V^{-1}m^{-1}}$, in agreement with literature values[4,8].

Supplementary Note 3. All possible combinations of SOT, STT, and VCMA for 3-terminal MTJ switching

SOT switching up to down				STT switching		SOT and STT	SOT and VCMA
REF up	$H_x > 0$	$V_{SOT} > 0$	AP-P	$V_{STT} > 0$	P-AP	subtract	add
				$V_{STT} < 0$	AP-P	add	subtract
		$V_{SOT} < 0$	P-AP	$V_{STT} > 0$	P-AP	add	add
				$V_{STT} < 0$	AP-P	subtract	subtract
	$H_x < 0$	$V_{SOT} > 0$	P-AP	$V_{STT} > 0$	P-AP	add	add
				$V_{STT} < 0$	AP-P	subtract	subtract
		$V_{SOT} < 0$	AP-P	$V_{STT} > 0$	P-AP	subtract	add
				$V_{STT} < 0$	AP-P	add	subtract
REF down	$H_x > 0$	$V_{SOT} > 0$	P-AP	$V_{STT} > 0$	P-AP	add	add
				$V_{STT} < 0$	AP-P	subtract	subtract
		$V_{SOT} < 0$	AP-P	$V_{STT} > 0$	P-AP	subtract	add
				$V_{STT} < 0$	AP-P	add	subtract
	$H_x < 0$	$V_{SOT} > 0$	AP-P	$V_{STT} > 0$	P-AP	subtract	add
				$V_{STT} < 0$	AP-P	add	subtract
		$V_{SOT} < 0$	P-AP	$V_{STT} > 0$	P-AP	add	add
				$V_{STT} < 0$	AP-P	subtract	subtract

Supplementary Table S1: Combined effects of SOT, VCMA, and STT. Magnetic configurations and corresponding combinations of STT and VCMA that either assist or hinder SOT switching in a 3-terminal MTJ based on a β-phase W SOT channel.

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