Magnetic logic driven by electric current

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Spin-based logic gates consume no power when idle, are compatible with CMOS circuitry, and can be seamlessly integrated with memory.

A hundred years ago, Heinrich Barkhausen heard the crackling sounds produced by magnetic domains expanding and contracting in an iron bar. Those clicks were the first experimental evidence of the jumpy processes associated with the displacements of the domain walls. The movements determine many of the useful properties of ferromagnets, including how readily they respond to an applied magnetic field in transformers and electric motors.

But controlling domain propagation is difficult. Microscopic magnetization processes are stochastic, and disorder is inevitably present. In this Quick Study, we discuss how domain walls can nevertheless be manipulated by an electric current in order to move, store, and process digital information encoded in their magnetizations.

Driving domains

Early proposals for manipulating magnetic domains date back to the 1960s. Memory devices based on the propagation of cylindrical domains, or bubbles, in perpendicularly magnetized thin films reached a remarkable level of circuit integration and speed for their time. Although they were eventually abandoned in favor of cheaper semiconductor memories, magnetic bubble memories spearheaded the application of lithography techniques to fabricate magnetic devices. Moreover, they revealed the possibility of combining digital memory and logic functions in the same medium. Unfortunately, the domains were manipulated by magnetic fields produced by a maze of metal wires, which are neither scalable nor energy efficient. That scenario has changed in recent years. Spin–orbit torques have emerged as the most effective tool to push domain walls around via direct current in magnetic nanowires, now rebranded as domain-wall racetracks.

A spin–orbit torque is an effect by which an electric current transfers orbital angular momentum from electrons flowing in a conductor to the spins of a magnet. The transfer is mediated by the spin–orbit interaction, which couples the electrons' orbital and spin moments. And its overall effect is a change in the magnetization's orientation, which depends on the strength and sign of the current. In the most common devices, the electric current flows in a heavy metal, such as platinum, deposited next to a magnetic layer. Spin–orbit torques offer a way to electrically manipulate the magnetization of different materials, including metals and insulators, without the need for external magnetic fields. The action of the spin–orbit torque on the spins inside a domain wall is equivalent to that of a magnetic field that drives the domain wall forward. At high enough current density in properly designed racetracks, spin–orbit torques can move domain walls at record speeds of 0.5–5 km/s.

Coupling domains

Whereas the spin–orbit torques can transfer magnetic information by displacing domain walls between different parts of a

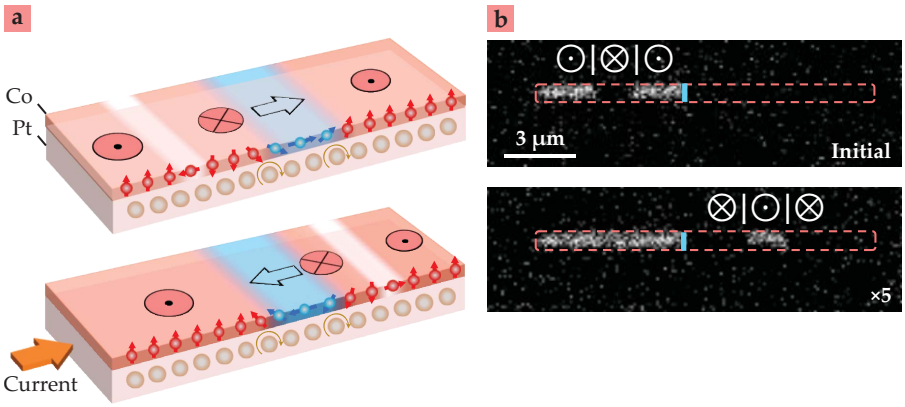

FIGURE 1. DOMAIN WALLS atop a strip of magnetic cobalt and platinum metal can be driven by an electric current. **(a)** Red regions signify up (⊙) and down (⊗) magnetization, white is the domain wall, and blue is the domain-wall inverter, or NOT gate, magnetized in-plane along the arrow. The illustrations show the initial state (top panel) and the current-driven inverter in action (bottom panel): Here the ⊙|⊗ domain wall propagates across the strip and changes to a ⊗|⊙ domain wall. **(b)** Kerr-effect images of a train of two domain walls, shown before and after 5 current pulses are applied. The inverter is shown as a blue line. (Adapted from Z. Luo et al., *Nature* **579**, 214, 2020.)

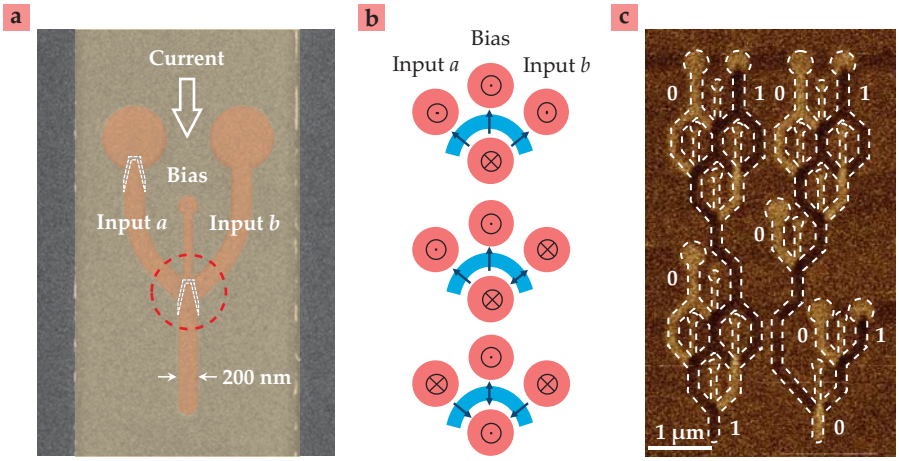

FIGURE 2. MAJORITY RULES. (a) In this scanning electron micrograph of a reconfigurable NAND/NOR logic gate, the current-carrying strip is tan colored. **(b)** In red and blue are circuit regions whose magnetizations are out of plane and in plane, respectively. The magnetization is shown for the two logic inputs, the bias, and the logic output for the gate. **(c)** Magnetic force microscopy image of a full adder gate, showing the sum (left) and carry (right) circuits. The light and dark regions in the device correspond to ⊙ and ⊗ magnetization, respectively. (Adapted from Z. Luo et al., *Nature* **579**, 214, 2020.)

multilayered wire, something more is needed to process that information and build a logic circuit. For a start, we need a coupling mechanism to perform combinatorial operations with domain walls. Our racetracks are made from a 1-nm-thick cobalt layer deposited on a 5-nm-thick platinum track and capped with aluminum oxide. That stack of materials produces the so-called Dzyaloshinskii–Moriya interaction (DMI), an unusual form of magnetic coupling between atomic spins—also mediated by the spin–orbit interaction—that occurs naturally in systems with broken inversion symmetry.

Unlike the usual magnetic exchange interaction, which causes the spins to align parallel or antiparallel to each other in ferromagnets and antiferromagnets, the DMI favors the orthogonal alignment of adjacent spins with a unique sense of rotation, or chirality. As shown in figure 1a, the alignment produces chiral domain walls with a left-handed rotation of the spins between up (⊙) and down (⊗) domains. That left-handed rotation is found in Pt/Co/AlO_x, and it is those chiral domain walls that can be moved under the action of a spin–orbit torque.

We have also exploited the DMI to induce coupling between different sections of a magnetic racetrack. More specifically, we have built devices in which different parts of a continuous Pt/Co/AlO_x racetrack have different orientations of magnetization. We built them by oxidizing selected regions of the Al cap layer; regions that are oxidized have out-of-plane (OOP), or perpendicular, magnetization, and regions that are unoxidized have in-plane (IP) magnetization. Akin to what happens inside a domain wall, the DMI produces a left-handed chiral alignment of magnetic moments in neighboring IP–OOP regions (figure 1a). If the DMI is strong enough, chiral ordering emerges spontaneously in racetracks composed of one or more sequences of IP–OOP elements. Moreover, switching the magnetization of an IP (OOP) element automatically causes the magnetization of the OOP (IP) element next to it to switch. That property allows for a key building block—a so-called domain-wall inverter—in Boolean logic circuits.

To be XOR not to be

A narrow IP region patterned into an OOP magnetized racetrack couples to its surroundings and forms one of the following left-handed configurations: ⊗→⊙ or ⊙←⊗. The DMI thus produces an antiparallel alignment of the OOP magnetization on the left and right of the IP region. When a domain wall in a racetrack is driven through such an IP region by a current-induced spin–orbit torque, the magnetization of the IP region flips. That, in turn, annihilates the incoming domain wall and nucleates a new domain wall of opposite polarity on the other side of the IP region. The new domain wall then continues to propagate along the current direction (figures 1a and 1b). The chirally coupled OOP-IP-OOP region therefore serves as an inverter capable of transforming an up–down domain wall into a down–up domain wall and vice versa. One can associate "1" and "0" with the down and up magnetization directions in the racetrack—a process equivalent to a NOT logical operation.

Building on the chiral coupling between OOP-IP-OOP regions, we designed majority gates where three OOP tracks (two inputs and one bias) meet at a common point (circled in red in figure 2a) delimited by an IP region, which connects them at the output track. The output is the opposite of the majority of the three converging tracks. The bias, specifically, dictates whether that corresponds to a NAND or a NOR function. A combination of the two gates completes our concept for current-driven domain-wall logic because any Boolean function can be implemented using them. Indeed, bifurcations in racetracks fan out, so that more gates can be cascaded on the same current line—no additional control circuitry required. As an example, we present a full adder circuit created by cascading 15 NAND gates in figure 2c.

In principle, the minimum size of a gate can be scaled down to dimensions approaching the width of a domain wall. That's about 10 nm in thin films. In combination with the current-dependent domain-wall velocity, that width constrains the speed of logic operations.

Additional resources

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