A Sustainable Future Enabled By Power Electronics

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Outline

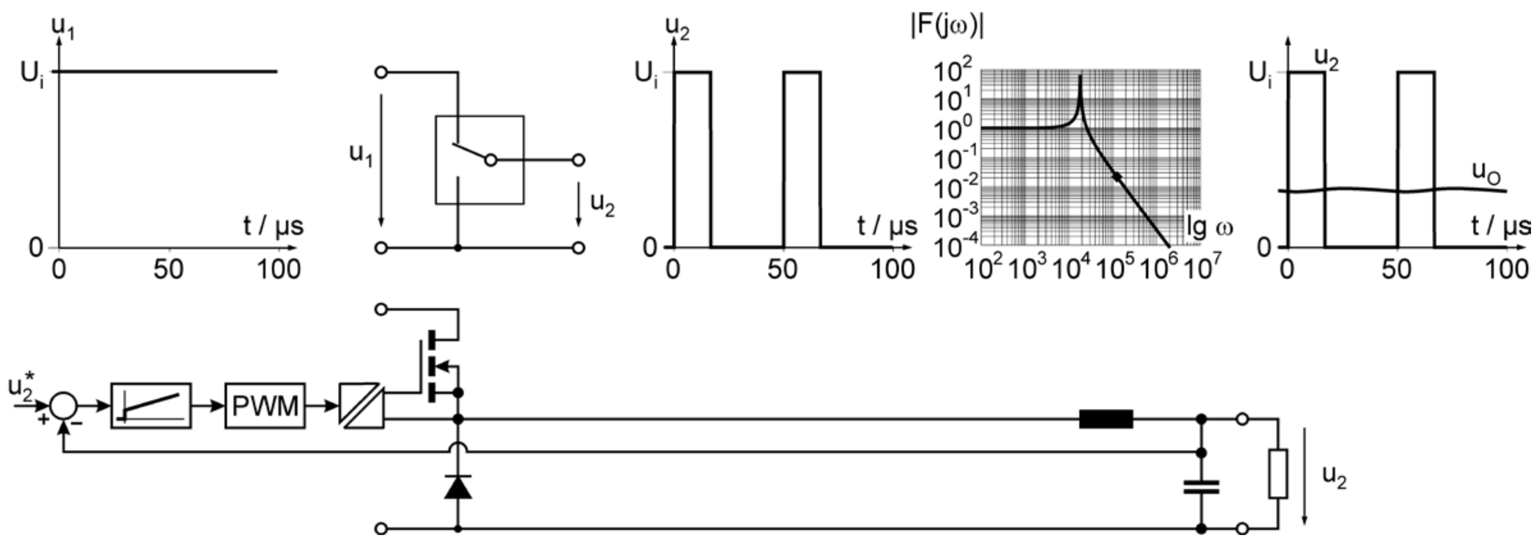
- Power Electronics 101
- Global Megatrends
- Resulting Requirements for Power Electronics
- *Multi-Objective Optimization Approach*
- *Google Little Box Challenge*
- Ultra Compact GaN Based Power Conversion
- Conclusion

Basic Structure of Electronic *Power* Processing Systems

Power Electronic Systems

▶ Power Electronics 101

■ Basic Principle Step-Down DC/DC Conversion



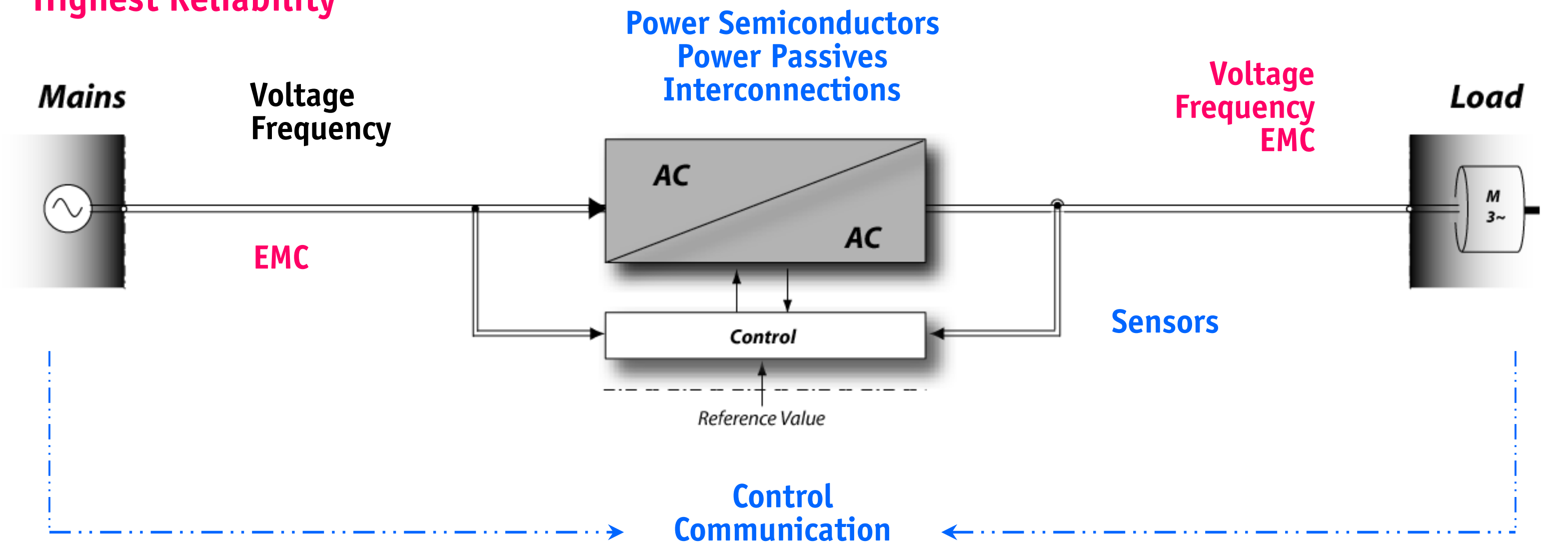
Power Semiconductors Circuits
Control Engineering
Electronics
Drives/El. Machines
Simulation

Sensors/Signal Electronics
Electromagnetic Systems
Energy Systems
EMC

Power Electronics 101

Electronic Power Processing

Highest Efficiency
Highest Compactness
Highest Dynamics
Highest Compatibility
Highest Reliability



▶ Power Electronics 101

■ Electronic Power Processing

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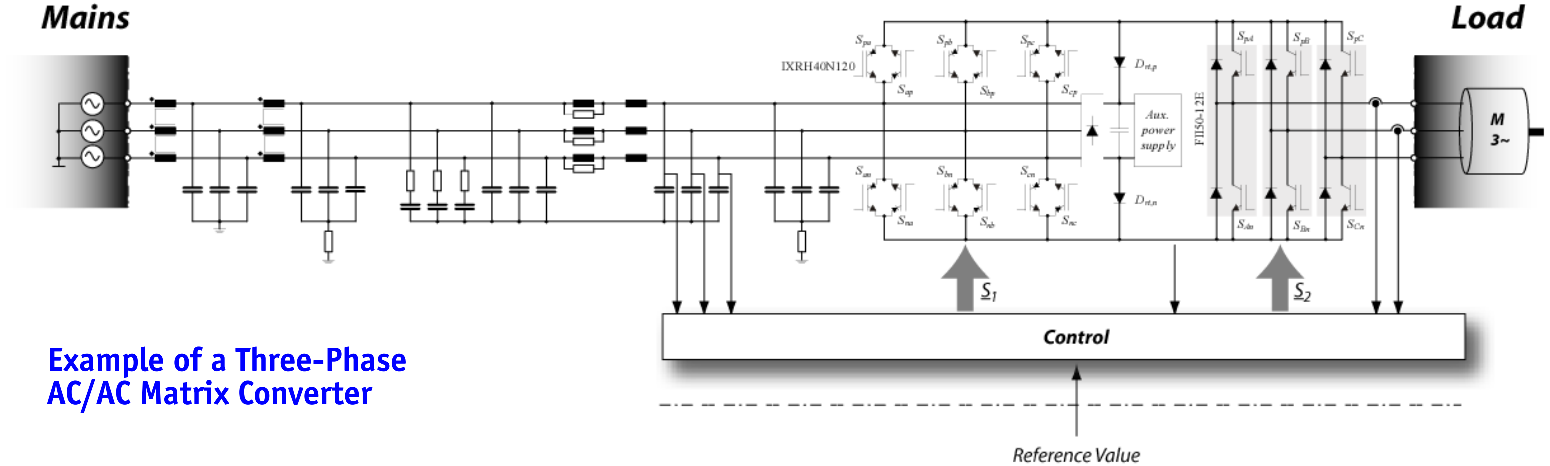
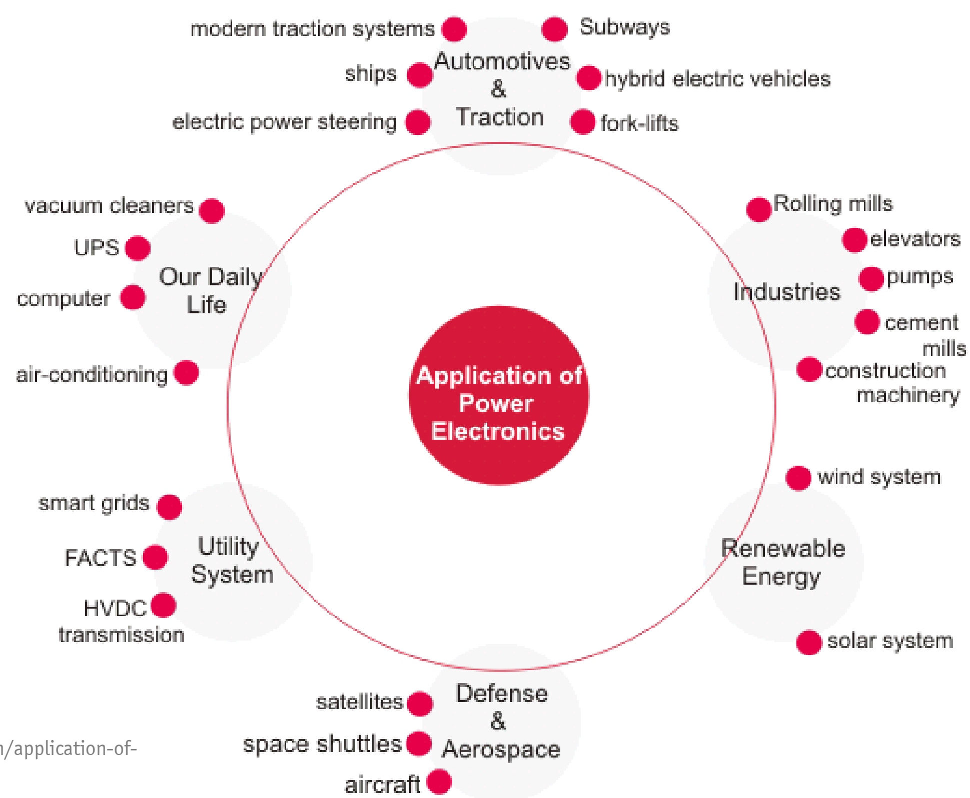


Example of a Three-Phase
AC/AC Matrix Converter

▶ Power Electronics Applications

- Industry Automation / Processes
- Communication & Information
- Transportation
- Lighting
- etc., etc.



Source: https://www.electrical4u.com/application-of-power-electronics/

.... Everywhere !

Global Megatrends

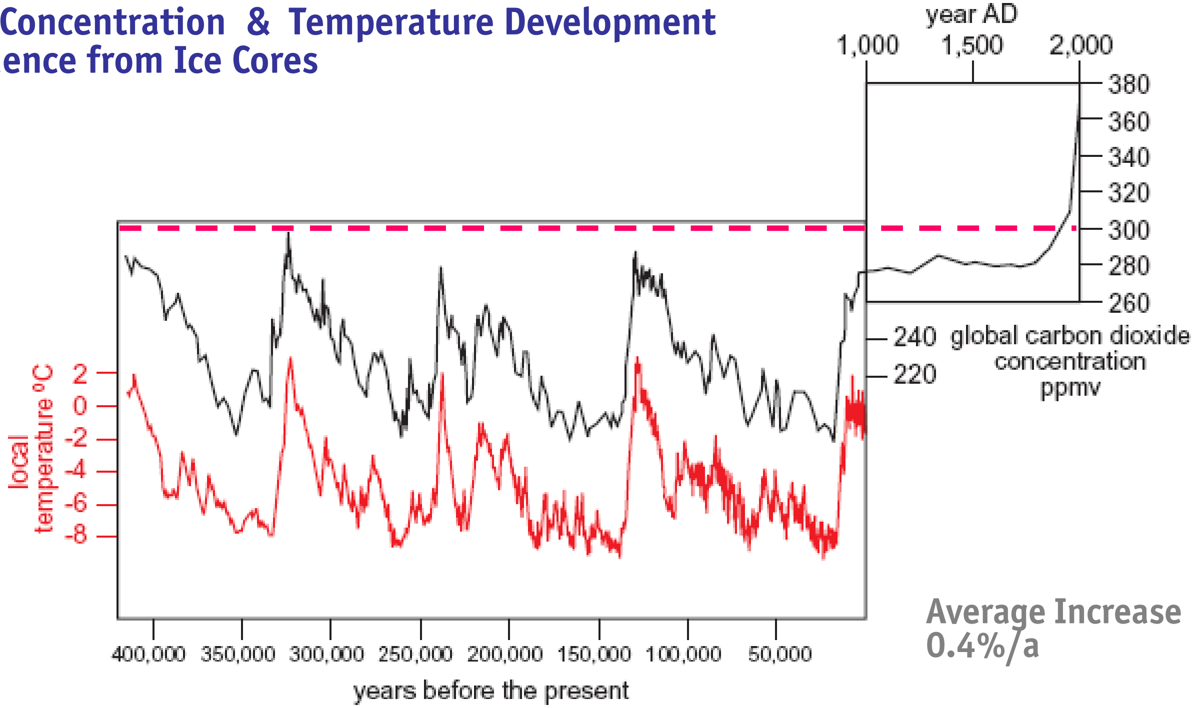
Climate Change
Digitalization
Sustainable Mobility
Urbanization
Alleviate Poverty
Etc.

Global Megatrends

- *Climate Change* →
- *Digitalization*
- *Sustainable Mobility*
- *Urbanization*
- *Alleviate Poverty*
- *Etc.*

▶ Climate Change

- CO_2 Concentration & Temperature Development
- Evidence from Ice Cores



Average Increase
0.4%/a

▶ Reduce CO_2 Emissions *Intensity* (CO_2/GDP) to Stabilize Atmospheric CO_2 Concentration
▶ 1/3 in 2050 → less than 1/10 in 2100 (AIST, Japan @ IEA Workshop 2007)

▶ Climate Change

- CO_2 Concentration & Temperature Development
- Evidence from Ice Cores

Source: H. Nilsson
Chairman IEA DSM Program
FourFact AB

▶ Reduce CO_2 Emissions *Intensity* (CO_2/GDP) to Stabilize Atmospheric CO_2 Concentration
▶ 1/3 in 2050 → less than 1/10 in 2100 (AIST, Japan @ IEA Workshop 2007)

→ *Utilize Renewable Energy* (1)

■ Enabled by Power Electronics

— Higher Reliability (!)
— Lower Costs

Medium-Voltage Power Collection and Connection to On-Shore Grid

Source: M. Prahm / Flickr

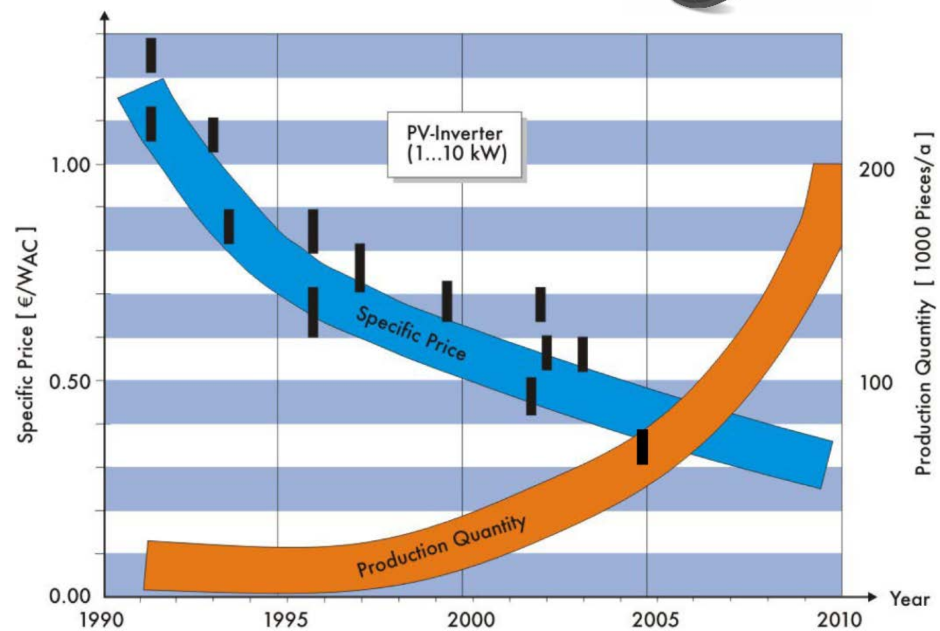
▶ Off-Shore Wind Farms
▶ Medium Voltage Systems

→ *Utilize Renewable Energy (2)*

■ Enabled by Power Electronics

— Extreme Cost Pressure (!)
— Higher Efficiency
— Higher Power Density

Source: SMA 2006



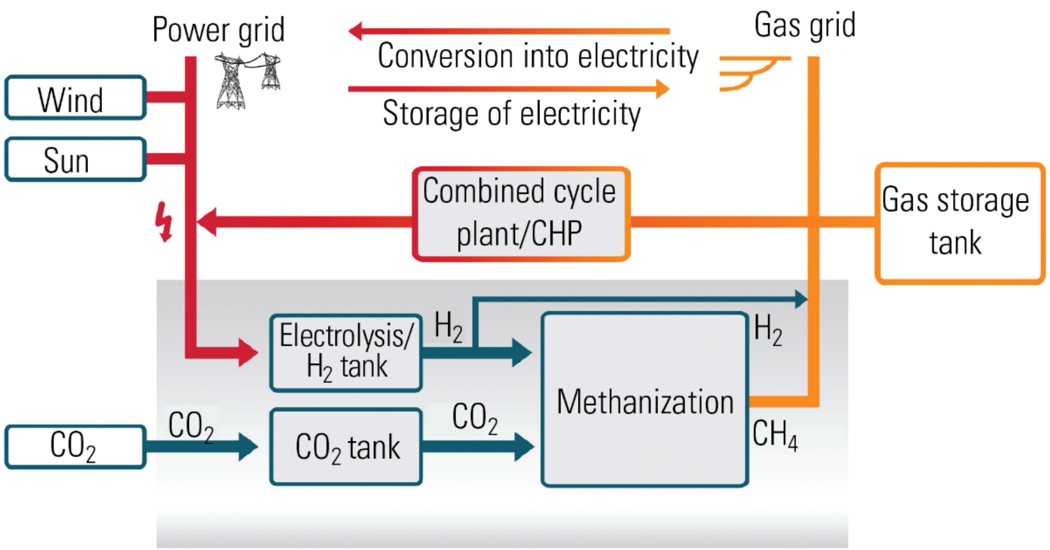
▶ Photovoltaics Power Plants
▶ Up to Several MW Power Level
▶ Future Hybrid PV/Therm. Collectors

→ *Utilize Renewable Energy (3)*

■ Enabled by Power Electronics

— Electrolysis for Conversion of Excess Wind/Solar Electric Energy into Hydrogen
→ Fuel-Cell Powered Cars
→ Heating

Hydrogenics 100 kW H_2-Generator (η=57%), High Power @ Low Voltage



Source: www.r-e-a.net

Global Megatrends

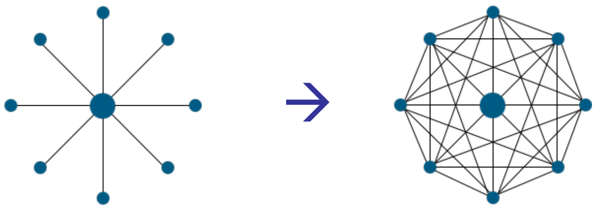
- Climate Change
- **Digitalization** →
- Sustainable Mobility
- Urbanization
- Alleviate Poverty
- Etc.

▶ Digitalization

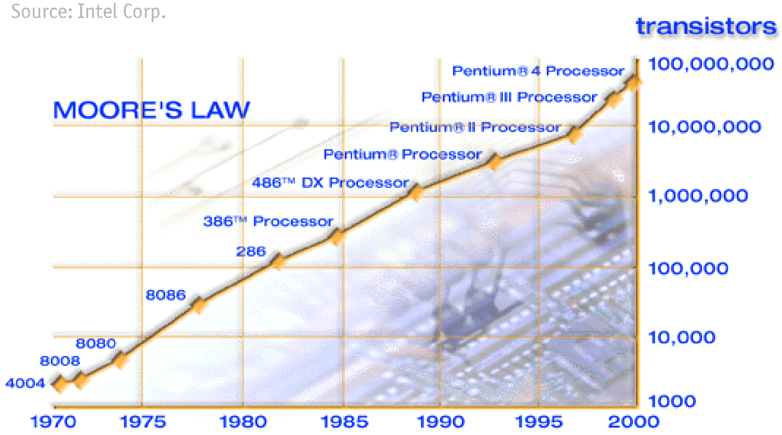
– Moving form Hub-Based to Community Concept Increases Potential Network Value Proportional to n^2)

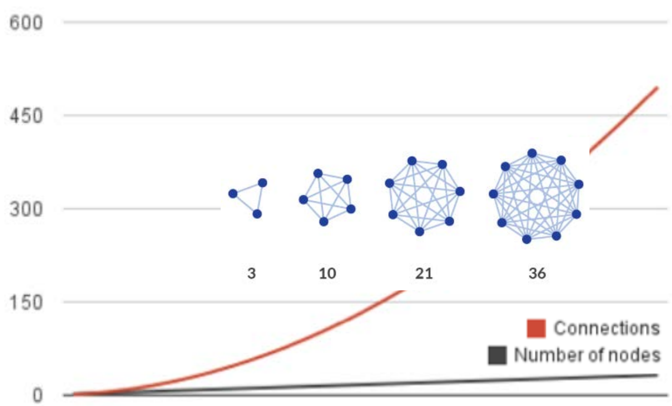
■ **Internet of Things (IoT) / Cognitive Computing**

— Ubiquitous Computing / BIG DATA
— Blockchain Tech. / DApps.
— Fully Automated Manufacturing / Industry 4.0
— Autonomous Cars
— Etc.



Source: Intel Corp.





▶ Moore's Law

▶ Metcalfe's Law

→ Green / Zero  Datacenters (1)

■ Enabled by Power Electronics

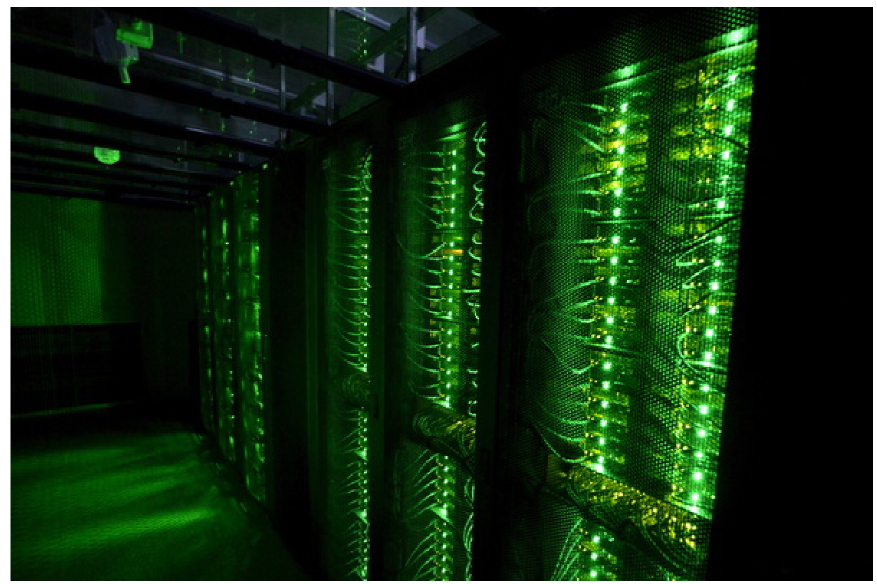
— Ranging from Medium Voltage to Power-Supplies-on-Chip
— Short Power Supply Innovation Cycles
— Modularity / Scalability

— Higher Power Density (!)
— Higher Efficiency (!)
— Lower Costs

Server-Farms
up to 450 MW
99.9999%/<30s/a
$1.0 Mio./Shutdown

Since 2006
Running Costs >
Initial Costs

Source: REUTERS/Sigtryggur Ari



33 Watts

→

60 Watts

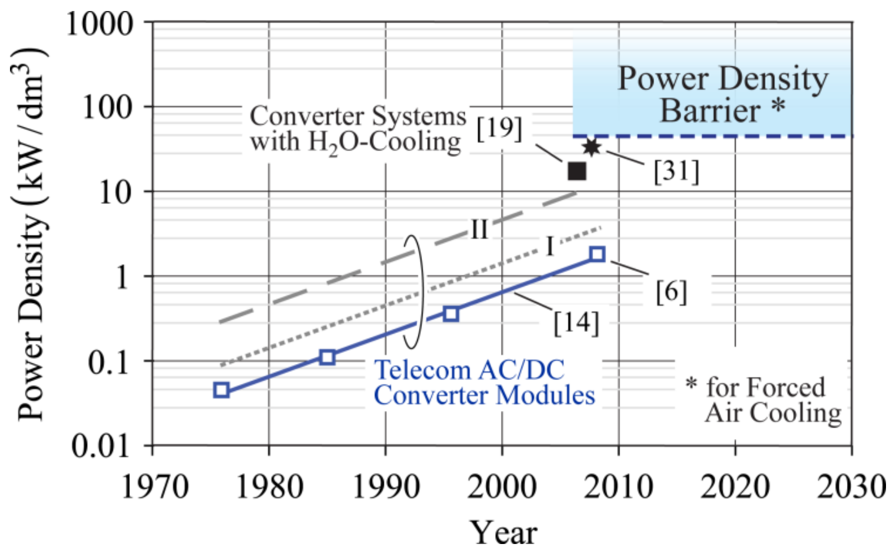
→ Green / Zero  Datacenters (2)

■ Enabled by Power Electronics

- Ranging from Medium Voltage to Power-Supplies-on-Chip
- Short Power Supply Innovation Cycles
- Modularity / Scalability

- Higher Power Density (!)
- Higher Efficiency (!)
- Lower Costs

▶ Power Density Increased by Factor 2 over 10 Years

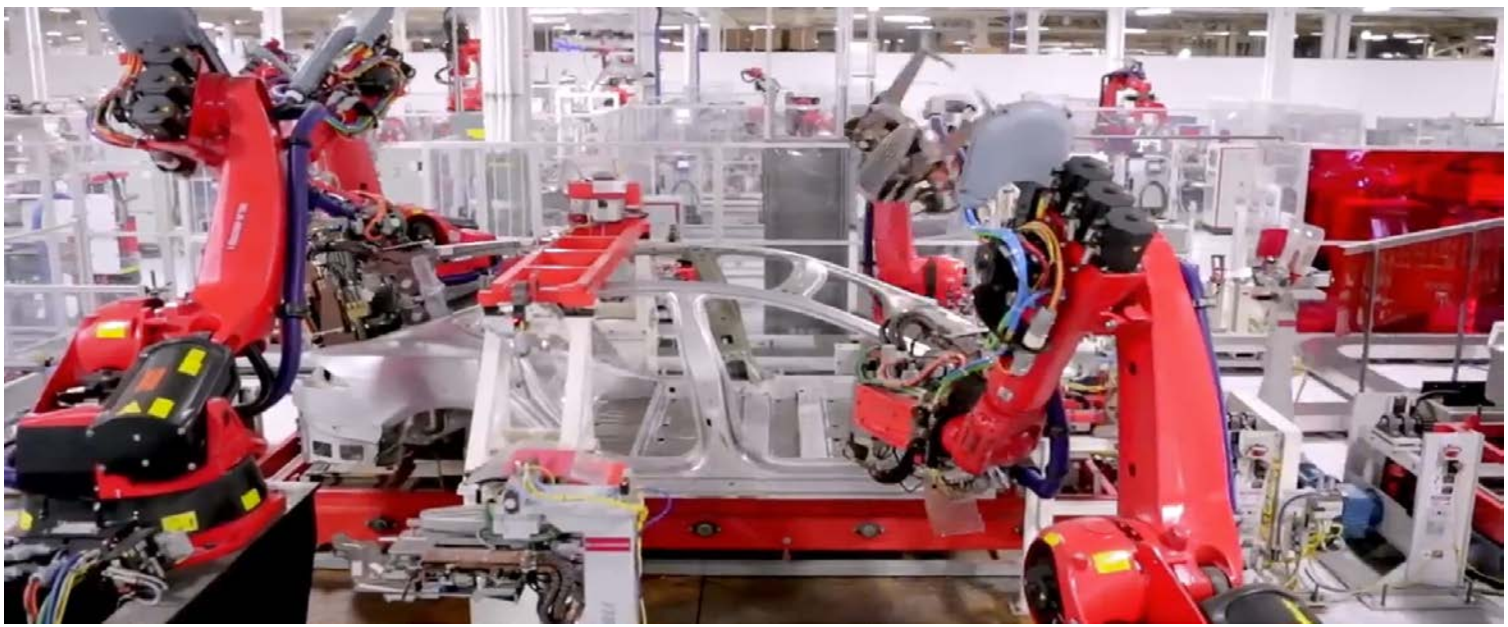


→ Fully Automated Manufacturing – Industry 4.0

■ Enabled by Power Electronics

— Lower Costs (!)
— Higher Power Density
— Self-Sensing etc.

Source: TESLA MOTORS

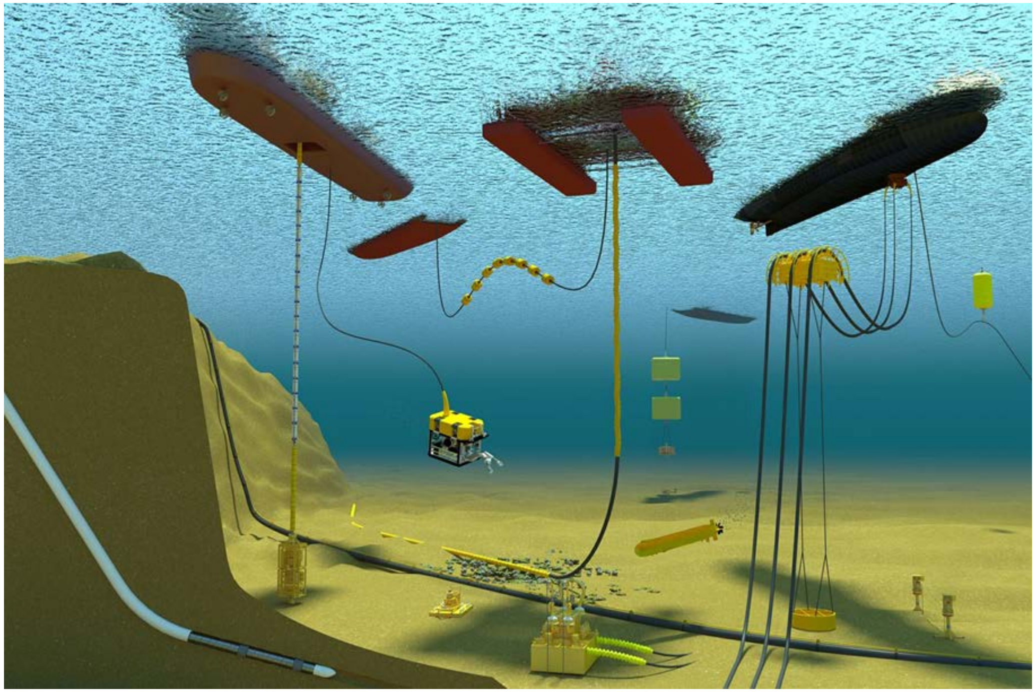


→ *Fully Automated Raw Material Extraction*

■ Enabled by Power Electronics

— High Reliability (!)
— High Power Density (!)

Source: matrixengineered.com



▶ ABB´s Future Subsea Power Grid → "Develop All Elements for a Subsea Factory"

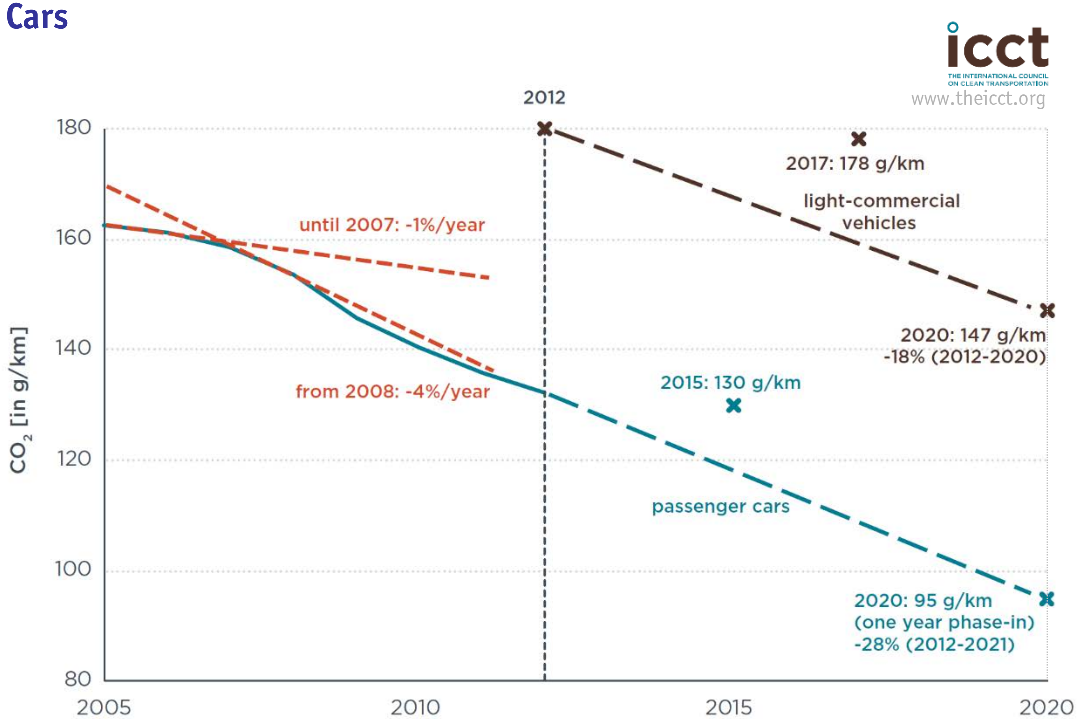
Global Megatrends

Climate Change
Digitalization
Sustainable Mobility →
Urbanization
Alleviate Poverty
Etc.

▶ Sustainable Mobility

■ EU Mandatory 2020 CO_2 Emission Targets for New Cars

— 147g CO_2/km for Light-Commercial Vehicles
— 95g CO_2/km for Passenger Cars
— 100% Compliance in 2021



▶ Hybrid Vehicles
▶ Electric Vehicles

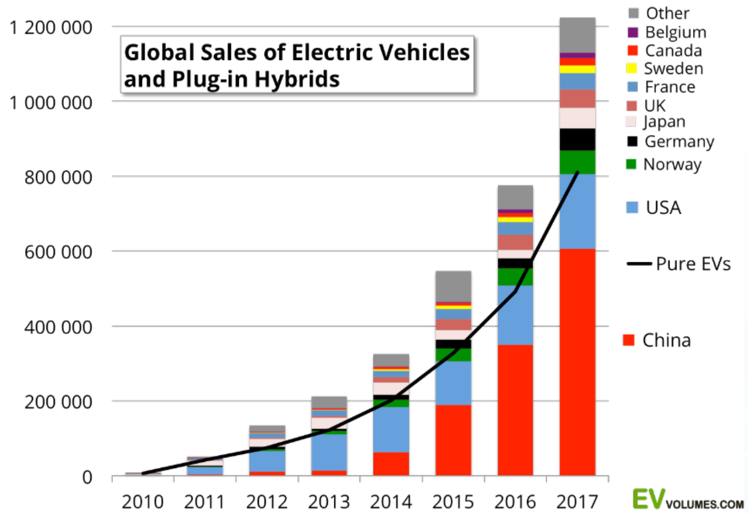
→ Electric Vehicles

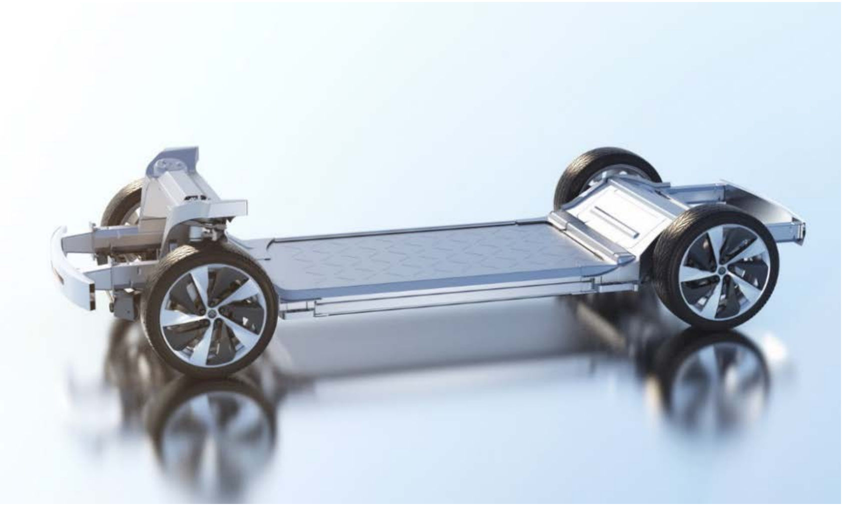
- **Enabled by Power Electronics** - Drivetrain / Aux. / Charger

— Higher Power Density
— Extreme Cost Pressure (!)

Faraday Future

FF-ZERO1
750kW / 322km/h
1 Motor per Wheel
300+ Miles Range
Lithium-Ion Batteries along the Floor



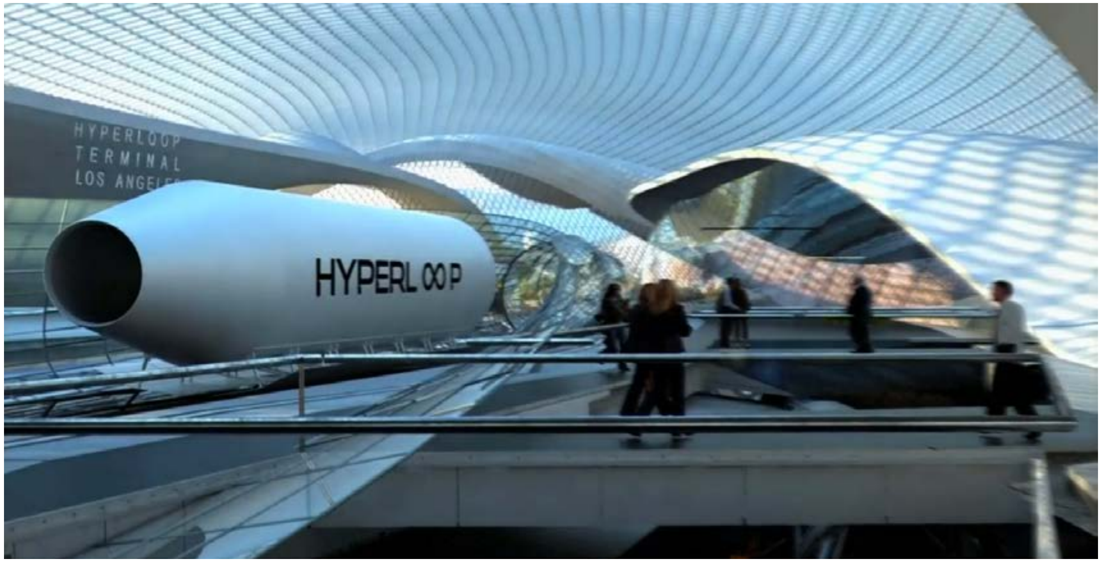


→ *Futuristic Mobility Concepts* (1)

■ Enabled by Power Electronics

— Hyperloop
— San Francisco → Los Angeles in 35min

HYPERLOOP POD COMPETITION
www.spacex.com/hyperloop



- ▶ Low Pressure Tube
- ▶ Magnetic Levitation
- ▶ Linear Ind. Motor
- ▶ Air Compressor in Nose

→ Futuristic Mobility Concepts (2)

■ Enabled by Power Electronics

— Cut Emissions Until 2050
* CO_2 by 75%,
* NO_x by 90%,
* Noise Level by 65%

Source: EADS
Future Hybrid
Distributed Propulsion Aircraft

▶ Eff. Optim. Gas Turbine
▶ 1000Wh/kg Batteries
▶ Distrib. Fans (E-Thrust)

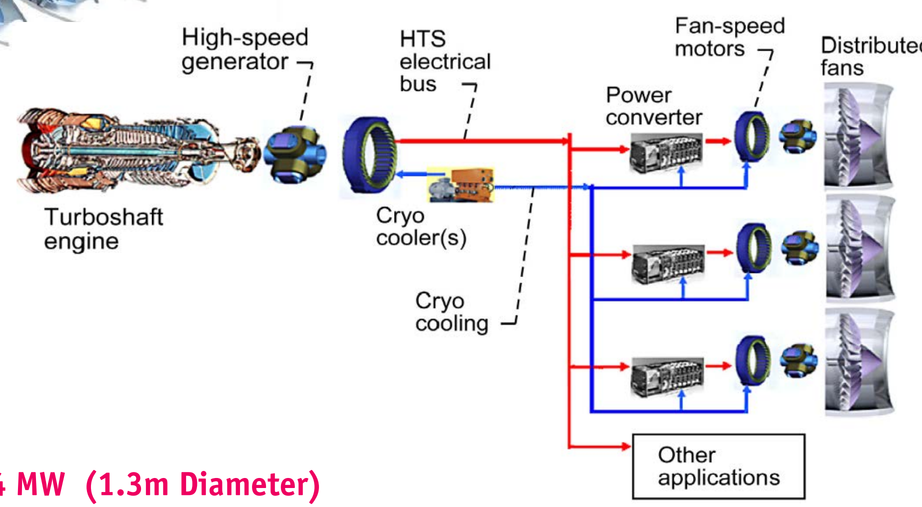
▶ Supercond. Motors
▶ Med. Volt. Power Distrib.

→ *Futuristic Mobility Concepts (3)*

■ Enabled by Power Electronics

Source:

NASA N3-X
Vehicle Concept using
Turboel. Distrib. Propulsion



- ▶ Electric Power Distribution
- ▶ High Flex. in Generator/Fan Placement
- ▶ Generators: 2 x 40.2MW / Fans: 14 x 5.74 MW (1.3m Diameter)

Global Megatrends

Climate Change
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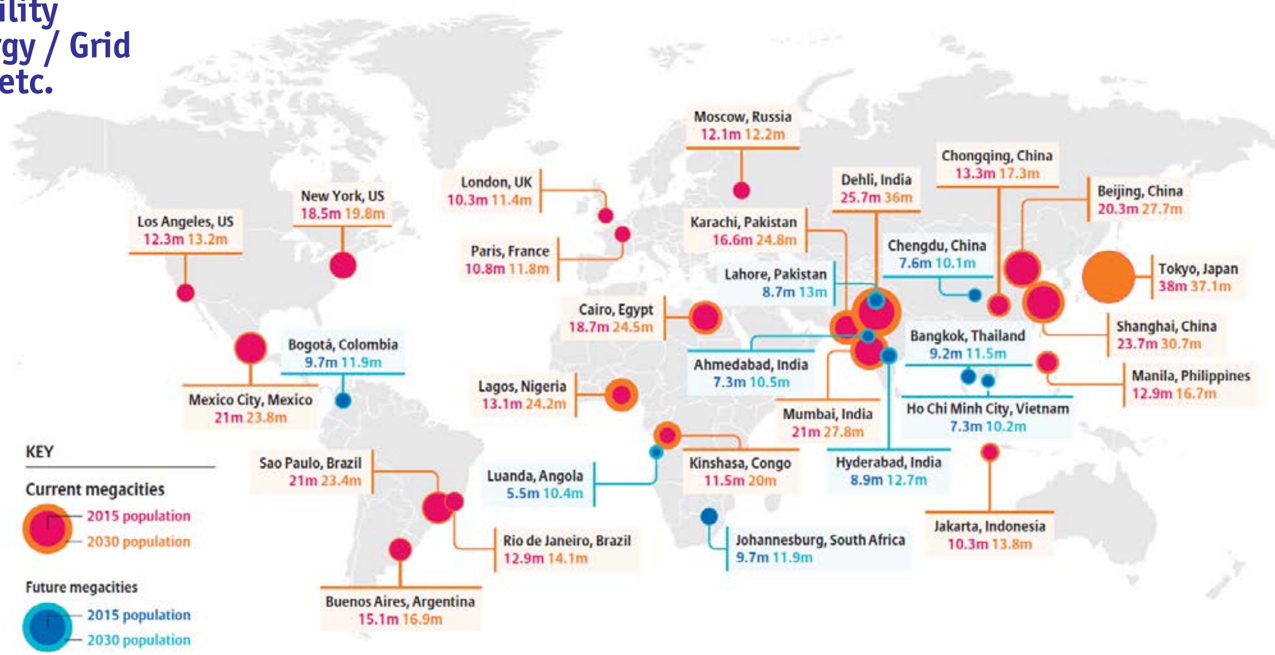
Sustainable Mobility
Urbanization →
Alleviate Poverty
Etc.

▶ Urbanization

- 60% of World Population Exp. to Live in Urban Cities by 2025
- 30 MEGA Cities Globally by 2023

— Smart Buildings
— Smart Mobility
— Smart Energy / Grid
— Smart ICT, etc.

Source: World Urbanization Prospects: The 2014 Revision



▶ Selected Current & Future MEGA Cities 2015 → 2030

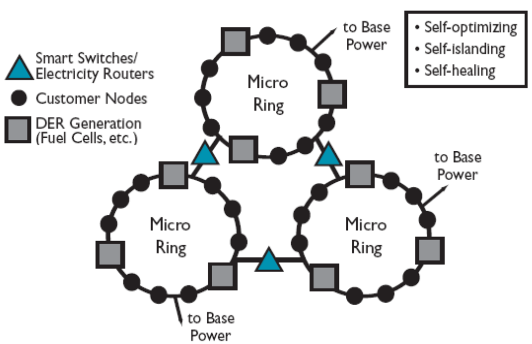
→ Smart Cities / Grid (1)

■ Enabled by Power Electronics

— *Masdar = "Source"*
— Fully Sustainable Energy Generation
  * Zero CO_2
  * Zero Waste
— EV Transport / IPT Charging
— to be finished 2025

Masdar CITY
www.masdar.ae

Source: EPRI ELECTRIC POWER RESEARCH INSTITUTE



→ *Smart Cities / Grid (2)*

■ Enabled by Power Electronics

— *Masdar = "Source"*
— Fully Sustainable Energy Generation
  * Zero CO_2
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Masdar CITY
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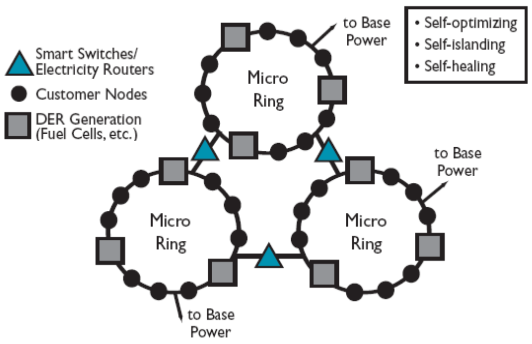

Global Megatrends

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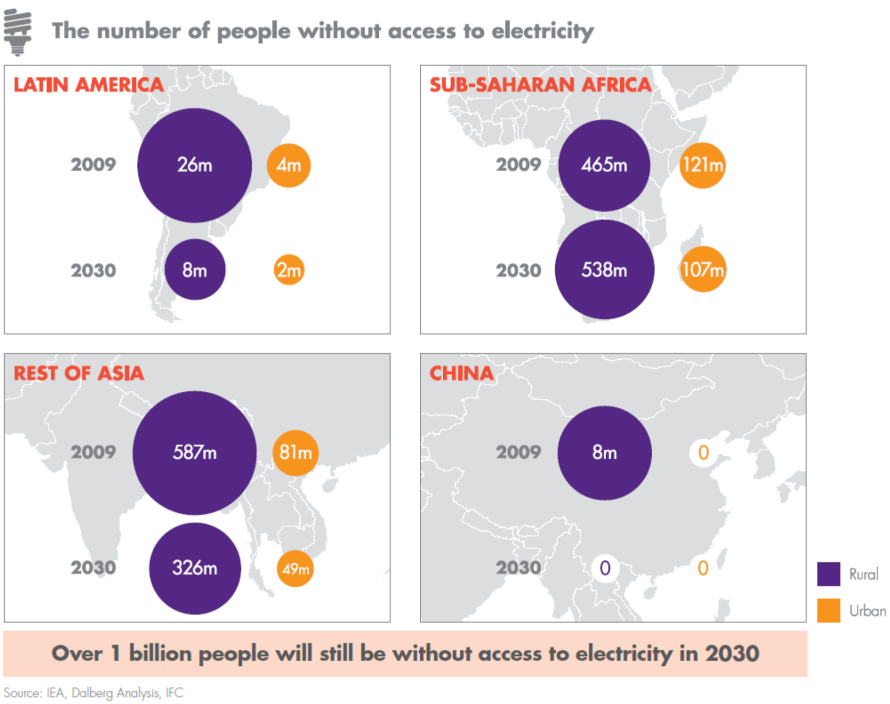
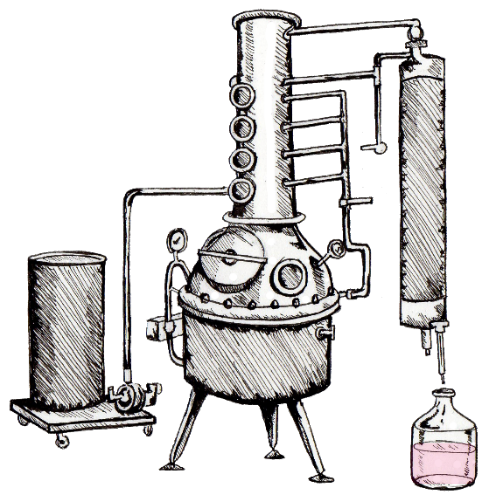
Alleviate Poverty →
Etc.

▶ Alleviate Poverty

- 2 Billion People are Lacking Access to Clean Energy
- Rural Electrification in the Developing World



▶ Urgent Need for Village-Scale Solar DC Microgrids etc.
▶ 2 US$ for 2 LED Lights + Mobile-Phone Charging / Household / Month (!)



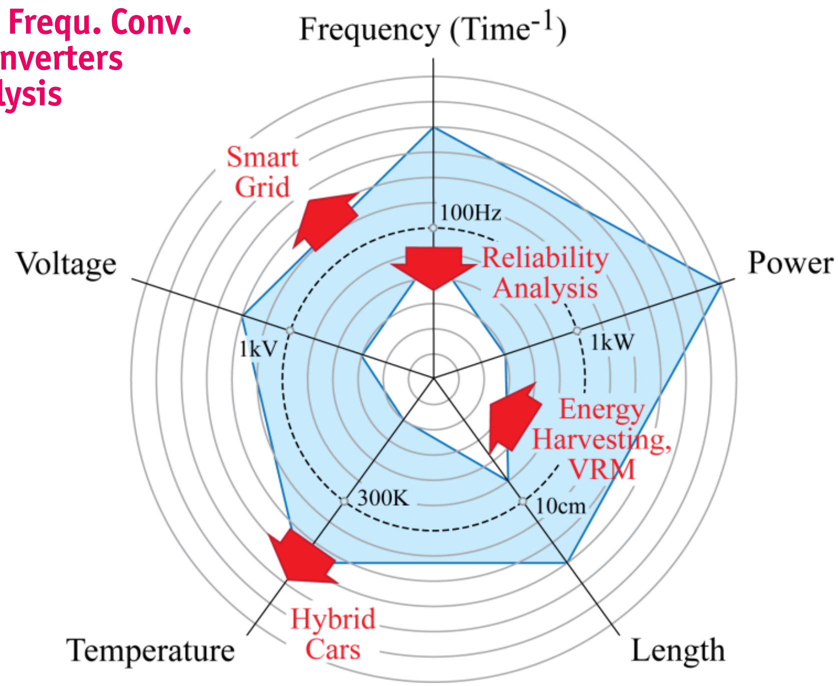
Source: whiskeybehavior.info

... in Summary

▶ Current / New Application Areas (1)

- Power Electronics Covers an Extremely Wide Power / Voltage / Frequency Range
- Extensions for *SMART xxx* / Mobility Trends / Availability Requirements

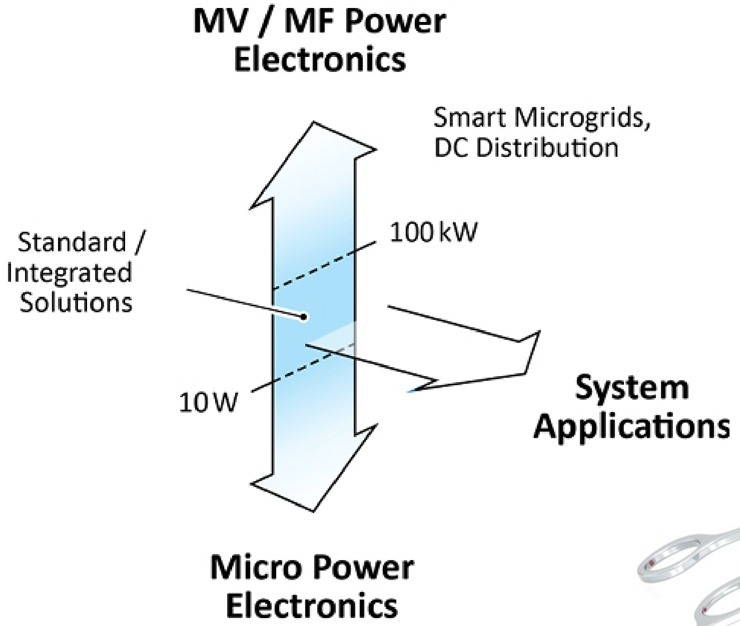
— Medium-Voltage / Medium. Frequ. Conv.
— 3D-Integr. of Low Power Converters
— Life-Cycle & Reliability Analysis



▶ Future Extensions of Power Electronics Application Areas

► Current / New Application Areas (2)

- Commoditization / Standardization for High Volume Applications
- Extension to Microelectronics-Technology (Power Supply on Chip)
- Extensions to MV/MF



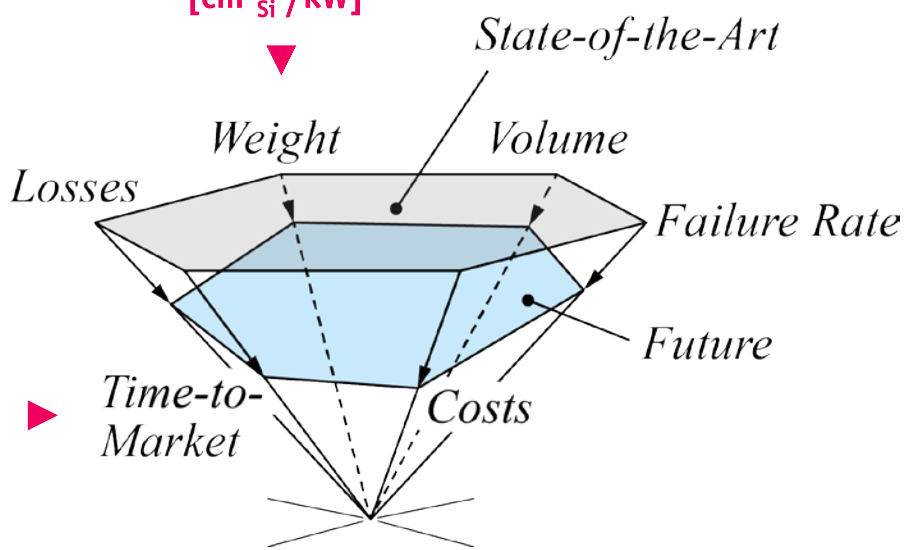
► Cost Pressure as Common Denominator of All Applications (!)
► Key Importance of Technology Partnerships of Academia & Industry

Power Converter Design Challenges

Mutual Coupling of Performances

Required Power Electronics Performance Improvements

Environmental Impact... $[kg_{Fe}/kW]$ $[kg_{Cu}/kW]$ $[kg_{Al}/kW]$ $[cm^2_{Si}/kW]$

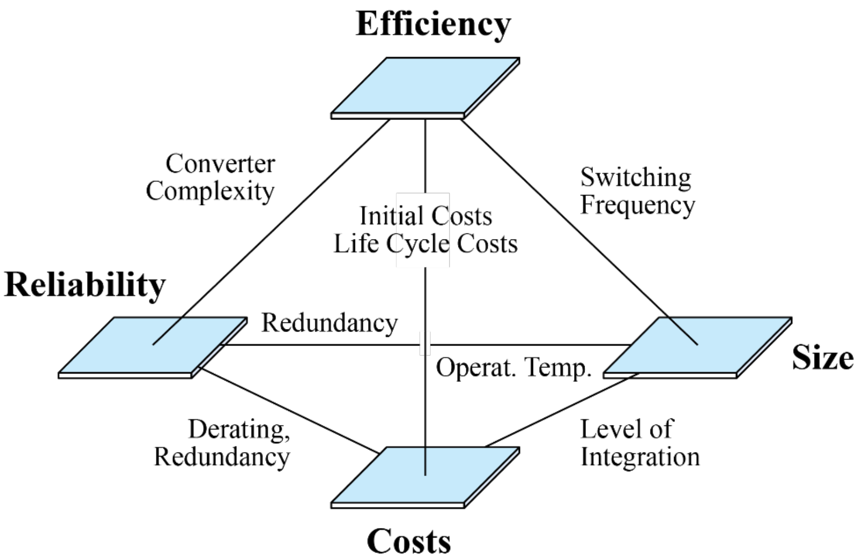


Performance Indices

- Power Density $[kW/dm^3]$
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/$]
- Relative Losses [%]
- Failure Rate $[h^{-1}]$

▶ Multi-Objective Design Challenge (1)

- Counteracting Effects of Key Design Parameters
- Mutual Coupling of Performance Indices → Trade-Offs



→ Large Number of Degrees of Freedom / Multi-Dimensional Design Space
→ Full Utilization of Design Space only Guaranteed by Multi-Objective Optimization

► Multi-Objective Design Challenge (1)

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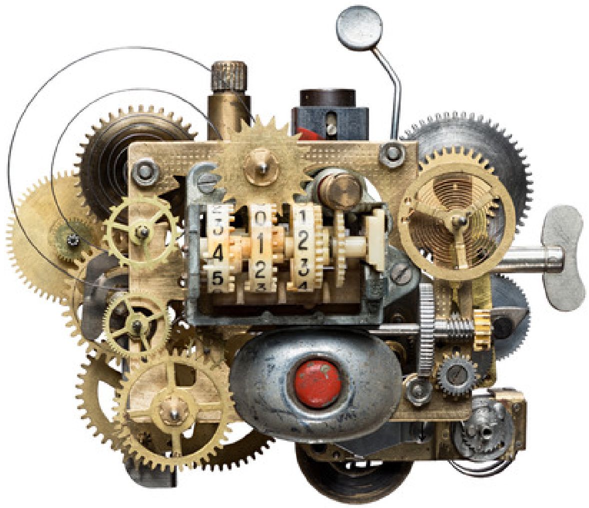
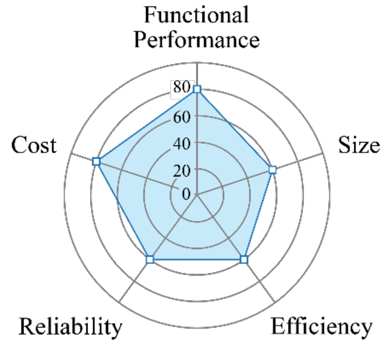


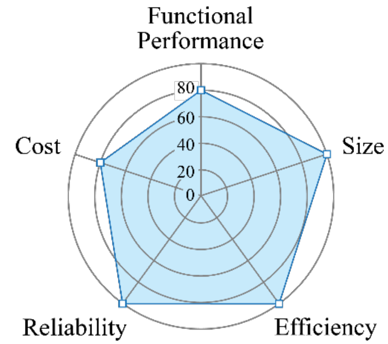
→ Large Number of Degrees of Freedom / Multi-Dimensional Design Space
→ Full Utilization of Design Space only Guaranteed by Multi-Objective Optimization

Multi-Objective Design Challenge (2)

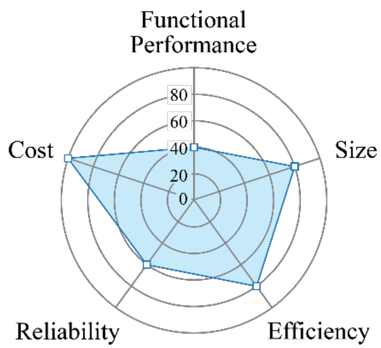
- Specific Performance Profiles / Trade-Offs Dependent on Application



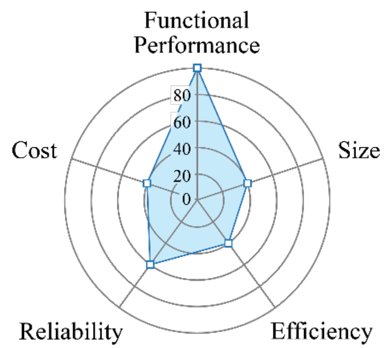
Industry Applications



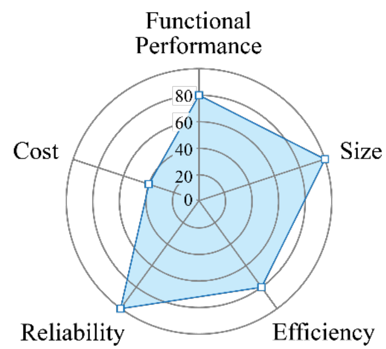
Information & Communication Industry



Domestic Applications



Laboratory Applications



Aerospace Applications

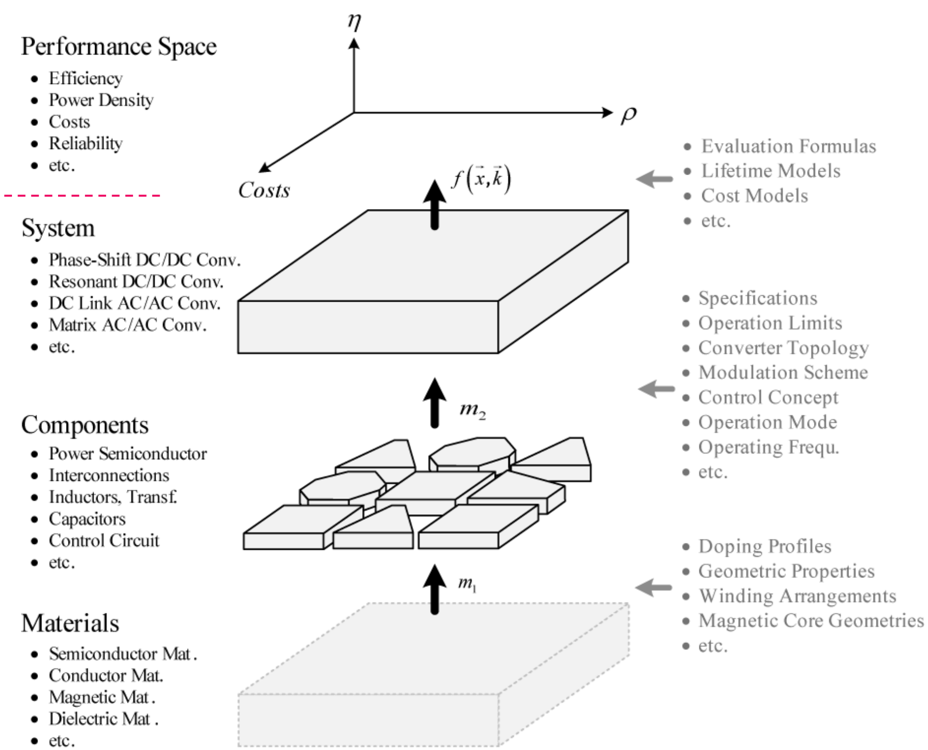
Multi-Objective Optimization

Abstraction of Converter Design
Design Space / Performance Space
Pareto Front
Sensitivities / Trade-Offs

► Abstraction of Power Converter Design

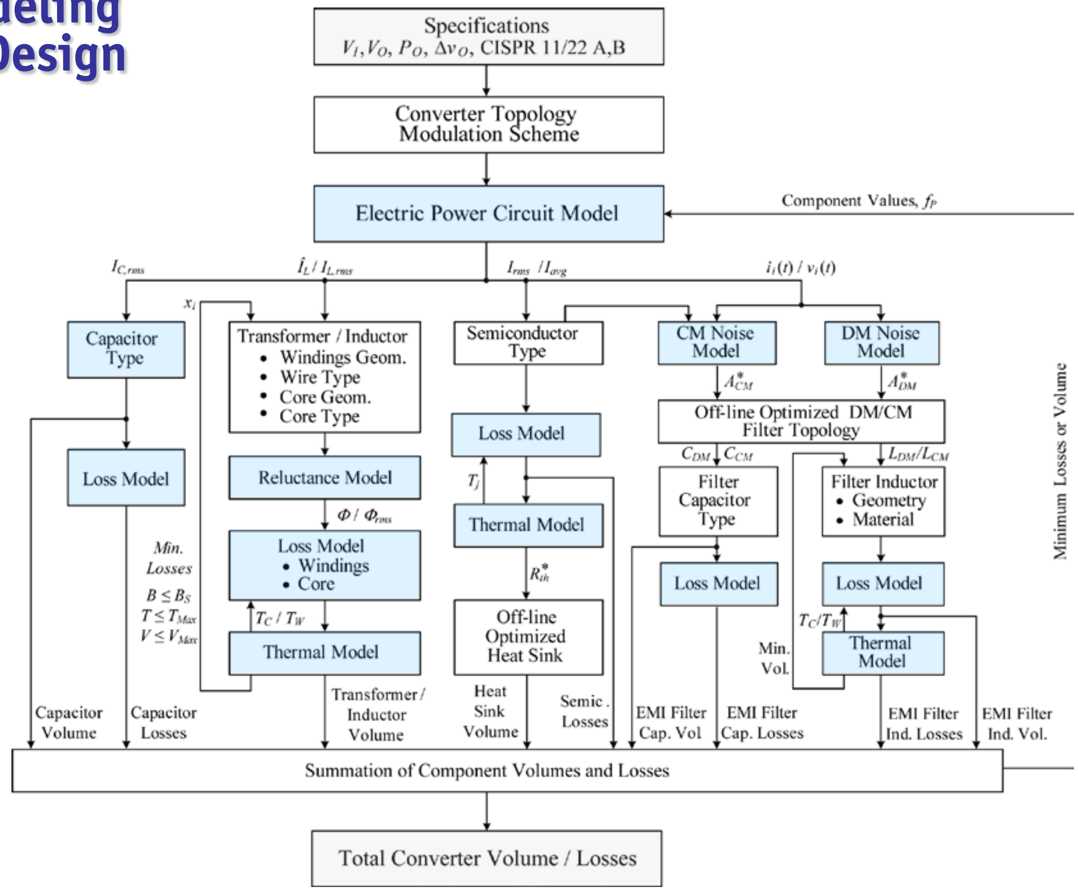
Performance Space

Design Space



→ *Mapping* of "*Design Space*" into System "*Performance Space*"

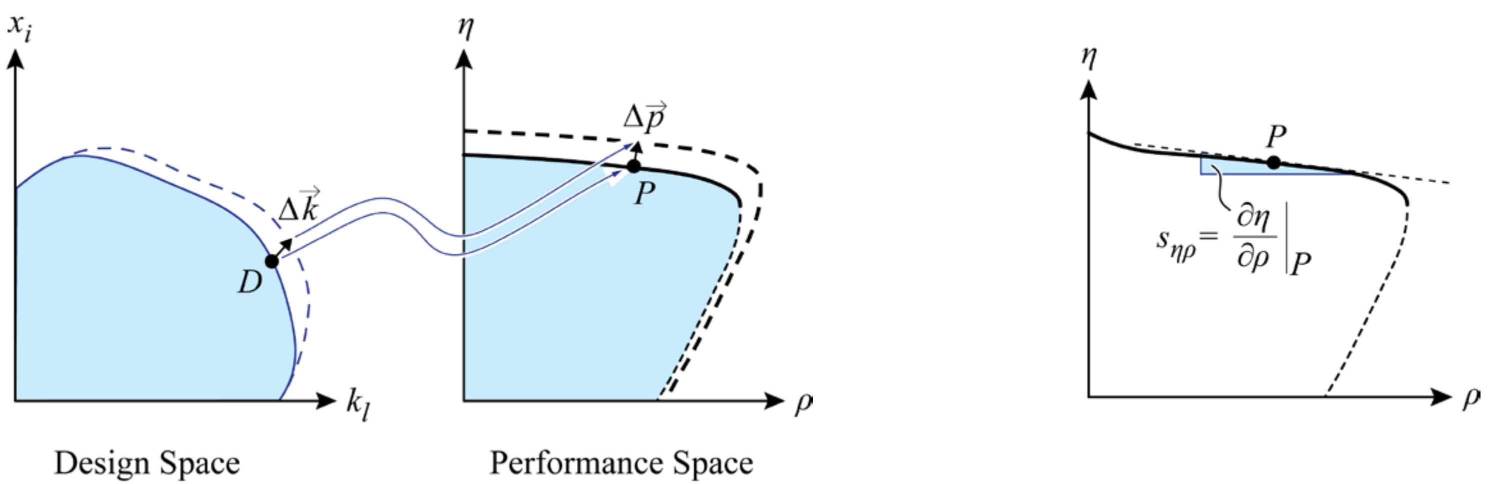
▶ Mathematical Modeling of the Converter Design



→ **Multi-Objective Optimization** – ***Guarantees Best Utilization of All Degrees of Freedom*** **(!)**

▶ Multi-Objective Optimization (1)

- Ensures Optimal Mapping of the "Design Space" into the "Performance Space"
- Identifies Absolute Performance Limits → Pareto Front / Surface

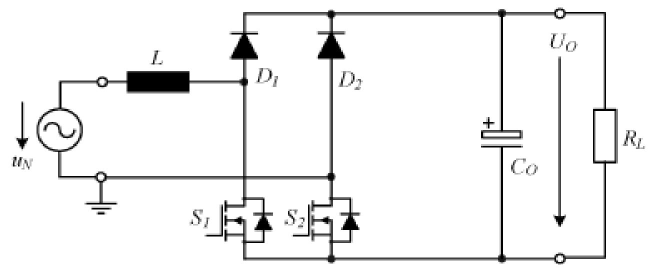


→ Clarifies Sensitivity $\Delta p / \Delta k$ to Improvements of Technologies
→ Trade-off Analysis

▶ Determination of the η-ρ-Pareto Front (a)

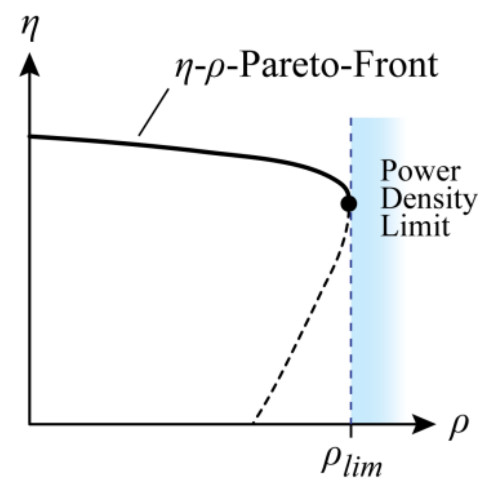
■ **Comp.-Level Degrees of Freedom of the Design**

— Core Geometry / Material
— Single / Multiple Airgaps
— Solid / Litz Wire, Foils
— Winding Topology
— Natural / Forced Conv. Cooling
— Hard-/Soft-Switching
— Si / SiC
— etc.
— etc.
— etc.



■ **System-Level Degrees of Freedom**

— Circuit Topology
— Modulation Scheme
— Switching Frequ.
— etc.
— etc.



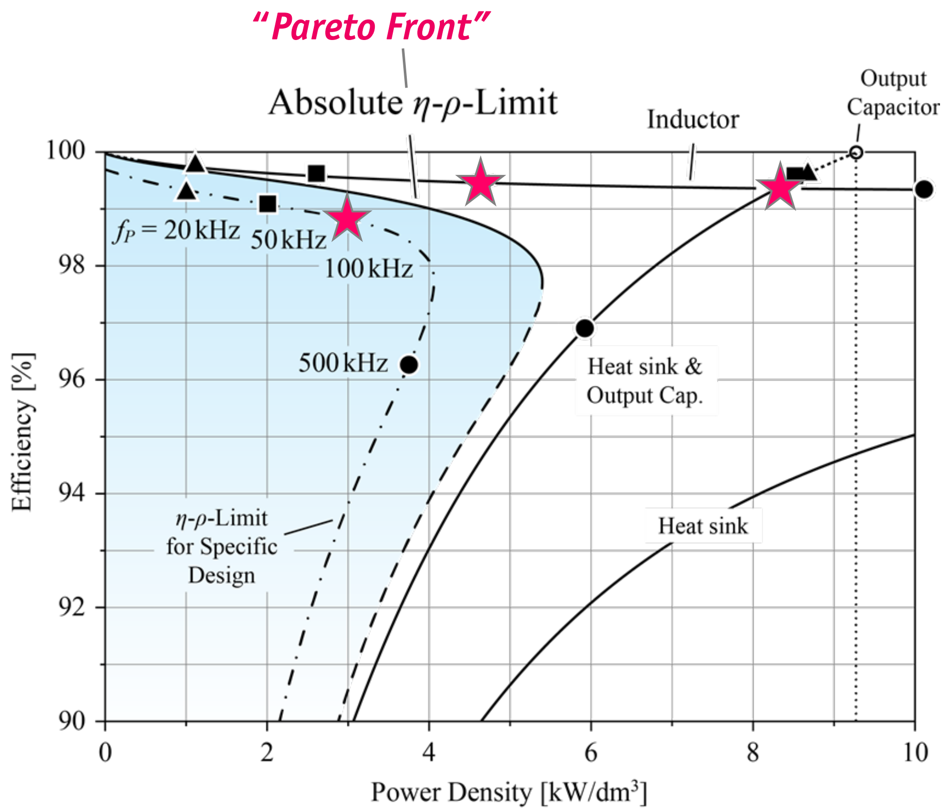
■ **Only η-ρ-Pareto Front Allows Comprehensive Comparison of Converter Concepts (!)**

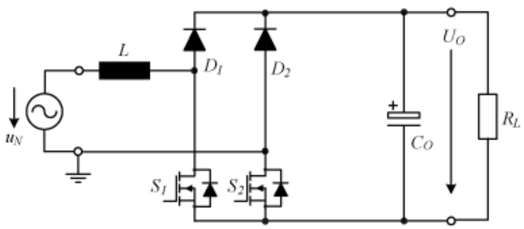
▶ Determination of the η-ρ-Pareto Front (b)

- **Example: Consider Only f_P as Design Parameter**

- **Only the Consideration of All Possible Designs / Degrees of Freedom Clarifies the Absolute η-ρ-Performance Limit**

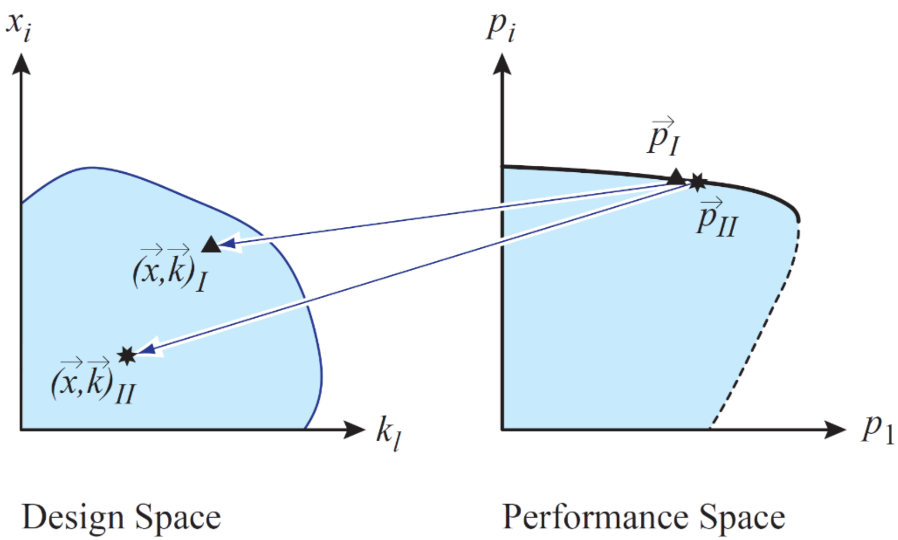
★ f_P =100kHz





▶ Multi-Objective Optimization (2)

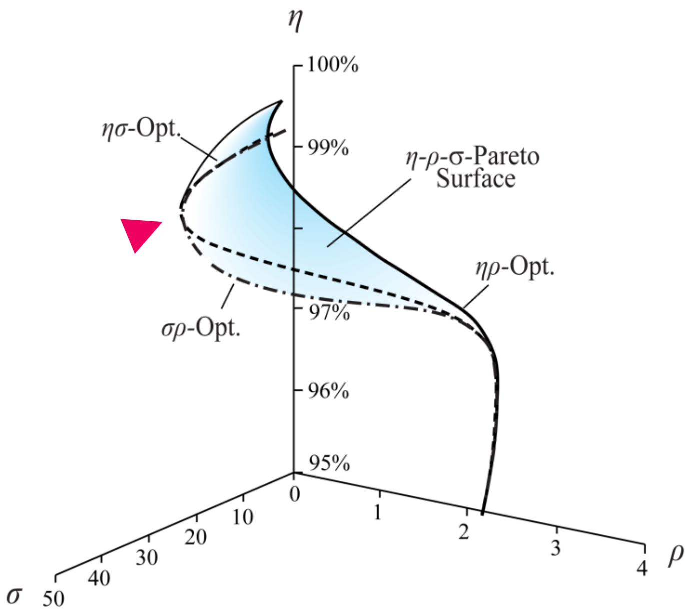
- Design Space Diversity
- Equal Performance for Largely Different Sets of Design Parameters

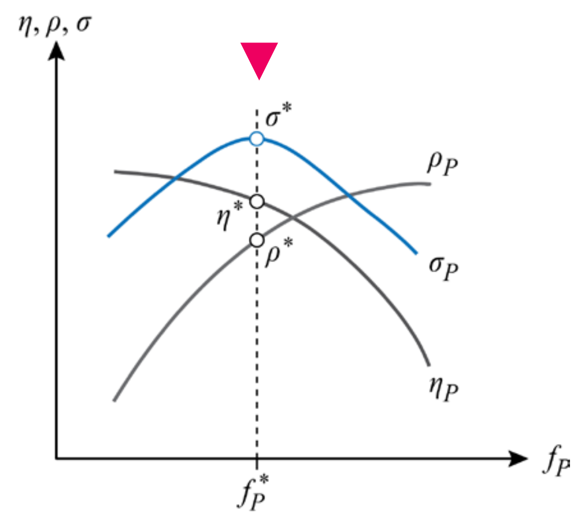


→ E.g. Mutual Compensation of Volume and Loss Contributions (e.g. Cond. & Sw. Losses)
→ Allows Optimization for Further Performance Index (e.g. Costs)

▶ Converter Performance Evaluation Based on η-ρ-σ-Pareto Surface

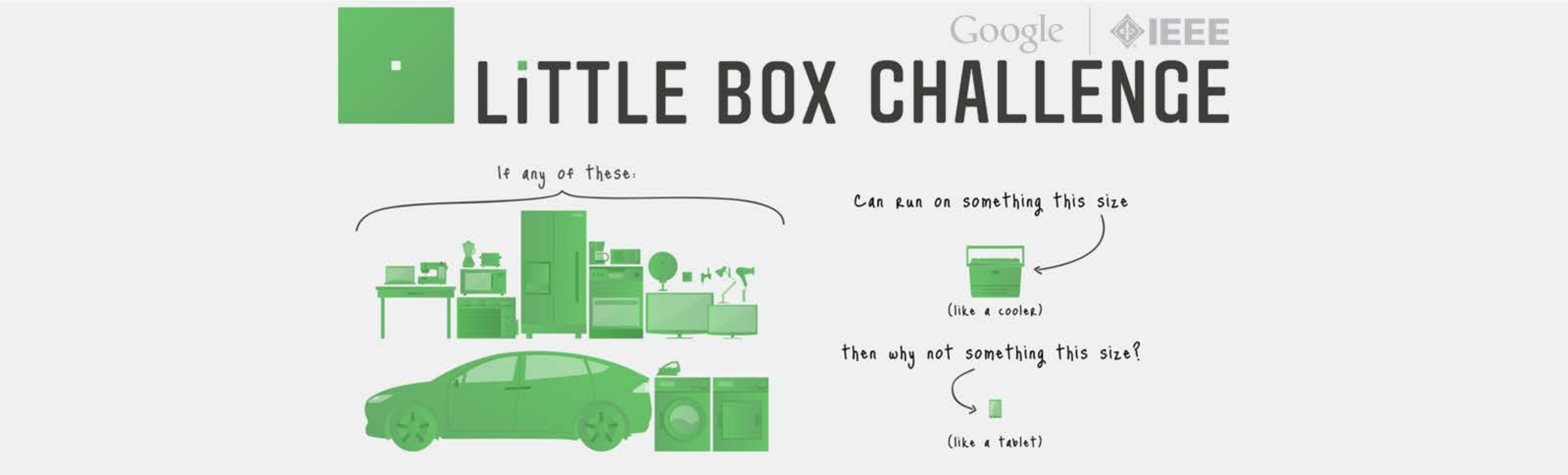
- Definition of a Power Electronics *"Technology Node"* → (η^*,ρ^*,σ^*,f_P^*)
- Maximum σ [kW/$], Related Efficiency & Power Density





→ Specifying Only a Single Performance Index is of No Value (!)
→ Achievable Perform. Depends on Conv. Type / Specs (e.g. Volt. Range) / Side Cond. (e.g. Cooling)

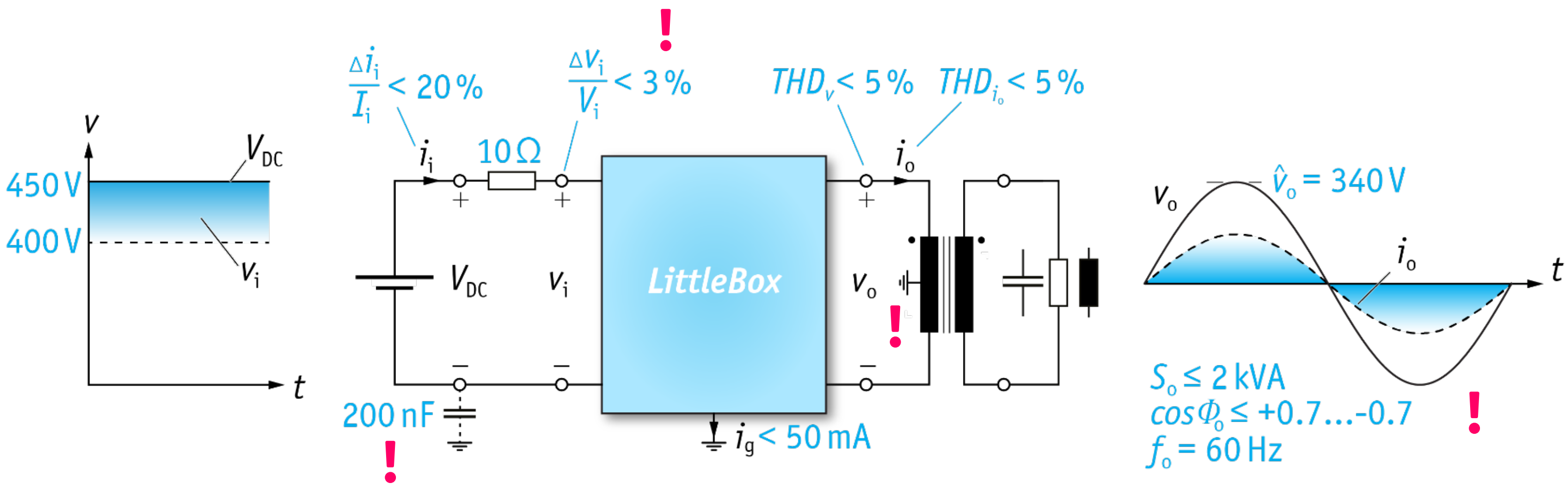
Case Study:
Google Little Box Challenge


Google | IEEE
LITTLE BOX CHALLENGE
If any of these:
Can run on something this size
(like a cooler)
then why not something this size?
(like a tablet)

LITTLE BOX CHALLENGE

Google | IEEE

- Design / Build the 2kW 1-ΦSolar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (> 50W/in³, multiply kW/dm³ by Factor 16)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B



■ **Push the Forefront of New Technologies in R&D of High Power Density Inverters**

The Grand Prize

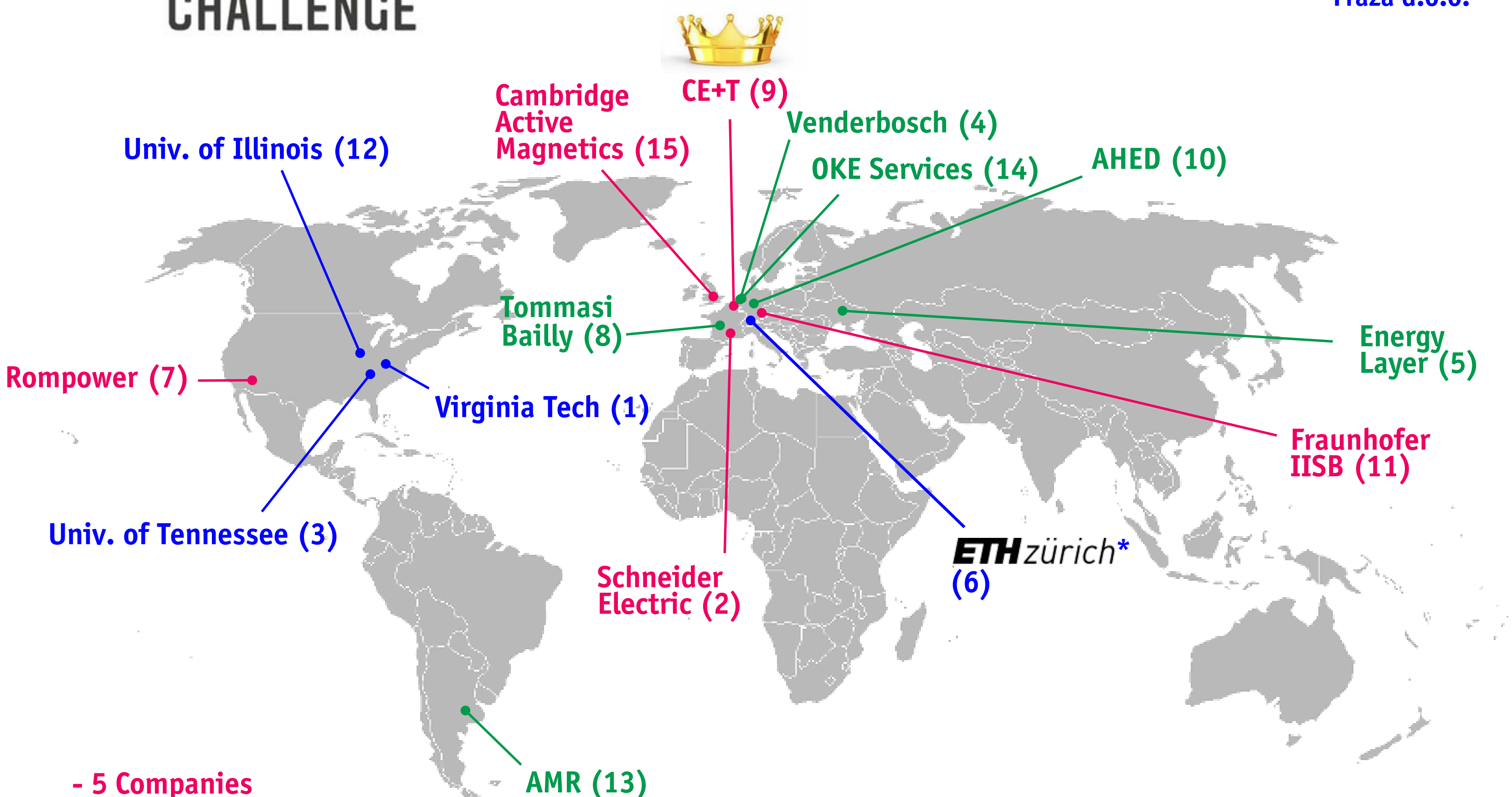
- Highest Power Density (> 50W/in^3)
- Highest Level of Innovation

$1,000,000

- Timeline
  - Challenge Announced in Summer 2014
  - 650 Teams Worldwide
  - 100+ Teams Submitted a Technical Description until July 22, 2015
  - 18 Finalists / Presentation @ NREL on Oct. 21, 2015, Golden, Colorado, USA
  - Testing @ NREL / Winner will be Announced in Early 2016

LiTTLE BOX CHALLENGE Finalists

* and FH IZM / Fraza d.o.o.



- 5 Companies
- 6 Consultants
- 4 Universities

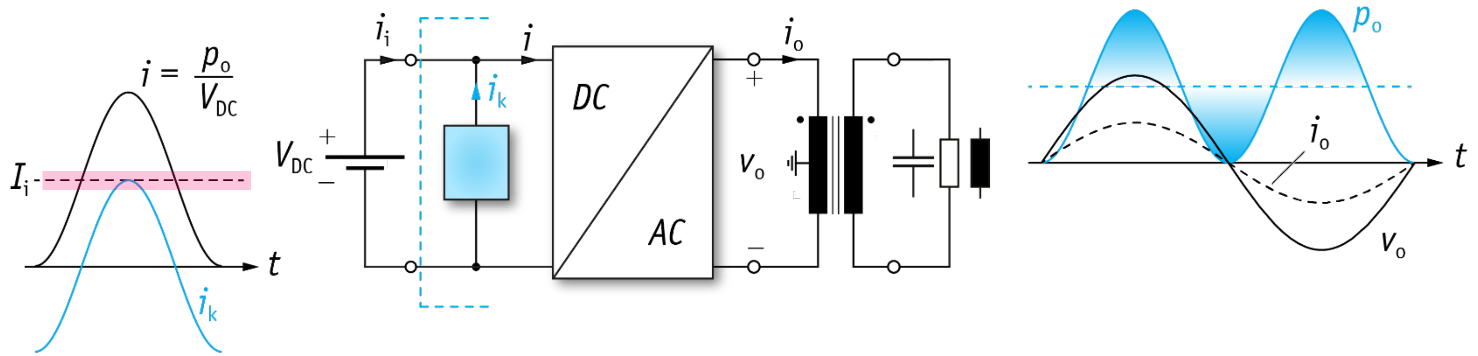
15 Teams/Participants in the Final @ NREL
Note: Numbering of Teams is Arbitrary

Little Box 1.0

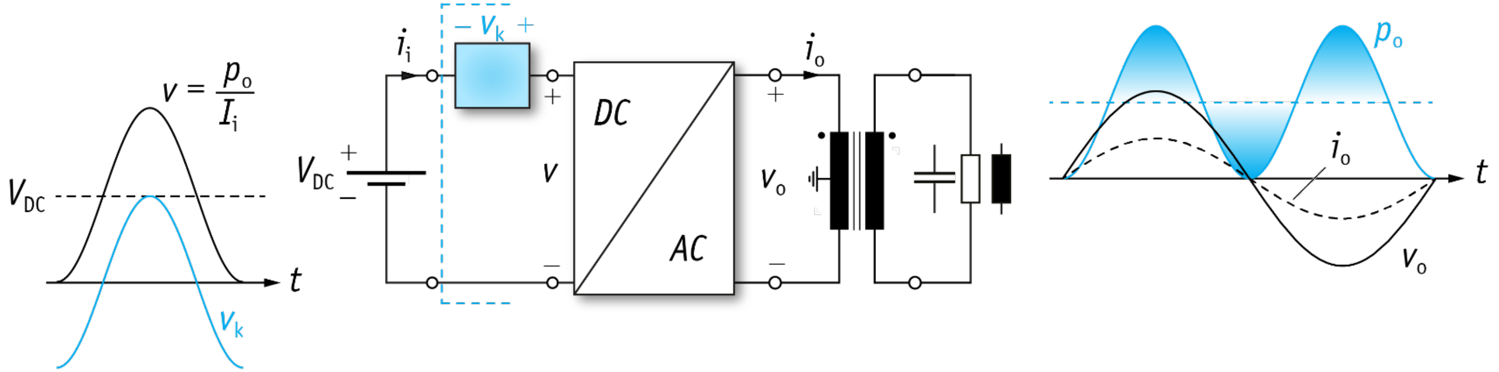
Power Pulsation Buffer
Inverter Topology
GaN Power Stage
Multi Air Gap Inductor
Thermal Management
Performance of Prototype System

▶ Power Pulsation Buffer

- **Parallel Buffer @ DC Input**



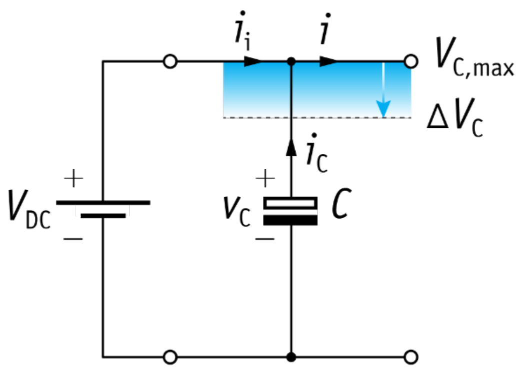
- **Series Buffer @ DC Input**

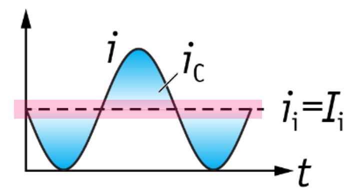


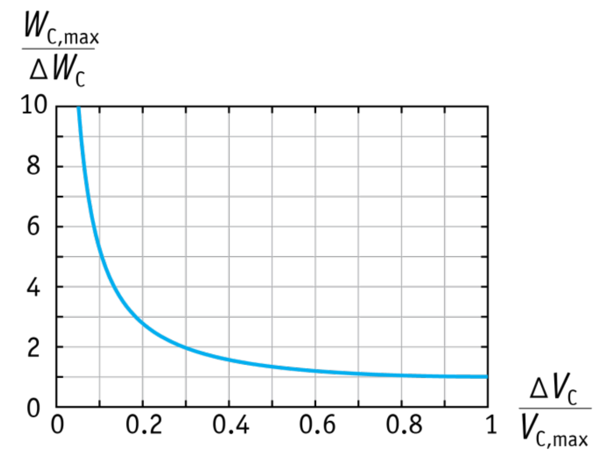
■ **Parallel Approach for Limiting Voltage Stress on Converter Stage Semiconductors**

▶ Passive Power Pulsation Buffer

- **Electrolytic Capacitor**







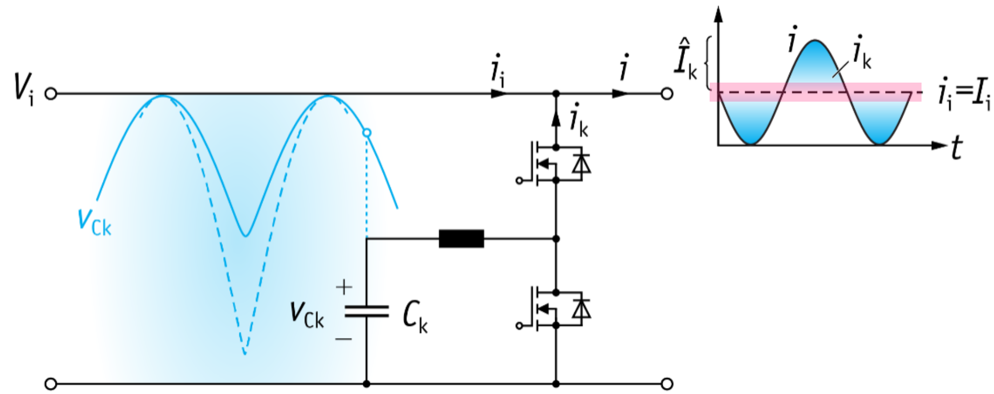
S_0 = 2.0 kVA
cos Φ_0 = 0.7
$V_{C,max}$ = 450 V
$\Delta V_C / V_{C,max}$ = 3 %

EPCOS
5 x 493μF/450 V
C = 2.46 mF

- **C > 2.2mF / 166 cm³ → Consumes 1/4 of Allowed Total Volume !**

▶ Full Active Power Pulsation Buffer (1)

- Large Voltage Fluctuation Foil or Ceramic Capacitor
- Buck- or Boost-Type DC/DC Interface Converter
- Buck-Type allows Utilizing 600V Technology



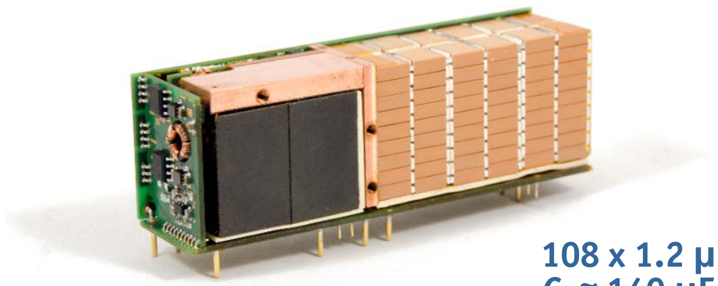
CeraLink TDK

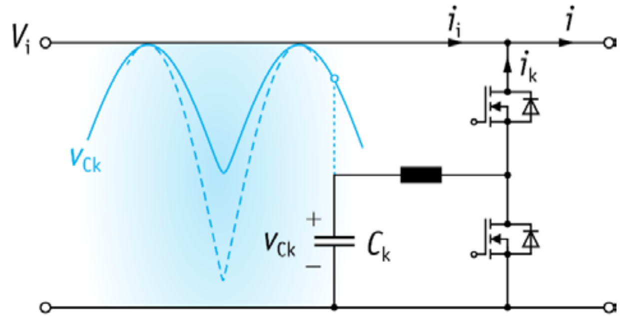
108 x 1.2 µF /400 V
$C_k \approx 140$ µF
$V_{Ck} = 23.7 cm^3$

- Significantly Lower Overall Volume Compared to Electrolytic Capacitor

▶ Full Active Power Pulsation Buffer (2)

- Large Voltage Fluctuation Foil or Ceramic Capacitor
- Buck- or Boost-Type DC/DC Interface Converter
- Buck-Type allows Utilizing 600V Technology





108 x 1.2 µF /400 V
$C_k \approx 140\ \mu F$
$V_{Ck} = 23.7 cm^3$

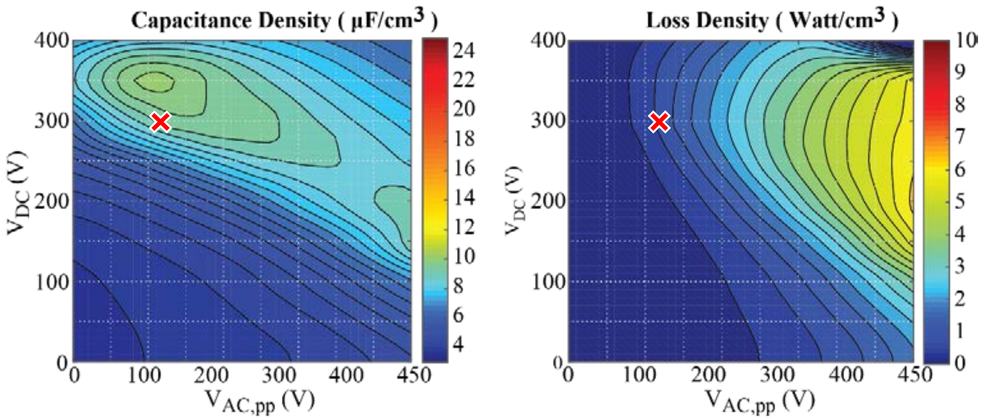
■ Significantly Lower Overall Volume Compared to Electrolytic Capacitor

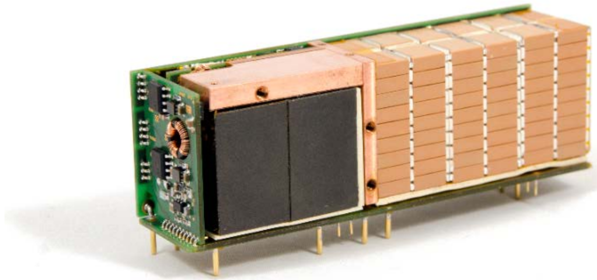
▶ CeraLink vs. Class II MLCC (X6S) Large-Signal Analysis

- **Variation of DC Bias and Superimposed AC Voltage @ 60°C Operating Temp.**

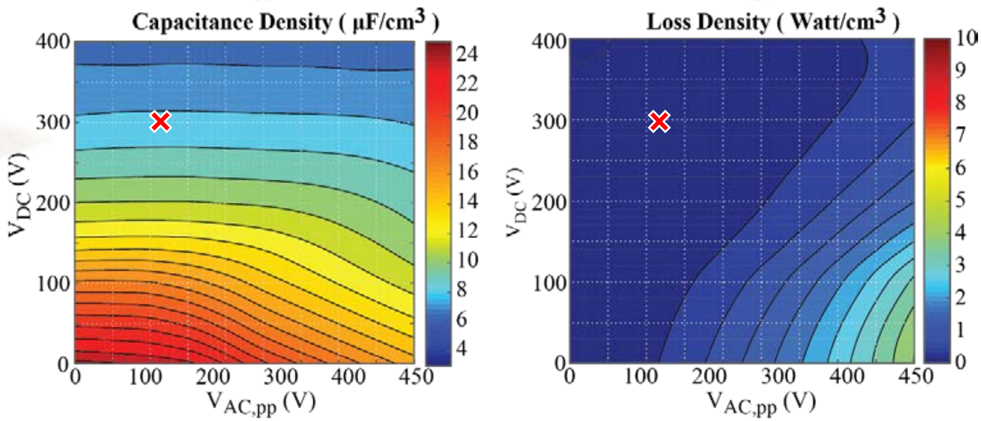
✕ **Designed Op. Point**

EPCOS/TDK CeraLink 2μF, 600V ▶





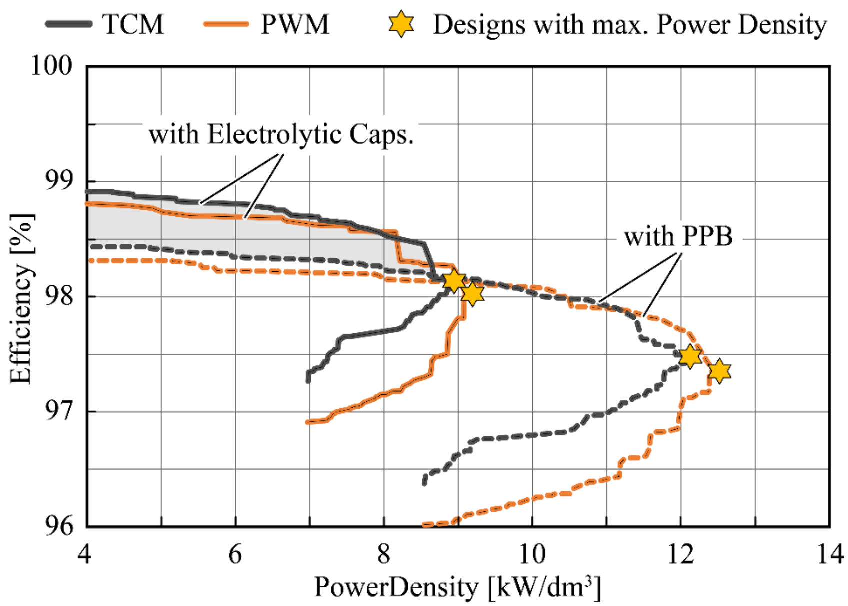
TDK Class II X6S MLCC 2.2μF, 450V ▶



■ **PPB Design Optimiz. Requires Large-Signal Capacitance and Power Loss Data in All Operating Points**

► Power Pulsation Buffer (PPB) vs. Electrolytic Capacitor

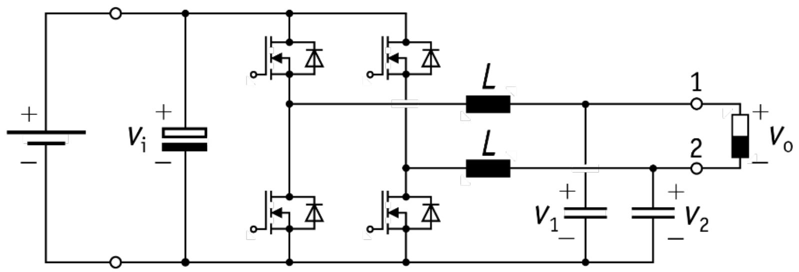
- Analysis for Google Little Box Challenge Specification ΔV/V < 3%
- Efficiency Benefit of PPB only for ρ > 9kW/dm³

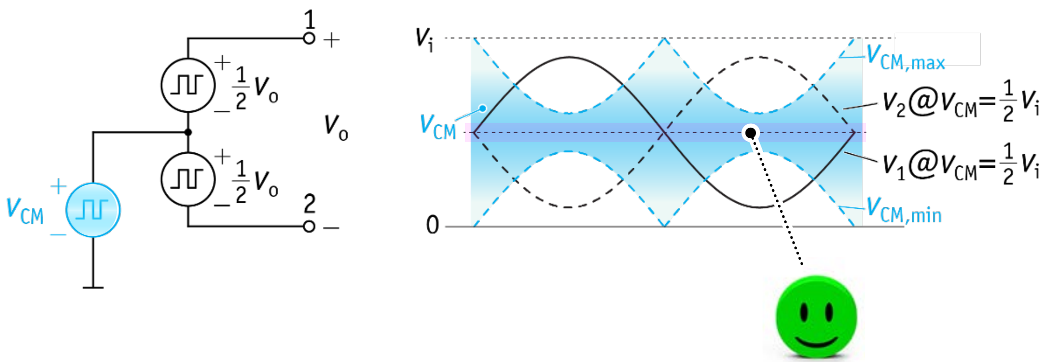


- Electrolytics Favorable for High Efficiency @ Moderate Power Density ($\Delta\eta$= +0.5%)
- Electrolytics Show Lower Vol. & Lower Losses if Large ΔV/V is Acceptable (e.g. for PFC Rectifiers)

▶ Symmetric PWM Full-Bridge AC/DC Conv. Topology

- Symmetric PWM Operation of Both Bridge Legs
- No Low-Frequency CM Output Voltage Component

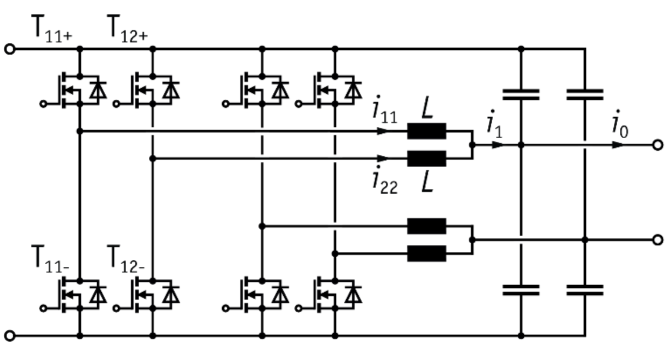


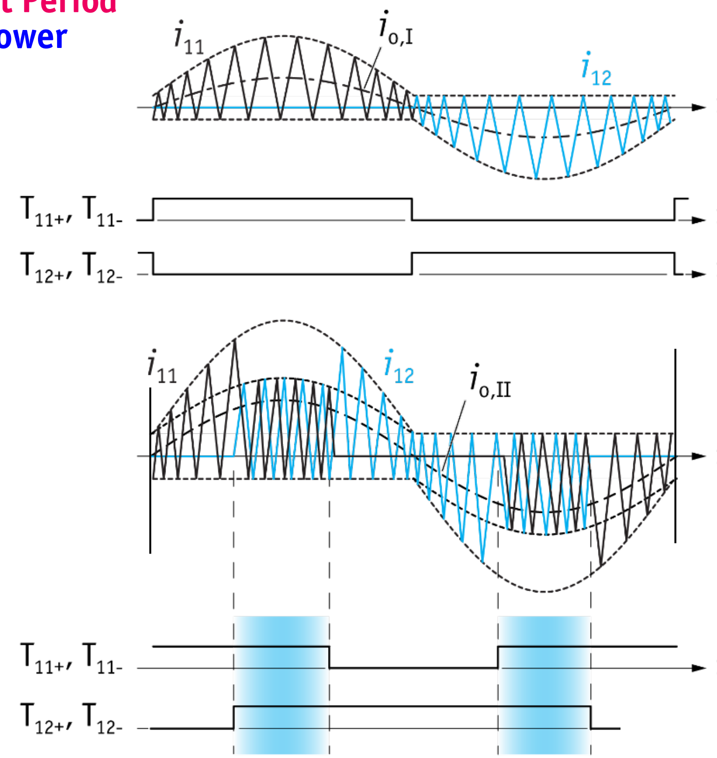


- DM Component of u_1 and u_2 Defines Output u_0
- CM Component of u_1 and u_2 Represents Degree of Freedom of the Modulation (!)

▶ 4D - Interleaving

- Interleaving of 2 Bridge Legs per Phase - Volume / Filtering / Efficiency Optimum
- Interleaving in Space & Time – Within Output Period
- Alternate Operation of Bridge Legs @ Low Power
- Overlapping Operation @ High Power

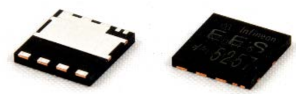




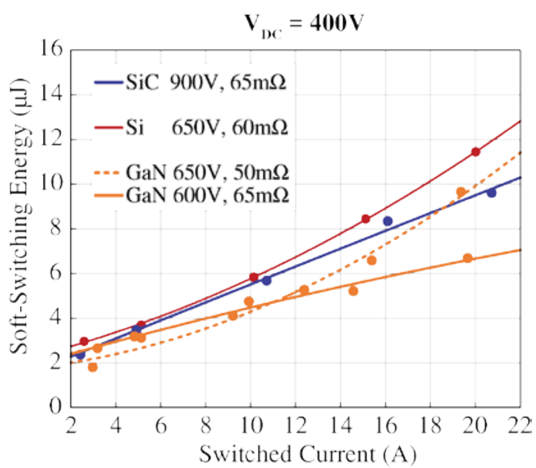
■ Opt. Trade-Off of Conduction & Switching Losses / Opt. Distribution of Losses

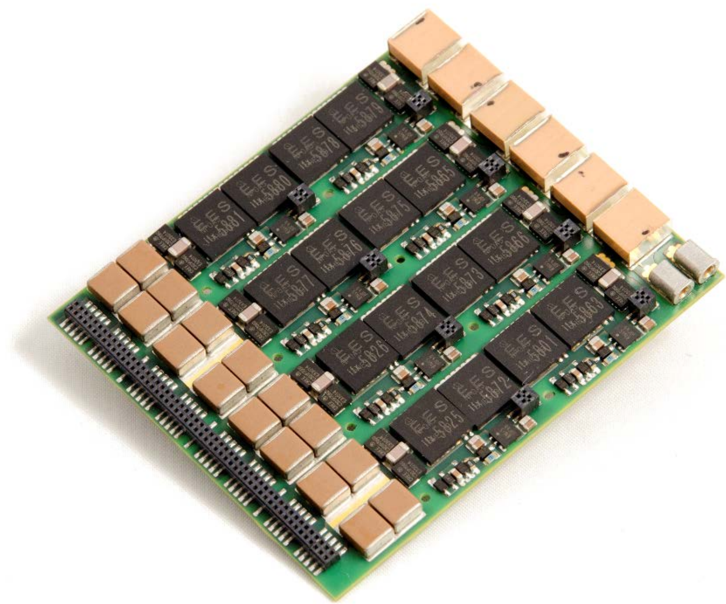
▶ Selected Power Semiconductors

- 600V IFX Normally-Off GaN GIT - ThinPAK8x8
- 2 Parallel Transistors / Switch
- Antiparallel CREE SiC Schottky Diodes



- 1.2V typ. Gate Threshold Voltage
- 55 mΩ $R_{DS,on}$ @ 25°C, 120mΩ @ 150°C
- 5Ω Internal Gate Resistance



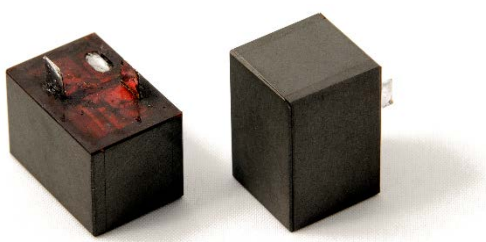


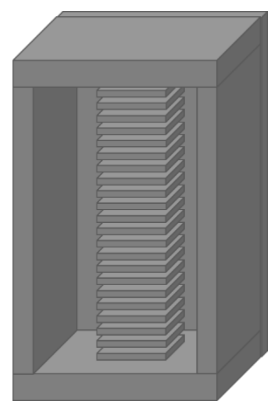
- CeraLink Capacitors for DC Voltage Buffering

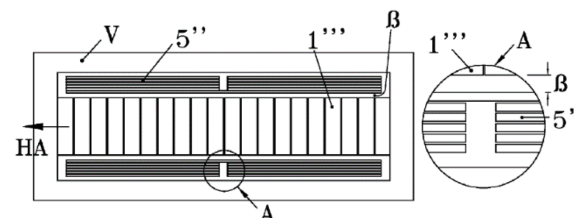
High Frequency Multi Air Gap Inductor

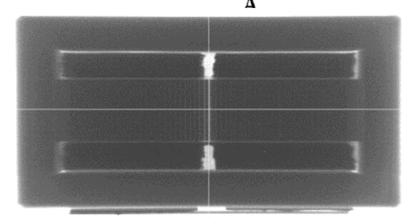
- Multi-Airgap Inductor with Multi-Layer Foil Winding Arrangement Minim. Prox. Effect
- Very High Filling Factor / Low High Frequency Losses
- Magnetically Shielded Construction Minimizing EMI
- Intellectual Property of F. Zajc / Fraza

- L= 10.5µH
- 2 x 8 Turns
- 24 x 80µm Airgaps
- Core Material DMR 51 / Hengdian
- 0.61mm Thick Stacked Plates
- 20 µm Copper Foil / 4 in Parallel
- 7 µm Kapton Layer Isolation
- 20mΩ Winding Resistance / Q≈600
- Terminals in No-Leakage Flux Area







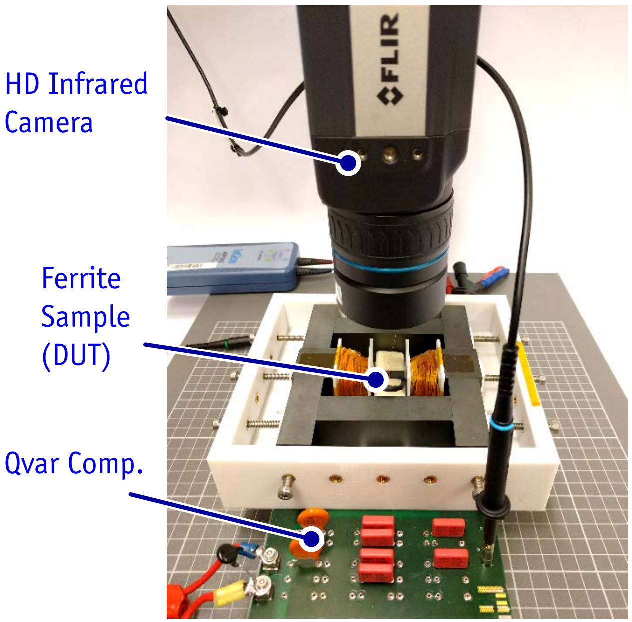


- Dimensions - 14.5 x 14.5 x 22mm^3

▶ Composite Core - Temperature Rise Recording

■ Temperature Rise Comparison of Solid Core and MAG Sample

- Sinusoidal Excitation 100 mT / 400 kHz
- Solid 3F4 (1 x 21.6 mm) vs. MAG 3F4 (7 x 3mm)
- ΔT = 10 °C, T_0 = 26.3 °C



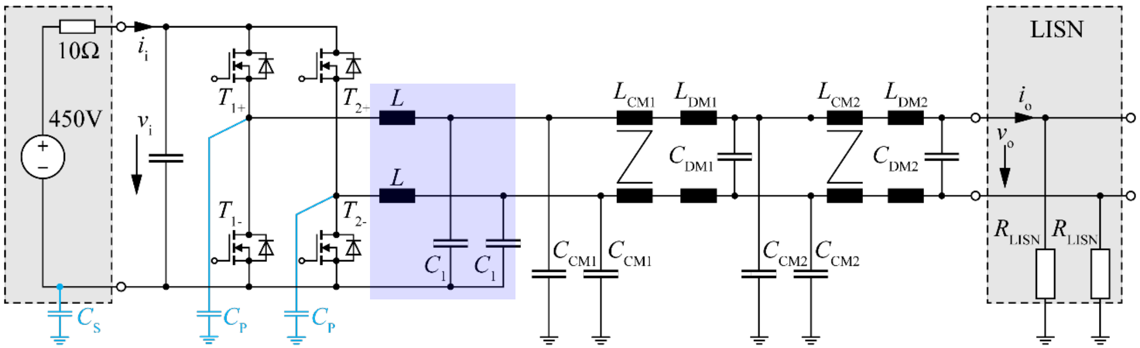
▲ Surface Loss Test Setup W/ Res. Cap. Bank and Infrared Camera

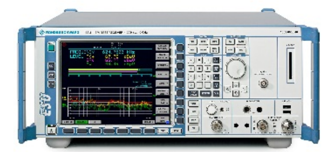
▲ 3F4 Solid Sample Temperature Rise

▲ 3F4 MAG Sample (7 x 3mm) Temperature Rise

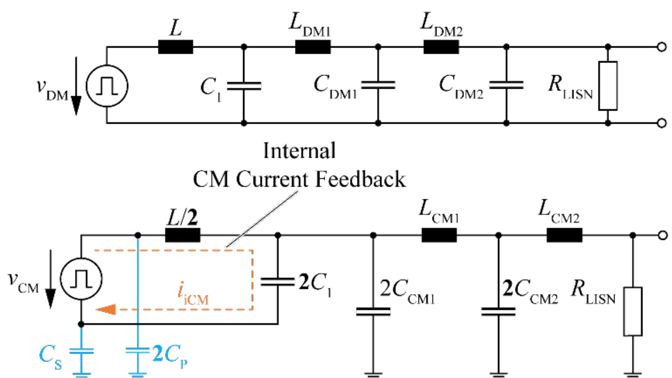
▶ EMI Filter (1)

- Filter Structure with Internal CM Capacitor Feedback
- Filtering to DC- (and optional to DC+)





Test Receiver

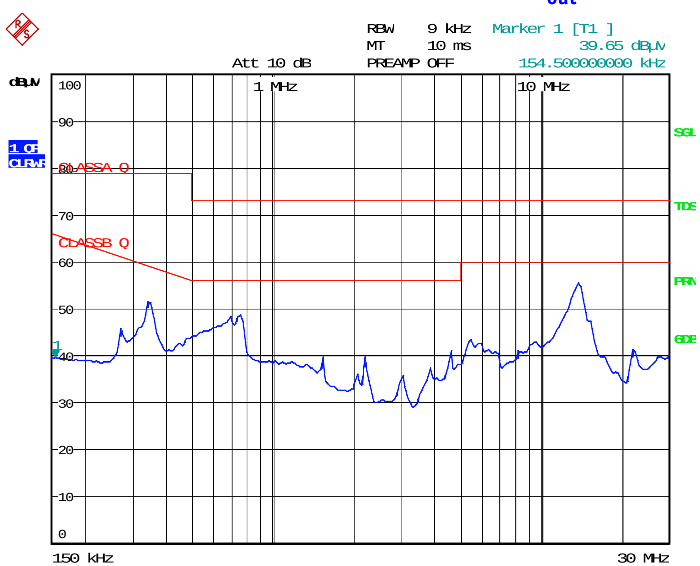


- No Limitation of CM Capacitor C_1 Due to Earth Current Limit → µF Instead of nF Can be Employed
- Allows Downsizing of CM Inductor and/or Total Filter Volume

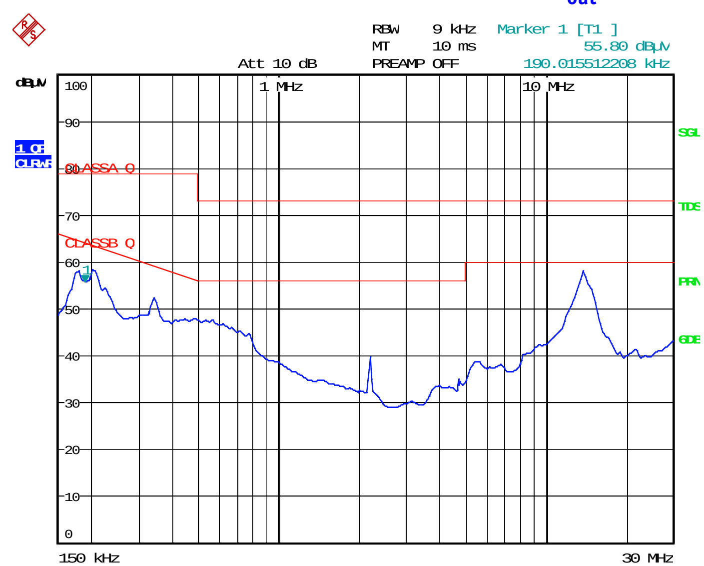
▶ EMI Filter (2)

- **System Employing Electrolytic Capacitors as 1-Φ Power Pulsation Buffer**

P_{out}= 400W



P_{out}= 2kW

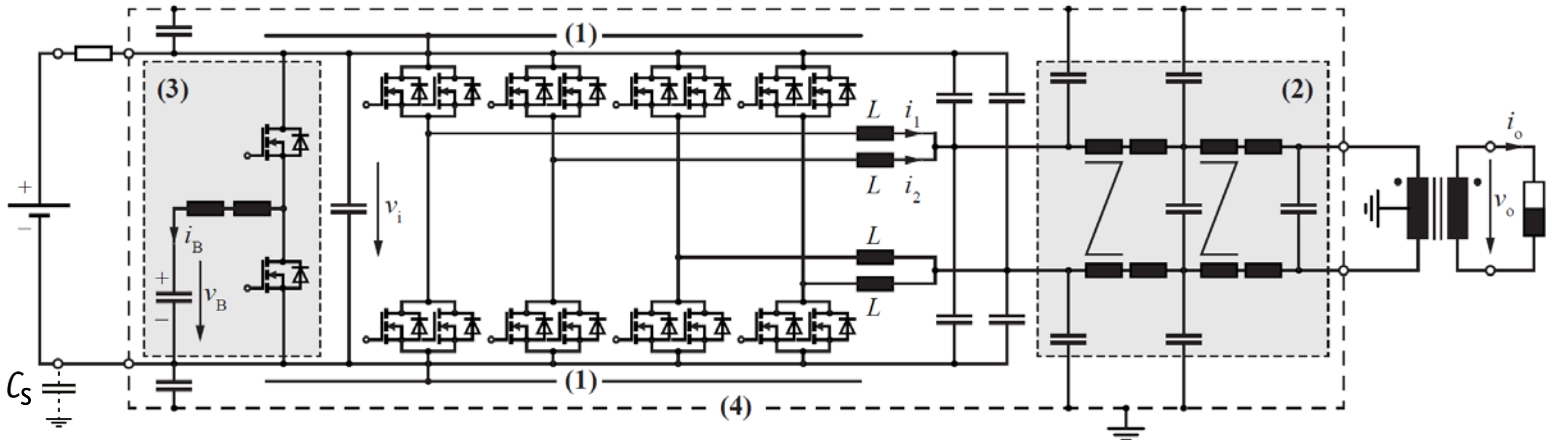


- **Compliant to All Specifications**

▶ Complete Little Box 1.0 Converter Topology

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- 2-Stage EMI AC Output Filter

(1) Heat Sink
(2) EMI Filter
(3) Power Pulsation Buffer
(4) Enclosure

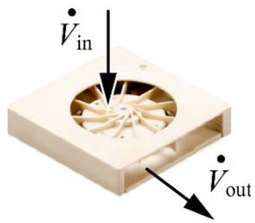


- ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM-Interleaving)
- Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure

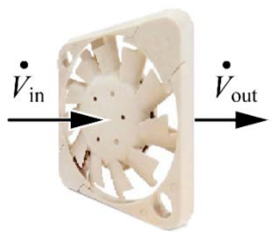
▶ Thermal Management Building Blocks

- **Overall Cooling Performance Defined by Selected Fan Type and Heatsink**

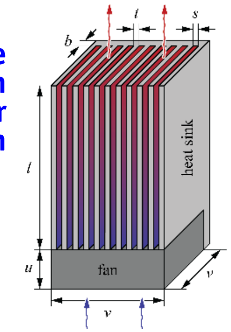
– Radial Blower



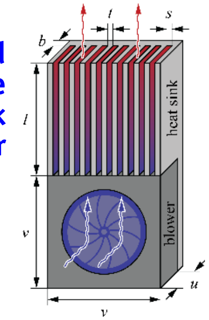
– Axial Fan

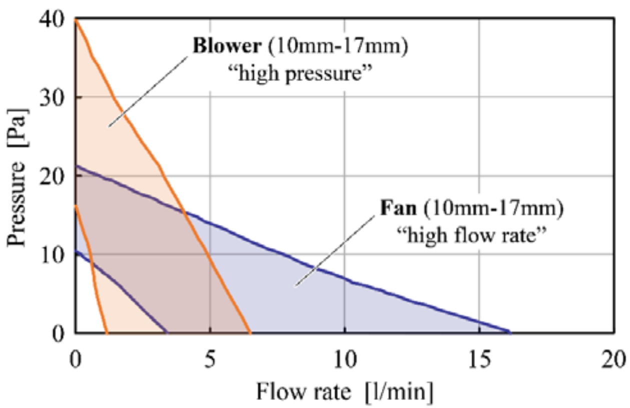


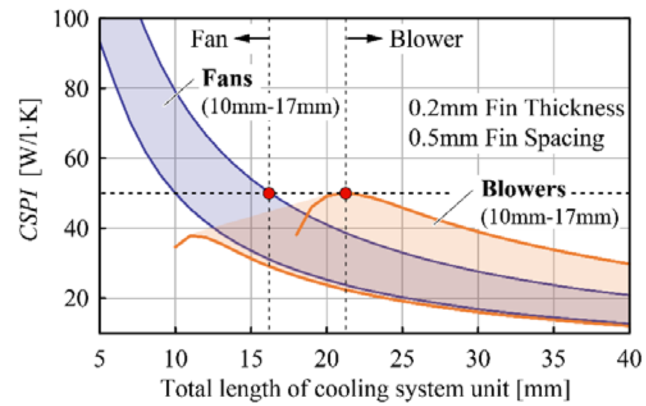
– Square Cross Section of Heatsink for Using a Fan



– Flat and Wide Heatsink for Blower





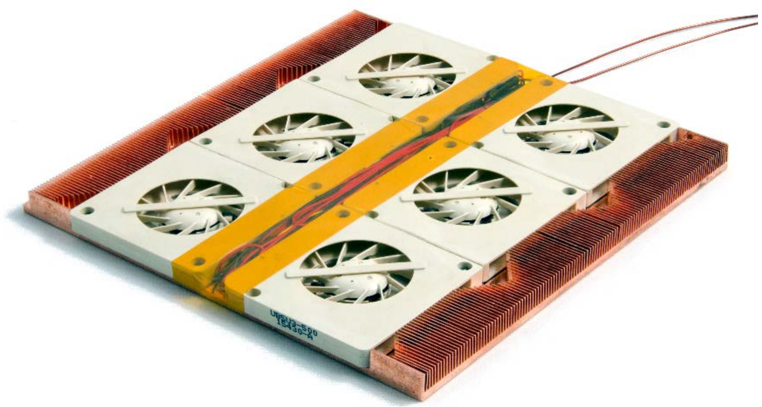


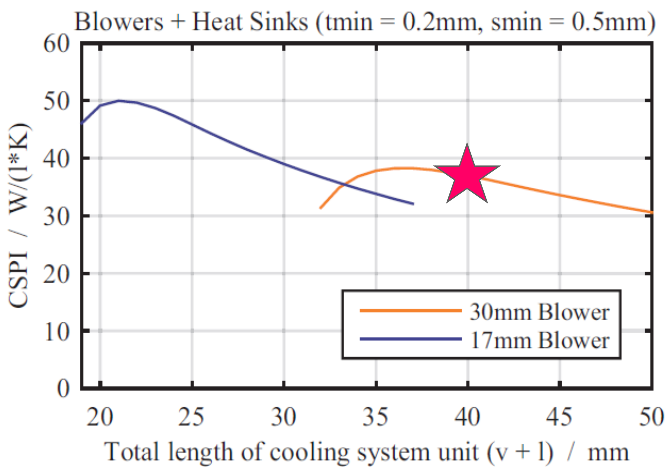
- Optimal Fan and Heat Sink Configuration Defined by Total Cooling System Length
- Cooling Concept with Blower Selected → Higher *CSPI* for Larger Mounting Surface

▶ Final Thermal Management Concept

- 30mm Blowers with Axial Air Intake / Radial Outlet
- Full Optimization of the Heatsink Parameters

- 200um Fin Thickness
- 500um Fin Spacing
- 3mm Fin Height
- 10mm Fin Length
- CSPI = 37 W/(dm³.K)
- 1.5mm Baseplate





- $CSPI_{eff}$= 25 W/(dm³.K) Considering Heat Distribution Elements
- Two-Side Cooling → Heatsink Temperature = 52°C @ 80W (8W by Natural Convection)

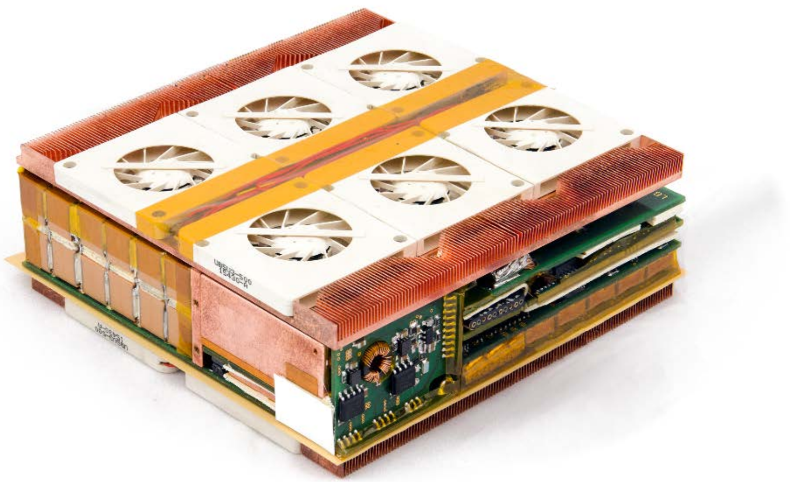
▶ Little Box 1.0 – Prototype (1)

- System Employing Active 1-Φ Power Pulsation Buffer

- 8.2 kW/dm³
- 8.9cm x 8.8cm x 3.1cm
- 96,3% Efficiency @ 2kW
- T_c=52°C @ 2kW

- Δu_{DC}= 1.1%
- Δi_{DC}= 2.8%
- $THD{+}N_U$ = 2.6%
- $THD{+}N_I$ = 1.9%

★ 135 W/in³



■ Compliant to All *Original* Specifications (!)

- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

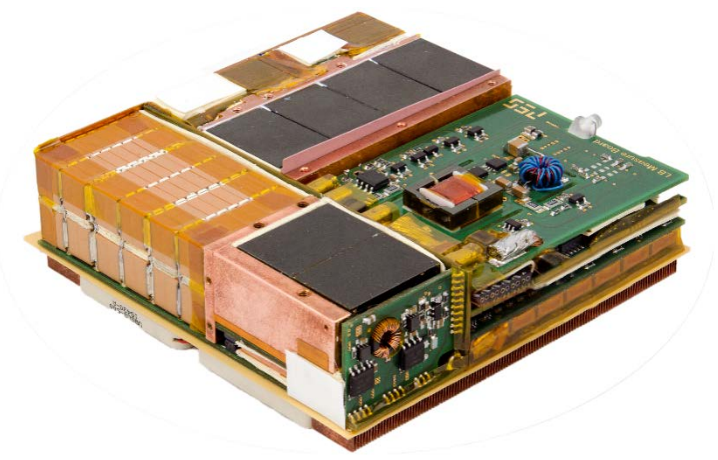
▶ Little Box 1.0 – Prototype (2)

- System Employing Active 1-Φ Power Pulsation Buffer

- 8.2 kW/dm^3
- 8.9cm x 8.8cm x 3.1cm
- 96,3% Efficiency @ 2kW
- T_c=52°C @ 2kW

- Δu_{DC}= 1.1%
- Δi_{DC}= 2.8%
- $THD+N_U$ = 2.6%
- $THD+N_I$ = 1.9%

★ 135 W/in^3



■ Compliant to All *Original* Specifications (!)

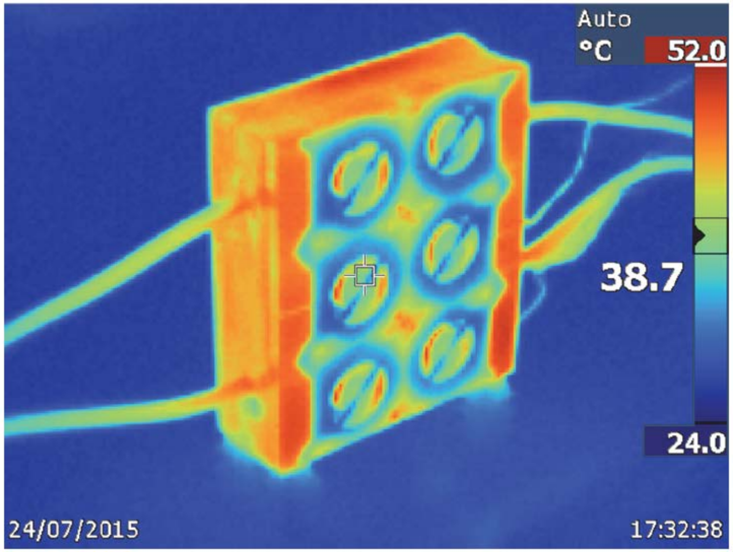
- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

▶ Little Box 1.0 – Prototype (3)

- System Employing Active 1-Φ Power Pulsation Buffer

- 8.2 kW/dm³
- 8.9cm x 8.8cm x 3.1cm
- 96,3% Efficiency @ 2kW
- T_c=52°C @ 2kW

- Δu_{DC}= 1.1%
- Δi_{DC}= 2.8%
- $THD{+}N_U$ = 2.6%
- $THD{+}N_I$ = 1.9%



■ Compliant to All *Original* Specifications (!)

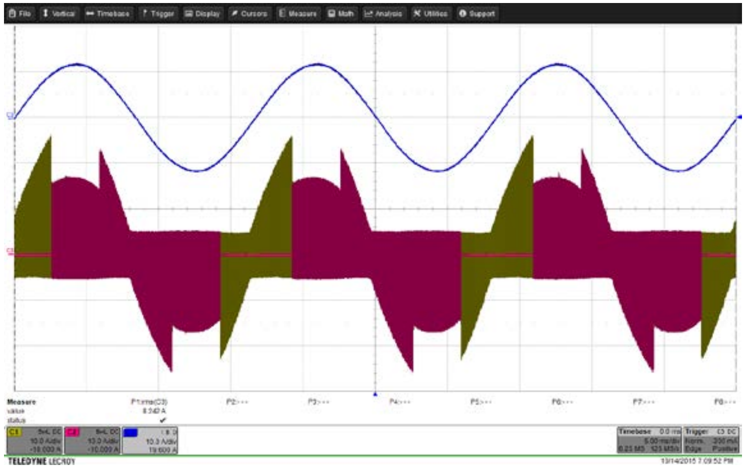
- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

▶ Little Box 1.0 – Measurement Results

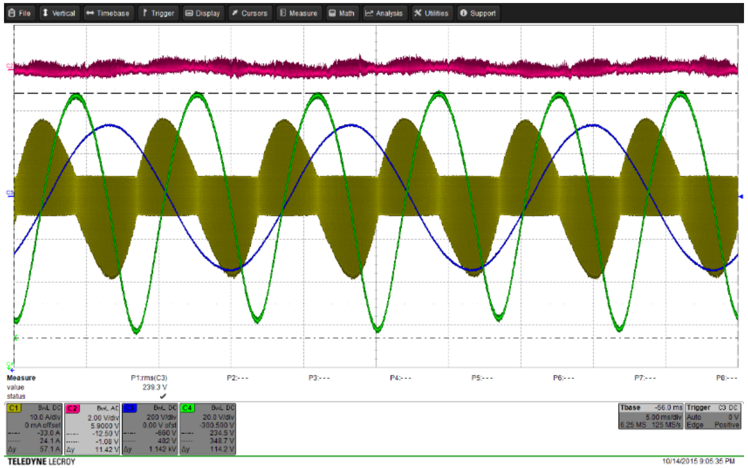
- System Employing Active Ceralink 1-Φ Power Pulsation Buffer

  - Ohmic Load / 2kW

Output Current (10 A/div)
Inductor Current Bridge Leg 1-1 (10 A/div)
Inductor Current Bridge Leg 1-2 (10 A/div)



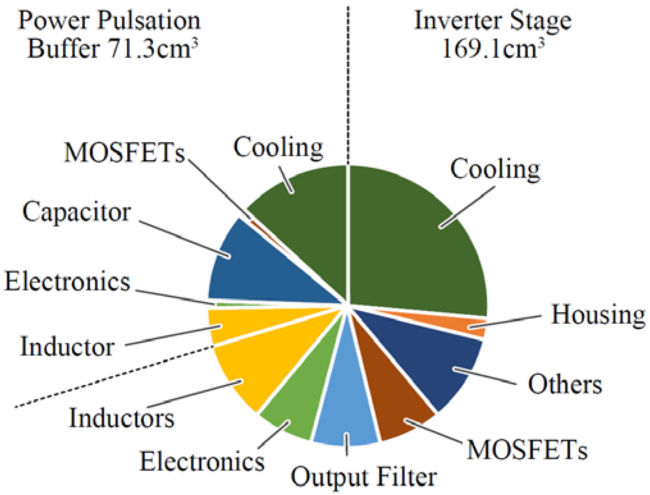
DC Link Voltage (AC-Coupl., 2 V/div)
Buffer Cap. Voltage (20 V/div)
Buffer Cap. Current (10 A/div)
Output Voltage (200 V/div)



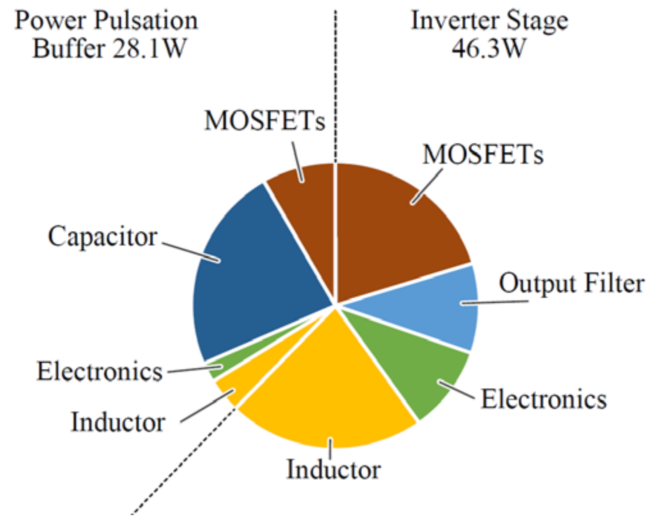
■ Compliant to All Specifications

▶ Little Box 1.0 – Volume & Loss Distribution

- **Volume Distribution (240cm³)**

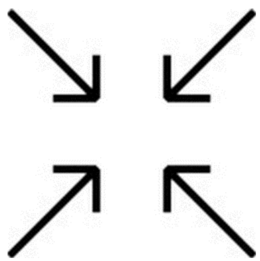


- **Loss Distribution (75W)**



- **Large Heatsink (incl. Heat Conduction Layers)**
- **Large Losses in Power Fluctuation Buffer Capacitor (!)**
- **TCM Causes Relatively High Conduction & Switching Losses @ Low Power**
- **Relatively Low Switching Frequency @ High Power – Determines EMI Filter Volume**

Little Box 2.0

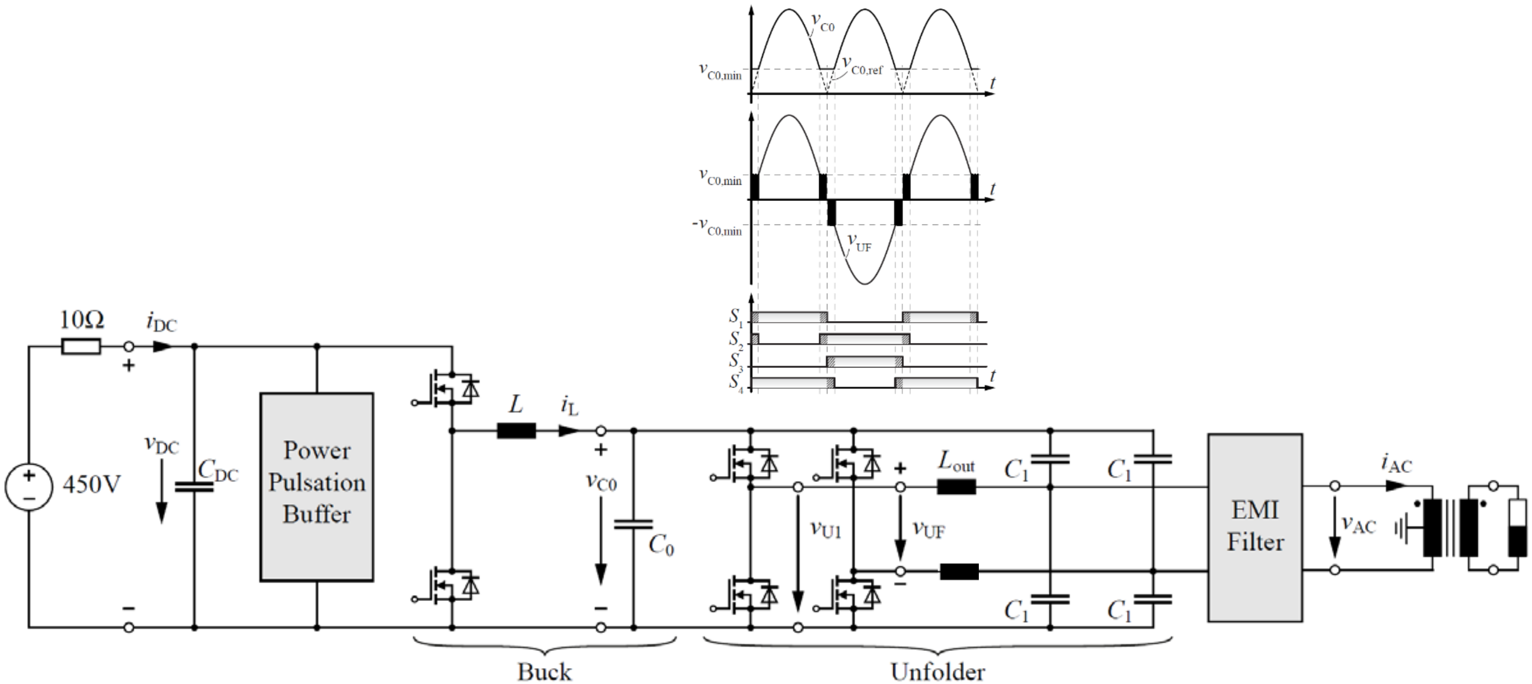


250 W/in³

DC/ | AC | Converter + Unfolder
PWM vs. TCM incl. Interleaving
ηρ-Pareto Limits for Non-Ideal Switches
Preliminary Exp. Results

► Little Box 2.0 – New Converter Topology

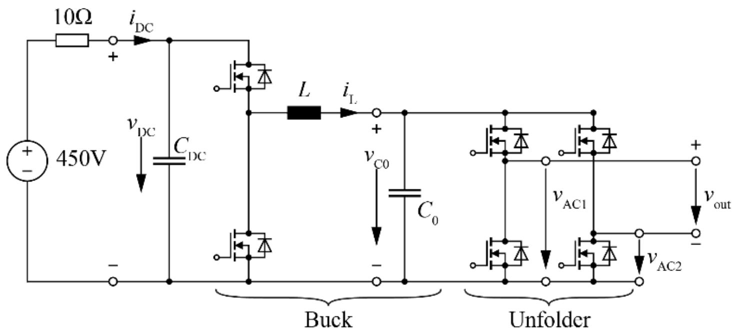
- Alternative Converter Topology - DC/|AC|- Buck Converter + Unfolder
- 60Hz-Unfolder (Temporary PWM for Ensuring Continuous Current Control)
- TCM or PWM of DC/|AC|- Buck-Converter

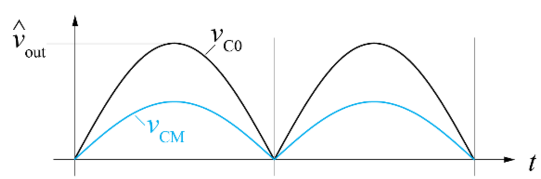


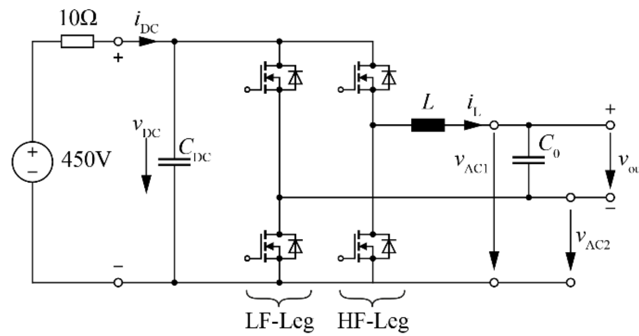
■ Full Optimization of All Converter Options for Real Switches / X6S Power Pulsation Buffer

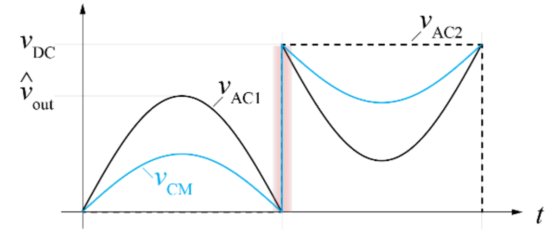
▶ Little Box 1.0 – New Converter Topology (2)

- Alternative Converter Topology → Only Single HF Bridge Leg + 60Hz-Unfolder
- DC/ | AC | - Buck Converter + Full-Bridge Unfolder OR HF Half-Bridge & Half-Bridge Unfolder







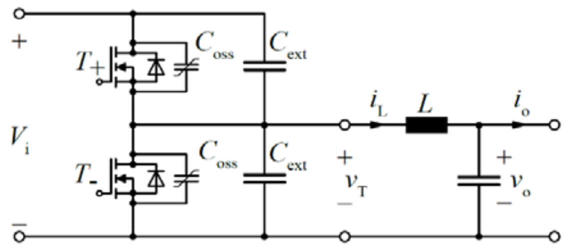


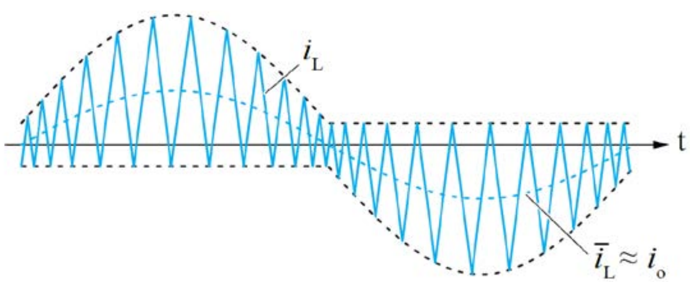
- v_{C0} Easy to Generate/Control
- Higher Conduction Losses Due to FB-Unfolder
- Lower CM-Noise (DC & n x 120Hz-Comp.)
- C_{CM}=700nF Allowed for 50mA

- v_{AC1} More Difficult to Generate/Control
- Lower Conduction Losses
- Higher CM-Noise (DC and n x 120Hz-Comp.)
- C_{CM}=150nF Allowed for 50mA

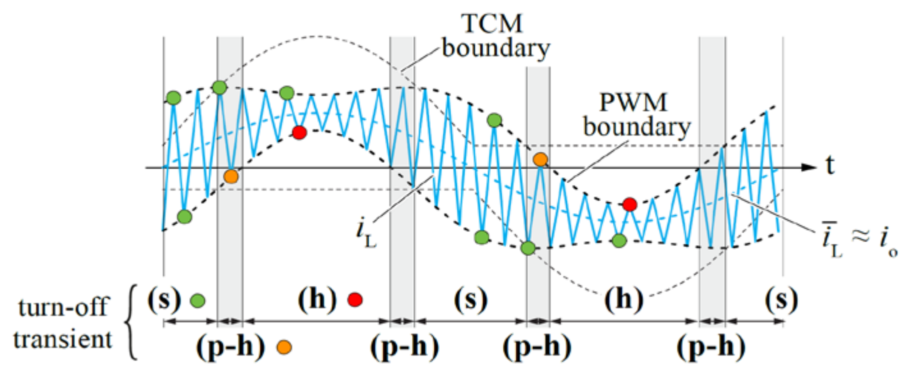
▶ TCM Vs. PWM W/ Large Current Ripple

- Very High Sw. Frequency f_S of TCM Around Current Zero Crossings
- Efficiency Reduction due to Residual TCM Sw. Losses & Gate Drive Losses Reduction
- Wide f_S -Variation Represents Adv. & Disadvantage for EMI Filter Design





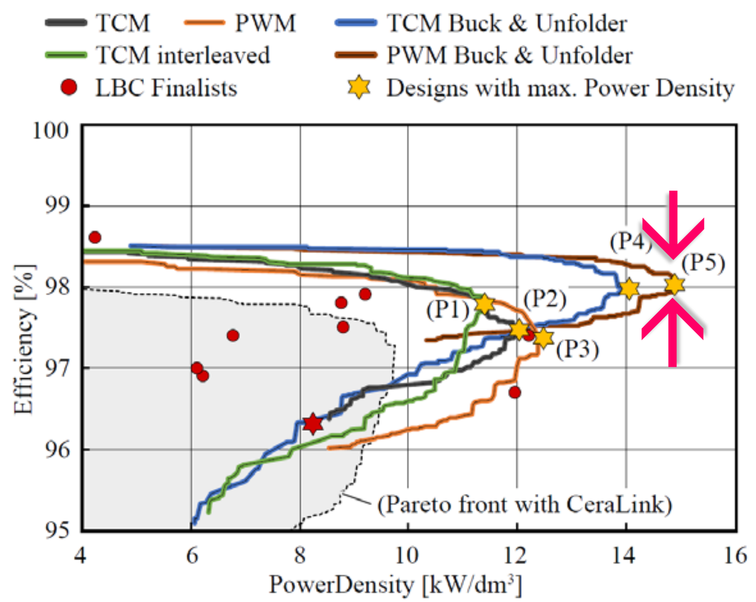
(s) Soft-Switching (ZVS)
(p-h) Partial Hard Switching
(h) Hard-Switching



- PWM -- Const. Sw. Frequency & Lower Conduction Losses
- PWM @ Large Current Rippel -- ZVS in Wide Intervals

▶ Little Box – Multi-Objective Optimization

- DC/|AC| - Buck Converter + Unfolder & PWM Shows Best Performance
- Full-Bridge Employs 2 Switching Bridge Legs - Larger Volume & Losses
- Interleaving Not Advantageous – Lower Heatsink Vol. but Larger Total Vol. of Switches and Inductors



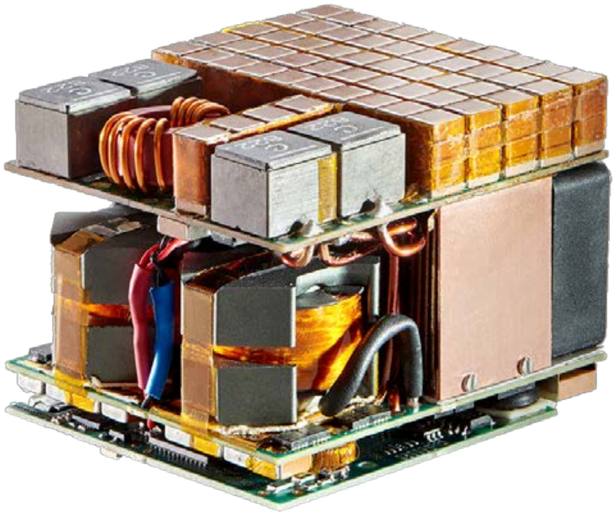
- ρ= 250W/in^3 (15kW/dm^3) @ η= 98% Efficiency Achievable for Full Optimization

▶ Little Box 2.0 – Prototype

- System Employing Active 1-Φ Power Pulsation Buffer

★ 243 W/in^3

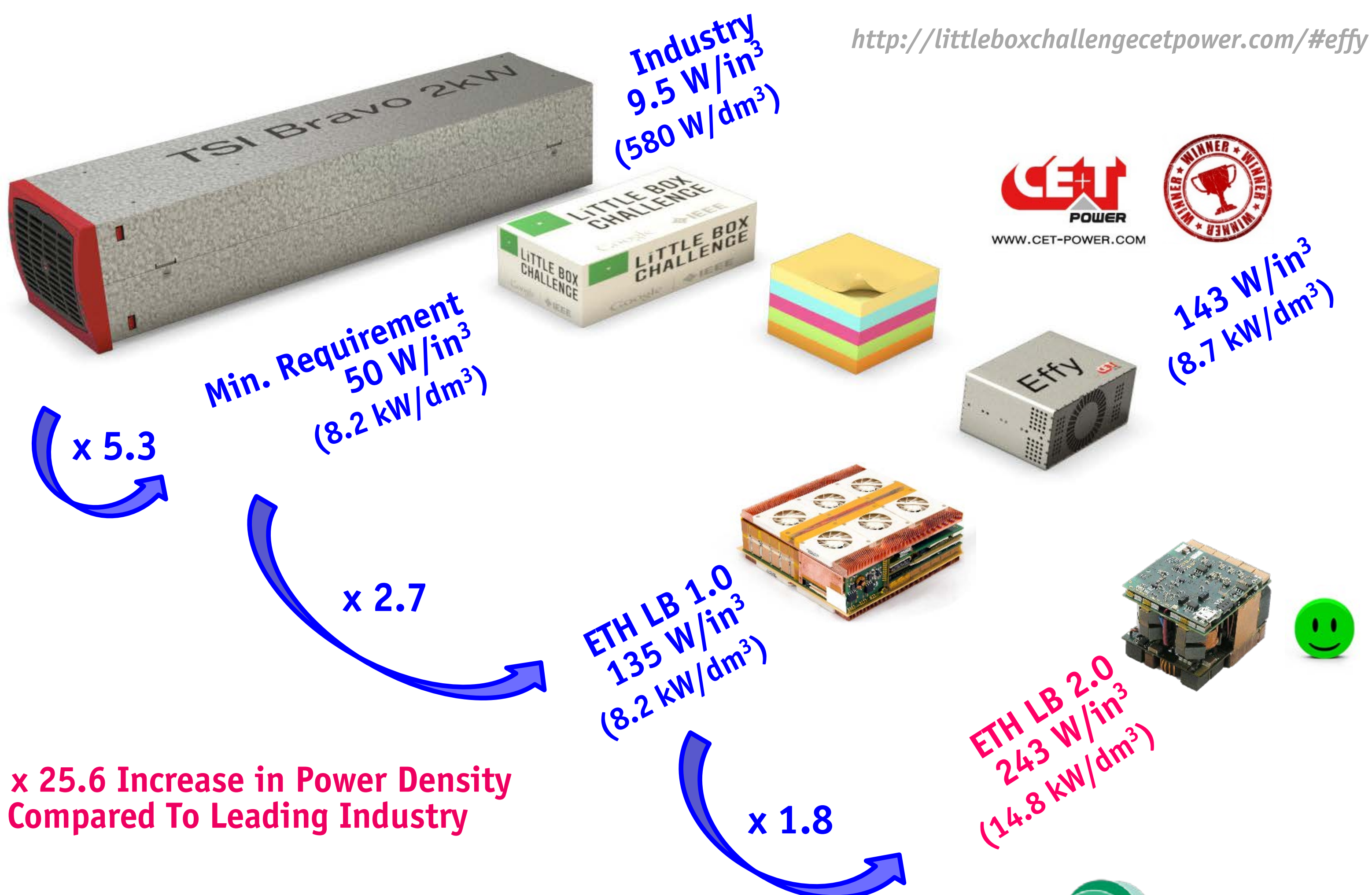
- 14.8 kW/dm^3
- 6.0 cm x 5.0 cm x 4.5 cm = 135 cm^3
- 97.8 % Efficiency @ 2kW



■ Compliant to Revised Specifications (!)

- Compliant to 50 mA Ground Current Lim.
- No Overstressing of Components
- All Own IP / Patents

▶ Little Box 2.0 – Power Density Benchmark



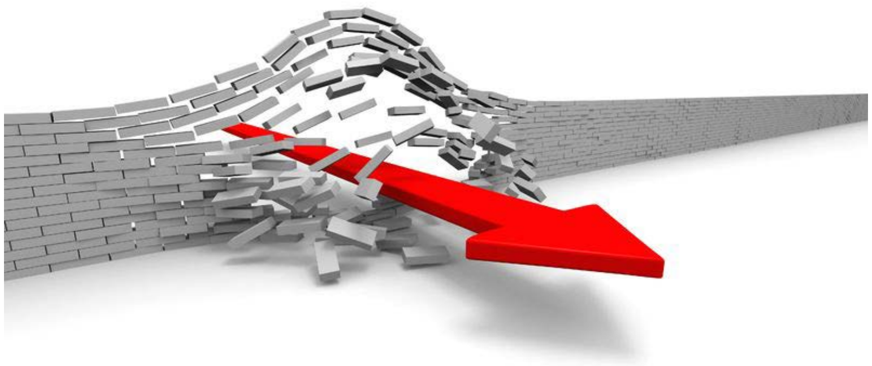
- x 25.6 Increase in Power Density Compared To Leading Industry

Conclusions

Summary
Future Power Electronics Development
"Stairway to Heaven"

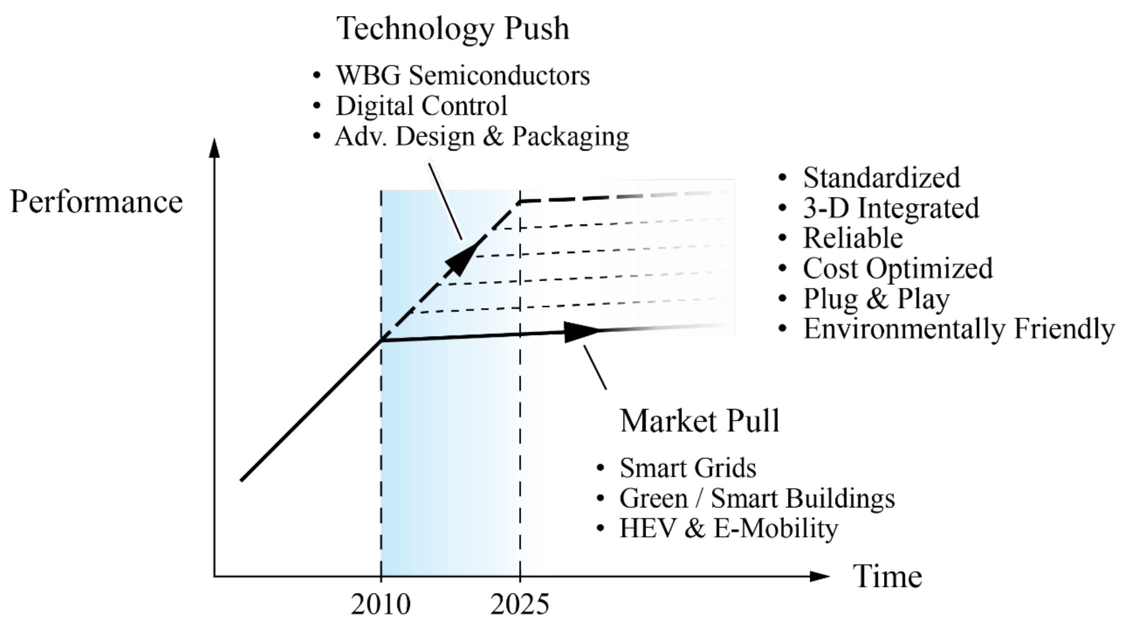
Summary

- Megatrends – Renewable Energy / Energy Saving / E-Mobility / "SMART XXX" Demand Increasing Performance at Lower Cost
- Large Number of Degrees of Freedom – Materials / Components / Topology / Control
- Multi-Objective Optimization Allows To Identify Best Designs For Given Specs. and Side Conditions
- ETH Among Top 10 Finalists in the GLBC – Comp. To Realize the World Smallest 2 kW PV Inverter
- Little Box 1.0 x 14 Increase of Power Density Comp. to Industry Standard
- Further Improved Little Box 2.0 x 25 Increase of Power Density



Future Development

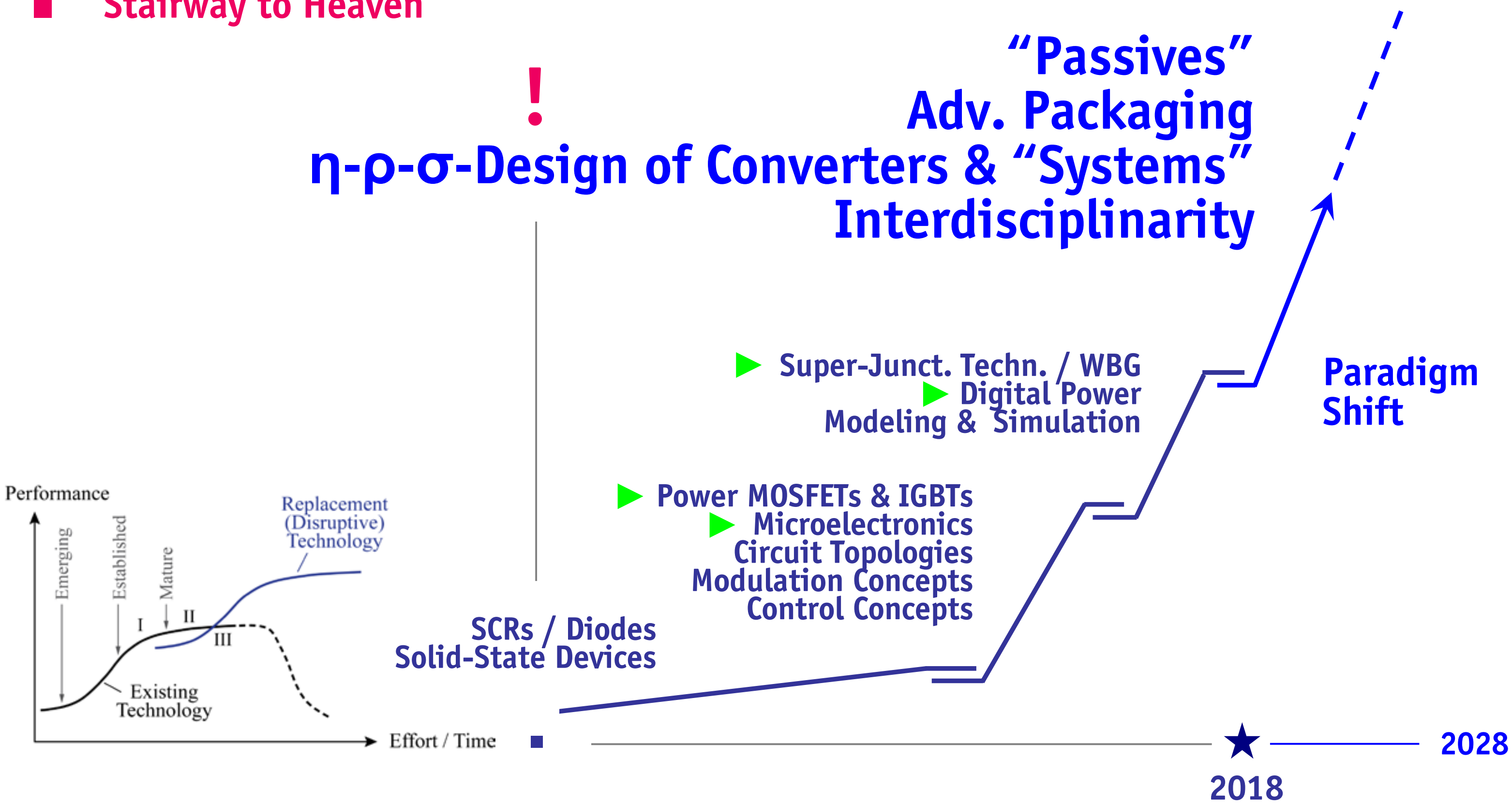
- Megatrends – Renewable Energy / Energy Saving / E-Mobility / "SMART XXX"
- Power Electronics will Massively Spread in Applications



→ More Application Specific Solutions
→ Mature Technology – Cost Optimization @ Given Performance Level
→ Design / Optimize / Verify (All in Simulation) - Faster / Cheaper / Better

▶ Extrapolation of Technology S-Curve

■ "Stairway to Heaven"



Thank You !