Printed Circuit Board Design for Direct Digital Synthesis

Dragonrider and Seadragon

MSc Quantum Engineering Semester Project

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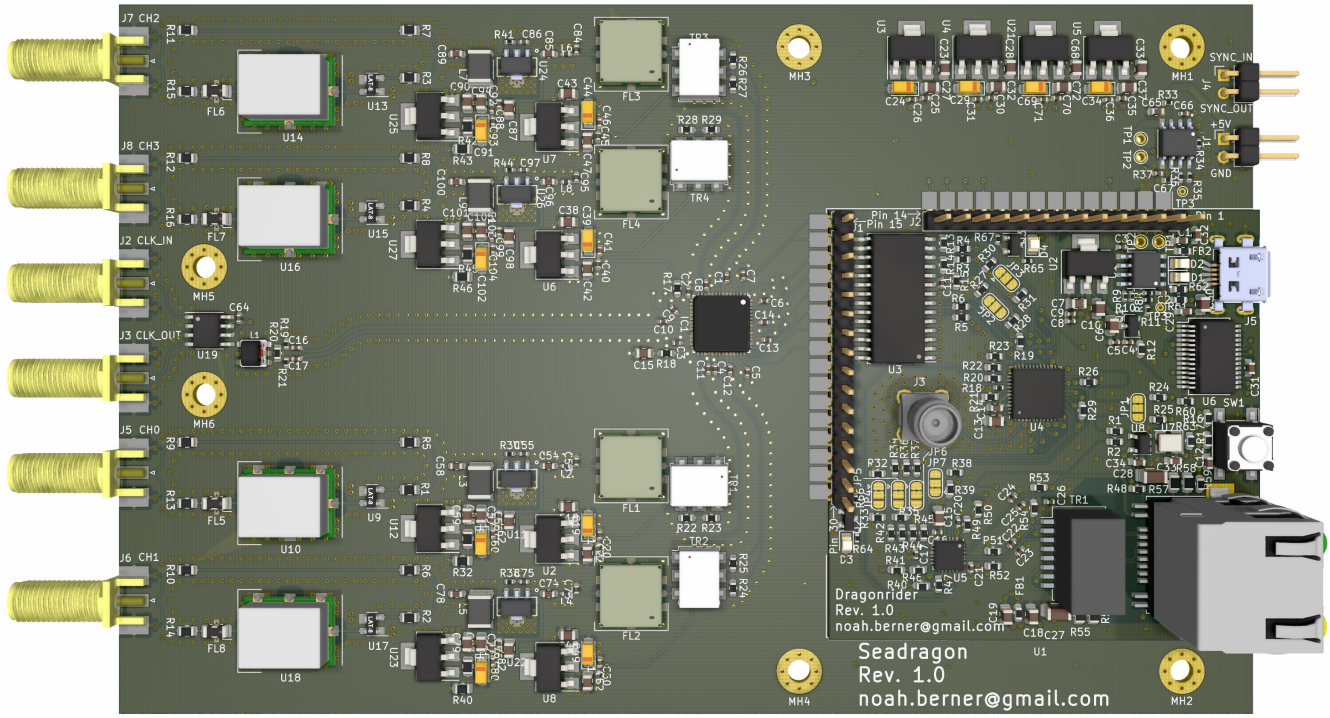

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Abstract

Direct digital synthesis (DDS) is a method of generating radio frequency (RF) signals used for, among other things, driving acousto-optic modulators (AOMs) that can modulate laser frequency, phase and amplitude. Precise laser control plays a key role in trapped ion experiments performed in the Trapped Ion Quantum Information (TIQI) Group at ETH. This semester project designs a printed circuit board (PCB) that replaces the current non-real time DDS system which operates at human time-scales and does not depend on real-time feedback from the experiment. The current system consists of a multitude of parts assembled by hand in contrast to the PCB which is almost fully assembled by the PCB manufacturer. This integration onto one board shows improvements over the current system in price, size, reduced complexity, frequency range, future adaptability due to the in-house design and possibly longer durability.

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Acronyms

AC alternating current

ACR Amplitude Control Register

AOM acousto-optic modulator

DAC digital-to-analog converter

DC direct current

DDS direct digital synthesis

DHCP Dynamic Host Configuration Protocol

DUT device under test

EEPROM electrically erasable programmable read-only memory

EMI electromagnetic interference

GND ground

GPIO general-purpose input/output

I^2C Inter-Integrated Circuit

IC integrated circuit

IP Internet Protocol

LO local oscillator

LPF low-pass filter

LUT lookup table

MAC medium access control

OS operating system

$\mathbf{P_{1dB}}$ 1 dB compression point

PCB printed circuit board

PHY physical layer

PLL phase-locked loop

RF radio frequency

RMII reduced media-independent interface

RPC remote procedure call

SDIO Secure Digital Input Output

SFDR spurious-free dynamic range

SMA SubMiniature version A

SMD surface-mount device

SNR signal-to-noise ratio

SPI Serial Peripheral Interface

TEM transverse electromagnetic mode

TIQI Trapped Ion Quantum Information

UART universal asynchronous receiver-transmitter

USB Universal Serial Bus

1 Introduction

Control over laser light is one of the most important tools in trapped-ion experiments. Lasers are employed in multiple facets of the experiment, from photoionization, laser cooling, state preparation via optical pumping, state readout via laser-induced fluorescence, as well as driving internal state transitions. These tasks rely on precise control of the laser amplitude, frequency, and phase, possibly even in real-time during the timescale of a single experimental cycle. One device commonly used for this purpose is an acousto-optic modulator (AOM). By modulating a piezoelectric transducer attached to an optical medium with a radio frequency (RF) drive, the resulting sound waves in the material create a periodically varying index of refraction. Laser light passing through the optical medium is then diffracted by this grating, in a phenomenon known as Bragg diffraction. This can be used to modulate the laser intensity, steer beam pointing, as well as shift the laser frequency and phase.

Direct digital synthesis (DDS) is a technique that is well suited for generating the control signals for the AOM devices, as it allows experiments to easily produce spectrally pure RF tones with well-defined frequency, amplitude, and phase. Experiments in the Trapped Ion Quantum Information (TIQI) Group at ETH typically will use several dozen AOMs, each driven by DDS. While many critical beamlines used to drive quantum logic gates require real-time control during a single experimental sequence, many beam paths are operated at essentially fixed frequencies and phases, and only need to be updated slowly, out of the loop of the main sequence. One of the signal generators used for these "fixed frequency" beamlines is a custom DDS solution comprising a Raspberry Pi, an Analog Devices AD9959 DDS evaluation board, a custom interface printed circuit board (PCB) with power delivery, and preamplifiers on each output. While this system is capable of synthesizing the required RF signal, it consists of multiple components which have to assembled by hand, creating an opportunity for streamlining by placing all components onto a single board which can be assembled almost completely by the PCB manufacturer. The current system is also not yet fully connected to the control system of the experiment.

In this semester project, a custom PCB is designed that houses all the components needed for DDS. Additionally, a board that controls the DDS Board is developed which can also be used for other control tasks. Throughout the semester project, the methodological approach consists of defining the design constraints and listing the options that fulfill these constraints. From these options, the most fitting option is chosen.

Section 2 describes the use-cases of DDS in the field of trapped-ion experiments, as well as the general working principle of DDS. Section 3 explains specific design considerations for a DDS PCB which are applied in practice in later sections. Section 4 details the design process of the DDS Board that was designed during this semester project. It also enumerates the expected characteristics of the PCB. Section 5 recounts the design process of the Control Board that was designed during this semester project. Section 6 elaborates the still open problems and next steps when going forward with using the PCBs developed in the semester project. Section 7 concludes this semester project. Appendix A describes in detail the proper usage of the Control Board and its capabilities. Appendix B explains the process of setting up and using the DDS Board. The digital appendix contains the design files of all the PCBs developed during the project.

2 Background

The background section explains topics on a theoretical level that are used in the thesis later on to derive practical design results and decisions. Section 2.3 will explain in detail how a DDS device operates and provides the background knowledge needed for the rest of the thesis.

2.1 Control of Trapped Ions

In experiments on the control of trapped ions, precisely controlled RF signals, such as the ones that are produced by DDS devices, are an important tool for several tasks. This section will explore some of the use cases of DDS devices in an ion trapping environment.

2.1.1 Paul Trap: Radio Frequency Electrodes

Confining a charged particle in all three dimensions is not possible when using static electric fields due to Laplace's equation:

$$\frac{\delta^2 V}{\delta x^2} + \frac{\delta^2 V}{\delta y^2} + \frac{\delta^2 V}{\delta z^2} = 0. \tag{1}$$

Due to this equation, a static electric potential can only be confining in a maximum of two dimensions and anti-confining in the other.

The Paul trap solves this problem by creating an average confining force in all three dimensions by using electric fields that change in time. These alternating electric fields, which are produced by electrodes around the charged particle, are switched between confining and anti-confining faster than the time it would take the ion to escape. In certain experiments, a DDS device that generates signals in the RF range is suitable to create such rapidly alternating electric signals.

2.1.2 Local Oscillators

Local oscillators (LOs) are strong reference signals which are often fed into a mixer to change the frequency of an input signal. A mixer has two input ports (in this case, one for the input signal and one for the LO) and produces one output signal which also contains frequency components of the sum and difference of the frequencies of the input signals. DDS devices can provide the oscillating electric signal for the LO. Due to the precision of DDS, the input signal can be mixed with accurate frequencies to provide an output signal with the desired frequency.

2.1.3 Laser Controlled Quantum Information Experiments

The TIQI Group at ETH performs experiments that involve information processing using trapped ions. For these experiments, the control of the energy levels of the ion, the readout of the levels, the interaction of the motion of the ions with these energy levels and the cooling of the ions to be trapped need to be performed reliably. All of these tasks involve lasers that need to have a specific frequency, phase, and amplitude. To get the needed level of precision on these metrics, AOMs are used to shift the frequency, phase, and amplitude of existing laser sources.

2.2 Acousto-Optic Modulators

AOMs are used to precisely shift the frequency ω, amplitude, and phase of an incoming light source by utilizing the acousto-optic effect which states that the refractive index of a transparent medium

is changed by traveling sound waves in that medium. This section gives a brief overview of the working principles of AOMs and the interested reader can find more information in [ST07]. An AOM typically consists of a piezoelectric transducer, a transparent medium like glass or quartz, and an acoustic absorber. The piezoelectric transducer is driven by an alternating current (AC) signal that causes the transducer to vibrate and create sound waves at frequency Ω in the attached transparent medium. The AC signal can be provided by a DDS device which will be explained in Section 2.3. The sound waves in the crystal change its optical density in a periodic way. A visualization of the AOM can be seen in Figure 1.

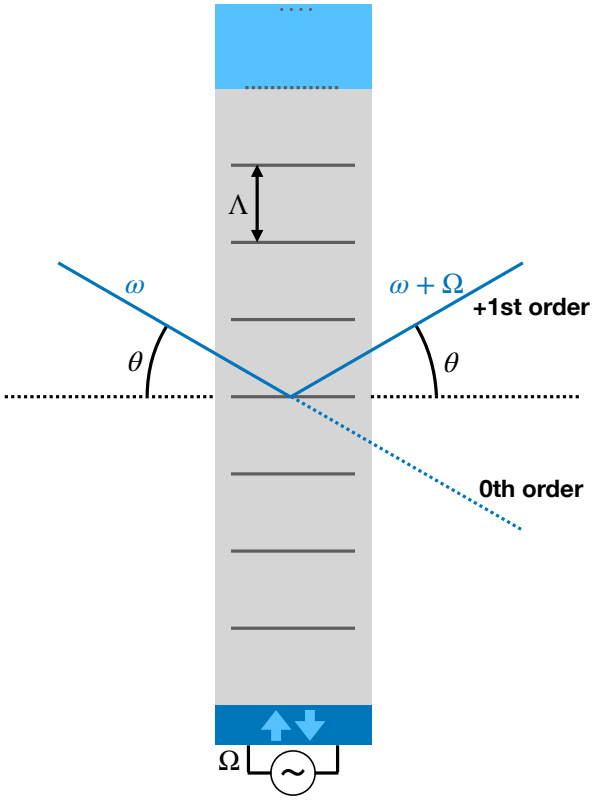


Figure 1: Visualization of an Acousto-Optic Modulator.

The transmitted light is referred to as the 0th order beam and the reflected light beam is referred to as ±1st order. The sign of the first order depends on whether the incident light goes against (+) or along (-) the sound waves. Figure 1 shows a configuration where the light is angled against the travel direction of the sound waves and thus resulting in a +1st order reflection. The incoming light beam is angled at θ to fulfill the Bragg condition:

$$\sin(\theta) = \frac{\lambda}{2n\Lambda}. \tag{2}$$

where $\lambda = \frac{2\pi c}{\omega}$ is the wavelength of light in vacuum, n is the refractive index of the transparent medium and $\Lambda = \frac{2\pi u}{\Omega}$ is the wavelength of the sound. Fulfilling the Bragg condition leads to the highest possible reflection intensity in ±1st order beam which is why most of the AOMs operate under the Bragg condition.

2.2.1 Intensity

The diffraction efficiency $\eta = \frac{I_1}{I}$, which is the fraction of the intensity at the 1st order I_1 compared to the total incident light intensity I, is proportional to the intensity of the acoustic wave I_S. In practice, a saturation occurs which leads to the relation

$$\eta \propto \sin^2(\sqrt{I_S}) \tag{3}$$

Thus for small acoustic intensities I_S we observe a linear relationship between the power of the electrical drive signal and the reflected light intensity I_1.

2.2.2 Frequency and Phase Shift

The frequency ω of the incident light will be shifted by the sound frequency Ω in the reflected light of $m = \pm 1$st order. This leads to the new reflected frequency

$$\omega_r = \omega + m\Omega. \tag{4}$$

The cause for the frequency shift can either be thought of as a Doppler shift which is caused by the moving planes of sound that reflect the beam or as energy and momentum conservation of the photons and phonons in the scattering process.

The phase of the diffracted beam is also shifted by the phase of the sound wave. It can be shifted by an arbitrary amount.

2.3 Direct Digital Synthesis

DDS is a method for generating analog waveforms from a time-varying digital signal. Often, this analog signal is a single tone, a sine wave. DDS devices are not limited to these single tone signals and can also generate other waveforms, such as square or triangular outputs. However, in this section, we will focus on sine wave generation since it presents us with an intuitive way of explaining the inner workings of DDS integrated circuits (ICs). This section is inspired by the articles [MS04] and [Pin19].

Note that there are also other solutions to produce analog waveforms such as analog phase-locked loop (PLL) and direct analog synthesis:

While **analog PLL** can be a more affordable solution, DDS offers a higher frequency resolution, higher frequency range, faster switching time, and has better phase-noise characteristics when they are compared using the same frequency reference. Furthermore, DDS ICs have become more affordable over time and are now in a competitive price range when compared to analog PLL devices [SM96].

Direct analog synthesis, which works by mixing base frequencies to create an output frequency, has the advantage of fast switching speeds and low phase noise. However, it suffers from a limited frequency range and poor frequency resolution. Increasing the resolution means an increase in the number of components in the device which can make designs complex [Che17].

2.3.1 Overview

A DDS device consists of a reference clock f_c, a phase accumulator, a phase-to-amplitude converter and a digital-to-analog converter (DAC). An overview of the whole system can be seen in Figure

2. The explanation of how all these parts work together to create an analog sine wave signal is explained in the following sections.

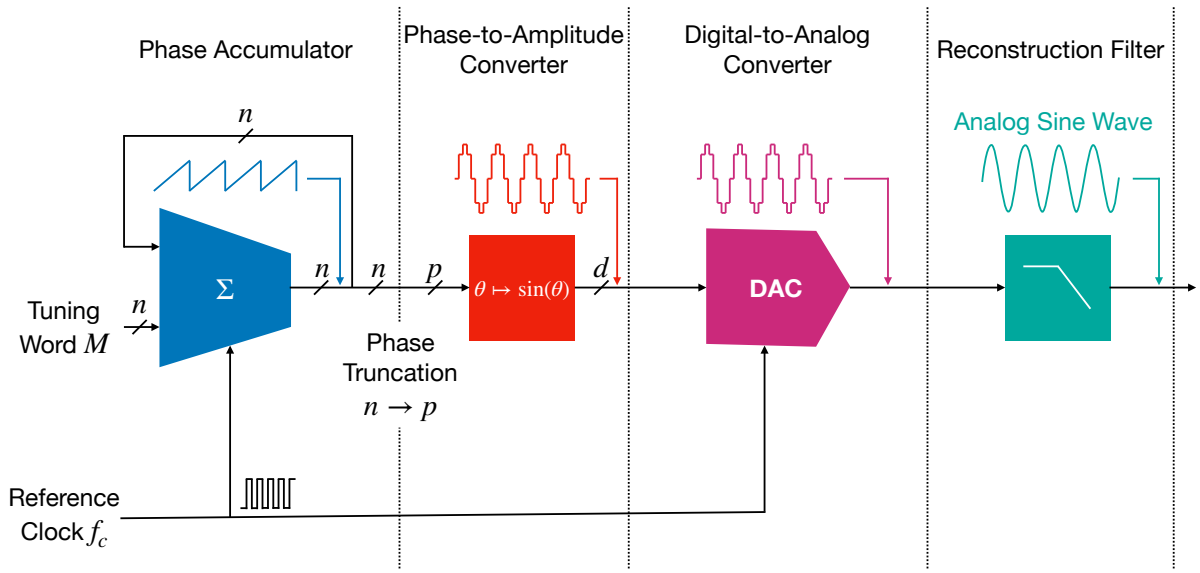


Figure 2: Direct Digital Synthesis Overview Including the Reconstruction Filter.

2.3.2 Phase Accumulator

The phase accumulator is responsible for generating the frequency of the output signal. It does so by keeping track of the current phase of the signal. A sinusoidal signal has a phase ranging from 0 to 2π. The phase accumulator counts from 0 to 2π in discrete steps. The step size is defined by the tuning word M, which consists of n bits. Thus the range of 0 to 2π is discretized into 2^n values that can be attained by the phase accumulator.

The counting of the phase accumulator can be visualized by a phase wheel with 2^n equally spaced values (dots) and an arrow that points to the current value of the phase accumulator. This visualization can be seen in Figure 3.

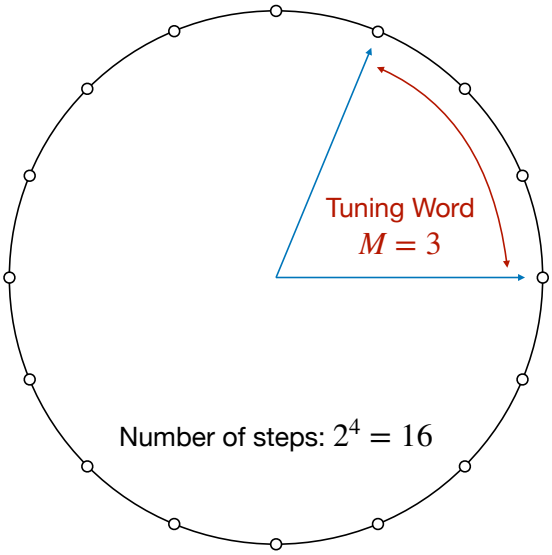
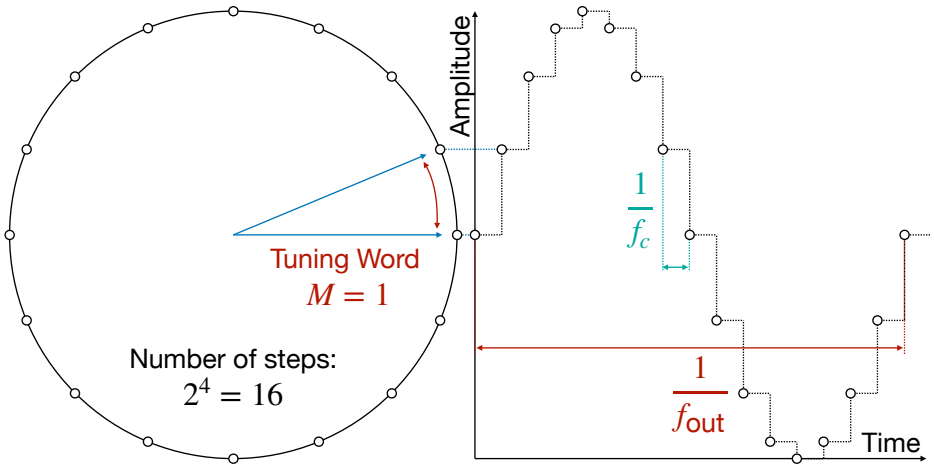


Figure 3: Digital Phase Wheel with $n = 4$ and $M = 3$.

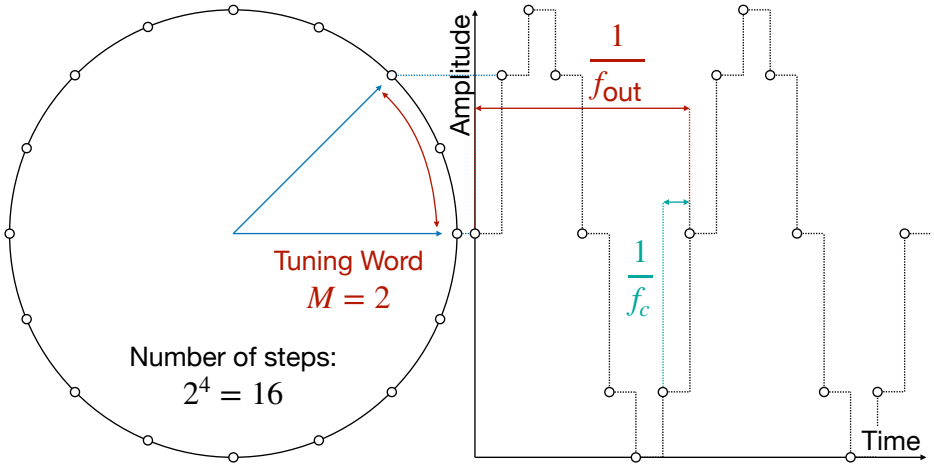
Each time the reference clock f_c completes a cycle, the hand of the phase accumulator moves by the amount of the tuning word M (one step). It takes the phase accumulator $\frac{2^n}{M}$ steps to complete a full cycle. Thus the output frequency of the signal, which is the inverse of the time it takes the phase accumulator to complete a cycle, is

$$f_{\text{out}} = \frac{M f_c}{2^n}. \tag{5}$$

During operation of the DDS, the only tunable parameter in Equation 5 is the tuning word M, since both the reference clock frequency f_c and the number of bits n of the phase accumulator are fixed. Thus, if we want to change the frequency of the output signal, we have to modify the value of M. Figure 4 shows two options of how M can be configured to change the output frequency. Figure 4b has a tuning word that is twice the tuning word of the tuning word in Figure 4a, leaving the output frequency of Figure 4b at twice the output frequency of Figure 4a.



(a) Tuning word $M = 1$ and output frequency $f_{out} = \frac{f_c}{16}$.



(b) Tuning word $M = 2$ and output frequency $f_{out} = \frac{2f_c}{16} = \frac{f_c}{8}$.

Figure 4: Digital Phase Wheel with Corresponding Digital Waveform for $n = 4$.

2.3.3 Nyquist Frequency

The value of f_{out} can be in the following range

$$\frac{f_c}{2^n} \leq f_{out} \leq \frac{f_c}{2}. \tag{6}$$

The upper bound stems from the Nyquist Sampling Criteria, which states, that the sampling rate (the reference clock) of a signal must be at least twice the rate of its highest frequency component. If the sampling frequency is less than twice the highest output frequency component, the signal will become distorted due to the alias at $f_c - f_{OUT}$ which will then be lower in frequency than f_{out} and thus not be filtered by the reconstruction filter (see Section 2.3.6). Since our sine wave only has one frequency component, the highest output frequency achievable is the Nyquist frequency at $\frac{f_c}{2}$.

2.3.4 Phase-to-Amplitude Converter

The phase-to-amplitude converter takes the output value θ of the phase accumulator and performs the operation $\sin(\theta)$ on it. Figure 4 shows how the phase accumulator and the phase-to-amplitude converter work together to produce the desired sine wave. The phase accumulator provides the

time value (modulo $\frac{1}{f_{out}}$) on the x-axis while the phase-to-amplitude converter uses that value as input and provides the corresponding amplitude value on the y-axis.

The phase-to-amplitude converter still works in digital space and often uses a lookup table (LUT) to perform the sine operation. Most of the time, the LUT has a smaller number of input bits than the n output bits of the phase accumulator. Thus, a phase truncation is performed, where only the p most significant bits are used as input to the phase-to-amplitude converter.

This phase truncation can contribute to phase noise, depending on the tuning word M (and thus the desired output frequency) that is chosen for the phase accumulator. If the ratio $\frac{M}{2^n}$ cannot be represented with the p bits available, the truncation error is greater than 0 and results in spurs in a spectral plot.

2.3.5 Digital-to-Analog Converter

The DAC takes the digital output value of the phase-to-amplitude converter and converts it to an analog voltage or current. For this purpose, it also needs the reference clock f_c (or a clock derived from f_c) as an input to know when to sample its input value and update the voltage on the output.

The DAC outputs a faithful, analog reconstruction of the stepped signal it receives and does not interpolate between the digital values. This leads to stepped analog signal which is simulated in Figure 6b. This stepping behavior, where the DAC holds the signal it receives for the time $\frac{1}{f_c}$, causes two unwanted effects. The first is that there are images (or aliases) of the wanted output signal f_{out} at the frequencies $f_c - f_{\text{out}}, f_c + f_{\text{out}}, 2f_c - f_{\text{out}}, 2f_c + f_{\text{out}}$, and so on. The second is a roll-off of the amplitude that behaves like

$$A(f_{\text{out}}) = \frac{\sin\left(\frac{\pi f_{\text{out}}}{f_c}\right)}{\frac{\pi f_{\text{out}}}{f_c}}. \tag{7}$$

This roll-off is specifically caused by the finite time $\frac{1}{f_c}$ that the frequency is held by the DAC. The rectangular time response corresponds to the $\text{sinc}\left(\frac{\pi f_{\text{out}}}{f_c}\right)$ frequency response seen in Equation 7. Both of the effects are visualized in Figure 5.

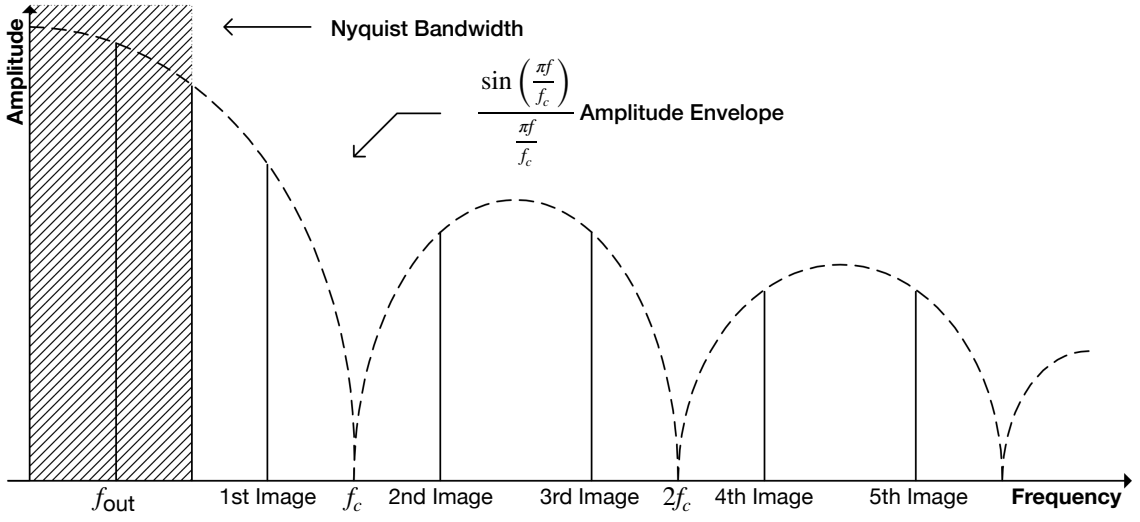
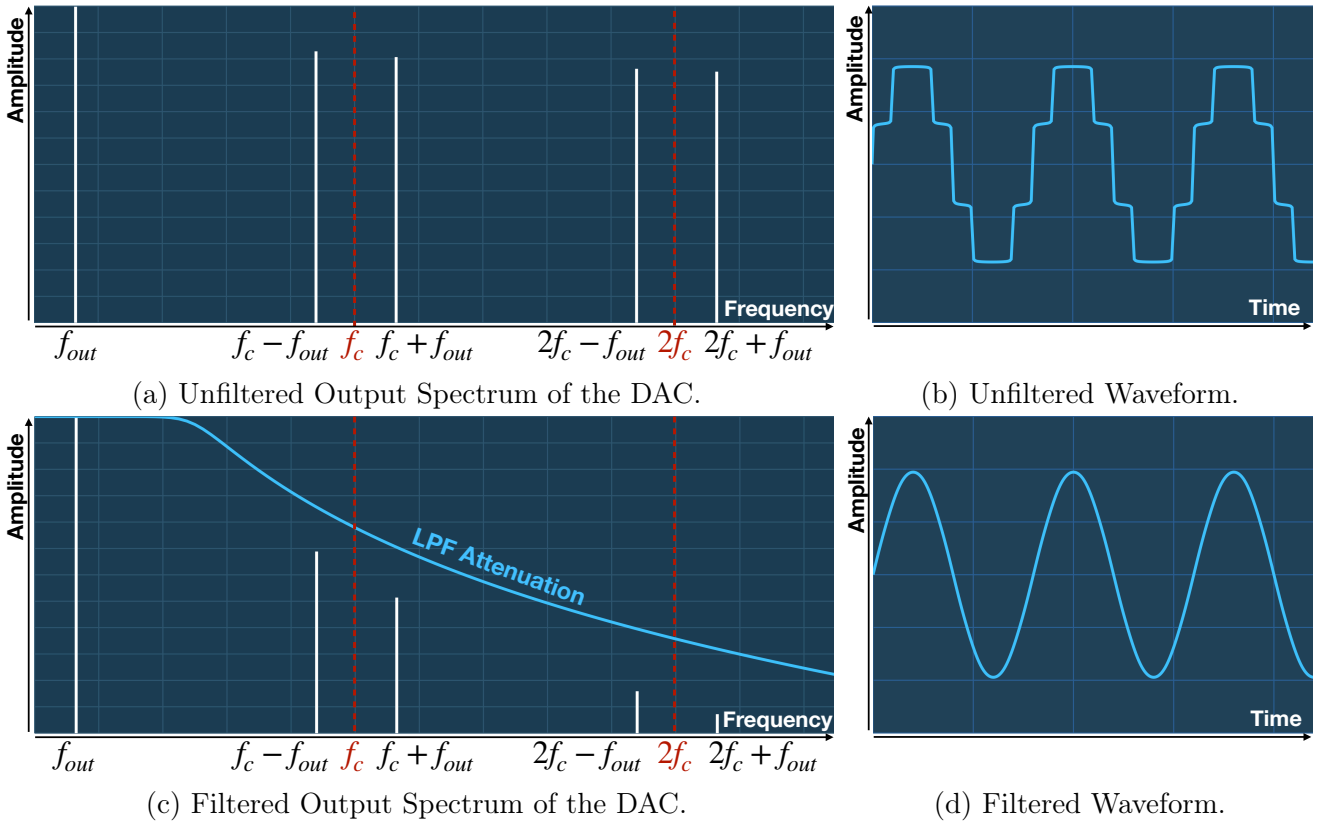


Figure 5: DAC Frequency Response Showing the Amplitude Roll-Off and Images (Image Source: Adapted from Analog Devices).

In order to reconstruct the single tone signal that we are interested in, we use a low-pass filter (LPF) to filter out these DAC images in the output signal of the DAC. This filter is called the reconstruction filter. See Figure 6 for a visualization of the unfiltered and filtered output signal of the DAC. The LPF attenuates the images at the frequencies $f_c - f_{\text{out}}, f_c + f_{\text{out}}, 2f_c - f_{\text{out}}, 2f_c + f_{\text{out}}, \ldots$, which leaves only the desired frequency component at f_{out}.



(a) Unfiltered Output Spectrum of the DAC.

(b) Unfiltered Waveform.

(c) Filtered Output Spectrum of the DAC.

(d) Filtered Waveform.

Figure 6: Output Spectrum and Waveform of the DAC without and with an LPF (Image Source: [20a]).

2.3.6 Reconstruction Filter

As seen in the previous section, it is crucial that the right external reconstruction filter is chosen, such that the correct waveform can be output while maximizing the available bandwidth of the DDS. The LPF should have a sharp cut-off at the Nyquist frequency to remove the unwanted image at $f_c - f_{\text{out}}$ and beyond, while still preserving the signal at f_{out}. The cut-off frequency should be close to the Nyquist frequency, because there $f_c - f_{\text{out}}$ and f_{out} overlap.

The sharpness of the cut-off in LPFs is achieved by using a higher-order filter. These filters can be constructed using RLC circuits using resistors, inductors, and capacitors or sourced as an integrated circuit.

3 Design Considerations

This section works through specific design considerations for constructing a PCB that handles DDS outputs and analog signals. However, these topics are general enough to warrant this theoretical section before it is applied in a practice in Section 4.

3.1 Driving a Center-Tapped Transformer with a Balanced Current-Output Digital-to-Analog Converter

The DDS device that we are going to consider for the PCB in Section 4.2 will have a DAC that has a balanced current output. That is, it converts the digital signal amplitude on its input into two differential currents on its two analog output pins. However, we want a single-ended signal since all subsequent components, like the reconstruction filter and amplifiers, will have a single input. We explain how a balanced current-output DAC can be interfaced with a center-tapped transformer to convert a differential signal into a single-ended signal to drive the load. This section is derived from the application note AN-912 [Gen07] and the interested reader will find a more in-depth treatment of the topic there.

Using a center-tapped transformer as the output interface for a balanced current output DAC has the following benefits:

- Direct current (DC) isolation between DAC output and the final load.
- Can aid in the rejection of common-mode signals present at the DAC output.
- Can mitigate the even harmonics resulting from an imbalance between the DAC outputs.
- The limited bandwidth of the transformer can suppress the Nyquist images as a pre-filter.

3.1.1 Balanced Current-Output Digital-to-Analog Converter

There are two different varieties of DACs that have a balanced current output: current source and current sink outputs. Current source outputs inject current into the external load (transformer) and current sink outputs draw current from the load. Both of these variants have two output pins: a normal pin with current I_A and a complementary pin with current I_B. The currents have the following relationship to the fractional digital code value α:

$$\begin{aligned} I_A &= \alpha I_{\text{MAX}}, \\ I_B &= (1-\alpha) I_{\text{MAX}}, \end{aligned} \tag{8}$$

where I_{MAX} is the maximum current that the DAC can deliver. Note that because of the relationship in Equation 8, the total output current $I_A + I_B$ is always equal to I_{MAX}.

3.1.2 Driving a Tapped Transformer

Figure 7 shows a balanced current-output DAC coupled to a tapped transformer. Note that this DAC is of the current-sourcing kind.

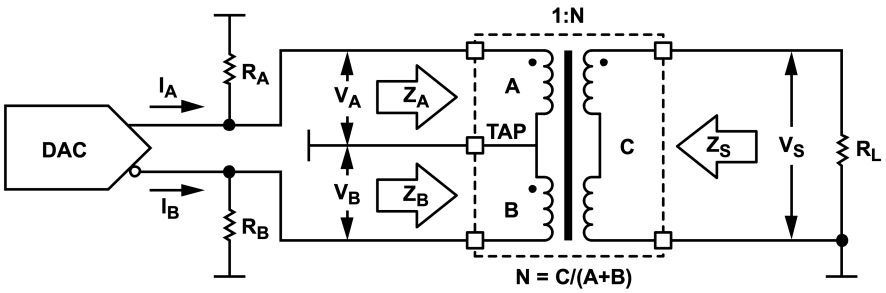


Figure 7: A Balanced Current-Output DAC Coupled to a Tapped Transformer (Image Source: [Gen07]).

Following is a list explaining the different parameters in Figure 7:

- N: Transformer Turns Ratio. The number of secondary windings (C) divided by the number of primary windings (A+B) of the transformer.
- R_A, R_B: DAC termination resistors that connect the outputs of the DAC to ground (GND)[1].
- R_L: Load resistance.
- Tap: The primary winding is split into two separate circuits at the tap. The tap connects to GND[2].
- v_A, v_B: Voltage drop-off between the output of the DAC and tap of the transformer. This voltage consists of the voltage produced by the DAC current source ($v_{\text{NORM}}, v_{\text{COMP}}$ (which would be at the same location as v_A, v_B in the Figure)), and the voltage produced by the interaction of the primary windings (A with B and B with A) of the transformer. Because of this interaction, v_A and v_B are twice as large as v_{NORM} and v_{COMP}.
- v_S: Voltage across the load.
- Z_A, Z_B: Focussing on Z_A, due to the conservation of energy one can convert impedances through the transformer, such that the impedances caused by R_B and R_L appear as a converted impedance Z_A in circuit A. Z_A consists of two parallel impedances. The converted impedance of R_L and the converted impedance R_B. The same holds for Z_B but with the converted impedances R_L and R_A.
- $Z_{\text{NORM}}, Z_{\text{COMP}}$ (not in the Figure): Impedance seen by each DAC output. Z_{NORM} is a parallel combination of Z_A and R_A. Z_{COMP} is a parallel combination of Z_B and R_B.
- Z_S: Source Impedance as seen by the load. Similarly to Z_A and Z_B this impedance consists of the two transformed impedances R_A and R_B in parallel.

Equation 9 thorugh Equation 12 will not be derived in this report. For a formal treatment and derivation refer to [Gen07]. The equations will be used in Section 4 for a derivation of the design constraints for certain parts on the PCB. The following practical simplifications to the system were made:

[1]Note that if the DAC was of the current sinking type, the DAC termination resistors would connect to a voltage source.

[2]Note that if the DAC was of the current-sinking type, the tap would connect to a voltage source.

- Use a center-tapped transformer (A = B).
- Equal values R_O for the DAC termination resistors ($R_A = R_B = R_O$).
- Impedance matching: equal source and load impedance ($Z_S = R_L$).

$$R_O = \frac{R_L}{2N^2} \tag{9}$$

The DAC termination resistance R_O is used to determine the appropriate DAC termination resistors for the circuit, as well as the differential impedance between the outputs of the DAC, which is $2R_O$.

$$v_s = \frac{\sqrt{2} I_{\mathrm{MAX}} R_L}{8N} \tag{10}$$

$$v_A = v_B = \frac{v_s}{2N} = \frac{\sqrt{2} I_{\mathrm{MAX}} R_L}{16N^2} \tag{11}$$

Current output DACs have a maximum voltage rating up to which they can sustain the current I_{MAX} to drive the resistive load. One needs to calculate v_A, v_B to see whether they do not violate the voltage compliance range of the current output DAC.

$$P_L = \frac{R_L}{2} \left(\frac{I_{\mathrm{MAX}}}{4N} \right)^2, \tag{12}$$

where P_L is the power delivered to the load. The output power of a DAC is a metric that is used to decide on the components that follow the DDS IC. Certain devices need a specific amount of power to work correctly, which can be achieved by placing amplifiers or attenuators after the DAC output.

3.2 Radio Frequency Impedance Matching on Printed Circuit Boards

Impedance matching is concerning itself with designing the input impedance of a load to match the output impedance of the signal source. This enhances the transfer of signal power or equivalently minimizes the reflections from the load. A standard value for the design of these impedances is $50\,\Omega$ which facilitates the interfacing of different components, instruments and the desired load. On PCBs, much like the matching of the characteristic impedance of coaxial wires, the traces connecting the different elements also have to be impedance matched to reduce reflections. Several idealized models describe the physics in certain trace configurations, three of which we are going to present in the following sections.

3.2.1 Microstrip

A microstrip is a type of transverse electromagnetic mode (TEM) transmission line on the outside layer of a PCB that is separated by a dielectric from a lower layer which consists of a solid copper GND plane. Figure 8 shows a visualization of the microstrip model.

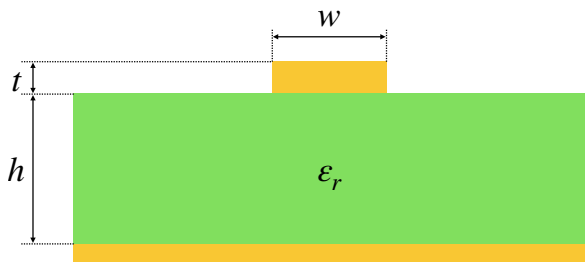


Figure 8: Visualization of the Microstrip Model.

The parameters of the model are:

- ε_r: Dielectric constant of the substrate.
- h: Thickness ("height") of the dielectric substrate.
- w: Width of the strip.
- t: Thickness of the strip.

An approximate expression for the characteristic impedance of a microstrip is given by Wheeler [Whe77]:

$$Z_{\text{microstrip}} = \frac{Z_0}{2\pi\sqrt{2(1+\varepsilon_r)}} \ln\left(1 + \frac{4h}{w_{\text{eff}}}\left(\frac{14+8/\varepsilon_r}{11}\frac{4h}{w_{\text{eff}}} + \sqrt{\left(\frac{14+8/\varepsilon_r}{11}\frac{4h}{w_{\text{eff}}}\right)^2 + \pi^2\frac{1+1/\varepsilon_r}{2}}\right)\right) \tag{13}$$

where Z_0 is the impedance of free space and w_{eff} is the effective width of the trace. The effective width w_{eff} is the the width w of the trace with an added correction for the thickness of the metallization:

$$w_{\text{eff}} = w + t\frac{1+1/\varepsilon_r}{2\pi} \ln\left(\frac{4e}{\sqrt{\left(\frac{t}{h}\right)^2 + \left(\frac{1}{\pi}\frac{1}{w/t+11/10}\right)^2}}\right) \tag{14}$$

The approximation in Equation 13 achieves asymptotic behavior in the following cases:

- Wide strip ($w \gg h$) and all ε_r.
- Narrow strip ($w \ll h$) and $\varepsilon_r = 1$ (dielectric substrate is vacuum) or $\varepsilon_r \gg 1$.

The approximation error is at most 2% (and 1% over most of the range) according to Wheeler [Whe77].

In practice, during this project, the impedance calculator of the PCB manufacturer JLCPCB was used [20c] since it already knows the stack's physical and electrical properties. It uses a coated microstrip model to calculate the characteristic impedance of the traces.

3.2.2 Coplanar Waveguide

Coplanar waveguides are a also type of transmission line which include a ground plane on the top layer on both sides of the trace. Figure 9 shows a visualization of the coplanar waveguide model. The new parameter g is the gap width between the ground planes and the trace.

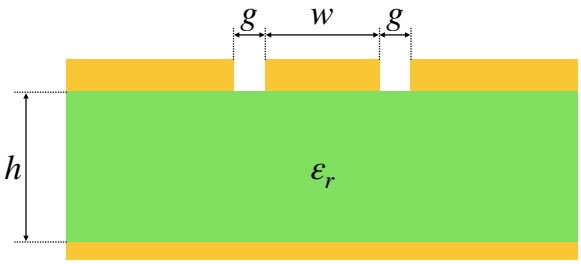


Figure 9: Visualization of the Coplanar Waveguide Model.

Since the equations for the waveguide model are more involved than the microstrip model, they will not be covered here. During the project, the calculator by CHEMANDY was used to calculate the characteristic impedance and determine the appropriate gap width g [19a].

3.2.3 Edge Coupled Microstrip Model

When routing differential traces on a PCB a common transmission line to use is the edge coupled microstrip. The model consists of two traces on the top layer that are separated by a dielectric from a lower layer which consists of a solid copper GND plane. A visualization of the edge coupled microstrip can be seen in Figure 10. The new parameter s is the separation between the two differential traces.

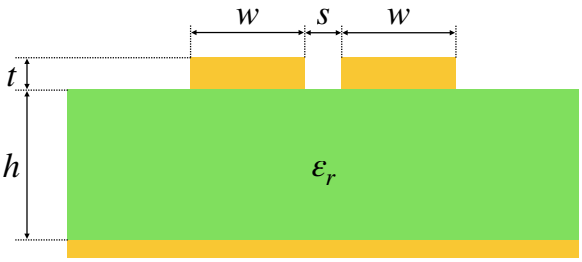


Figure 10: Visualization of the Edge Coupled Microstrip Model.

Again, the equations for the differential impedance of the edge coupled microstrip model are much more involved than the microstrip model and thus will not be covered here. In practice, during this project, the impedance calculator of the PCB manufacturer JLCPCB was used [20c].

4 Seadragon Direct Digital Synthesis Circuit Board Design

This section describes the design process of the DDS Board the constraints that had to be met, the options that fulfill these constraints, and the decisions that were made based on these options. Figure 11 shows a simplified schematic of the finished DDS Board, named Seadragon, and can serve as an overview for the upcoming sections. You can refer back to it while reading through these sections describing the separate parts to see how they interact with other parts and fit into the big picture.

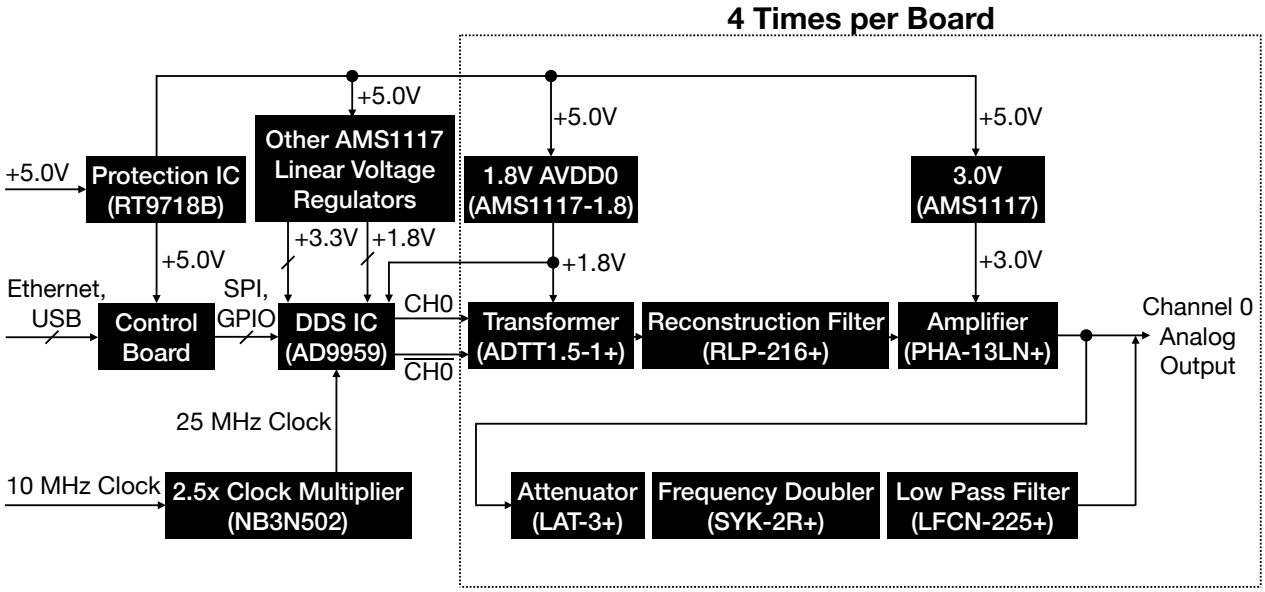


Figure 11: Simplified Schematic of the Seadragon DDS Board. Only 1 Channel is Drawn. The Names of the ICs are in Parentheses.

4.1 Target Output Power

Typical AOMs require an input RF power between 1.5 to 5 W, thus we design the DDS Board with the goal in mind to use a second-stage amplifier connected to the DDS Board. One example of a common amplifier is the Mini-Circuits ZHL-1-2W+ amplifier which will bring the output signal power to 2 W $\approx$ 33 dBm which is a usable level for some AOMs. This amplifier has a typical 1 dB compression point (P_{1dB}) at 33 dBm, at which the amplifier deviates 1 dB from its linear amplifying behavior. Reaching this point means that the output power of the amplifier starts to saturate. If the input power is further increased, the amplifier will become a non-linear device which will produce distortion, harmonics, and intermodulation products. Thus an amplifier should always be operated at an input power that is less than the P_{1dB} minus the gain. The minimum gain of the ZHL-1-2W+ is 29 dB. Accounting for loss in the coaxial lines connecting the board and amplifiers, which is around 1-2 dB, this yields a maximum target output power of 33 dBm $-$ 29 dB + 1 dB = 5 dBm for our DDS Board.

4.2 Direct Digital Synthesis Integrated Circuit

The first part on a DDS PCB that should be chosen is the DDS chip since it will govern all the constraints for the other parts of the board. As discussed in Section 2.3, a DDS IC has parameters that need to be chosen according to the specifications of the project. For this project, two major constraints had to be fulfilled by the DDS chip to be useful.

- Variable output frequency f_{out} should be at least between 10 MHz and 200 MHz because these are frequencies typically used in experiments.
- It should have multiple channels with a controllable relative phase.

The 10 MHz constraint is not much of a worry since most DDSs can achieve frequencies well below 1 kHz[3].

The 200 MHz constraint means that we need a DDS that can accept a reference clock f_c of at least 400 MHz, because the Nyquist Sampling Criterion (see Section 2.3.3) limits the output frequency f_{out} to half the sampling rate. In practice, you want to have a slightly higher Nyquist frequency $\frac{f_c}{2}$ than your highest desired f_{out} because the reconstruction filter has not a perfect cut-off at $\frac{f_c}{2}$ but ramps down over some frequency period (see Figure 6c).

One can construct a board with multiple phase-linked channels in two ways. One option is a DDS IC that has multiple output channels and the other is multiple ICs that are linked together to synchronize their internal clocks. The first option is preferred since it reduces complexity, price, and board space.

In Table 1 are the integrated circuits that were considered for the project. At the moment, there are only two manufacturers that produce DDS ICs and one of them only sells one chip. Throughout this thesis, tables are color-coded using the following scheme:

- Red: Constraint violated.
- Yellow: Constraint fulfilled but not optimal.
- Blue: Constraint fulfilled.

Manufacturer	Name	Number of Channels	Synchronization Possible	Maximum Clock Frequency
Renesas	ISL5314	1	No	125 MHz
Analog Devices	AD9910	1	Yes	1 GHz
Analog Devices	AD9914	1	Yes	3.5 GHz
Analog Devices	AD9915	1	Yes	2.5 GHz
Analog Devices	AD9106	4	No	180 MHz
Analog Devices	AD9958	2	Yes	500 MHz
Analog Devices	**AD9959**	**4**	**Yes**	**500 MHz**

Table 1: Options for the DDS IC.

[3]Note that at such low frequency ranges the 2nd and 3rd order harmonics are close to the fundamental signal and thus will not be filtered out by the reconstruction filter. It depends on your implementation and specific use case, how much these harmonics will adversely affect your signal generation

Since only one chip fulfills both constraints optimally, the AD9959 from Analog Devices is the obvious choice. It is also the chip that is already used in the existing solution, so some software might be reusable later on and the users are already somewhat familiar with the possibilities of the AD9959.

Table 2 lists specifications of the AD9959 that are important for the further design of the board.

Number of Channels	4 (synchronized)
Max. Clock Frequency	500 MHz
Internal PLL Clock Multiplier	4x to 20x (integer)
DAC Output Type	Balanced current-output sink
DAC Voltage Compliance Range	AVDD $\pm$ 0.5 V
DAC I_{MAX}	10 mA
Power Supply	Analog (1.8 V): AVDD0, AVDD1, AVDD2, AVDD3, BG_VDD, CLK_VDD. Digital (1.8 V): DVDD. Digital I/O (3.3 V): DVDD_I/O.
Current Draw	Typ: 300 mA, Max: 370 mA.
Power Dissipation	Typ: 540 mW, Max: 680 mW.

Table 2: Specifications of the AD9959 (Source: [08]).

4.3 Center-Tapped Transformer

Since the AD9959 uses balanced current-output DACs of the current-sinking type, we can use the Equations 9 through 11 to determine a DAC-transformer interface that will result in an optimal signal transmission to our $R_L = 50\,\Omega$ load.

Let us first determine which impedance ratio N we should consider for our center-tapped transformer. Equation 12 tells us that the highest power delivered to the load is achieved by having the smallest N. There are step-down transformers that have a value of $0 < N < 1$, but on Mini-Circuits none were available that had a center tap. However, we can use a transformer with a value of $1 < N$ and reverse it, such that the secondary side is connected to the DAC outputs and the primary side connects to the load. For this configuration, the center tap has to be on the secondary side and the primary impedance has to be $50\,\Omega$. Then, the new N becomes $N' = \frac{1}{N}$. Thus we are now looking for a higher N to increase the output power of our circuit.

There are however also two other factors that are influenced by our choice of N:

- The voltage drop-off v_A and v_B between AVDD and the DAC outputs has to in the compliance range of the AD9959. This means that $|v_A| = |v_B| < 0.5\,V$. Using Equation 11 we find

$$N = \frac{1}{N'} = \sqrt{\frac{16|v_A|}{\sqrt{2} I_{\mathrm{MAX}} R_L}} \Rightarrow N < \sqrt{\frac{16\ 0.5\,\mathrm{V}}{\sqrt{2}\ 10\,\mathrm{mA}\ 50\,\Omega}} \approx 3.4 \tag{15}$$

- The differential impedance between the DAC output traces has to be in a range that allows the traces to be routed on the PCB. To achieve a high differential impedance for a given

board thickness, the trace width must be small. To achieve a low differential impedance, the trace width must be large. The range of differential impedances that can be routed using the JLC7628 Stackup is 70 Ω to 140 Ω. The upper bound is quite strict since a PCB manufacturer cannot make traces arbitrarily thin and uncertainty increases at small sizes. The lower bound is less strict since one can almost always enlarge traces, however they might need to be thinned to connect to certain pads of components.

The differential impedance is $R_{\text{DIFF}} = 2R_O$ and if we use Equation 9 we find

$$N = \frac{1}{N'} = \sqrt{\frac{R_{\text{DIFF}}}{R_L}} \Rightarrow 1.2 \approx \sqrt{\frac{70\,\Omega}{50\,\Omega}} < N < \sqrt{\frac{140\,\Omega}{50\,\Omega}} \approx 1.7 \tag{16}$$

In summary, all the constraints for the transformer that interfaces with the DAC outputs of the AD9959 are the following:

- Frequency range between 10 MHz and 250 MHz. The upper bound should be matched as close as possible since that helps reduce the DAC images. The lower bound should be as low as possible, down to 1 MHz since that is the lower bound of the amplifier in Section 4.5.
- Primary impedance of 50 Ω.
- Impedance Ratio $1.2 < N < 1.7$, where the lower bound is not that strict.
- Center-tapped.

In Table 3 the transformers from Mini-Circuits that were considered for this project are listed and their properties are compared.

Name	Frequency Range (MHz)	Impedance Ratio N
ADTT1-1+	0.3 - 300	1
TT1-6+	0.004 - 300	1
T1-1T+	0.08 - 200	1
T1-6T+	0.015 - 300	1
TC1-1T+	0.4 - 500	1
ADT1.5-1+	0.5 - 650	1.5
ADTT1.5-1+	**0.25 - 300**	**1.5**
TC1.5-52T+	0.5 - 550	1.5
TT1.5-1+	0.075 - 500	1.5
ADT2-1T+	0.4 - 450	2
T2-1T+	0.07 - 200	2
TC2-1T+	3 - 300	2

Table 3: Options for the Transformer Interfacing with the DACs Outputs. All transformers have a primary impedance of 50 Ω and are center-tapped on the secondary side or on both.

The transformer ADTT1.5-1+ is the only transformer that optimally fulfills the constraints, thus it is chosen to be connected in a reversed configuration into the circuit between the DACs and the load. The evaluation board to the AD9959 uses the same transformer type but with $N = 1$

(ADTT1-1+) and for a load impedance $R_L = 100\,\Omega$. For the ADTT1.5-1+ we get the following values out of the Equations 9 through 12.

$$R_O = \frac{50\,\Omega}{2\left(\frac{1}{1.5}\right)^2} \approx 56\,\Omega \tag{17}$$

$$v_s = \frac{\sqrt{2}\ 10\,\text{mA}\ 50\,\Omega}{8\ \frac{1}{1.5}} \approx 133\,\text{mV} \tag{18}$$

$$v_A = v_B = \frac{v_s}{2N} = \frac{\sqrt{2}\ 10\,\text{mA}\ 50\,\Omega}{16\left(\frac{1}{1.5}\right)^2} \approx 99\,\text{mV} \tag{19}$$

$$P_L = \frac{50\,\Omega}{2}\left(\frac{10\,\text{mA}}{4\ \frac{1}{1.5}}\right)^2 = 0.35\,\text{mW} \approx -4.5\,\text{dBm} \tag{20}$$

Equation 19 shows us that the voltage drop-offs v_A and v_B of our system are well within the 500 mV compliance range of the AD9959 DACs, as expected by the calculations made in Equation 15. Equation 17 means that our DAC termination resistors need to have a value of 56 Ω and that the differential impedance between the DAC outputs is $R_{\text{DIFF}} = 2R_O = 112\,\Omega$.

4.4 Reconstruction Filter

The LPF in this system will be an IC that is sourced from Mini-Circuits. Building and testing a reconstruction filter (and frequency multiplier filter) was out of the scope of this semester project. Since it is single-ended it has to be placed after the transformer. Its constraints are the following:

- Cut-off frequency (F2) as close as possible to 250 MHz.
- Sharp cut-off, meaning that stopband F3 - F2 should be small and that the rejection at F3 should be high.

Table 4 show the options available on Mini-Circuits for the reconstruction filter.

Name	Passband (Cut-Off) F2 (MHz)	Stopband F3 (MHz)	Reject. at F3 (dB)	F3 - F2 (MHz)	Stopband F4 (MHz)	Reject. at F4 (dB)	Footprint Area (mm^2)
LFCN-160+	230	330	20	100	480 - 2700	35	5
RLP-216+	**232**	**295 - 340**	**20**	**63**	**340 - 1300**	**40**	**79**
SXLP-225+	250	340 - 440	20	90	440 - 1600	40	184
LFCN180+	270	370	20	100	535 - 2350	40	5

Table 4: Options for the Reconstruction Filter.

For the reconstruction filter, the choice is far from obvious. All of these filters have different fall-off curves and the rejections are not measured the same way across the filters. The choice to use the RLP-216+ was made because it has a very steep cut-off (F3 - F2 = 63 MHz) and its cut-off frequency at 232 MHz is a good value for the frequencies this board is intended to generate (up to 200 MHz). Also, the measurements made by Mini-Circuits suggest that the RLP-216+ has a rejection at F3 of 30-50 dB and 70 dB at F4, so the numbers in the datasheet in Table 4 do not tell

the full story. At first, we wanted to use the LFCN-160+ for its compact size, but the rejection (20 and 35 dB) of the filter was projected to be too small for use as a reconstruction filter.

The decision process was also guided by using the simulation of the DDS output using the ADIsimDDS [20a] which revealed[4] that the AD9959 in combination with the RLP-216+ reconstruction filter delivers a signal with acceptable fidelity up to around 200 MHz. However, to achieve certainty that the reconstruction filter RLP-216+ is the right choice, real-world testing of the DDS Board is required.

4.5 Pre-Amplifier

To reach the target output power of 5 dBm and also the required power for the frequency doubler (at least 12 dBm) described in Section 4.7 we need a pre-amplifier that can amplify the -4.5 dBm output signal that we calculated in Equation 20. The requirements for this amplifier are the following:

- Low noise figure to compromise the signal as little as possible.
- Frequency range of 10 to 200 MHz.
- Gain of at least 16.5 dB (12 dBm - (-4.5 dBm)).
- P_{1dB} of at least the gain plus -4.5 dBm.
- Low power consumption since there are going to be four amplifiers on one board and high power consumption could lead to a high of thermal dissipation at the linear voltage regulators or the need to route thick traces on the board.

Table 5 shows some of the options available on Mini-Circuits.

Name	Frequency Range (MHz)	Gain (dB)	Noise Figure (dB)	P1dB (dBm)	Projected Output Power (-4.5 dBm) + Gain (dBm)	Power Consumption (W)
PHA-13LN+	**1 - 1000**	**22.4**	**1**	**24.5**	**17.9**	**0.21**
LHA-13LN+	1 - 1000	22.4	1.1	23.3	17.9	0.22
PHA-13HLN+	1 - 1000	22.7	1.1	28.7	18.2	1.9
TSS-13LN+	1 - 1000	22.8	1.1	24.5	18.3	0.22
LHA-13HLN+	1 - 1000	22.7	1.2	28	18.2	1.9
TSS-13HLN+	1 - 1000	23	1.4	28.4	18.5	1.9
PSA-39+	DC - 6000	23	2.2	10.7	18.5	0.16

Table 5: Options for the Pre-Amplifier. All values reflect the typical behavior and can change depending on the frequency.

Three amplifiers fulfill the constraints that we set and we chose the PHA-13LN+ because it had the lowest noise figure (see the discussion on noise in Section 4.6). With this choice, the output signal will have an approximate power of 18 dBm. This is too high for the amplifier ZHL-1-2W+

[4]The parameters for the simulation are: Clock Input: 25 MHz, Multiplier: 20x, Target Output Frequency: 200 MHz, Filter Topology: Inverse Chebyshev, Order: 7, Fc: 232 MHz, Stop Band Atten.: 60dB.

that will be connected to the board (see Section 4.1). However, it was decided not to include an attenuator on the non-frequency-doubled output line, because it is possible to regulate the output power on the AD9959 via software. There is a 10-bit register per channel that steers the fraction of output power on that channel that the AD9959 provides. It is the responsibility of the user not to overdrive the connected load. The benefit of not including an attenuator is that the board might also be used for other use-cases where an output power of up to 18 dBm might be beneficial.

4.6 Noise Characteristics

The datasheet of the AD9959 describes the noise of the DACs in both wideband and narrow-band spurious-free dynamic range (SFDR) in dBc (decibels relative to the carrier signal). SFDR is the strength ratio of the fundamental signal to the strongest spurious signal in the output.

The datasheet of the PHA-13LN+ describes the noise of the amplifier by the noise figure in dB. The noise figure is a measure of how the the signal-to-noise ratio (SNR) is degraded by a device [20f]. The SNR is defined as the ratio of the power of a signal to the power of background noise in dB. Kester [Kes09] gives a good description on the differences between the SNR and SFDR and other noise measurements.

For the following calculations we will treat the SFDR measurements of the AD9959 as SNR measurements. This is obviously imprecise but the only possibility since the AD9959 does not specify its SNR and the noise figure is only applicable to an SNR measurement.

Freuquency	1 MHz	5 MHz	10 MHz	50 MHz	100 MHz	150 MHz	200 MHz
AD9959 SNR (dB) (this is actually the wideband SFDR)	-65	-65	-65	-62	-59	-56	-53
PHA-13LN+ Noise Figure (dB)	2.9	1.7	1.2	0.93	0.93	0.92	0.91
Output SNR (dB)	-62	-63	-64	-61	-58	-55	-52

Table 6: Noise Estimate of the AD9959 DDS IC Combined with the PHA-13LN+ amplifier.

Table 6 shows the expected result that the output SNR is not notably worsened by the PHA-13LN+ low noise amplifier.

4.7 Frequency Doubler

It was decided that a frequency multiplier that doubles the frequency on a separate output line should be added to effectively double the possible output frequency range. This separate line would not have the same signal integrity as the non-doubled line, but it would give the users the freedom to do experiments that need higher frequencies while still being able to use the same device with minor modifications to the board. The constraints for the frequency doubler were the following:

- Input frequency range between 100 MHz and 200 MHz, giving an output frequency range of 200 to 400 MHz. The reason for this range is that for output frequencies lower than 200 MHz the normal line will be used.
- Input power range minus the conversion loss should yield an output power of ≈ 5 dBm as discussed in Section 4.1. It is not desirable to add another amplifier after the frequency

multiplier for several reasons (additional noise, cost, board space, power management, and so on).

- High F1 fundamental (input frequency) suppression since the input frequency is hard to filter out after the frequency multiplication because it is lower than the output frequency. F3, F4 can be filtered out with a LPF with a cut-off frequency at 400 MHz.

Table 7 lists the options available for a 2x frequency multiplier at the desired frequency range from Mini-Circuits.

Name	Input Frequency Range (MHz)	Input Power Range (dBm)	Conversion Loss (dB)	Expected output Power Range (dBm)	F1 Suppression (dBc)
AMK-2-13+	10 - 500	4 - 10	11.4	(-7.4) - (-1.4)	45
LK-3000+	70 - 1500	12 - 15	10.5	1.5 - 4.5	27
SYK-2-33+	50 - 1500	11 - 15	11.5	(-0.5) - 3.5	30
SYK-2R+	**10 - 1000**	**12 - 16**	**10.5**	**1.5 - 5.5**	**35**

Table 7: Options for the 2x Frequency Multiplier.

Both the LK-3000+ and the SYK-2R+ fulfill the first two constraints. The choice was made to use the SYK-2R+ because of its higher F1 suppression, i.e. the third constraint.

4.7.1 Attenuator

On the line of the frequency multiplier, it makes sense to include an attenuator before the multiplier as this line is solely fed into the multiplier and the multiplier could be damaged should it receive the full output power of 18 dBm of the amplifier. This attenuator should have the following properties:

- Frequency range between 100 MHz and 200 MHz since this is on the frequency doubler line.
- An attenuation of 3 dB ensures a safe input power to the frequency multiplier of around 15 dBm while still keeping the output power of the frequency multiplier high at around 15 dBm - 10.5 dBm = 4.5 dBm.
- The attenuator needs to have a maximum input power above 18 dBm $\approx$ 0.06 W which turns out to not constrain the choice at all since all attenuators in the list fulfill it.
- High return loss which is the ratio in dB of the incident power sent towards the device under test (DUT) to the reflected power. For example, if a device has a return loss of 10 dB and an input signal with power 30 dBm = 1 W enters the device, 30 dBm - 10 dB = 20 dBm = 0.1W of the power is reflected. Thus 1 W - 0.1 W = 0.9 W is transmitted.

Table 8 shows the attenuators with 3 dB attenuation and their properties available on Mini-Circuits.

Name	Frequency Range (MHz)	Return Loss Typ. (dB)	Maximum Input Power (W)
GAT-3+	DC - 8000	32.3	0.5
KAT-3+	DC - 43500	24.9	2
LAT-3+	**DC - 2500**	**32.3**	**0.5**
PAT-3+	DC - 7000	36.6	1
QAT-3+	DC - 50000	23.1	2
RCAT-03+	DC - 20000	14.0	2
YAT-3A+	DC - 18000	25.7	2

Table 8: Options for the 3 dB attenuator.

All the attenuators in the list fulfill the constraints and the choice to take the LAT-3+ was made because it offered a high return loss in a compact form factor.

4.7.2 Filter

A frequency doubler also produces unwanted spikes at three and four times the input frequency, where the 4x multiplication is especially pronounced. These unwanted frequencies can be filtered out by a LPF after the frequency multiplier. This LPF should have the following properties:

- Cut-off frequency (F2) as close as possible to 400 MHz.
- Sharp cut-off, meaning that stopband F3 - F2 should be small and that the rejection at F3 should be high.

Table 9 shows the options available on Mini-Circuits for the frequency range that we are interested in.

Name	Passband (Cut-Off) F2 (MHz)	Stopband F3 (MHz)	Reject. at F3 (dB)	F3 - F2 (MHz)	Stopband F4 (MHz)	Reject. at F4 (dB)	Footprint Area (mm^2)
LFCN-225+	**350**	**460**	**20**	**110**	**510**	**40**	**5.1**
XLF-42M+	350	660	30	310	6800	40	25
RLP-340+	365	475	20	110	560	40	79
XLF-221+	370	570	14	200	3500	20	9
SALF-325+	383	480	20	97	580	40	184
LPF-B375+	395	440	20	45	-	-	252
SXLP-400+	435	500	20	65	-	-	210

Table 9: Options for the Low Pass Filter After the Frequency Multiplier.

There are lots of options available and there is no clear best option for the LPF after the frequency multiplier. The LFCN-225+ was chosen because it should be adequate for filtering out frequencies above 400 MHz that are already attenuated a little by the frequency multiplier. It is also compact and was already on hand since I ordered it as a reconstruction filter during the project for which it was unfit.

4.8 Clock Multiplier

The clock that will steer the AD9959 and its DACs is a common 10 MHz laboratory clock reference, the SRS FS725, that synchronizes various devices needed for experiments in the TIQI lab. The AD9959 has a 20x maximum PLL clock multiplier. Thus we need to bring the 10 MHz clock up to 25 MHz externally if we want to clock the AD9959 at its full 500 MHz. For this, a 2.5x clock multiplier is used. Table 10 shows the properties of the clock multiplier IC that was selected for the DDS Board.

Manufacturer	ON Semiconductor
Name	NB3N502
Maximum Clock Output Frequency	190 MHz
Input Clock Frequency Range	2 - 50 MHz
Clock Multiplication	Adjustable (2x, 2.5x, 3x, 3.33x, 4x, 5x)
Operating Voltage	3 - 5.5 V
Power Supply Current Typ.	20 mA

Table 10: Properties of the NB3N502 Clock Multiplier.

4.9 Power Delivery: Linear Voltage Regulators

The power delivery to the various devices on the board is handled by linear voltage regulators that take the 5 V input voltage and regulate it down to 3.3 V, 3 V, and 1.8 V. The reason why we choose linear voltage regulators over the typically more efficient switching DC-DC converters is that the switching converters operate at frequencies in the high kHz or low MHz domain which might lead to electromagnetic interference (EMI) on the board that could increase the noise the output signal and because a low conversion efficiency was not a big concern since the device is not battery powered.

Linear voltage regulators dissipate heat energy that is proportional to the difference between the input and output voltage. The dissipated power can be bounded by Equation 21:

$$P_D \leq (V_{\text{IN}} - V_{\text{OUT}})I_{OUT}, \tag{21}$$

where P_D is the dissipated power, V_{IN}, and V_{OUT} are the in- and output voltages, and I_{OUT} is the output current. This equation will be used to calculate the total power dissipation of the DDS Board in Section 4.13. Note that the linear dependency of the power dissipation on the input voltage is one of the reasons why the input voltage to the board was chosen as 5 V and not a higher value. The higher V_{IN} the higher the power dissipation at each voltage regulator. The other reason for choosing 5 V is that is readily available in a lab environment.

The linear voltage regulators used on the board are AMS1117-1.8, AMS1117, and AMS1117-3.3 for an output voltage V_{OUT} of 1.8 V, 3 V, and 3.3 V respectively. They were chosen because they were available as components from JLCPCB for direct assembly at the PCB manufacturing site and because they had a high enough current rating for our purposes (see Section 4.13). Table 11 shows some of the properties of the AMS1117.

Manufacturer	Advanced Monolithic Systems
Name	AMS1117
Output Current	1 A
Output Voltage V_{OUT} (1.5 V, 1.8 V, 2.5 V, 2.85 V, 3.3 V, 5.0 V))	Adjustable or Fixed
Maximum Input Voltage	15 V
Max. Dropout Voltage (Difference Between V_{IN} and V_{OUT})	1.3 V

Table 11: Properties of the AMS1117 Linear Voltage Regulator.

4.10 Overvoltage, Undervoltage and Overcurrent Protection

The DDS Board includes an IC that protects the linear voltage regulators (and possibly other parts on the board) from overvoltage, undervoltage and overcurrent if a user was to mistakenly provide more than 5 V to the system. The IC used for this purpose is the TPS25921A and its properties can be seen in Table 12.

Manufacturer	Texas Instruments Inc.
Name	TPS25921A
Overvoltage Protection	Adjustable (set to 5.5 V)
Undervoltage Protection	Adjustable (set to 4.5 V)
Maximum Input Voltage V_{IN}	20 V
Overcurrent Protection	Adjustable (set to 1.6 A)

Table 12: Properties of the TPS25921A Overvoltage, Undervoltage and Overcurrent Protection IC.

4.11 Routing

The DDS Board is a 4 layer board that is impedance matched using the JLC7628 stackup from JLCPCB [20e]. There are two categories of layers that can be used while routing a PCB: Reference planes (GND and other voltages) and signals. It is recommended to stack the layers symmetrically, as the board can otherwise warp during the manufacturing process [Ott09]. This leaves us with the two options for the 4 layer board shown in Table 13:

	Option 1	Option 2
Top Outer Layer	Signals	Reference Plane
Top Inner Layer	Reference Plane	Signals
Bottom Inner Layer	Reference Plane	Signals
Bottom Outer Layer	Signals	Reference Plane

Table 13: Options for the Stackup of a 4 Layer PCB.

Option 1 has the advantages that signals do not have to travel through vias to reach components, that reference planes on the inner layers are continuous and not broken up by components and that debugging and rework to the PCB is generally easier because of the exposed signal traces. Option

2 has the advantage of shielding the signals from EMI because of the external reference planes. For both the DDS Board and the Control Board, Option 1 was chosen.

The layers on the DDS Board are organized in the following way:

1. Top outer layer: Analog and digital signal traces with an adjacent ground plane. All analog signals are routed on the top layer to remove the possibility of adding noise by using vias.

2. Top inner layer: Ground Plane. This is necessary to conform to the impedance matching models (see Section 3.2).

3. Bottom inner layer: Analog and digital power traces and 5 V power plane. The 5 V power plane simplifies the delivery of power to all the linear voltage regulators.

4. Bottom outer layer: Digital signal traces with an adjacent ground plane. This layer is used to route otherwise crossing digital signals.

4.11.1 Impedance Matching of the DDS Board Traces

The digital traces have been designed to have a characteristic impedance of 68 Ω so that they match the impedance for the digital traces on the Control Board (see Section 5.8). Using the JLCPCB impedance calculator [20c] we find a trace width of 5.87 mils ≈ 0.15 mm for the digital traces.

The analog traces have a characteristic impedance of 50 Ω to match all the parts on the board. Using the JLCPCB impedance calculator [20c] we find a trace width of 11.55 mils ≈ 0.29 mm for the digital traces. Since we also have a ground plane around the traces, we use CHEMANDY's calculator [19a] to calculate the gap width between the traces and the ground plane for the coplanar waveguide model. The calculations result in a gap width $g = 5\,\text{mils} = 0.127\,\text{mm}$.

The differential outputs of the AD9959's DACs have a differential impedance of $2R_O = 112.5\,\Omega$. Using the JLCPCB impedance calculator [20c] we find a trace width of 6.04 mils ≈ 0.15 mm and a trace separation of 8 mils ≈ 0.2 mm.

The reference clock also has a differential routing on the board after it is transformed from a single-ended signal to a differential signal. Its differential impedance is $2 \cdot 25\,\Omega = 50\,\Omega$. The JLCPCB impedance calculator [20c] does not support the calculation of differential impedances below 70 Ω. This is not ideal, since we do not know what the reason for the limit is. It could be that the approximation in this calculation does not hold at these low differential impedances. Since the clock signal is digital, it might not be as much of a problem if it is not perfectly impedance matched. Testing will reveal, whether the clock signal has a high enough fidelity for the DDS to function correctly.

Other calculators have delivered a range of results for the trace width and trace separation for a differential impedance of 50 Ω and an approximate value was chosen that was somewhere close the average of the calculated values, giving a trace width of 18.7 mils ≈ 0.47 mm and a trace separation of 5 mils = 0.127 mm. The trace width did not fit into the pin layout of the AD9959 and the traces had to be slightly thinned to 0.35 mm at the end. Testing the DDS Board will reveal whether that adjustment leads to EMI on the board or reflections in the clock traces.

4.11.2 Radio Frequency Trace Considerations

The analog RF traces on the DDS Board have been routed such they do not have any corners. Instead, they have rounded bends to reduce the possibility of EMI occurring on the board.

Fencing vias have been placed along the sides of the analog traces to increase the isolation of the analog traces from noise.

4.12 Amplifier Test Board

During the design phase of the DDS Board, a prototype board was designed to test the amplifier, frequency multiplier, and power delivery to the amplifier. Apart from the linear voltage regulator (which is the MCP1827S-3002E), the design consists of the same parts as the actual DDS Board. Figure 12 shows a render of the fully assembled test board.

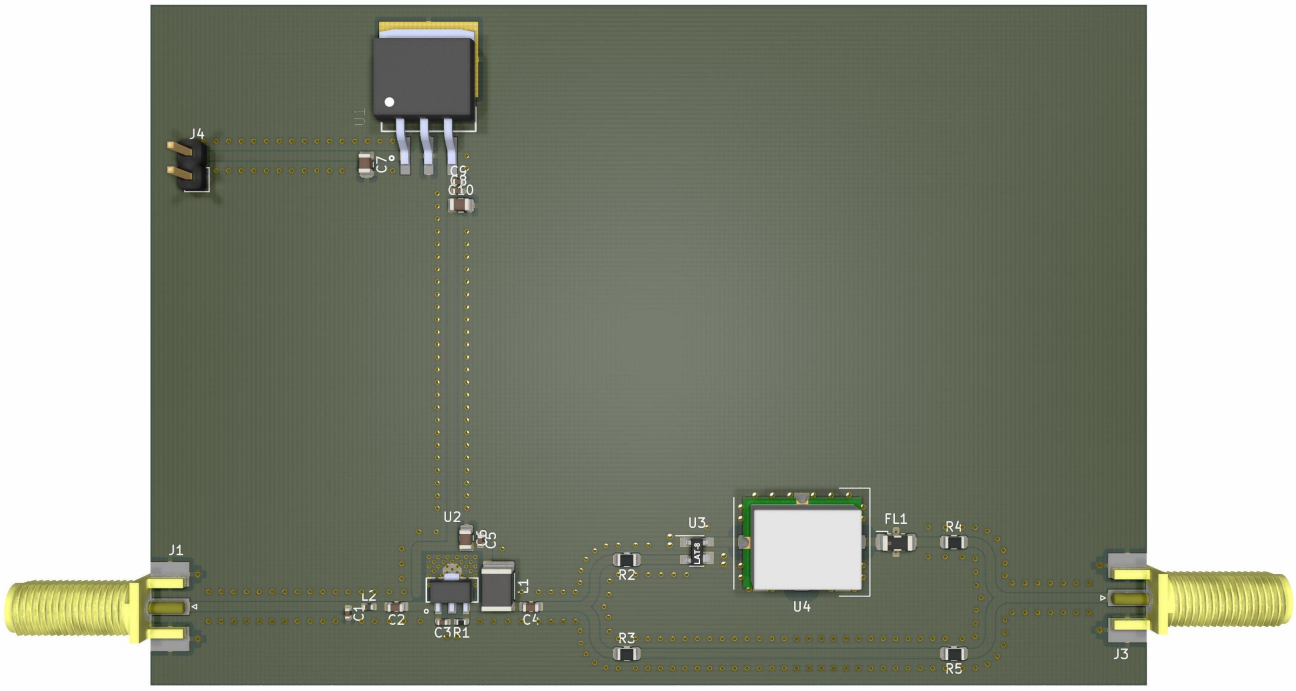


Figure 12: Render of the Amplifier Test Board with the Linear Voltage Regulator (U1), the In- and Output SMA Connectors (J1 and J3), the Amplifier (above R1 and C3), the Attenuator (U3), the Frequency Multiplier (U4) and the LPF after the Frequency Multiplier (FL1).

The amplifier test board was assembled during the project and tested. Because of delivery delays of the frequency multiplier SYK-2R+, we could not test or assemble the frequency-doubled lines (upper line on the render). The amplifier was tested using a network analyzer and the test results can be seen in Figure 13.

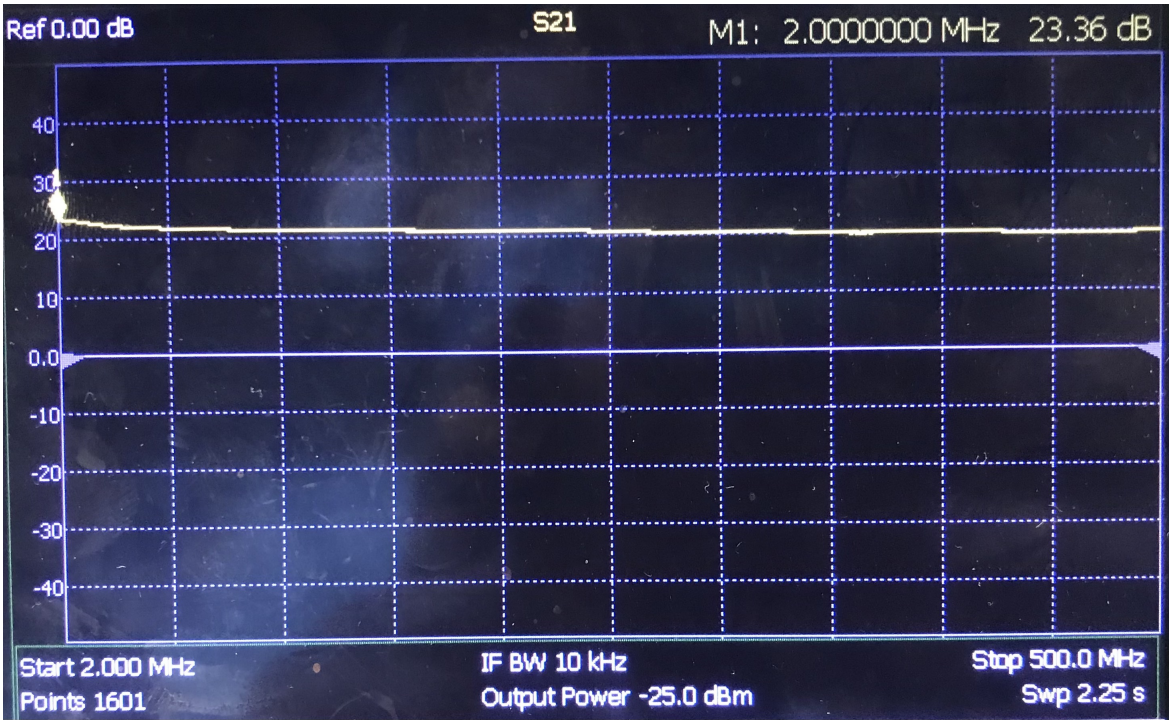


Figure 13: Network Analyzer Data for the Gain of the PHA-13LN+ Amplifier in the Frequency Range of 2 - 500 MHz.

The network analyzer is a device with two ports that outputs a signal on one of the ports and measures the incoming signal on the other port. It then compares the two signals and can plot differences in the phase or amplitude of the two signals. In the case of Figure 13 the amplitude difference of the output signal to the input signal was plotted for the frequency range from 2 to 500 MHz. We see the expected gain of around 22 dB of the PHA-13LN+ minus the insertion loss of the input transmission line connecting the DUT to the analyzer since it was calibrated using only one line.

4.13 Summary and Specifications

The final design of the Seadragon DDS Board that is capable of producing RF signals in the frequency range of 1 up to 400 MHz with four phase-matched channels at an output power of up to 19 dBm with a size of 100x160 mm (see Figure 14). It meets the design criteria that were set out and is smaller, less expensive, should be more reliable, and has a larger frequency range than the system it replaces. It should also be possible to synchronize multiple DDS Boards using the SYNC_IN and SYNC_OUT pins leading to even more phase-matched channels[5].

[5]There are multiple modes which synchronize the clock of the AD9959 slave devices (using pin SYNC_IN) to the clock of the AD9959 master device which uses the pin SYNC_OUT to connect (for more details, see "SYNCHRONIZING MULTIPLE AD9959 DEVICES" in the AD9959 datasheet [08]).

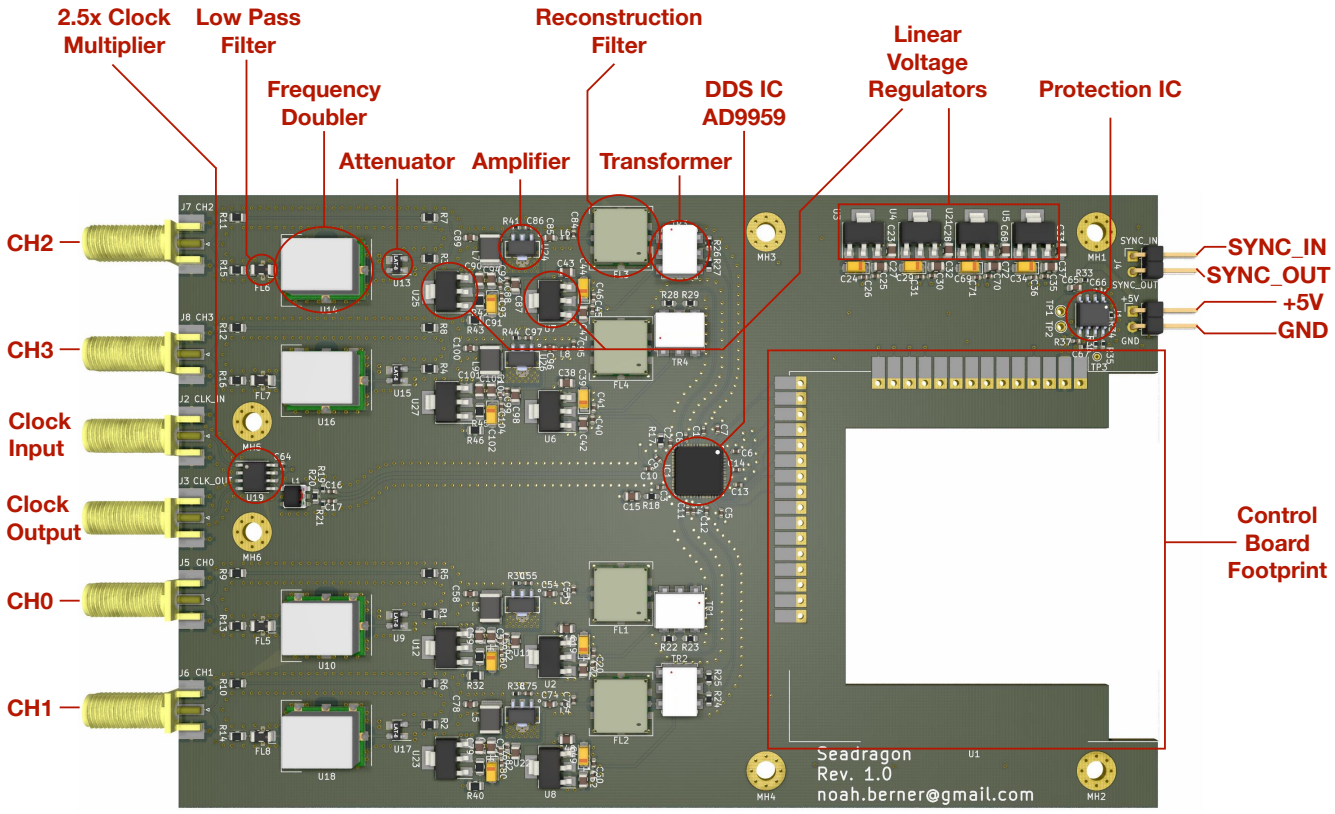


Figure 14: Annotated Render of the Final Design of the Seadragon DDS Board.

The DDS Board could not be manufactured and tested during the semester project, but theoretical calculations about some of its properties can be made and verified in the future by testing. The data in the Tables 14 through 16 was retrieved from the respective datasheets for a temperature of 25° C. If a value was not available linear interpolation was used. The calculations were performed with the highest precision available and then rounded to two significant figures since that was the lowest precision of any given value.

Table 14 show the output power at different frequency ranges. Observe that the input power to the frequency multiplier is always in the recommended range of 12 to 16 dBm, except for 200 MHz. Through future testing of the DDS Board we will be able to determine if the frequency multiplied output up to 200 MHz will deliver an acceptable signal or not. Also, the output power of the frequency multiplier after the filter is within the acceptable range for the ZHL-1-2W+ amplifier after accounting for the loss in the lines.

Output Frequency	1 MHz	10 MHz	50 MHz	100 MHz	150 MHz	200 MHz
AD9959 Output Power	-4.5	-4.5	-4.5	-4.5	-4.5	-4.5
After Amplitude Roll-Off (see Equation 7)	-4.5	-4.5	-4.7	-5.1	-5.9	-7.0
After Transformer Insertion Loss	-4.8	-4.8	-5.1	-5.6	-6.7	-8.2
After Reconstruction Filter Insertion Loss	-4.9	-4.8	-5.2	-6.0	-7.3	-9.0
After Amplifier Gain (Standard Output)	**19**	**19**	**17**	**16**	**15**	**13**
2x Frequency Output	2 MHz	20 MHz	100 MHz	200 MHz	300 MHz	400 Mhz
After Attenuator	16	16	14	13	12	10
After Frequency Multiplier Conversion Loss	-	5.4	4.3	3.1	1.7	-0.082
After LPF Insertion Loss (Frequency Doubled Output)	**-**	**5.2**	**3.9**	**2.5**	**0.35**	**-6.9**

Table 14: Theoretical Calculations of the Output Power of the DDS Board for Different Output Frequencies. All Values are in dBm and Represent the Output Power After the Loss or Gain of the First Column Has Been Applied.

Table 15 shows the expected power dissipation of the various components on the board. It might be necessary to manufacture a thermally conducting backplane or heat sink to passively transfer the 2.2 W of dissipated heat away from the board.

Component	Typical Power Dissipation (W)	Maximum Power Dissipation (W)
AD9959 DDS IC	0.54	0.68
3.3 V Regulator	0.10	0.10
1.8 V AVDDx Regulator (4x on Board)	0.12	0.15
1.8 V DVDD Regulator	0.34	0.46
3.0 V Amplifier Regulator (4x on Board)	0.14	0.14
LAT-3+ Attenuator at 19 dBm (4x on Board)	0.040	0.040
Total:	**2.2**	**2.6**

Table 15: Theoretical Calculations of the Power Dissipation of the DDS Board.

Table 16 calculates the current draw from the power supply by any given component. The expected maximum current draw of 1.2 A is below the overcurrent protection of approximately 1.4 A and should thus not interrupt the normal behavior of the DDS Board.

Component	Typical Current Draw (A)	Maximum Current Draw (A)
AD9959 DDS IC	0.30	0.37
NB3N502 Clock Multiplier	0.020	0.020
PHA-13LN+ Amplifier (4x on Board)	0.071	0.071
Controller Board (see Table 19)	0.14	0.57
Total:	**0.75**	**1.2**

Table 16: Theoretical Calculations of the Current Draw of the DDS Board.

5 Dragonrider Microcontroller Circuit Board Design

The AD9959 needs to interface with the rest of the equipment in the TIQI lab and thus it must integrate well with the existing infrastructure. This section describes the design of the separate Control Board, named Dragonrider, that is used to fulfill the task of controlling the DDS Board and interfacing it with the lab equipment.

The constraints for the Control Board are the following:

- Serial Peripheral Interface (SPI) and 10 general-purpose input/output (GPIO) pins to control the AD9959.
- Ethernet and Universal Serial Bus (USB) port as an interface for the lab control equipment.
- Python compatibility since Python is an accessible language and most of the code for the old system is written in Python, which might be reused or can serve as a starting point for software of the new system.
- Flash memory that runs the firmware or operating system (OS) as the SD cards in the current system tend to fail over time.
- Most of the components should be available on JLCPCB meaning that the board can be mostly assembled by the manufacturer and the prototyping phase can be accelerated.
- Flexible design that can also be used for other projects.

Sections 5.2 through 5.7 will explain the different components of the board and why they were chosen. Figure 15 shows a simplified schematic of the Control Board and serves as an overview to show the separate components in the context of the whole Control Board.

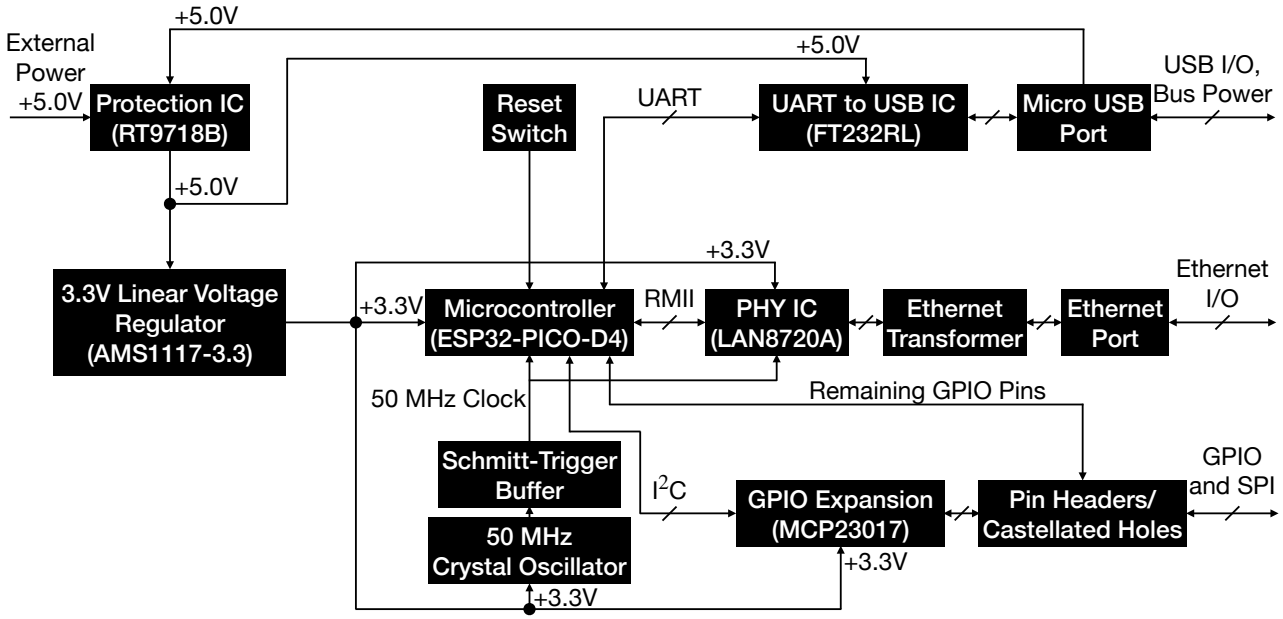


Figure 15: Simplified Schematic of the Dragonrider Control Board. The Names of the ICs are in Parentheses.

5.1 Python on a Microcontroller

Since the fourth constraint rules out the Raspberry Pi as our controller board because it uses an SD card as its booting medium, which tended to fail periodically in the old system, it was decided to use a microcontroller as the control IC. MicroPython is a full Python compiler and runtime that implements a subset of the Python standard library and is optimized to run on microcontrollers [Geo17]. Since MicroPython implements all the functions in the current control software of the AD9959 and is also compatible with the TIQI-remote procedure call (RPC) protocol, which is the default network communication protocol in the TIQI Group, it is a great fit as firmware for the microcontroller.

5.2 ESP32 Microcontroller

While many microcontrollers support the MicroPython runtime, only a few support an Ethernet connection. The ESP32 microcontroller family is the most used of them as it implements the medium access control (MAC) layer already into the IC and only needs an external chip to implement the physical layer (PHY). The Control Board uses an ESP32-PICO-D4 which has several advantages:

- Available as a part on JLCPCB.
- Integrates 4MB of flash memory which is more than enough to support MicroPython.
- Small form factor (7x7 mm).
- Integrated clock circuitry and decoupling capacitors.
- 50 Ω impedance matched Wi-Fi and Bluetooth antenna circuit. This is less of a benefit for this project as the Wi-Fi and Bluetooth on the Control Board for the DDS Board will be disabled, but it might be useful for other projects using this Control Board.

5.3 Physical Layer Integrated Circuit

The LAN8720A is the PHY IC that acts as the interface between the ESP32 and the Ethernet port used in this project. It was chosen because it was available on JLCPCB and it already has a software implementation in MicroPython in conjunction with the ESP32 which will save time during the software development phase. The ESP32 and the LAN8720A connect using the reduced media-independent interface (RMII) interface which is synchronized using a clock at 50 MHz. The RMII clock circuit on this Control Board is implemented using a 50 MHz oscillating crystal and a Schmitt-Trigger buffer. The Ethernet port is connected to the LAN8720A using an Ethernet transformer. Using all these components the ESP32 can have an Ethernet connection with little software development. This Ethernet connection will be the main communication channel between the Control Board and the rest of the lab.

5.4 Universal Asynchronous Receiver-Transmitter to Universal Serial Bus

The ESP32 implements the universal asynchronous receiver-transmitter (UART) protocol which we will use to connect the ESP32 to a USB connector. The IC that interfaces the UART pins from the ESP32 with the USB connector is the FT232RL. The USB port can be used for programming and debugging the Control Board.

5.5 General-Purpose Input/Output Expansion

The ESP32-PICO-D4 only has 28 GPIO pins, 6 of which are input only. Table 17 shows how many of the pins are already occupied by the connections for the PHY chip and the UART to USB converter.

	GPIO Pins	Input Pin
Available on the ESP32-PICO-D4	22	6
RMII to LAN8720A	12	1
UART to FT232RL	4	0
SPI to AD9959	3	0
Other to AD9959	9	1

Table 17: GPIO Pin Count of the Control Board.

We see that we lack 6 GPIO pins to connect the ESP32 to the AD9959. To circumvent this problem we use a GPIO expander to wire the connections to the AD9959 that are not involved in the SPI protocol since the SPI protocol relies on fast, direct communication from the ESP32. The MCP23017 GPIO expander provides 16 additional GPIO pins while only using up 2 GPIO and 2 input pins on the ESP32 using the Inter-Integrated Circuit (I^2C) protocol. The I^2C connection to this GPIO expander are optional and thus can free up the 2 GPIO and 2 input pins, if a project in the future does not need the additional GPIO pins and would rather have a direct connection to the ESP32.

5.6 Power Delivery

The Control Board can be powered either by USB bus or by an external 5 V power supply. An AMS1117-3.3 linear voltage regulator is used to convert the 5 V down to 3.3 V for all the devices on the board.

5.7 Overvoltage, Undervoltage and Overcurrent Protection

The Control Board uses the same TPS25921A protection IC as the DDS Board (see Section 4.10). However, the overcurrent protection has been lowered to ≈ 1.0 A as the Control Board draws less current than the DDS and Control Board combined.

5.8 Routing

The Control Board is a 4 layer board that is impedance matched using the JLC7628 stackup from JLCPCB [20e]. The layers are organized in the following way (following the same practices explained in Section 4.11):

1. Top outer layer: Signal traces with an adjacent ground plane. All high-speed signals (RMII and traces from the LAN8720A to the Ethernet transformer and port) are routed on the top layer to remove the possibility of adding noise by using vias.

2. Top inner layer: Ground Plane. This is necessary to conform to the impedance matching models (see Section 3.2).

3. Bottom inner layer: 3.3 V power plane which simplifies the delivery of power to all the parts on the Control Board.

4. Bottom outer layer: Signal traces with an adjacent ground plane. This layer is used to route otherwise crossing digital signals.

5.8.1 Impedance Matching of the DDS Board Traces

The digital traces have been designed to have a characteristic impedance of 68 Ω so that they match the impedance of the LAN8720A which outputs signals with an impedance of 68 Ω on the RMII. Using the JLCPCB impedance calculator [20c] we find a trace width of 5.87 mils ≈ 0.15 mm for the digital traces.

The analog trace leading to the SMA connector for the antenna is routed using a characteristic impedance of 50 Ω. Using the JLCPCB impedance calculator [20c] we find a trace width of 11.55 mils ≈ 0.29 mm for the digital traces. Since we also have a ground plane around the traces, we use CHEMANDY's calculator [19a] to calculate the gap width between the traces and the ground plane for the coplanar waveguide model. The calculations result in a gap width $g = 5\,\text{mils} = 0.127\,\text{mm}$.

The differential connections between the LAN8720A and the Ethernet transformer, as well as the connections between the Ethernet transformer and the Ethernet port have a differential impedance 100 Ω. Using the JLCPCB impedance calculator [20c] we find a trace width of 6.89 mils ≈ 0.18 mm and a trace separation of 6 mils ≈ 0.15 mm.

5.9 Summary and Specifications

The final design of the Dragonrider Control Board is a versatile board that cannot only control the DDS Board and interface it with the rest of the lab equipment but can also be used for other projects. It has an Ethernet and USB port, up to 20 GPIO ports and 3 input ports. It is capable of running MicroPython, has a compact form factor of 60x60 mm and it meets the design criteria that were set out in Section 5. Figure 16 shows a render of the Control Board.

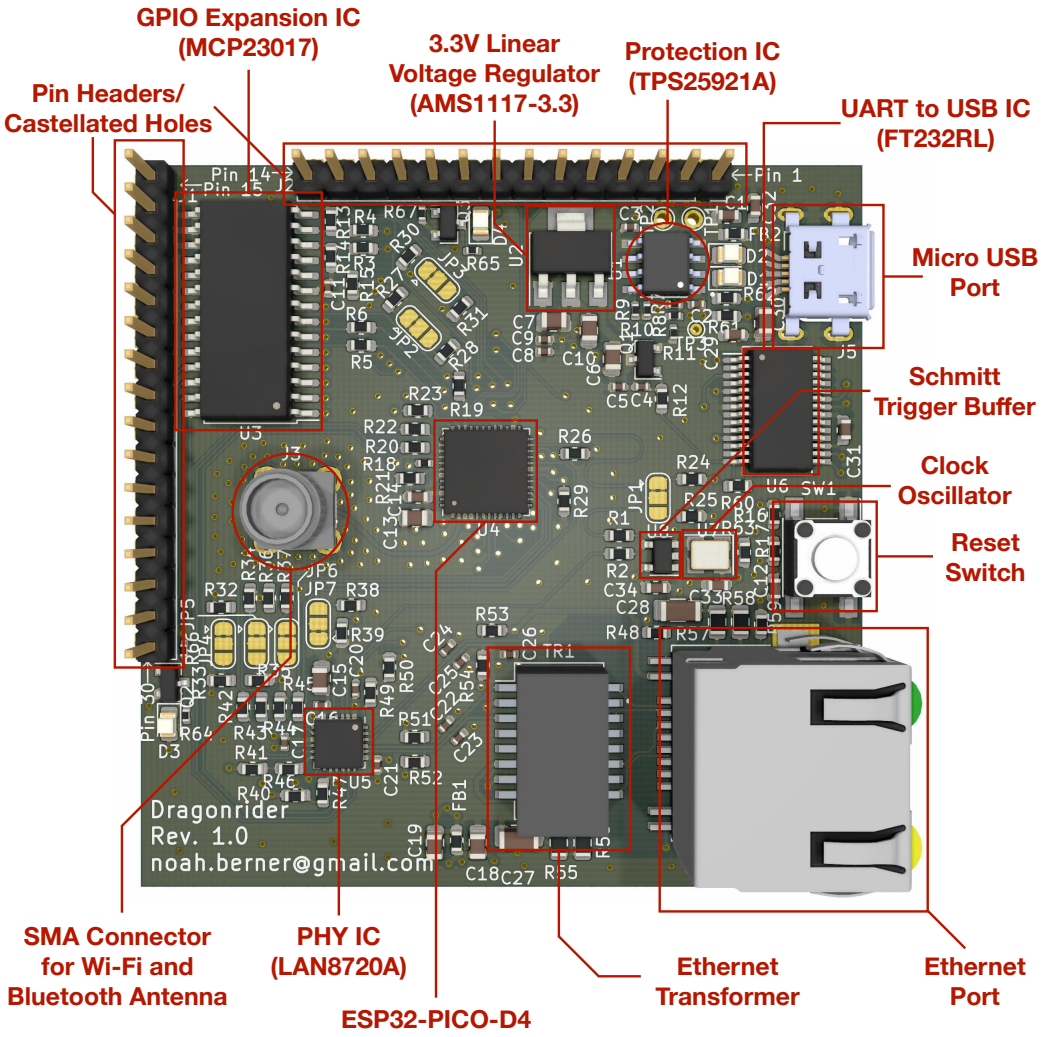


Figure 16: Annotated Render of the Final Design of the Dragonrider Control Board.

The data in the Tables 18 and 19 was retrieved from the respective datasheets for a temperature of 25° C. The calculations were performed with the highest precision available and then rounded to two significant figures since that was the lowest precision of any given value.

Table 18 shows the expected power dissipation of the various components on the board. The heat dissipation on the Control Board is dependent on the compute operations performed on the ESP32. It is expected that the software to control the DDS Board is not computationally demanding because only slow changes (on human time-scale) to the DDS parameters are necessary and thus the server that is running on the Control Board needs only slow communication to the outside world. Thus the power dissipation on the Control Board is likely small enough that passive dissipation without a heat sink is sufficient. For other, more demanding applications it might be necessary to attach a heat sink to the ESP32 IC or a rigid backplane to the Control Board.

Component	Typical Power Dissipation (W)	Maximum Power Dissipation (W)
ESP32-PICO-D4	0.26	1.7
3.3 V Regulator	0.25	0.97
LAN8720A	0.16	0.18
FT232RL	0.075	0.50
MCP23017	0.0033	0.0033
Total:	**0.75**	**3.3**

Table 18: Theoretical Calculations of the Power Dissipation of the Control Board.

Table 16 calculates the current draw from the power supply or USB bus by any given component. The expected maximum current draw of 0.57 A is below the overcurrent protection of approximately 0.93 A and should thus not interrupt the normal behavior of the Control Board.

Component	Typical Current Draw (A)	Maximum Current Draw (A)
ESP32-PICO-D4	0.080	0.50
LAN8720A	0.045	0.049
FT232RL	0.015	0.015
MCP23017	0.001	0.001
Crystal Oscillator	0.0038	0.0045
Total:	**0.14**	**0.57**

Table 19: Theoretical Calculations of the Current Draw of the Control Board.

5.9.1 Testing the Control Board Revision 0

A test version of the Control Board, dubbed Revision 0, was manufactured during the timeframe of the project. Revision 0 did not have a GPIO expansion IC. It was possible to verify that MicroPython can be installed on the Control Board and that the Ethernet and USB interface both function properly.

The only problem identified by the testing of Revision 0 was that the RT9718B protection IC that was used on Revision 0 detected a problem ($\overline{\text{WRN}}$ low) and protected the output by shutting down the voltage output. This problem was temporarily fixed by bridging the in- and output of the protection IC, thus forgoing the protection, to power the board. The source of the problem could not clearly be identified, but might be linked to the battery voltage monitoring input being connected directly to GND. Future revisions of the Control Board, such as Dragonrider Rev 1.0, use a different protection IC called TPS25921A because the RT9718B was no longer available on JLCPCB and because the reason for the unexpected protection could not be identified.

6 Future Work

Due to the limited time on the project, some tasks were left to be carried out in the future. These can be sorted into the three categories of software, testing, and case design. The following sections go into more detail on each topic.

6.1 Software Development

The hardware development and PCB design are the priority of this project and thus software development was postponed. However, during the PCB design phase, software development was always a concern and it was a goal to make future software development as trouble-free as possible. For example, the reason why MicroPython was chosen as the firmware of the Control Board, was because all of the existing code was written in Python and can thus largely be carried over to this project. The choice to use MicroPython majorly influenced the choice of various components on the Control Board. Following are some programs that have to be written or adjusted to make the DDS Board work in the intended way:

- Current DDS system: The current software that steers the AD9959 evaluation board from a Raspberry Pi has to be adapted to work in the MicroPython environment of the ESP32.
- Output power calculations: An idea to make the DDS Board software even more user friendly is to let the user pick the output power of a channel in dBm instead of a value from 0% to 100%. For more information see Section B.4.1
- TIQI RPC: see Section B.4.2.

6.2 Testing the Direct Digital Synthesis Board

When it is possible to manufacture the board, these are the first things we would like to evaluate:

- Simulation of the DDS output using the ADIsimDDS [20a] suggests that the AD9959 in combination with the RLP-216+ reconstruction filter delivers a signal with acceptable fidelity up to around 200 MHz (see Section 4.4). The fidelity of the actual output signal of the DDS Board should be tested and compared to the simulation at different frequencies to ensure that the simulation matches the real-world performance and that the board produces predictable signals with appropriate filtering.
- Testing the analog signal output power: The calculations in Table 14 should be verified, such that safe operation of the DDS board can be guaranteed. Driving a load with too much power can destroy it. This test can also help determine the loss and reflections in the PCB traces which is useful for the software-based output power calculations (see Section B.4.1).
- Testing the current draw: Table 16 calculates the typical and maximum current draw of the DDS Board. Verifying that these numbers are correct is important to select the right power supply.
- Thermal test: Measuring the heat spread on the PCB can give insight on whether a heat sink is needed to dissipate the heat or not. It can also lead to thermal noise sources in the signal (for example if one of the channels receives more heat than the others).

- 200 MHz input frequency doubler test: We saw in Table 14 that the input frequencies of 200 MHz and a bit below have too little signal power (10 dBm instead of the recommended 12 dBm) for the SYK-2R+ frequency multiplier. They are also heavily attenuated by the LPF after the frequency multiplier leading to a final output power of ≈ -6.9 dBm. Testing input frequencies up to 200 MHz on the frequency-doubled output can reveal up to which frequency a usable signal can be generated.

This is not an exhaustive list and there are other tests that can reveal more on the specifications of the DDS Board. It should serve as a starting point for future users and developers. In my opinion, the most important test is verifying the fidelity of the output signal and comparing it to the simulation results. The test shows whether the right reconstruction filter was chosen and thus, whether we need to change it or build our own.

6.3 Enclosure Design

To shield the DDS Board from outside noise, a case that encloses it should be designed and built. The DDS Board has been designed in a standard Eurocard form factor of 100x160 mm. For more information on the physical dimensions of the DDS Board read Section B.6.

6.3.1 Heat Sink

Table 15 and Table 18 show that the fully assembled DDS Board can potentially dissipate ≈ 3.0 W (the maximum is ≈ 5.9 W) during operation. This might make a heat sink or fan necessary, that transfers the heat away from the board and dissipates it into the environment. This heat sink or fan can be mounted using the M3 mounting holes in the DDS Board. For details, see Section B.6.

7 Conclusion

This semester project set out to improve the current DDS system of the TIQI Group by designing a custom PCB that houses all components needed for DDS on one board. The final design delivers on this goal and presents a solution that

- is easy to assemble (only a small number of parts have to be hand soldered as most of the components have been chosen such that the PCB manufacturer can solder them),
- has a larger frequency range (up to 400 MHz instead of 200 MHz),
- is possibly more durable since we have a dedicated independent controller running on solid-state memory, dedicated and specified for a particular task,
- is cheaper (the expected cost of the entire system (including Control Board and DDS Board with DDS IC, amplifiers, power delivery, frequency doubler,...) is about the same as the AD9959 evaluation board which is only one part of the current system),
- is smaller, which can provide greater scalability for experiments where a lot of DDS signals are needed (the fully assembled DDS Board (including amplifiers, Control Board, frequency doubler, power delivery,...) has a smaller surface area than the evaluation board alone, not including the amplifers and the rest of the current system),
- is future-proof due to the in-house design which can easily be modified.

Throughout the thesis, multiple design options have been considered and the most fitting parts have been chosen, leading to a design that, on paper, functions in an optimal way. Also, the separate design of the Control Board leads to the possibility to use it on other projects with similar control needs.

Developing the software for the DDS Board and integrating the board into the lab infrastructure was not possible during the project. However, the hardware design considerations regarding future software development should ease the process considerably.

Unfortunately, the time frame of the project did not allow for thorough testing of the complete DDS Board and only the Control Board could be tested in a limited way. The tests that were performed on the Control Board showed, that it worked in the intended way apart from the protection IC which will require more testing.

The future testing of the DDS Board will ultimately reveal whether the newly designed solution is capable of replacing the current solution.

A Dragonrider Microcontroller Board Documentation

The Control Board, named Dragonrider, features a versatile design that can be used in many different projects due to its compact size and many features. For a complete list of all the specifications, see Section 5.9. This documentation is aimed at readers who want to use the Control Board in their project or for users that want to use it in conjunction with the DDS Board.

A.1 Pinout

Figure 17 shows a schematic symbol of the Control Board. This symbol is available for KiCad in the digital appendix of the thesis. Following are explanations of the individual pins.

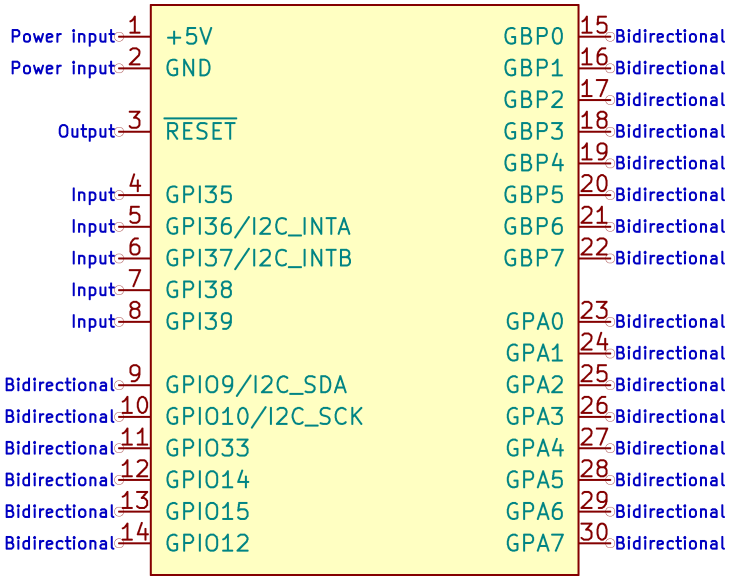


Figure 17: Schematic Symbol of the Control Board.

- Pin 1: If an external power supply is used (see Section A.3), connect pin 1 to the +5 V terminal of the power supply.
- Pin 2: If an external power supply is used (see Section A.3), connect pin 2 to the negative terminal or GND of the power supply.
- Pin 3: $\overline{\text{RESET}}$ is a shared active-low reset signal that is used on the Control Board to reset the PHY (LAN8720A) and GPIO expansion (MCP23017) chip simultaneously. It is broken out to pin 3 so that it can be used as an active-low reset signal for other devices that might need to be reset simultaneously to the PHY and GPIO expansion, for example after restarting the board.
- Pin 4,7 and 8: These three pins are input pins that lead directly to the ESP32. On the ESP32 they are named GPIO35 (pin 4), GPIO38 (pin 7) and GPIO39 (pin 8). Note: Even though these pins are named GPIOxx, they can only be used as inputs to the ESP32 and not as outputs.
- Pin 5 and 6: These pins are the same as pins 4,7 and 8 with the pin names GPIO36 (pin 5) and GPIO37 (pin 6). However, if the GPIO expansion chip (MCP23017) is enabled (see

Section A.5), they are already used as interrupt signals from the MCP23017 and should not be used externally.

- Pin 11 to 14: These four pins are true GPIO pins that lead directly to the ESP32. On the ESP32 they are named GPIO33 (pin 11), GPIO14 (pin 12), GPIO15 (pin 13) and GPIO12 (pin 14). They can be used as both input and output pins.
- Pin 9 and 10: These pins are the same as pins 11 to 14 with the pin names GPIO9 (pin 9) and GPIO10 (pin 10). However, if the GPIO expansion chip (MCP23017) is enabled (see Section A.5), they are already used for the I^2C communication to control the MCP23017 and should not be used externally.
- Pin 15 to 30: The pins 15 to 30 are the additional GPIO pins that stem from the MCP23017 GPIO expansion chip. They can be configured as inputs or outputs. Note that these GPIO pins are only available if the GPIO expansion chip (MCP23017) is enabled (see Section A.5)

A.2 Control Interface

The Control Board has two main ways how it can control outside equipment:

- Pin Headers: If the Control Board is set up as a floating device on its own, you can install pin headers into the holes on the pins 1 through 14 (14 pin headers) and 15 through 30 (16 pin headers). The pin header holes have a standard 0.1 inch pitch.
- Castellated Holes: On the two edges of the board that feature the pin header holes, there are also castellated holes that can be used to solder the Control Board onto another PCB. The recommended land pattern for the PCB that accommodates the Control Board can be seen in Figure 18. Note that the holes in the land pattern are optional since the pin headers do not have to be installed in this case. The holes can help with alignment during the soldering process. This land pattern can be found for KiCad in the digital appendix.

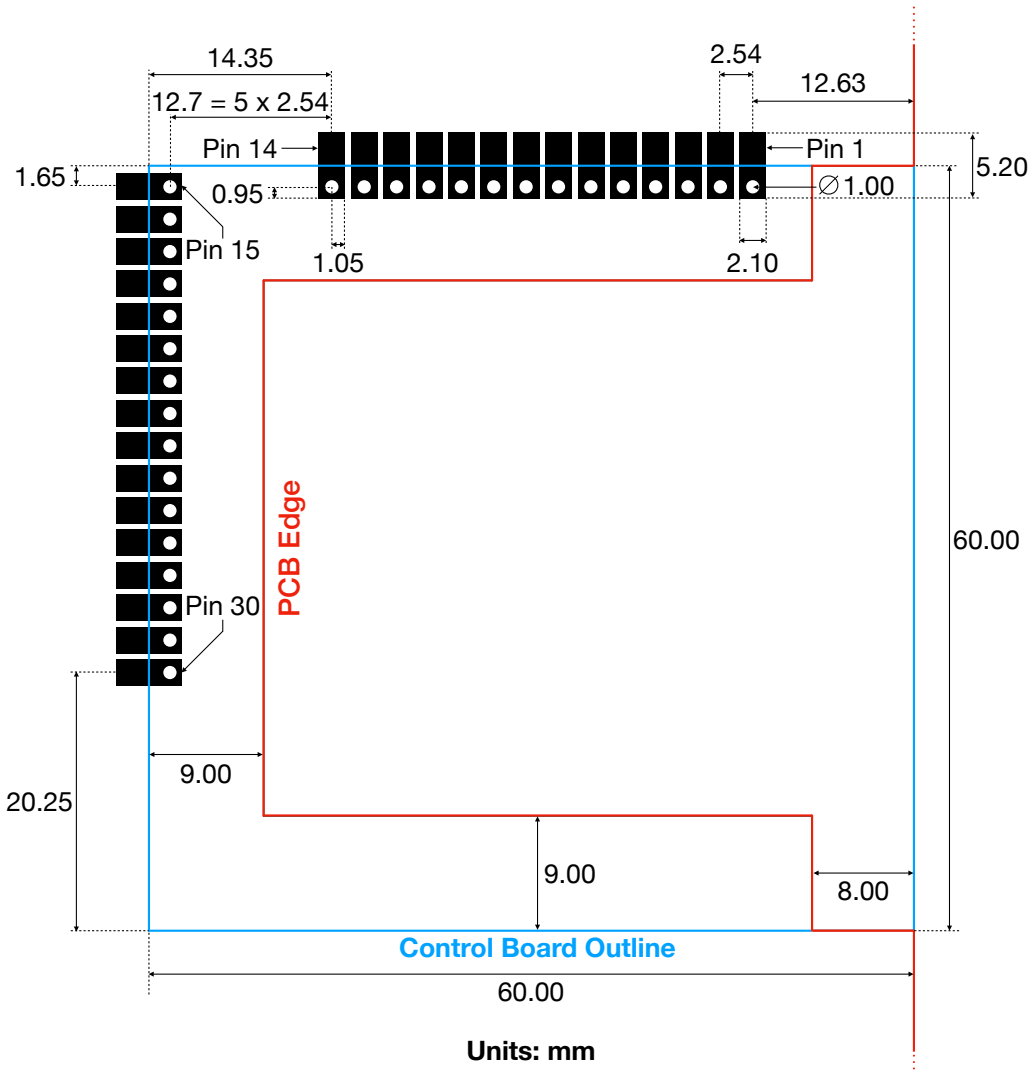


Figure 18: Recommended PCB Land Pattern for the Control Board. Drill Holes Are Optional.

A.3 Power Supply

The Control Board can be powered either by USB bus or by an external power supply, which are both protected by the TPS25921A protection IC (see Section 5.7).

- USB Bus Power: Power over USB can be used without modifications to the Control Board up to a current draw of 100 mA. If more current is needed, then one can reprogram the electrically erasable programmable read-only memory (EEPROM) of the FT232RL IC to support up to 500 mA. To do this, use the FT_Prog utility [16a] which allows you to reprogram the EEPROM using a USB connection.

  A USB connection cannot support currents that are larger than 500 mA. Thus if you need more current than 500 mA you must use an external power supply. This is the case when using the Control Board to control the DDS Board.

- External Power Supply: When using an external power supply, only use power supplies with a supply voltage of 5 V. Otherwise, damage to the board may occur. For an estimate on the current draw of the Control Board, refer to Table 19. Attention: Make sure to connect pin 1

to the positive terminal of the power supply (+5 V) and pin 2 to the negative terminal or GND. The Control Board does not have reverse-voltage protection and may be damaged if these pins are connected the wrong way around.

A.4 Software for the Control Board: MicroPython

Although the Control Board can be used with the standard firmware that is shipped with the ESP32, the Control Board was designed to run the MicroPython firmware. To install MicroPython on the ESP32, follow this guide: [GSC20]. Note that the ESP32-PICO-D4 does not have SPIRAM, meaning that the "GENERIC" MicroPython firmware has to be installed and not the "GENERIC-SPIRAM".

A.4.1 Enabling the Ethernet Port

Once MicroPython is installed, run a Python script like the one in Listing 1 to enable the Ethernet port of the Control Board. Running this script is necessary since the clock has to be disabled (GPIO32 is pulled low with a pull-down resistor) during boot-up of the ESP32. The clock input on GPIO0 is also a strapping pin of the ESP32 and has to be high during the booting sequence of the ESP32. The script in Listing 1 can be found in the digital appendix. After running the script with an Ethernet cable plugged in, the board should automatically receive an Internet Protocol (IP) address from the router using the Dynamic Host Configuration Protocol (DHCP) protocol.

```
import machine
import network
import time

#GPIO32 is the clock enable pin for the RMII Clock
clk_en = machine.Pin(32, machine.Pin.OUT)

#GPIO5 is the active low reset pin for the LAN8720A
lan8720_nRESET = machine.Pin(5, machine.Pin.OUT)

#Enable the clock, which is disabled by default
clk_en.value(1)

#Reset the LAN8720A so that it synchronizes to the newly enabled clock
lan8720_nRESET.value(0)
time.sleep(100e-6) #reset assertion time: 100us
lan8720_nRESET.value(1)

#Activate the RMII interface between the ESP32 and LAN8720A
lan = network.LAN(mdc = machine.Pin(23),
                  mdio = machine.Pin(18),
                  phy_type = network.PHY_LAN8720,
                  phy_addr = 0,
                  clock_mode = network.ETH_CLOCK_GPIO0_IN)
print(lan.active(1))
print(lan.ifconfig())
```

Listing 1: Python Script to Enable the Ethernet Capabilities of the Control Board.

A.5 General-Purpose Input/Output Expansion

The MCP23017 is an optional GPIO expansion IC that is enabled by default. It provides an additional 16 GPIO pins (pins 15 through 30), while using up 2 GPIO and 2 input pins of the ESP32. The MCP23017 on the Control Board has the I^2C hardware address 0x20.

A.5.1 Disabling the General-Purpose Input/Output Expansion

Should an application for the Control Board not need the additional GPIO pins, while needing more direct and possibly faster connections to the ESP32, then one can disable the GPIO expansion to regain the 2 GPIO (GPIO9, GPIO10) and 2 input pins (GPIO36, GPIO37) of the ESP32. To disable the GPIO expansion you need to desolder certain 0 Ω resistors on the Control Board:

- R15: To cut the power to the MCP23017, desolder the resistor R15. This can be sufficient in certain cases and you might not need to desolder any other resistors.
- R3, R4, R5, and R6: If the traces experience noise because of the still intact connections to the pins on the MCP23017 you can desolder the resistors R3 (GPIO10), R4 (GPIO9), R5 (GPIO36) and R6 (GPIO37) to completely disconnect the MCP23017 from all traces on the Control Board.

If the GPIO expansion is disabled, pins 15 through 30 will not work.

A.5.2 General-Purpose Input/Output Expansion Software

When using the Control Board with the MicroPython firmware (see Section A.4), there are two open-source libraries that simplify the use of the GPIO expansion with the MCP23017 IC. The libraries are "micropython-mcp23017" by Mike Causer [Cau19] and "micropython-mcp230xx" by ShrimpingIt [17b]. They both fulfill the same purpose and the choice of which one to use comes down to the preference of the developer.

A.6 Wi-Fi and Bluetooth Antenna

The ESP32 supports both Wi-Fi and Bluetooth natively and if one of those communication protocols is to be used, an antenna has to be installed on the Control Board. To install an antenna, solder an SMA connector onto footprint J3. Then, screw in an SMA Wi-Fi and Bluetooth antenna that has the right frequency range and an impedance of 50 Ω.

A.7 Jumpers

The Control Board features seven solder jumpers which are used to bring the ESP32 and the LAN8720A PHY IC into different modes during the boot phase. The solder jumpers have a default connection that is already made by the manufacturing process. To alter the state of the solder jumpers, one has to cut the existing copper connection and solder the pads together of the newly desired connection. The default connections are made for the standard operation of the Control Board and in general, will not have to be modified. The jumpers are arranged such that the upper side of the jumper connects to the high (1) voltage level of 3.3 V while the lower side of the jumper is connected to the low (0) voltage level of GND. The upper side of the Control Board is the side with the pins 1 through 14. Figure 16 shows the Control Board in its correct orientation.

- JP1: ESP32 Strapping Pin on GPIO0. If it is high (default) during boot, the ESP32 goes into SPI boot mode. If it is low during boot ESP32 goes into download boot mode. See [19b] for more details.
- JP2: ESP32 Strapping Pin on GPIO5. This controls the timing of the Secure Digital Input Output (SDIO) slave protocol of the ESP32. See [19b] for more details. The default value is high, which is also useful since this pin is used as the $\overline{\text{RESET}}$ signal for the PHY and GPIO expansion IC.
- JP3: ESP32 Strapping Pin on GPIO15 (also called MTDO). This also controls the timing of the SDIO slave protocol of the ESP32. It has the second function of controlling the debug output over UART (and thus USB). If it is high (default) during boot it enables debug messages over U0TXD (GPIO1) during booting. If it is low during boot, it disabled debug messages over U0TXD (GPIO1) during booting.
- JP4, JP5, and JP6: Mode strapping pins of the LAN8720A PHY IC. They steer the capabilities of the LAN8720A chip. See [16b] for more details. By default (all three jumpers high) all capabilities and auto-negotiation are enabled. The jumpers correspond to JP4 (Mode 0), JP5 (Mode 1), and JP6 (Mode 2).
- JP7: PHY Address 0 Configuration Strap of LAN8720A PHY IC. This pin is used to give the PHY a unique address should there be more than one PHY in a design. See [16b] for more details. This pin has the default value low.

B Seadragon Direct Digital Synthesis Board Documentation

The DDS Board, named Seadragon, is a device that provides DDS on 4 phase-locked channels. For a complete list of all the specifications, see Section 4.13. This documentation is aimed at readers who want to use the DDS board in their lab, who want to write software, or who would like to build an enclosure or heat sink for the device.

B.1 Soldering the AD9959 IC

The LFCSP-56 package of the AD9959 has an exposed pad underneath that needs to be soldered onto the GND pad on the DDS Board. To help with this process, an exposed area of copper with thermal reliefs has been created on the copper layer on the back. This exposed area can be heated with a soldering iron which should transfer the heat through the vias onto the top layer.

B.2 Reference Clock Input/Output

The DDS Board needs an external 10 MHz clock to be supplied on the SMA connector J2. This clock is multiplied on the board using the 2.5x multiplier giving a 25 MHz clock. It is multiplied again in the AD9959 by a factor of 20 resulting in the final 500 MHz clock.

The DDS Board also has a reference clock output on the SMA connector J3, that can be used to daisy chain multiple clock dependent devices together. Should the clock output not be used, then one should terminate the SMA connector J3 using a terminator with 50 Ω impedance and the appropriate power handling capability.

B.3 Power Supply

The DDS Board requires the use of an external power supply with a supply voltage of 5 V and has a typical current draw of 0.75 A with a maximum expected draw of 1.2 A (see Table 16). Do not power the DDS Board with any other voltage or damage to the board may occur. The power supply needs to be connected to the pin headers of the footprint J1. Attention: Make sure to connect pin 1 of J1 to the positive terminal of the power supply (+5 V) and pin 2 of J1 to the negative terminal or GND. The DDS Board does not have reverse-voltage protection and may be damaged if these pins are connected the wrong way around.

Attention: Do not power the board unless the output channels (J5, J6, J7, J8) are properly terminated. The termination needs to have an impedance of 50 Ω and have a power handling capability of 0.1 W = 20 dBm or more. Otherwise, damage to the board may occur.

B.4 Software for the DDS Board

While different firmware for the ESP32 might work to control the DDS Board, the DDS board is designed to be controlled by a Control Board running the MicroPython firmware (see Section A.4). The use of MicroPython allows us to reuse and adapt the code written for the DDS setup that the DDS Board is replacing since it is written in Python. Even though, MicroPython has support for many of the standard Python libraries, there might be some adjustments that have to be made to make the current software compatible with the DDS Board.

B.4.1 Output Power Calculation

In the current implementation of the DDS device, the user enters a value between 0% and 100% to scale the amplitude for the output signal. This leads to unpredictable output powers since the output power scales differently for different frequencies for various reasons. An improvement to this system could be that the user enters the desired amplitude in dBm and the frequency of the signal and the software on the Control Board calculates the value between 0 and 1 for the Amplitude Control Register (ACR) of the AD9959.

The calculations are the same as in Table 14:

1. Calculate the output power of the AD9959 with the ADTT1.5-1+ transformer using Equation 20.

2. Use Equation 7 to subtract the amount of loss that stems from the DAC's stepping behavior.

3. Subtract the transformer insertion loss using the ADTT1.5-1+ datasheet [20b]. Use linear interpolation (or any other interpolation method) if a value for a frequency is missing.

4. Subtract the reconstruction filter insertion loss using the RLP-216+ datasheet [20g]. Use linear interpolation (or any other interpolation method) if a value for a frequency is missing.

5. Add the amplifier gain using the PHA-13LN+ datasheet [17c]. Use linear interpolation (or any other interpolation method) if a value for a frequency is missing.

6. If the standard output is used, then these are all the calculations needed and the result is the maximum output power that the DDS Board can deliver at this frequency. This can now be scaled using the ACR of the AD9959 to a lower value that the user desires. If the frequency doubler is to be used (see Section B.5), we need to perform the calculations 7 through 9.

7. Subtract the attenuation using the LAT-3+ datasheet [20d]. Use linear interpolation (or any other interpolation method) if a value for a frequency is missing.

8. Subtract the frequency multiplier conversion loss using the datasheet SYK-2R+ [16c]. Use linear interpolation (or any other interpolation method) if a value for a frequency is missing.

9. Subtract the LPF insertion loss using the LFCN-225+ [19c]. Use linear interpolation (or any other interpolation method) if a value for a frequency is missing.

10. The result of the calculations delivers the maximum output power that the DDS Board can deliver at this frequency when using the frequency doubler. This can now be scaled using the ACR of the AD9959 to a lower value that the user desires.

With these calculations, the software could also provide a function with which a user can ask for the power output range at a certain frequency. Also, checks can be used to make sure that only valid values are entered for the output power.

Note that the values obtained through the above calculations might be off from the measured signal power (for example due to loss/reflections in the traces on the PCB). One can add a last stage to the software calculations in which these offsets are corrected to match the measured output signal power.

B.4.2 Trapped Ion Quantum Information Remote Procedure Call

TIQI RPC is the default network communication protocol in the TIQI Group. It is based on msgpack-rpc [17a]. TIQI RPC already has an implementation in Python that can likely be adopted to work in the MicroPython environment on the Control Board. Using TIQI RPC as the communication protocol of the Control Board (and thus the DDS Board) facilitates the communication of the Control Board with the rest of the lab equipment.

B.5 Enabling the Frequency Doubled Output

In the default configuration of the DDS Board, the standard output is enabled while the frequency-doubled output is disabled. The configuration is based on $0\,\Omega$ resistors that can be desoldered and soldered to adjust which output should be used:

- Channel 0: To enable the frequency-doubled output and disable the standard output, desolder the resistors R5 and R9 and solder them onto the empty footprints R1 and R13.
- Channel 1: To enable the frequency-doubled output and disable the standard output, desolder the resistors R6 and R10 and solder them onto the empty footprints R2 and R14.
- Channel 2: To enable the frequency-doubled output and disable the standard output, desolder the resistors R7 and R11 and solder them onto the empty footprints R3 and R15.
- Channel 3: To enable the frequency-doubled output and disable the standard output, desolder the resistors R8 and R12 and solder them onto the empty footprints R4 and R16.

B.6 Dimensions and Mounting Capabilities

Figure 19 shows the dimensions of the fully assembled DDS board. The schematic is intended to be used as a guideline for readers who want to build an enclosure or a heat sink for the DDS Board. There are six M3 mounting holes to facilitate the mounting of a heat sink or the securing of the DDS Board in a box. The DDS Board has been designed with 2 mm part clearance on the side, where no surface-mount devices (SMDs) are placed, so that it can slide into a Eurocard housing. The DDS Board has a standard Eurocard format of 100x160 mm.

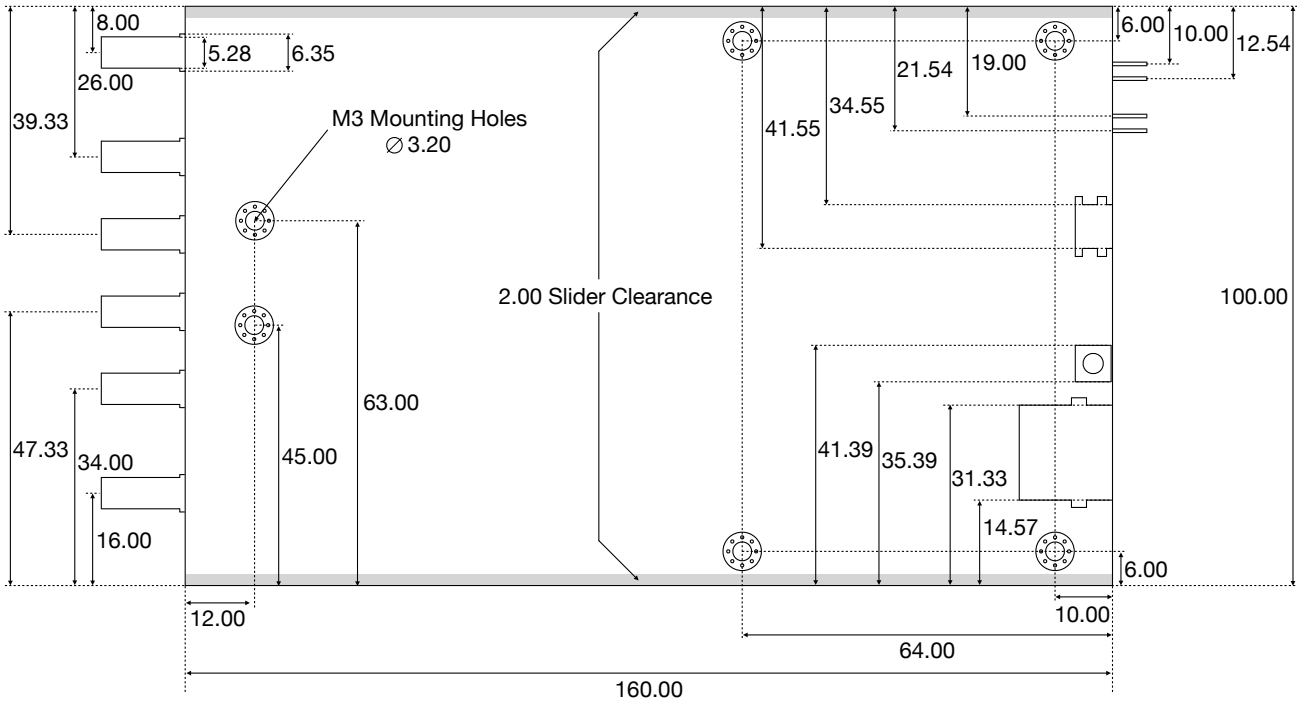


Figure 19: Dimensions of the Fully Assembled DDS Board (Including the Control Board).

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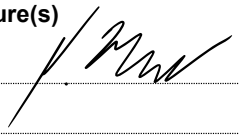
Richterswil, 21.11.2020	

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