Eidgenössische Technische Hochschule Zürich
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PCB design of an opamp circuit in a laser frequency stabilization feedback loop based on the Pound-Drever-Hall locking technique

Semester Project

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A big thank you to all members of HyQu. Thanks to all of you the working environment at the lab is very pleasant and I enjoyed every moment I was there. Additionally I learned a lot about the field of transduction and superconducting qubits during lunch, Journal Club and Group Meeting.

A special acknowledgement goes to Markus Strässle of the electronics workshop, who happily shared his many years of experience in the field of electrical circuits and PCBs with me.

Last but not least, I want to explicitly thank my friends and family, who support me 24/7 and make me enjoy my stay in Zürich.

Abstract

The goal of this project is to make a PCB which maps DC to high KHz frequency signals in the range [-1V,+1V] inverted, amplified and shifted to the range [0V,+6V] and [0V,+8V] with minimal additional phase delay. After designing the electrical circuit and PCB all the components are soldered on the board such that it can be characterized. Ultimately the board is used in a PDH lock, which is a feedback system for stabilizing the frequency of a laser. Additionally, two more circuits and PCBs for introducing a voltage offset and interfacing a switch were designed.

Contents

Chapter 1

Laser frequency stabilization with the Pound-Drever-Hall locking technique

A perfect laser emits light only at one specific frequency. The emission spectrum of such a perfect laser is thus given by one Dirac-delta peak. However in reality this is never the case and the peak in the emission spectrum of a physical laser will always have a finite linewidth. The smaller the linewidth, the more stable we call the laser. The frequency of the emitted laser light will fluctuate on different timescales. Fluctuations over short timescales ($\sim$ 1µs-100ms) are called noise and can be caused by e.g. vibrations and laser diode current noise. Fluctuations over long timescales (>1s) on the other hand are called drifts. These can be caused by imperfections in temperature control or changes in environmental factors like air pressure and humidity.

Experiments might require a more stable laser than the ones available in the lab or on the market. Laser frequency stabilization is the field of research that deals with improving the linewidth of a given laser and thus correcting for these frequency fluctuations, usually through the means of feedback. One of the frequently applied frequency stabilization techniques is the Pound-Drever-Hall lock (PDH lock) [1]. The term "lock" is used because another device (e.g. a more stable optical cavity) is used as a reference. The goal of the PDH lock is then to transfer the stability of this reference cavity to the laser by correcting its frequency fluctuations [2]. Note that the opposite is also possible: an optical cavity that is being locked to a laser, as mentioned in section 1.7. Another reason for using a lock can be the need for a laser to always be on resonance with a cavity (or vice versa), without necessarily decreasing its linewidth. The latter will be the purpose in our case as explained in the next paragraph.

At the Hybrid Quantum Systems group the laser and PDH lock will be used in the microwave-to-optical transduction experiment, where quantum information in a superconducting qubit is coupled to standing modes in an optical cavity through a high-overtone bulk acoustic wave resonator (HBAR). For this the coupling laser should always be on resonance with the optical cavity, which is the reason for using the PDH lock. The schematical setup of this experiment is shown in figure 1.1

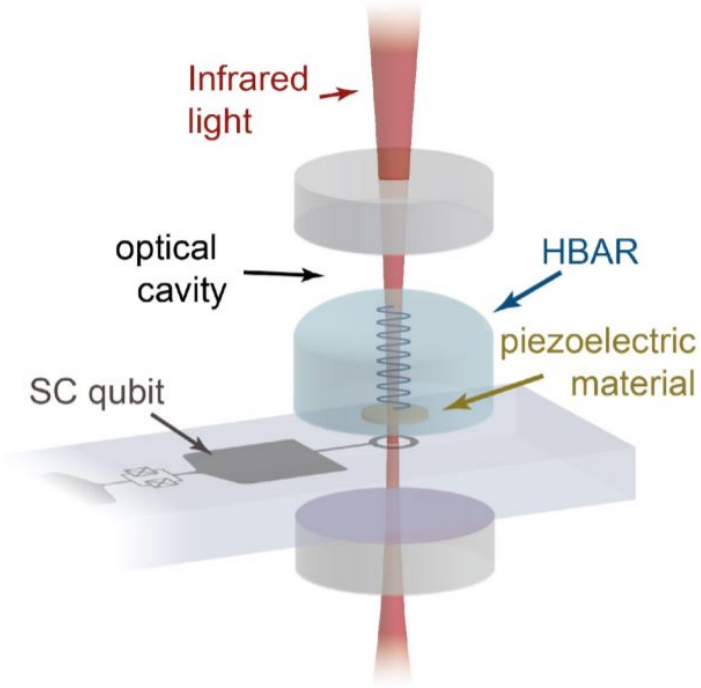

Figure 1.1: Schematical microwave-to-optical transduction experiment setup

1.1 Fabry-Pérot cavity

In the PDH-lock the laser is locked to a Fabry-Pérot cavity. Such a cavity consists of two parallel reflective mirrors as can be seen in figure 1.2. The incident light shines onto the first mirror and can either be reflected with E-field reflection coefficient r_1' or enter the cavity with E-field transmission coefficient t_1. The transmitted light then traverses the cavity and when it encounters the second mirror it is either reflected or transmitted with coefficients r_2 and t_2 respectively. If it is reflected it traverses back to the first mirror where it is reflected or transmitted with coefficients r_1 and t_1' respectively. The photons can keep going back and forth in the cavity following the procedure of these last two steps until it leaves the cavity at one of both sides. The working principle of a Fabry-Pérot cavity is based on multi-beam interference. Only when the frequency of the incident light is close to one of the cavity resonaces, a notable optical power of circulating light inside the cavity can be realized. On resonance the incident field and the leakage beam out of the cavity destructively interfere. In the critically coupled case (i.e. when both mirrors are lossless and have the same reflectivity) these cancel eachother out completely. In the meantime the incident light leaking into the cavity and the circulating light inside the cavity are interfering constructively. The further off resonance, the more light is directly reflected at the first mirror. At anti-resonance the field is completely reflected because the weak field leaking out of the cavity is interfering constructively with the promptly reflected beam. [3]

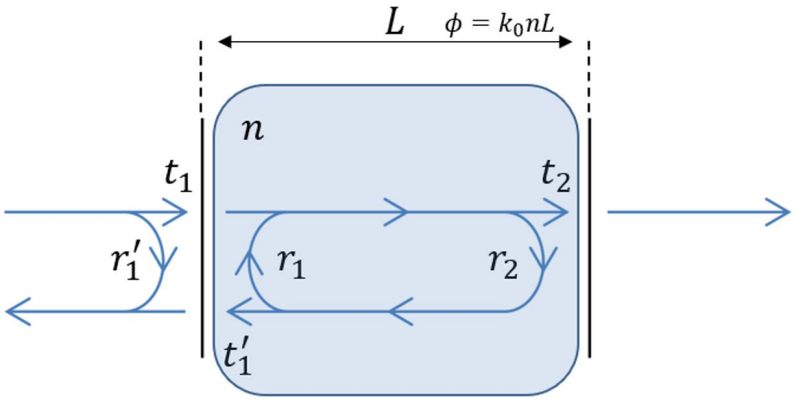

Figure 1.2: Fabry-Pérot cavity scheme

Based on the scheme that was just established for the different possible paths the photons can take, the power transmittance T for the complete cavity can be calculated as following, with ϕ being the phase accumulated through half a roundtrip in the cavity ($\phi = k_0 nL$):

$$
\begin{aligned}
T &= |t|^2 \\
&= |t_1 t_2 e^{j\phi} + t_1 r_2 r_1 t_2 e^{j3\phi} + t_1 r_2 r_1 r_2 r_1 t_2 e^{j5\phi} + \dots|^2 \\
&= \left| t_1 t_2 e^{j\phi} \sum_{k=0}^{\infty} [r_1 r_2 e^{j2\phi}]^k \right|^2 \\
&= \left| \frac{t_1 t_2 e^{j\phi}}{1 - r_1 r_2 e^{j2\phi}} \right|^2 \\
&= \frac{\left(\frac{|t_1 t_2|}{1 - r_1 r_2}\right)^2}{1 + \frac{4 r_1 r_2}{(1 - r_1 r_2)^2} \sin^2\phi} \\
&= \frac{T_{max}}{1 + F \sin^2\phi}
\end{aligned}
\tag{1.1}
$$

The maximal power transmittance T_{max} depends on the mirrors and is maximized under the following conditions for the cavity:

$$
T_{max} = 1 \Leftrightarrow \begin{cases} r_1 = r_2 & \text{symmetrical.} \\ t_1^2 t_2^2 = (1 - r_1^2)(1 - r_2^2) & \text{lossless mirrors.} \end{cases}
\tag{1.2}
$$

Under these conditions, since we have lossless mirrors, The corresponding power reflectivity R is then given by $R = 1 - T$. Experimentally this is only true to a very good approximation. The resulting power reflectivity spectrum is plotted in figure 1.3.

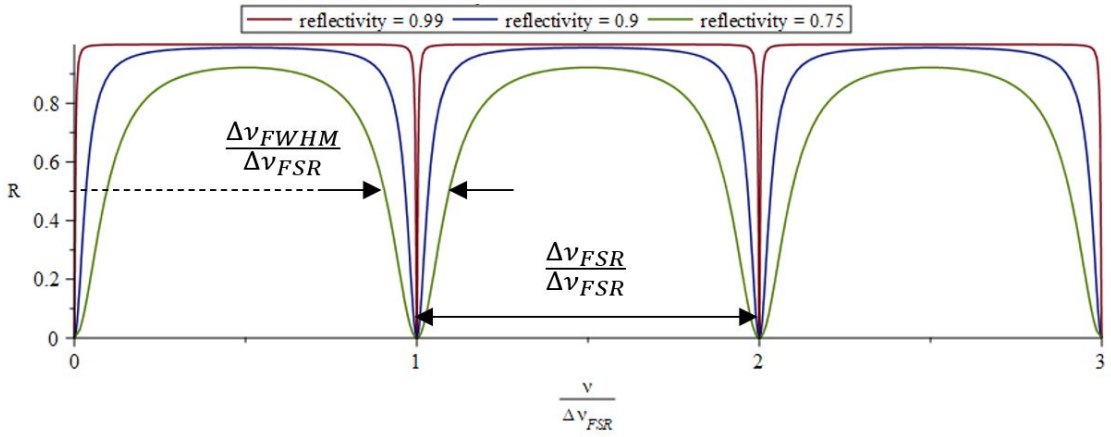

Figure 1.3: Power reflectivity R for a Fabry-Pérot cavity with symmetrical, lossless mirrors in three cases with different E-field reflection coefficients

For a given cavity, maximizing the power transmittance (or equivalently minimizing the power reflectivity) gives a peak condition on the frequency of the incident light:

$$T = T_{max} \Leftrightarrow \sin\phi = 0 \Leftrightarrow \nu = m\frac{c}{2L} = m\Delta\nu_{FSR} \tag{1.3}$$

The peaks in the reflectivity spectrum (called resonances) given in figure 1.3 are thus equally spaced. The difference in frequence between two consecutive peaks is called the free spectral range $\Delta\nu_{FSR}$ of the cavity. From the formula $\Delta\nu_{FSR} = \frac{c}{2L}$ we see that it is equal to the inverse of the roundtrip time of the cavity (i.e. the time light needs to make one roundtrip in the cavity).

Another important cavity parameter that is also marked in figure 1.3 is the cavity linewidth $\Delta\nu_{FWHM}$ where FWHM stands for Full Width at Half Maximum. The cavity linewidth is equal to the inverse of the photon decay time (i.e. the average time for a photon to decay out of the cavity due to the non-perfectly reflecting mirrors), which in the case of lossless mirrors is given by $t_{photondecay} = -\frac{t_{roundtrip}}{\ln(|r_1|^2|r_2|^2)}$.

Ultimately, combining these two parameters results in the cavity Finesse $\mathcal{F}$, which is a good measure for the quality of a cavity. From its definition the Finesse can be interpreted as the average amount of times a photon goes back and forth inside the cavity before decaying through one of the non-perfectly reflecting mirrors.

$$\mathcal{F} = \frac{\Delta\nu_{FSR}}{\Delta\nu_{FWHM}} = -\frac{2\pi}{\ln(|r_1|^2|r_2|^2)} \tag{1.4}$$

In an experiment the quality factor typically is then defined as $Q = \frac{\nu}{\Delta\nu_{FWHM}} = \frac{\nu}{\Delta\nu_{FSR}}\mathcal{F}$

In the derivation of the PDH error signal we will also make use of the reflection coefficient for the cavity defined as the reflected electric field over the incident electric field. The following case is being considered: $r_1 = r_2 = r$, $t_1' = t_2 = t, t_1 = t', r_1' = r', \phi = k_0 nL = \frac{\omega L}{c} = \frac{\omega}{2\Delta\nu_{FSR}}$.

$$\begin{aligned} F(\omega) &= \frac{E_{ref}}{E_{inc}} \\ &= r' + t'rte^{i2\phi} \sum_{k=0}^{\infty} [r^2 e^{i2\phi}]^2 \\ &= r' + \frac{t'rte^{i2\phi}}{1 - r^2 e^{i2\phi}} \\ &= -r + \frac{r(1-r^2)e^{i2\phi}}{1 - r^2 e^{i2\phi}} \\ &= r\frac{e^{i2\phi} - 1}{1 - r^2 e^{i2\phi}} \\ &= r\frac{e^{i\frac{\omega}{\Delta\nu_{FSR}}} - 1}{1 - r^2 e^{i\frac{\omega}{\Delta\nu_{FSR}}}} \end{aligned} \tag{1.5}$$

Where we used Stokes' relations for r, t, r', t': $r' = -r$ and $tt' = 1 - r^2$.

In the Fabry-Pérot cavity discussed so far, the setup consisted of two parallel plane mirrors. These plane mirrors have to be alligned very well in order to keep the light confined. That is why typically used cavities are made of one or two mirrors that have some curvature, specified by the radius of curvature R_1 and R_2. The following stability criterium can be derived for a cavity [4]:

$$0 \leq \left(1 - \frac{L}{nR_1}\right)\left(1 - \frac{L}{nR_2}\right) \leq 1 \tag{1.6}$$

The quantity $1 - \frac{L}{nR_i}$ is called the stability parameter g_i.

1.2 Phase modulation

1.2.1 The need for phase modulation

Zooming in on the power reflectivity spectrum (figure 1.3) at the area around one of the peaks results in figure 1.4. One might consider to use the reflectivity (or equivalently the power of the transmitted light, so the transmittance) for frequency stabilization around resonance. However there are two problems with this approach. The biggest problem is that the reflectivity is symmetric around resonance. By measuring the reflectivity (or equivalently the transmittance) it is not possible to tell at which side of resonance the incoming laser light is and thus it is impossible to know which way the frequency should be corrected. The second problem is the minimum of the reflectivity at resonance, meaning that there is no first order frequency dependence in the reflectivity at resonance.

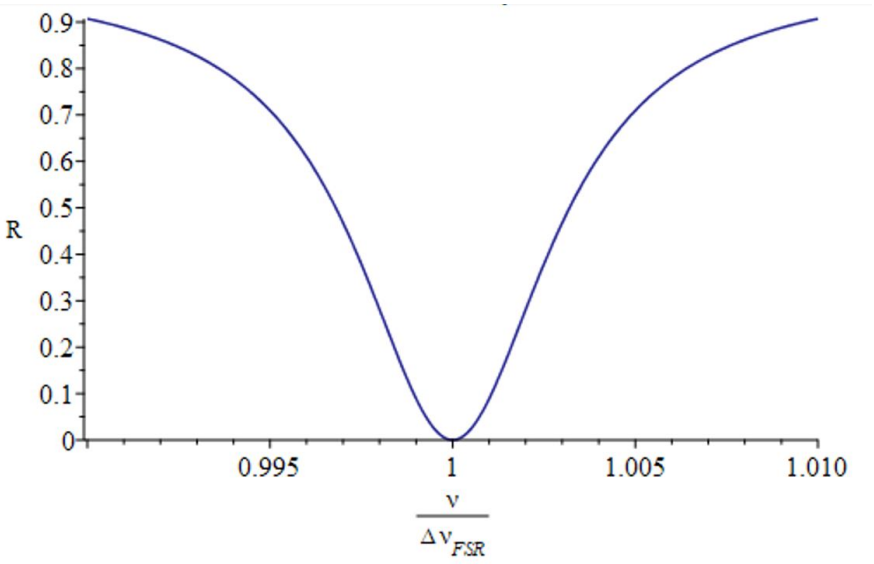

Figure 1.4: Power reflectivity R of a Fabry-Pérot cavity around one of the minimal reflectivity peaks

The next idea one might have, is still to look at the reflectivity but now make use of the fact that the derivative of the reflectivity is antisymmetric around resonance. By varying the frequency a little bit it is known at which side of resonance the frequency is. However there is one problem that remains. With this method it is impossible to distinguish between spectral noise and intensity noise of the laser. The reason for this is that a change in the reflected power can be caused by two different processes. On the one hand if the intensity of the laser light fluctuates, the total power and thus also the reflected power will fluctuate. On the other hand if the frequency of the emitted laser light fluctuates, the reflected power will also fluctuate according to the curve in figure 1.4.

Another approach would be to use the reflection coefficient $F(\omega)$ instead of the power reflectivity, since the phase of the reflection coefficient is already antisymmetric (as shown in figure 1.5). However also with this approach there are some issues. The first issue being the discontinuous phase around resonance (jump of 180 degrees). The second issue is the fact that it is very difficult or even impossible to measure the phase directly, which is the main reason why this approach is not used.

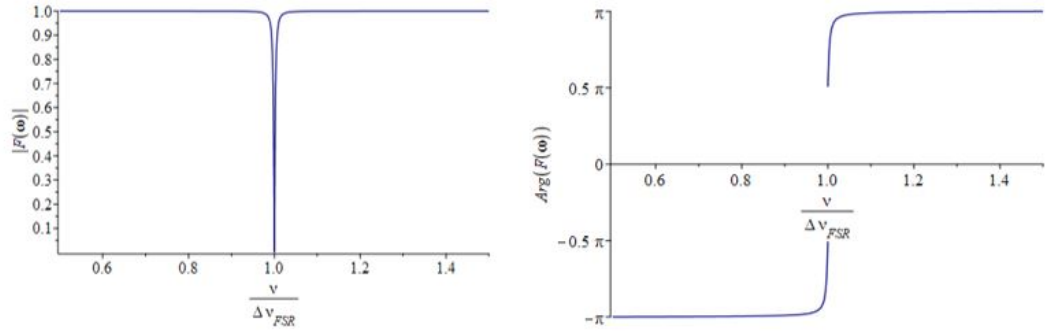

Figure 1.5: Reflection coefficient $F(\omega)$

The trick of the PDH-lock is based on the second approach, but instead of varying the frequency a little bit, optical sidebands will be introduced in the spectrum of the emitted light by sending the emitted photons through an electro-optic modulator. In this report the Pockels effect is used to accomplish phase modulation of the emitted laser beam. To see that this approach results in an error signal which is not affected by laser intensity fluctuations up to first order, a mathematical expression of the error signal needs to be introduced. The decoupling of the intensity and frequency noise is further discussed in section 1.6. Another approach would be to directly modulate the frequency. [2]

1.2.2 Pockels effect

The Pockels effect is based on the non-linearity in the true nature of optics. In general the relation between the polarizability and the electric field is not linear but given by:

$$\mathbf{P}(t) = \epsilon_0(\chi^{(1)}\mathbf{E}(t) + \chi^{(2)}\mathbf{E}^2(t) + \chi^{(3)}\mathbf{E}^3(t) + \ldots) \tag{1.7}$$

Specifically the quadratic susceptibility $\chi^{(2)}$ is important in the Pockels effect. For most materials this $\chi^{(2)}$ is too small to be useful in experiments, but one material which exhibits strong quadratic susceptibility is Lithium Niobate ($LiNbO_3$), with reported values for the most useful tensor element of $\chi^{(2)}_{zzz} = -20.6 \pm 2.1 \frac{\text{pm}}{\text{V}}$ [5].

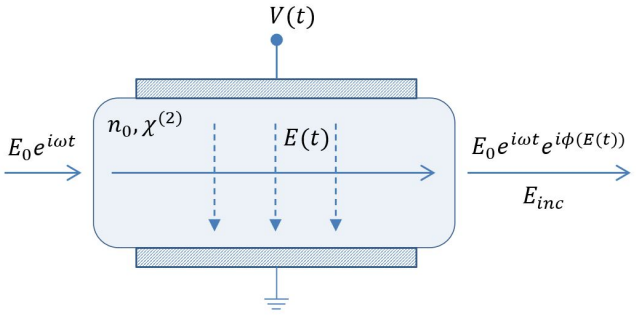

Figure 1.6: Pockels effect

The linear effect that the electric field has on the refractive index because of the quadratic susceptibility, is called the Pockels effect. Consider the setup demonstrated in figure 1.6. A voltage difference is applied over two electrodes enclosing a material exhibiting strong quadratic susceptibility (with standard refractive index n_0). This induces an electric field through that medium, which will influence the refractive index in a linear way, expressed by the formula for the Pockels effect [6], where $r_{ijk} = -\frac{2\chi^{(2)}_{ijk}}{n_i^4}$:

$$n(E) = n_0 - \frac{1}{2} r n_0^3 E \tag{1.8}$$

Note that all electric fields are considered to lie along the same direction, such that only one tensor element r_{ijk} is influencing the refractive index. To simplify the notation this tensor element is replaced by r. When light now traverses through this medium, it will accumulate a phase which depends on the electric field between the electrodes:

$$\phi(E) = \phi_0 - k\frac{1}{2} r n_0^3 E L \tag{1.9}$$

For an incident field $E_0 e^{i\omega t}$ the electric field after passing through the medium is thus given by $E_0 e^{i\omega t} e^{i\phi(E(t))}$. Now consider a parallel plate capacitor such that the applied voltage and the electric field are related in the following way: $V(t) = E(t)d$. When a sinusoidal drive voltage $V(t) = V_0 \sin\Omega t$ is used, the resulting electric field of the light passing through the medium is given by the following expression:

$$E_{inc} = E_0 e^{i\omega t} e^{i\phi_0} e^{-i\frac{1}{2} r n_0^3 L \frac{V_0}{d} \sin\Omega t} = \tilde{E}_0 e^{i(\omega t + \beta \sin\Omega t)} \tag{1.10}$$

Note that the name incident electric field E_{inc} is used because in the next section it is this field that will be sent in to a Fabry-Pérot cavity. In the following the tilde (introduced by absorbing the $e^{i\phi_0}$ into E_0) will be dropped. The parameter $\beta = -\frac{1}{2} r n_0^3 L \frac{V_0}{d}$ is introduced out of convenience.

By using a Jacobi-Anger expansion [7] it can be seen how this phase modulation effectively creates sidebands.

$$\begin{aligned} E_{inc} &= E_0 e^{i(\omega t + \beta \sin\Omega t)} \\ &= E_0 e^{i\omega t} \sum_{k=-\infty}^{+\infty} J_k(\beta) e^{ik\Omega t} \\ &\approx E_0 \left[J_0(\beta) e^{i\omega t} + J_1(\beta) e^{i(\omega+\Omega)t} - J_1(\beta) e^{i(\omega-\Omega)t} \right] \end{aligned} \tag{1.11}$$

In this expression J_k represents the Bessel J function of order k. To get an intuition why this approximation is valid the relative power in the carrier and first order sidebands is plotted in figure 1.7. From the red line it can be seen that the approximation is valid if β doesn't become too large. Later it will become clear that the optimal results are obtained for $\beta = 1.08$ (marked with the vertical orange dashed line), for which the approximation still holds, as can be seen from the figure.

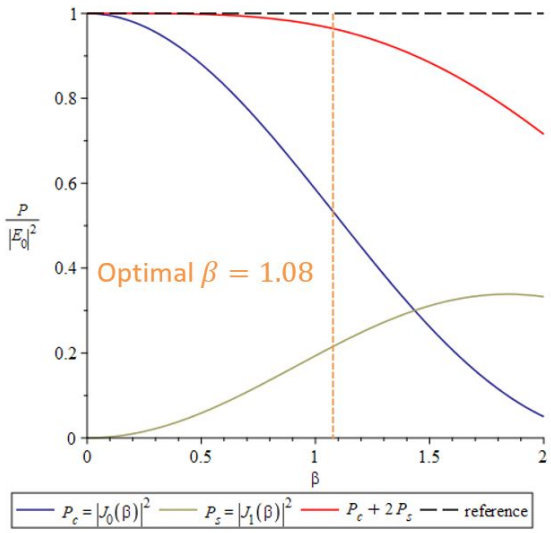

Figure 1.7: Relative power in carrier and first order sidebands

1.3 PDH error signal

The goal of this section is to combine the Fabry-Pérot cavity and the phase modulation from the previous two sections to end up with a signal that is antisymmetric and linearly depending on the emitted frequency. This signal will then be called the PDH error signal. The derivation of this error signal is following the approach of "An introduction to Pound-Drever-Hall laser frequency stabilization" by Eric Black [2].

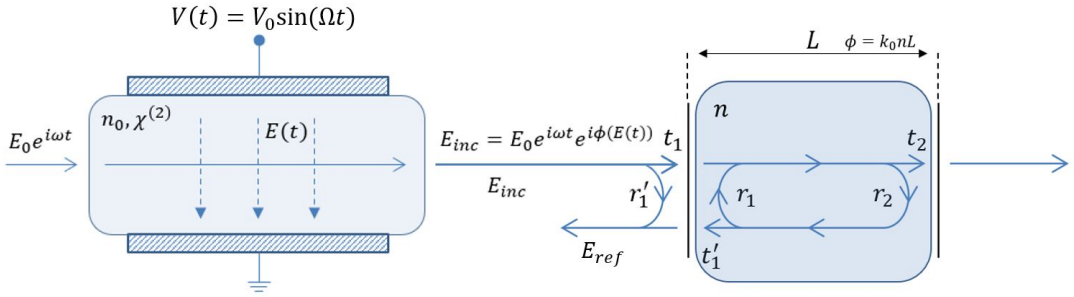

Figure 1.8: Combined setup of the electro-optic modulator and the Fabry-Perot cavity

The combined setup is shown in figure 1.8. When the phase modulated laser beam (which can be approximated by the carrier and two first-order sidebands as given in equation 1.11) is incident on the cavity, the reflected beam can easily be calculated using the expression for the reflection coefficient in equation 1.5:

$$E_{ref} \approx E_0 \left[F(\omega) J_0(\beta) e^{i\omega t} + F(\omega+\Omega) J_1(\beta) e^{i(\omega+\Omega)t} - F(\omega-\Omega) J_1(\beta) e^{i(\omega-\Omega)t} \right] \quad (1.12)$$

As mentioned in the previous section it is not straightforward to measure the electric field directly, but measuring the intensity or power is easy, using a photodetector. The power of the reflected electric field P_{ref} is given by the following expression:

$$\begin{aligned} P_{ref} = |E_{ref}|^2 = {} & P_c |F(\omega)|^2 + P_s [|F(\omega+\Omega)|^2 + |F(\omega-\Omega)|^2] \\ & + 2\sqrt{P_c P_s} \Re\mathrm{e}[F(\omega) F^*(\omega+\Omega) - F^*(\omega) F(\omega-\Omega)] \cos\Omega t \\ & + 2\sqrt{P_c P_s} \Im\mathrm{m}[F(\omega) F^*(\omega+\Omega) - F^*(\omega) F(\omega-\Omega)] \sin\Omega t \\ & + (2\Omega \text{ terms}) \end{aligned} \quad (1.13)$$

In this expression $P_c = |E_0 J_0(\beta)|^2$ and $P_s = |E_0 J_1(\beta)|^2$ represent the power of the beam present in the carrier and one of the sidebands respectively. The terms oscillating at frequency Ω are a result of the interference between the carrier and one of the sidebands,

while the terms oscillating at frequency 2Ω are a result of the interference between the two different sidebands.

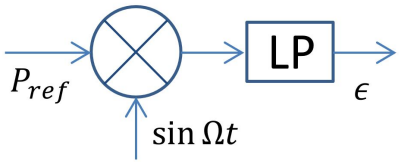

Figure 1.9: Scheme of sending P_{ref} through a frequency mixer and Low Pass filter

To isolate the term on the third line in equation 1.13, the power of the reflected beam is mixed with the sinusoidal voltage signal used to drive the electro optic modulator. The ouput of the mixer is then sent through a Low Pass filter in order to isolate only the non-oscillating terms. This sequence is schematically shown in figure 1.9. Based on Simpson's formulas for multiplying sines and cosines, the resulting signal, called the error signal ϵ, is given by the following expression:

$$\epsilon = 2\sqrt{P_c P_s}\Im\mathrm{m}[F(\omega)F^*(\omega+\Omega) - F^*(\omega)F(\omega-\Omega)] \tag{1.14}$$

This resulting error signal is plotted in figure 1.10

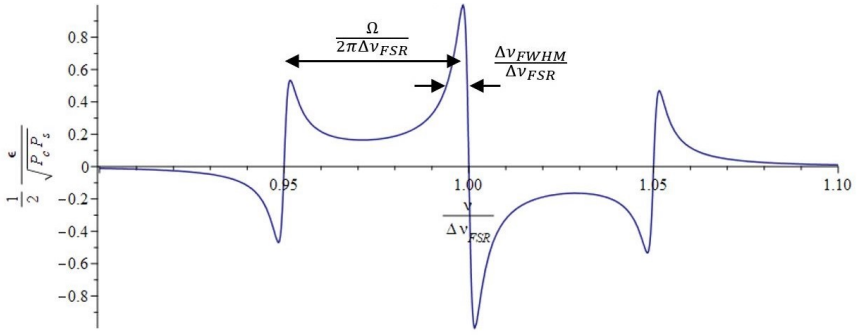

Figure 1.10: PDH error signal

To simplify this expression further, the fast modulation regime is considered. To operate in this regime the modulation frequency Ω needs to be large with respect to the the Fabry-Pérot cavity linewidth $\Delta\nu_{FWHM}$ and the carrier frequency needs to be close to resonance. In that case the sidebands can be assumed to be off-resonant and thus $F(\omega \pm \Omega) \approx -1$. Using this in the expression for the error signal results in the following:

$$\epsilon \approx -4\sqrt{P_c P_s}\Im\mathrm{m}[F(\omega)] \tag{1.15}$$

Around resonance the error signal can be simplified even more. The frequency can then be written as $\nu = N\Delta\nu_{FSR}+\Delta\nu$ with $\Delta\nu \ll \Delta\nu_{FWHM}$. Assuming to have a high Finesse cavity, the Finesse can be approximated by $\mathcal{F} = -\frac{2\pi}{\ln(r^4)} \approx \frac{\pi r}{1-r^2}$. This approximation is valid because for both expressions the Laurent series around $x = 1$ is given by $\frac{1}{x-1} + \frac{1}{2} + \mathcal{O}(x-1)$. Note that this is a plausible assumption, since this is also desirable for a nice cavity to lock a laser to. Together this results in the following simplified expression for the reflection coefficient (given in equation 1.5) close to resonance:

$$\begin{aligned} F(2\pi(N\Delta\nu_{FSR} + \Delta\nu)) &= r\frac{e^{i\frac{2\pi(N\Delta\nu_{FSR}+\Delta\nu)}{\Delta\nu_{FSR}}} - 1}{1 - r^2 e^{i\frac{2\pi(N\Delta\nu_{FSR}+\Delta\nu)}{\Delta\nu_{FSR}}}} \\ &= r\frac{e^{i\frac{2\pi\Delta\nu}{\Delta\nu_{FSR}}} - 1}{1 - r^2 e^{i\frac{2\pi\Delta\nu}{\Delta\nu_{FSR}}}} \\ &\approx r\frac{1 + i\frac{2\pi\Delta\nu}{\Delta\nu_{FSR}} - 1}{1 - r^2} \\ &= i\frac{r}{1-r^2}\frac{2\pi\Delta\nu}{\mathcal{F}\Delta\nu_{FWHM}} \\ &\approx i\frac{2}{\Delta\nu_{FWHM}}\Delta\nu \end{aligned} \tag{1.16}$$

Using this result the PDH error signal in the fast modulation regime near resonance can be approximated by:

$$\epsilon \approx D\Delta\nu = -\frac{8\sqrt{P_c P_s}}{\Delta\nu_{FWHM}}\Delta\nu \tag{1.17}$$

From this expression it is clear that near resonance the error signal linearly depends on the frequency fluctuation. The scaling factor is the frequency discriminant D. From its expression it can be seen that the more stable the cavity (i.e. the smaller the cavity linewidth), the larger the frequency discriminant and thus the steeper the error signal around resonance. Hence a small change in frequency will induce a bigger difference in error signal. As a consequence of the larger frequency discriminant the cavity becomes also more difficult to lock to, since the frequency range for which the error signal is useful shrinks as well. As a check for this formula the linear approximation near resonance and the error signal are plotted together in figure 1.11.

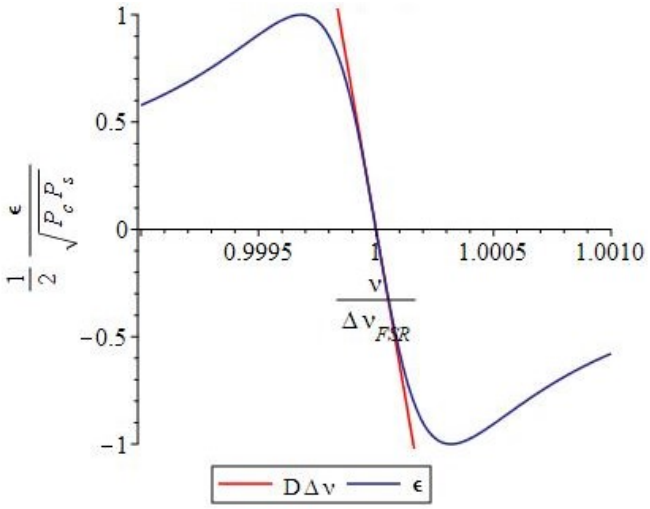

Figure 1.11: PDH error signal and its linear approximation near resonance

Note that even though the carrier is on resonance where there would be no reflected light, there is still an error signal with appreciable power because the sidebands are still reflected and can interfere with the leakage beam from the cavity.

The linear behaviour of the error signal plotted in figure 1.11 is only valid very close to resonance. However from figure 1.10 it can be seen that the error signal keeps the right polarity up to a frequency of $\frac{\Omega}{2\pi}$ away from resonance, which is still useful, especially for getting in to the lock.

Maximizing the frequency discriminant $D = -\frac{8|E_0^2 J_0(\beta) J_1(\beta)|}{\Delta\nu_{FWHM}}$ with respect to parameter β, results in the value $\beta^* = 1.082$ for which equation 1.11 is a good approximation of the full Jacobi-Anger expansion, as shown in figure 1.7.

1.4 The complete PDH lock setup

The complete PDH-lock setup is given in figure 1.12. The laser emits light which is sent through an electro-optic phase modulator based on the Pockels effect, which is sinusoidally driven by a voltage controlled oscillator. The resulting beam (approximately only consisting of the carrier and two sidebands) is then incident on a Fabry-Pérot cavity. The power of the reflected beam is then detected by a photodetector which converts the detected power in an analog signal. This signal is then mixed with the sinusoidally signal generated by the voltage controlled oscillator and afterwards sent through a low pass filter to end up with the PDH error signal ϵ. A PID controller then processes this error signal and outputs a signal between -1V and +1V, which contains the information about which direction the laser frequency has to be corrected for. However the laser takes input signals in the range of 0-6V and 0-8V for fast and slow feedback respectively. To fully utilize both of these ranges two PCBs are designed to map signals between -1V and +1V on the respective range by shifting and amplifying the signal, with minimal additional phase delay for signals with frequencies up to the high kHz range. The design of this circuit and PCB are discussed in the next chapters. Note that in the setup also a phase shifter is introduced. The reason for this is to account for different phase delays in both of the signal arms that are ultimately mixed together in the mixer. In practice however, no phase shifter is used and instead the modulating frequency is slightly tuned until the phase delay results in a nice error signal.

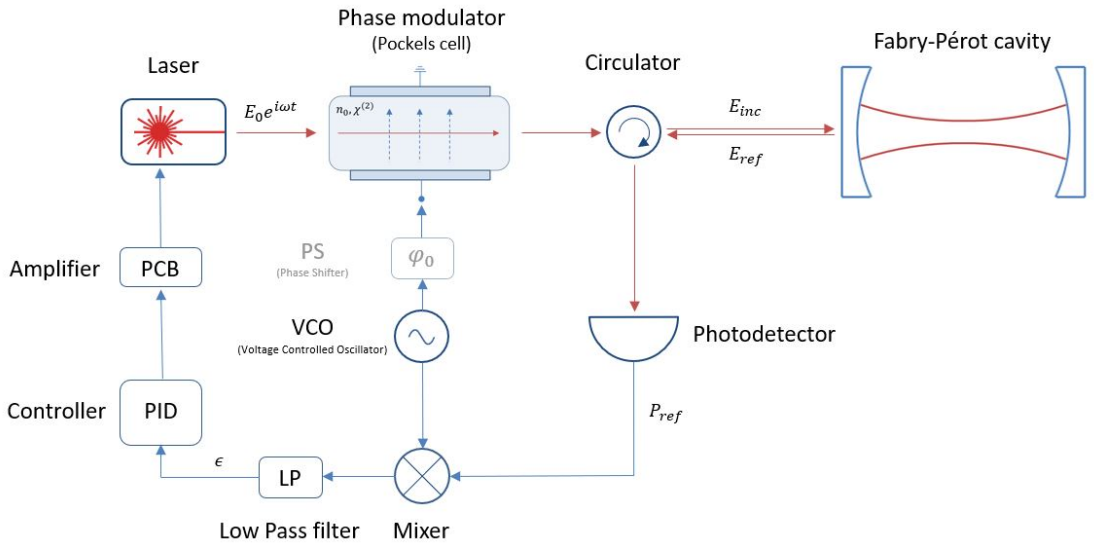

Figure 1.12: Complete PDH-lock setup

1.5 An intuitive picture of PDH locking in the complex plane

For a better understanding of why the PDH locking technique works, it is useful to look at what happens with the electric field of the reflected beam in the complex plane (in a rotating frame at frequency ω). This is shown in figure 1.13. Near resonance the electric field of the carrier can be approximated by $E_c \approx i\sqrt{P_c}\frac{\Delta\omega}{\pi\Delta\nu_{FWHM}}$ and the total electric field of the two sidebands together is given by $E_s = -i2\sqrt{P_s}\sin\Omega t$.

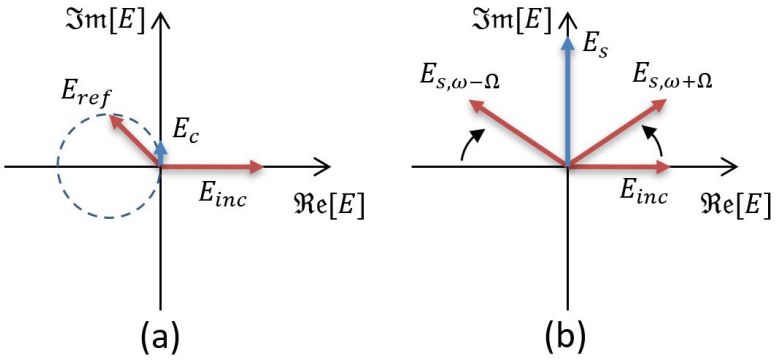

Figure 1.13: The electric field representation in the complex plane in a rotating frame at frequency ω. (a) The reflected electric field lies on a circle going through the origin (cf. figure 1.5). When ω is close to the cavity resonance the reflected electric field is very small (close to the origin) and approximately imaginary. (b) The electric field of the two sidebands is rotating at frequency $\pm\Omega$ (so in opposite directions). When the two sidebands are added the resulting electric field for the sidebands is purely imaginary and oscillating at frequency Ω.

Near resonance the power of the beam reflected of the cavity can then be approximated as follows:

$$P_{ref} = |E_c + E_s|^2 \approx P_c\left(\frac{\Delta\omega}{\pi\Delta\nu_{FWHM}}\right)^2 + P_s - 4\sqrt{P_cP_s}\frac{\Delta\omega}{\pi\Delta\nu_{FWHM}}\sin\Omega t - 2P_s\cos 2\Omega t \tag{1.18}$$

After mixing and the low pass filter only the third term survives and we end up with the same error signal as given in equation 1.19. One important feature to point out is that there is also an error signal for frequency fluctuations faster than the cavity's photon decay time. This shows that the PDH locking technique is not limited by the cavity linewidth. Intuitively this can be explained as follows. The reflected beam consists of two parts: the promptly reflected beam (which never entered the cavity) and the leakage beam. The promptly reflected beam is directly related to the incident beam (without

any additional delay). The leakage beam on the other hand acts as a stable reference averaging both the frequency and the phase of the laser over the cavity's photon decay time. An error signal will be generated in case the promptly reflected beam is not equal to the stable reference leakage beam. [2]

1.6 Noise considerations

In theory the noise can be divided in three categories. The first category consists of noise which leaves the system insensitive up until first order. Some examples of noise in this category are variations in laser power, response of the photodiode, modulation depth, relative phase of the two signal going into the mixer or modulation frequency. Note that all these contributions vanish up to first order because we are locking at resonance, where the reflected carrier vanishes. The fact that the variations in laser power leave the system invariant up to first order is important because this was one of the flaws in the other more primitive methods, as discussed in section 1.2.1. That this is indeed the case can be seen from the mathematical expression of the error signal:

$$\begin{aligned}\epsilon &\approx -\frac{8\sqrt{(P_c+\delta P_c)\frac{1-(P_c+\delta P_c)}{2}}}{\Delta\nu_{FWHM}}\Delta\nu \\ &\approx -4\sqrt{2}\frac{\sqrt{P_c(1-P_c)}}{\Delta\nu_{FWHM}}\Delta\nu - 2\sqrt{2}\frac{1-2P_c}{\sqrt{P_c(1-P_c)}\Delta\nu_{FWHM}}\delta P_c\Delta\nu \end{aligned} \tag{1.19}$$

In the second step a first order Taylor expansion was made around P_c. Now it is clear from the resulting expression that the variation in laser power is only present together with the spectral variation and thus it leaves the error signal invariant up to first order. The second category contains first order sensitive noise sources, which fall off for large modulation frequency Ω. An example of this kind of noise are the variations in sideband power at the modulation frequency. As a last category there is the shot noise, which for sufficiently large modulation frequency Ω is the dominant noise source. Note that shot noise is noise due to the quantum mechanical fluctuations in the phase quadrature of the electromagnetic field. By using squeezing it is in principle possible to go below the shot noise limit. The spectral density of shot noise in E_{ref} is given by $S_e = \sqrt{2\frac{hc}{\lambda}(2P_s)}$. Dividing this by the frequency discriminant D results in the spectral density of frequency noise:

$$S_f = \frac{\sqrt{hc^3}}{8\mathcal{F}L\sqrt{\lambda P_c}} \tag{1.20}$$

It is worth pointing out that the fundamentel shot noise limit doesn't depend on the power in the sidebands directly, but rather depends on the power in the carrier. [2]

1.7 Final remarks on PDH locking

In this chapter it was shown that the setup in figure 1.12 provides an error signal ϵ which is proportional to the laser frequency fluctuation near resonance. The proportionality constant (the frequency discriminant) is inversely depending on the cavity linewidth.

Using the PDH lock for frequency stabilization has the following advantages:

- The laser is operating at resonance of the Fabry-Pérot cavity.
- The error signal (which is related to the spectral noise) is decoupled from laser intensity noise.
- The technique is not limited by the linewidth of the cavity.
- For large enough Ω the system is only limited by shot noise up to first order.

Note that the PDH locking technique can actually be used for two goals:

1. Stabilizing the laser frequency by locking the laser to (often a more stable) optical cavity. (This is the final goal of this project.)
2. Measuring small changes in cavity length by locking the cavity to (often a more stable) laser. Usually one obtains this more stable laser by first locking it via the first method to another cavity. (This is used in the field of gravitational wave astronomy).

Chapter 2

Opamp circuit

In this chapter the electrical circuit for shifting and amplifying the feedback signal discussed in section 1.4 is designed. This circuit is based on the working mechanism of an operational ampilifier. The operational amplifier, often abbreviated as opamp, is an electrical circuit which approximates the behaviour of an ideal differential amplifier. It is often used for negative feedback.

2.1 The operational amplifier

The purpose of an opamp is to amplify a differential input voltage.

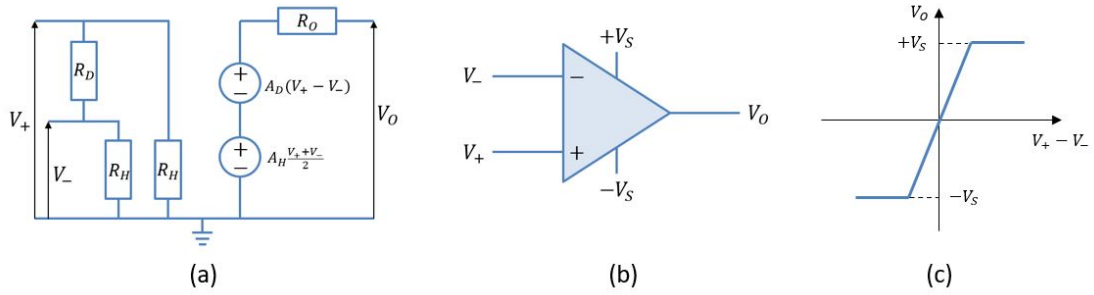

Figure 2.1: (a) The principal schematic of a differential amplifier. (b) Standard electrical symbol of an opamp with symmetric supply voltage V_S. (c) Differential input - output characteristic of an opamp.

In figure 2.1 the principal electrical schematic of a differential amplifier is shown. The output voltage V_O is thus given by:

$$V_O = A_D(V_+ - V_-) + A_H\frac{V_+ + V_-}{2} \tag{2.1}$$

$V_D = V_+ - V_-$ is called the differential input voltage and $V_H = \frac{V_+ + V_-}{2}$ is referred to as the homopolar input voltage or the common mode. The common mode rejection ratio $CMRR = 20\log\left(\frac{A_D}{A_H}\right)$. For good differential differential amplifiers the CMRR is very

high such that the output voltage is approximately given by $V_O = A_D(V_+ - V_-)$. For an ideal differential amplifier the following holds for R_D, R_H, A_D, A_H:

$$\begin{cases} R_D = R_H = \infty \\ R_O = 0 \\ A_D = \infty \\ A_H = 0 \end{cases} \tag{2.2}$$

In an opamp circuit the voltage amplification is so large, that even super small input voltage differences drive the opamp into saturation (figure 2.1 (c)). So the only steady state apart from being saturated (= output voltage at $+V_S$ or $-V_S$), is to have a near zero differential input. This regime can be achieved with the basic negative feedback circuits of the next section, which can be solved basically by setting $V_+ = V_-$.

2.2 Basic opamp circuits

2.2.1 Inverting amplifier

An inverting amplifier can be achieved by the circuit shown in figure 2.2. The resulting output voltage is given by:

$$V_{out} = -\frac{R_2}{R_1} V_{in} \tag{2.3}$$

The input impedance is R_1 and the output impedance is low.

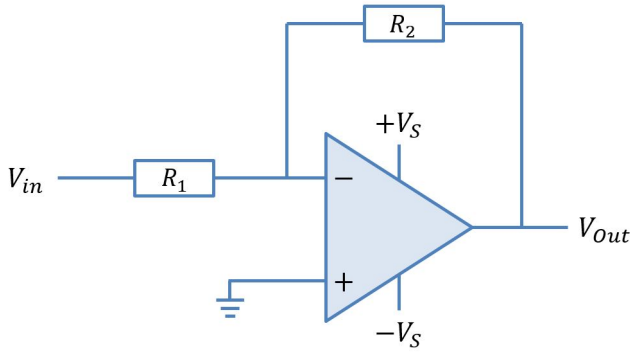

Figure 2.2: Electrical circuit of an inverting amplifier using an opamp.

2.2.2 Non-inverting amplifier

A non-inverting amplifier can be achieved by the circuit shown in figure 2.3. The resulting output voltage is given by:

$$V_{out} = \left(\frac{R_2}{R_1} + 1\right) V_{in} \tag{2.4}$$

The input impedance is very high and the output impedance is low.

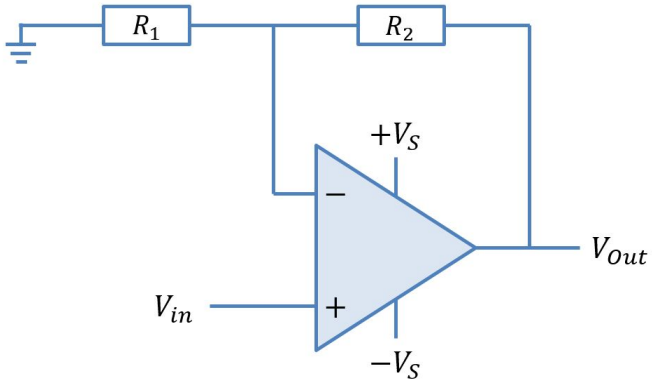

Figure 2.3: Electrical circuit of a non-inverting amplifier using an opamp.

2.2.3 Voltage follower

A voltage follower (also called buffer) can be achieved by the circuit shown in figure 2.4. The resulting output voltage is given by:

$$V_{out} = V_{in} \tag{2.5}$$

The input impedance is very high and the output impedance is low. The voltage follower thus transforms the impedance (from a high impedance to a low impedance). This is useful because now the signal source is not loaded with the circuit connected to the output. Since the input impedance is very high, the opamp will draw only a minimal amount of current from the input signal source. Meanwhile, the output acts as an almost perfect voltage source, since it has a low output impedance.

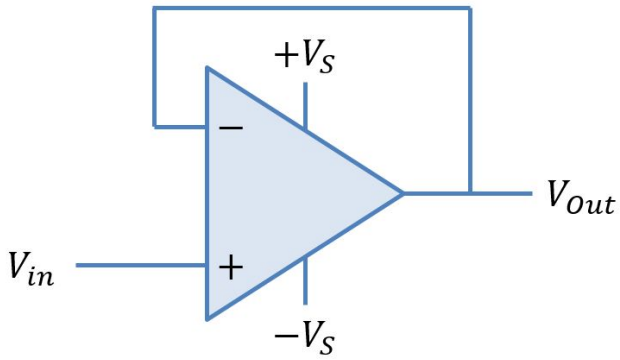

Figure 2.4: Electrical circuit of a voltage follower using an opamp.

2.3 Basic electrical circuit

As described in section 1.4, the purpose of the electrical circuit is the following: an input signal in the range between -1V and +1V needs to be inverted, amplified and shifted without phase delay to a signal in the range between 0V and 8V (resp. 6V) for slow (resp. fast) frequency stabilization. While the amplification and shift are necessary, the inversion is merely out of convenience, because it results in a simpler circuit. Figure 2.5 shows the basic electrical circuit that is able to perform this voltage range mapping. The circuit is basically an inverting amplifier which has its reference voltage biased by a voltage divider. In this section it is shown which resistor values (or at least which ratios of resistor values) have to be used to map $[-1\text{V}, +1\text{V}]$ (inverted) on a general interval $[0\text{V}, \kappa\text{V}]$. In the case needed for the PDH-lock κ is 6 or 8. Note that the electrical circuit is in principle able to map any input range inverted on any output range, as long as the symmetrical supply voltage of the opamp is large enough. In the next section additional circuit elements are introduced for various reasons.

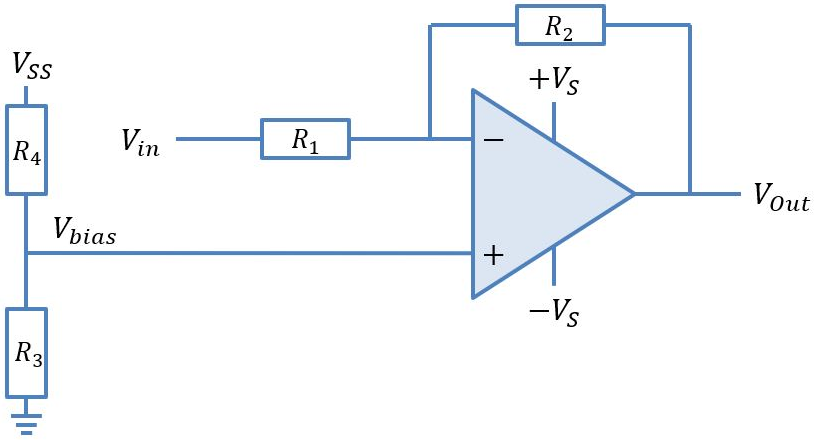

Figure 2.5: Basic electrical circuit for voltage range mapping.

Using equation 2.3 for the inverting amplifier and equation 2.4 for the non-inverting amplifier it can easily be seen that the output voltage is given by this expression:

$$V_{out} = -\frac{R_2}{R_1} V_{in} + \left(\frac{R_2}{R_1} + 1\right) V_{bias} \tag{2.6}$$

From this relation the following two conditions can be derived:

$$\frac{R_2}{R_1} = \frac{\kappa}{2} \tag{2.7}$$

$$\left(\frac{R_2}{R_1} + 1\right) V_{bias} = \frac{\kappa}{2} \tag{2.8}$$

Equation 2.8 can be simplified, using equation 2.7 and the formula for a voltage divider $V_{bias} = \frac{R_3}{R_3+R_4} V_{SS}$ with V_{SS} the voltage provided by a supply source. This results in the following condition:

$$\frac{R_4}{R_3} = V_{SS}\left(1 + \frac{2}{\kappa}\right) - 1 \tag{2.9}$$

The 2 PCBs for the PDH lock will be driven by USB connection, which provides +5V. Using a DC/DC-converter this +5V is then converted in +12V and -12V. That is why V_{SS} is taken to be +12V.

Table 2.1 shows the resulting numbers for the two PCBs in the PDH-lock.

	$\frac{R_2}{R_1}$	$\frac{R_4}{R_3}$	R_1	R_2	R_3	R_4
0-6V	3	15	1.4 kΩ	4.2 kΩ	560 Ω	8.4 kΩ
0-8V	4	14	1.4 kΩ	5.6 kΩ	600 Ω	8.4 kΩ

Table 2.1: Table with the required ratios of resistor values for mapping onto the respective voltage range. In the last four columns a set of possible resistor values is given that achieve these required ratios. Note that $V_{SS} = +12$V.

2.4 Full electrical circuit

The basic electrical circuit of figure 2.5 has multiple extensions. A voltage follower is introduced at the input. Resistor R_5 with a very small resistance of $100\,\Omega$ is added to make sure as little current as possible is drawn to the non-inverting input of the opamp. The capacitors C_2 and C_3 are added to form an active and a passive low pass filter respectively. Hence they result in a cutoff frequency for the circuit. They are included for stability reasons and noise reduction. Because of this the combination of C_1, R_6 and R_7 is also added to the circuit. The electrical circuit with all these extensions included is shown in figure 2.6.

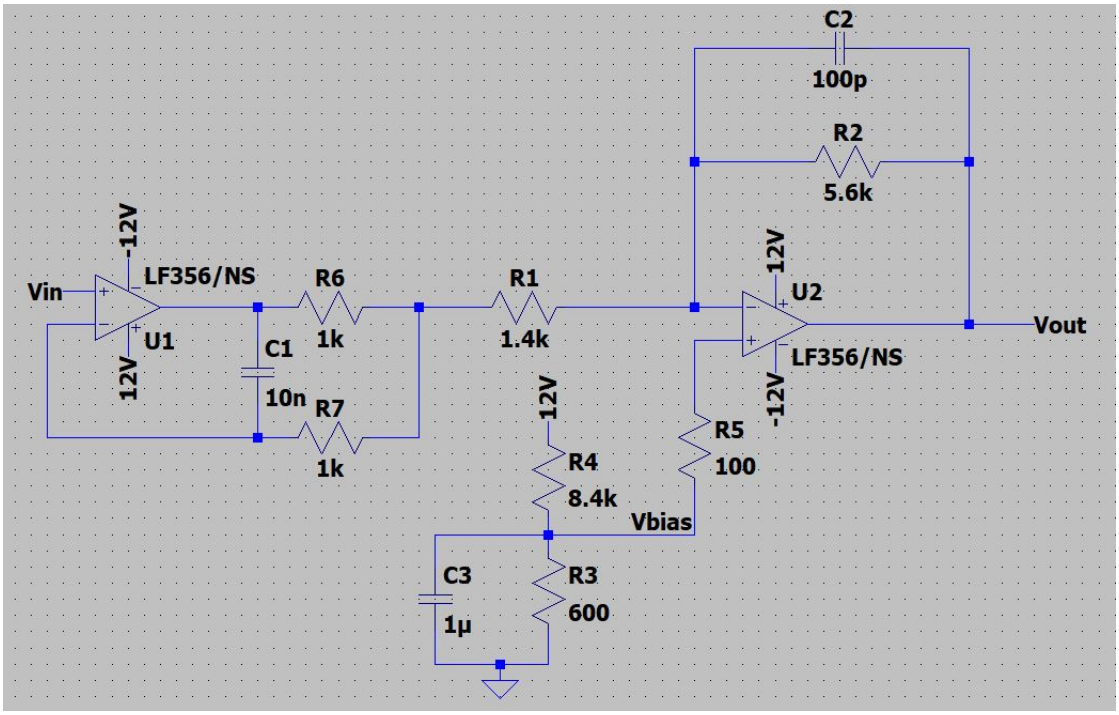

Figure 2.6: Full electrical circuit for inverted voltage range mapping. The values shown are for the version which maps [-1V,+1V] on [0V, 8V].

To show that this electrical circuit works, a simulation is made in LTSpice XVII. For an input oscillating at 100 kHz the simulated output signal is plotted in figure 2.7. This is exactly the desired result. Note that the simulation is able to use the exact opamp that is later used in the real PCB.

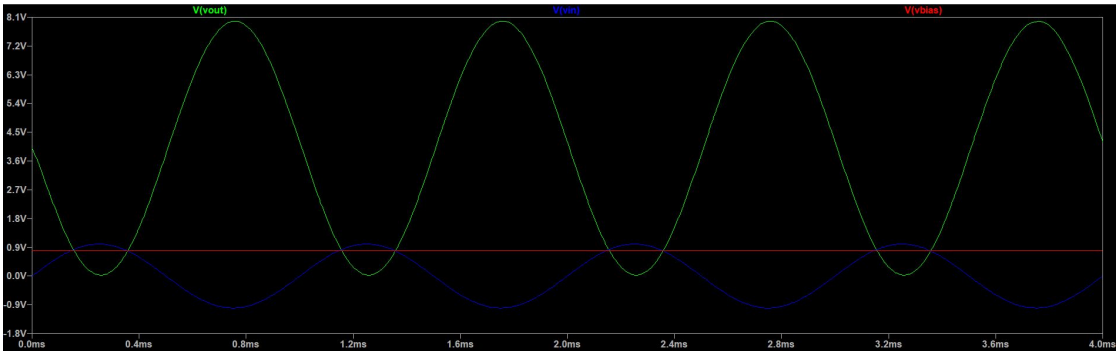

Figure 2.7: Simulation of the bias and output voltage for a sinusoidally input signal with amplitude +1V, no offset and oscillating at 1 kΩ. The target voltage range is [0V, 8V].

There exist different types of opamps. These different types make use of different types of transistors. The three most common transistor techologies are bipolar junction transistors (BJT), field effect transistors (FET), complementary metal-oxide semiconductor (CMOS) as a type of MOSFET. BJT, FET, CMOS is listing the types in increasing order in terms of approximating the characteristic curve of an ideal differential amplifier. For our purposes, the Texas Instruments LF356 JFET input opamp is chosen. The main reason for choosing a FET opamp is because they have the fastest response, which is desirable for not getting additional phase delay in the circuit. Additionally with a BJT based model too much current was being drawn at the inputs, which is a problem with older opamps.

In the complete opamp circuit needed on the PCB, also the power supply and the connectors need to be included. The resulting scheme with everything included is shown in figure 2.8. The input and output signal is connected with SMA connectors (a type of coaxial connectors). At both input and output two diodes are added for overvoltage protection in the way that can be seen in figure 2.8. This technique is called clamping. As soon as the input (output respectively) voltage exceeds one of the supply voltages of the opamp (plus the forward voltage over the diode itself), the current is sent into the supply pins of the opamp, instead of into the input (output respectively) pin of the opamp, where it could damage the opamp. A micro-USB connector is added to power the whole opamp circuit. Note that the ground of this power supply (GNDREF in figure 2.8) is separated from the ground of the signal (GND in figure 2.8). A USB connection standardly provides +5V. This +5V is then via a switch (to easily switch on and off the power supply for the whole circuit, without disconnecting the micro-USB connector) sent into the Traco Power TDR3-0522 DC/DC converter. As the name suggests this component converts the +5V into +12V and -12V, which is extremely useful for operating the opamps. Another extension with respect to the circuit in figure 2.6 are the bypass capacitors C_4 and C_5. These bypass capacitors don't let the DC voltage pass but provide a low resistance path for AC noise to go to ground instead of going into the opamp supply

pin. Usually it is best to place these bypass capacitors as close to the opamp supply pins as possible. Note that these bypass capacitors also have an additional advantage: when a sudden voltage drop (a spike) occurs in the power supply these capacitors can release their accumulated charge to counteract the supply voltage fluctuation. The last added feature is an LED which indicates whether the power supply is switched on or off.

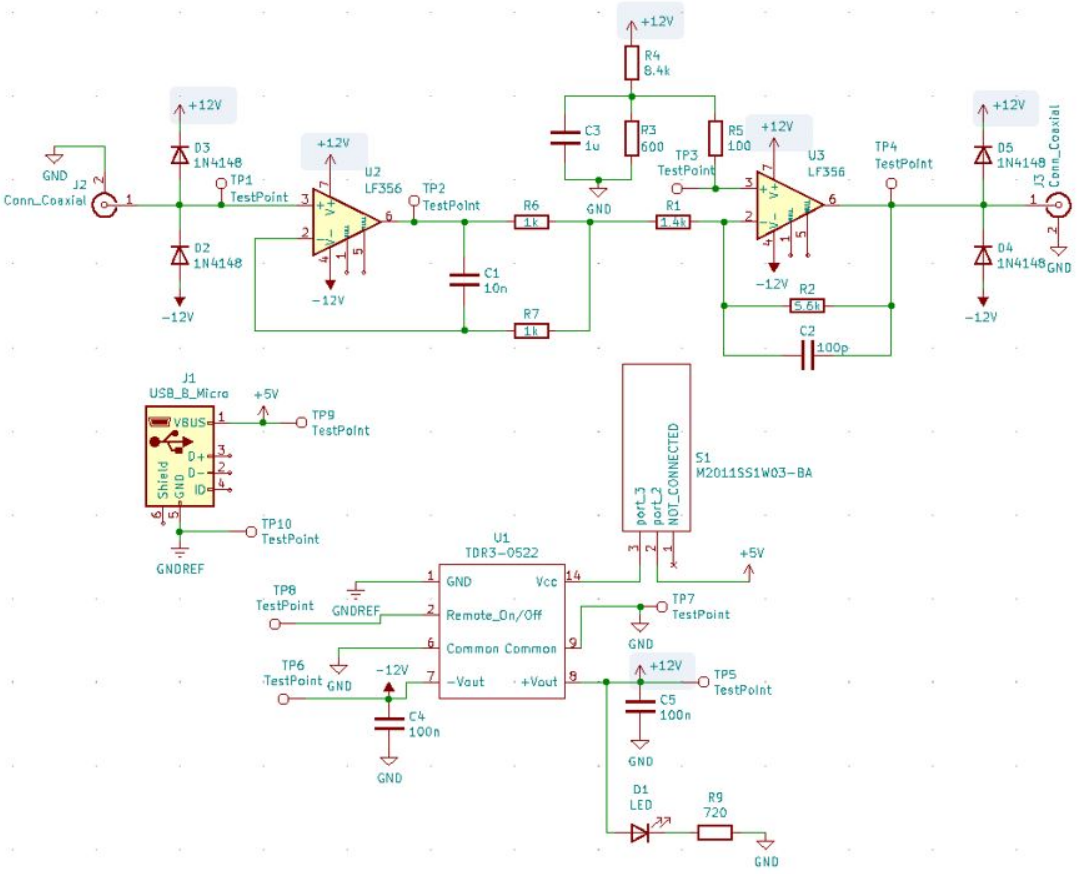

Figure 2.8: Full electrical circuit, including power supply and connectors. The different connections to the +12V net are indicated with blue markings.

Chapter 3

PCB design

In this chapter first the general steps of designing a pcb are explained and applied to the opamp circuit of figure 2.8. During this semester project two PCBs were designed for other purposes as well. These are shown afterwards.

3.1 General process for designing a PCB applied to the opamp circuit for the PDH lock

To design the PCBs the open source software KiCad (version 5) is used. The design process of a PCB can be divided in 6 subtasks (see figure 3.1). The next subsections all elaborate more on one of the different subtasks.

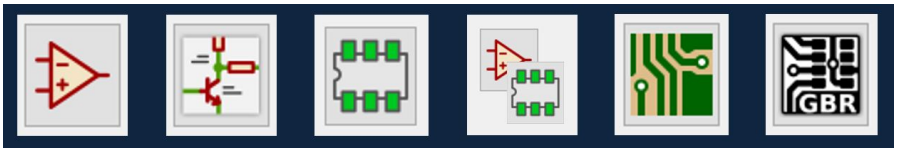

Figure 3.1: Symbolic representation of the 6 steps in designing a PCB: Symbol editor, Electrical schematic, Footprint editor, assigning footprints to symbols, designing PCB, generating Gerber and drill files.

3.1.1 Symbol editor

The first step in designing PCBs is to have a symbol for all electrical components that will be used in the electrical schematic in the next step. A symbol contains all inputs, outputs, passive connections, supply inputs and supply outputs of the specified electrical component.

By default there are already many libraries loaded in KiCad. Make sure to check first whether the needed symbol is already available in one of these. If this is not the case it is possible to design it yourself in the Symbol Editor and save it in your own library. Figure 3.2 shows an example of this for the DC/DC-converter, where the symbol is saved in the "PersonalSymbols" library. Note that the connections also need to be labeled with pin numbers. These have to match the pin numbers of the component's footprint (step

3). It is also possible to add pins with "no connection", however this is not necessary. In the example of figure 3.2 there is no connection specified for pins 3, 4, 5, 10, 11, 12 and 13. Note that sometimes it is not necessary to design the complete symbol yourself, because it is possible to just edit a similar one that is already available in one of the libraries. `Mouser.ch` sometimes also provides the symbol and footprint (step 3) for the components available for sale on their webshop.

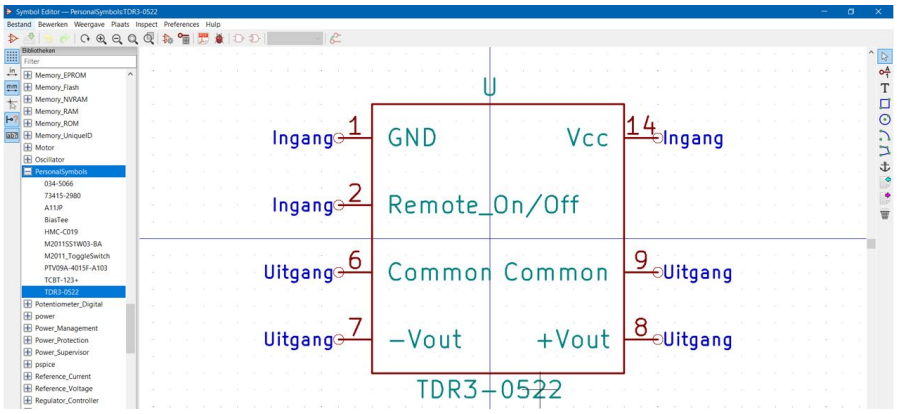

Figure 3.2: Symbol Editor: Traco Power DC/DC converter TDR3-0522.

3.1.2 Electrical schematic

In the second step the symbols for all components are placed and connected with wires. For the opamp circuit this is shown in figure 2.8. In practice steps 1 and 2 are often performed simultaneously, meaning that one usually just designs a symbol when he/she needs it to place in the electrical circuit. To make the drawing clearer, it is recommended to make use of nets (typically for power) / labels (typically for a signal). These nets/labels connect all specified locations without the need for an explicitly drawn wire. This is usually very useful for the ground and power. In figure 2.8 the following nets are used: GNDREF, +5V, GND, +12V and -12V. Another useful feature to add are testpoints (as is also done in figure 2.8). After the fabrication of the PCB and when all components are soldered on the PCB these testpoints can be very useful to test the board.

3.1.3 Footprint editor

Once the drawing of the electrical circuit is finished, one can move on to the third step: making footprints for all components. A footprint is the alignment of pads and or holes. Pads are used for soldering with surface mounted technology (SMT) and holes for soldering with through hole technique (THT). Again, by default there are already a lot of footprint libraries available. However the footprints of some components are not in there. For these components one can again first look at `Mouser.ch` whether the footprint is available there. If this is the case, it is easy to extract these using the SamacSys

Library Loader application. If this is not the case, it is possible to design the footprints yourself. Check the component's datasheet for the required dimensions and pin layout. Always check the dimensions, also with the footprints, you don't design yourself. Make sure the pin layout matches the one of the corresponding symbol of step 1. An example of a footprint is given in figure 3.3. Note that this footprint is a combination of SMT pads and THT holes. The electrical connections are the fine pads 1, 2, 3, 4 and 5. The other pads and holes are only for mounting purposes, such that the connector doesn't break off.

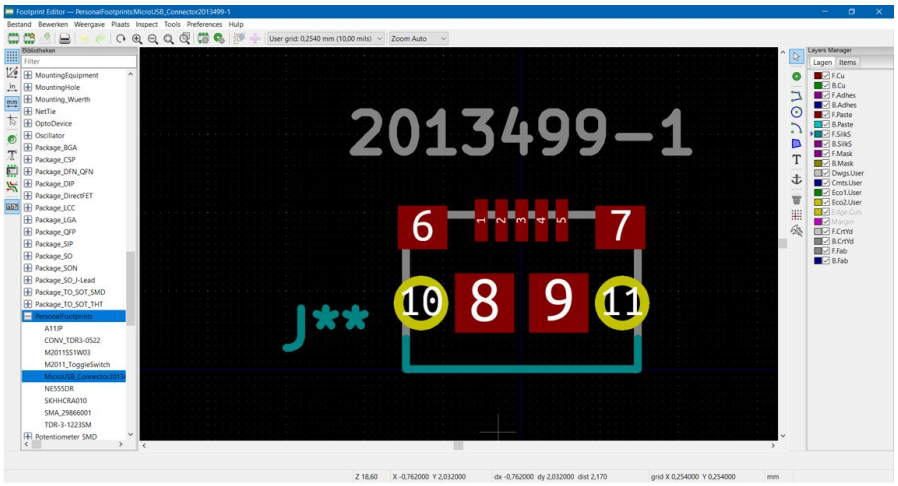

Figure 3.3: Footprint Editor: TE Connectivity micro-USB connector 2013499-1.

3.1.4 Assigning footprints to symbols

In the fourth step a footprint is associated with all symbols in the electrical circuit of step 2. An example of how this looks like is shown in 3.4. In the middle column you select which component you want to assign a footprint to. In the left column you choose the library, in which the footprint is saved. This library then opens in the right column, where you can select the desired footprint by double-clicking on it.

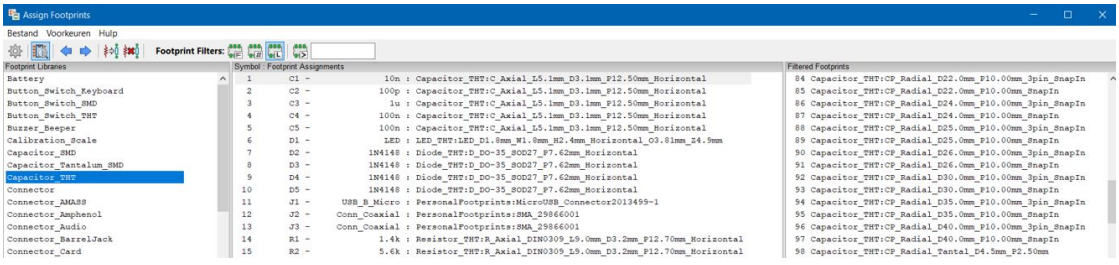

Figure 3.4: Assigning footprints to symbols

3.1.5 Designing PCB

Once all components are assigned a footprint, it is time for the fifth and main step in de PCB design process. First you have to press the "update PCB from schematic" button in the toolbar at the top. Now all the footprints appear on the screen. The white lines connecting the different pads/holes of the components with eachother show all the connections that still need to be drawn. Start by arranging all the components in a logical way, meaning that it is preferable to have components close to eachother that are also close together on the electrical schematic, just to keep a clearer overview of the PCB. Once you have a nice arrangement of the components you can start by drawing the wires between the pads/holes. For an easy current flow it is preferably to only have straight lines and 135° angles. Make use of the different layers. In the PCB for the opamp circuit (shown in figure 3.5) 2 layers are used: red for the top copper layer and green for the bottom copper layer. Vias are a useful tool to connect top and bottom wires, which makes it possible to cross another wire. For larger or more dense PCBs it can be an idea to use one layer only for horizontal wires and the other layer only for vertical wires.

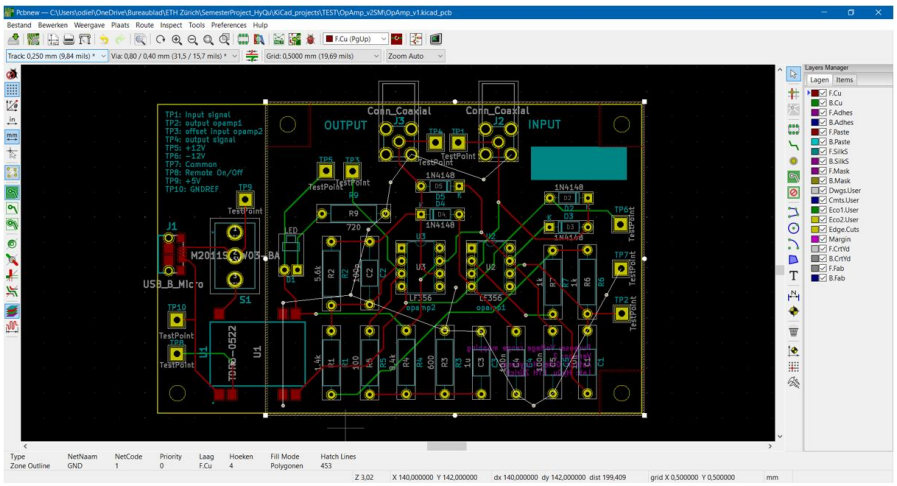

Figure 3.5: Designing PCB: PCB for opamp circuit without ground planes filled

Note that in the PCB in figure 3.5 there are still some white lines, meaning that some connections are still missing. In this case these white lines are connecting all GND nodes. Instead of connecting all these nodes with wires, one can also fill a layer with copper to get a whole plane at the respective voltage. In this case both top and bottom layer are made ground planes. However one could for example also use a +12V layer. If you use filled layers instead of wires, make sure there is an easy path for the current to travel through it. If both layers are at the same voltage (e.g. ground plane) it is possible to make shorter paths by also using vias for the planes. In figure 3.6 the same PCB is shown, but now with the filled ground layers. The small white circles in the red plane are the ground plane vias. It can be seen that the ground plane is not extending over

the whole PCB. The reason for this is galvanic isolation because the supply voltage of +5 is using a different ground (GDNREF).

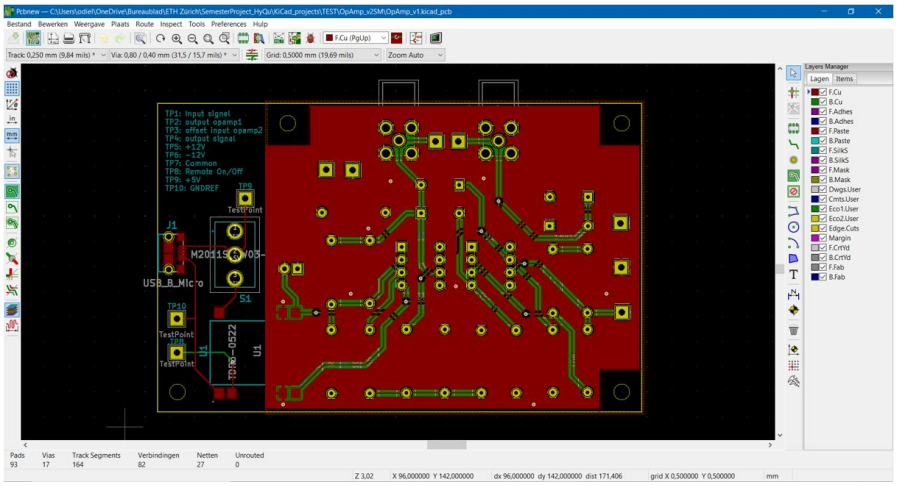

Figure 3.6: Designing PCB: PCB for opamp circuit with ground planes filled

The yellow lines mark the edge cuts. There are also 4 yellow circles to make mounting holes in the PCB. When designing mounting holes, make sure they are placed at a "normal" distance from eachother (e.g. a distance that can be expressed as a whole number in centimeters). Around these holes there is a region where the ground planes don't extend just to make sure that there is definitely no connection between the screws and the copper layer to avoid ground loops. The blue and purple are representing the top and bottom silkscreen layer respectively. This will be visible on the PCB after printing. If you want to write something on the back layer, make sure to mirror the text. The blue text in the left top corner contains information on the different testpoints. That way it is possible to test the board without constantly having to look at the electrical schematic. The blue rectangle in the right top corner is just a small place designed to write down the mapped range (e.g. [0V,+8V]).

By right-clicking on a component it is also possible to assign a 3D model to the component. KiCad has a 3D viewer (under the view menu at the top), which shows a nice visualized model of how the PCB is going to look like. The 3D visualization of the opamp circuit PCB is shown in figure 3.7. These 3D models can also be used to have a quick check whether the ground plane is able to extend through the whole plane (i.e. whether there is enough space between all the wires as wires should always be separated from each other by the ground plane).

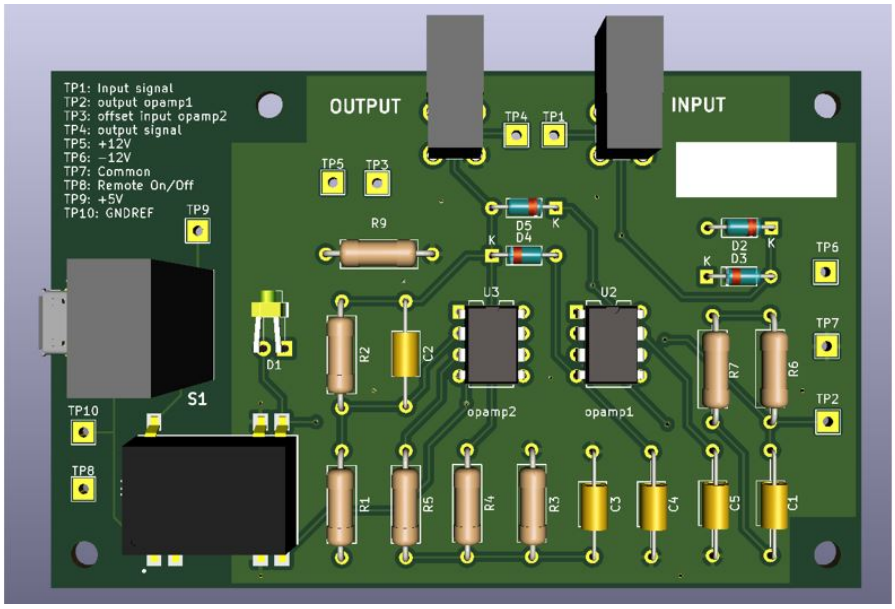

Figure 3.7: Designing PCB: Opamp cicuit PCB in 3D Viewer

3.1.6 Generating Gerber and drill files

When the PCB is fully designed, there is only one last step to do: exporting the right files to place an order at one of the PCB printing companies. For this project the PCBs were ordered at `pcbway.com`. These companies usually provide detailed information about which options need and don't need to be ticked when generating the Gerber and drill files. The Gerber files contain the information about one specific layer. The drill files contain the information about the holes. For PCBWay this information can be found on `https://www.pcbway.com/blog/help_center/Generate_Gerber_file_from_Kicad.html`. Don't forget to order a stencil if some components need to be surface mounted.

3.2 Two other PCBs designed during this project

3.2.1 Voltage offset circuit for synchronizing the lock-in with signal generator clocks (applied in Max' experiment)

The purpose of this circuit is to add a DC voltage to a high frequent AC signal (oscillating at frequencies around 10MHz). In this circuit a symmetric voltage divider and a non-inverting amplifier (as shown in subsection 2.2.2) with amplification factor 2 (so $\frac{R_2}{R_1} = 1$) are combined to effectively get a summing circuit. The two inputs of this summing circuit are the AC signal on one hand and the DC offset on the other hand. The DC offset is reached by using a voltage divider between +12V and ground. To be able to vary the DC offset a potentiometer is introduced as one of the resistors of this voltage divider. The circuit is driven by a micro-USB connection (so +5V) which is then converted in +12V and -12V with the Traco Power TDR3-0522SM as was the case in the opamp circuit for the PDH lock. A double BNC connector is used to connect both the input and the output to the board. The opamp used in this setup is the Intersil CA3130EZ opamp with MOSFET input and CMOS output. It can process signals up to 15MHz. The electrical circuit, PCB and 3D model of the PCB are shown in figures 3.8, 3.9 and 3.10 respectively.

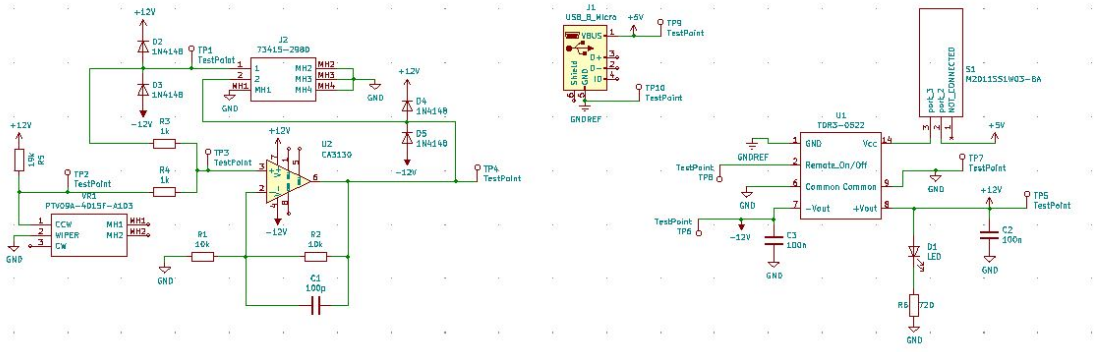

Figure 3.8: Electrical circuit of opamp based tunable voltage offset circuit

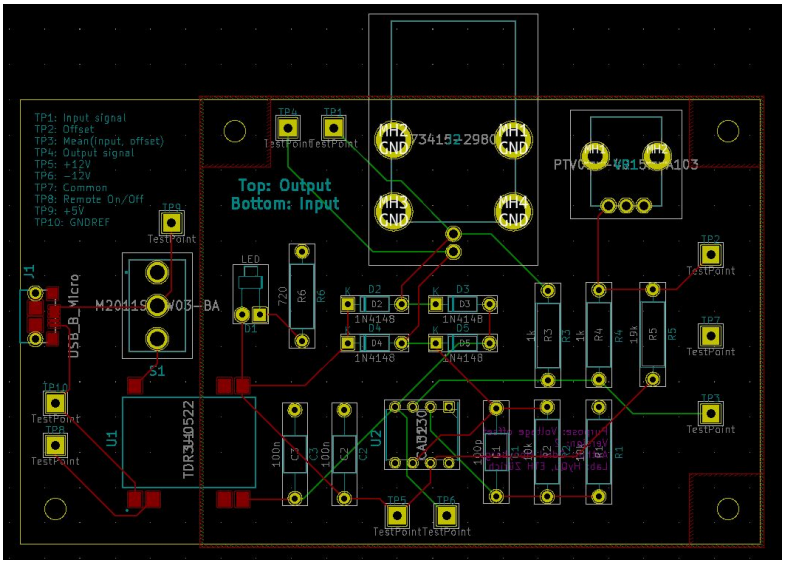

Figure 3.9: PCB of opamp based tunable voltage offset circuit

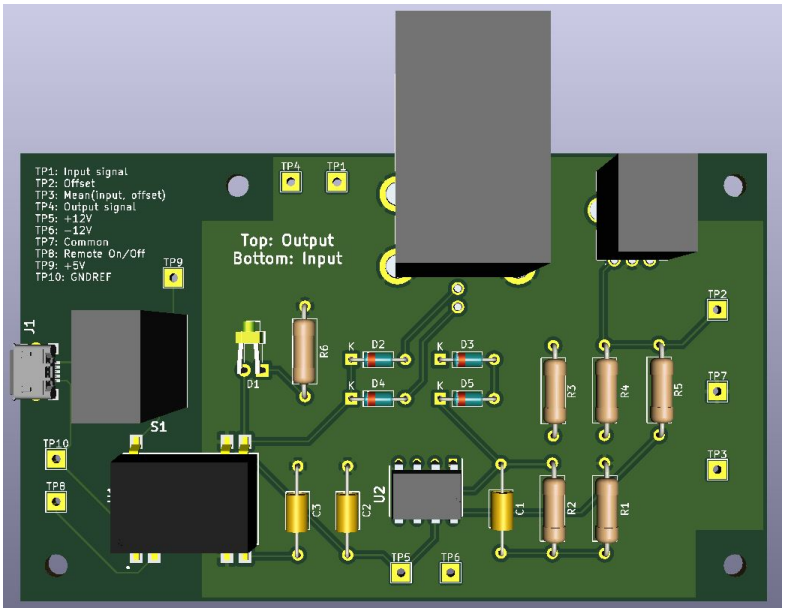

Figure 3.10: 3D model of PCB of opamp based tunable voltage offset circuit

Note that for adding a DC offset to an AC signal such summing circuit is actually more complicated than necessary. An easier way of doing this would be to use a bias tee, as used in the next subsection.

3.2.2 Interface with voltage offset circuit for controllable fast HMC-C019 switch (applied in Uwe's experiment)

The working of the HMC-C019 switch is as follows: an input signal is either directly transmitted to the output or the output is 0V. Which one happens depends on the marker. When the marker is above +3.5V the input signal is transmitted. When the marker is below +1.5V the output is 0V. The problem is that the generated marker is 0V when signaling OFF and only +3V when signaling ON. To resolve this it suffices to add +1V as DC offset such that the OFF signal is +1V (which is below +1.5V) and the ON signal is +4V (which is above +3.5V). Instead of using a summing circuit based on an opamp as in subsection 3.2.1, a more clever solution is used: a bias tee (see figure 3.11). A bias tee is an electrical circuit that is specifically designed to add a DC and an AC signal. To do so it makes use of the fact that an RF (AC) signal can easily pass through a capacitor but cannot cross an inductor, while a DC signal can easily pass through an inductor but cannot cross a capacitor. The RF signal is connected to a capacitor and the DC signal to an inductor. Next the capacitor and the inductor are connected such that at this connection the signal is given by the sum of the RF and DC signal. To filter AC noise in the DC signal a bypass capacitor connects the DC input port to ground. The bias tee used in this PCB is the Mini-Circuits PBTC-3GW+, which can process RF signals in the range between 100 kHz and 3000 MHz. The marker is a square pulse with a rise time of a few nanoseconds and a duration of a few microseconds. The bias tee should thus be able to process the marker.

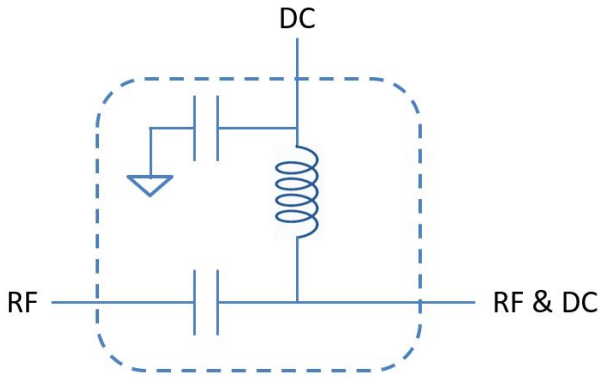

Figure 3.11: The basic working scheme of a bias tee.

The PCB for the bias tee based voltage offset circuit is shown in figure 3.12. It also includes the footprint of an SMA connector (for the marker), 2 BNC connectors (for the +5V and +1V voltage supply), pins and space (including mounting holes) for the HMC-C019 switch. On the outer side of both BNC connectors there is also some space provided to fix an SMA cable (e.g. with tape) which directly connects to the input or output of the switch.

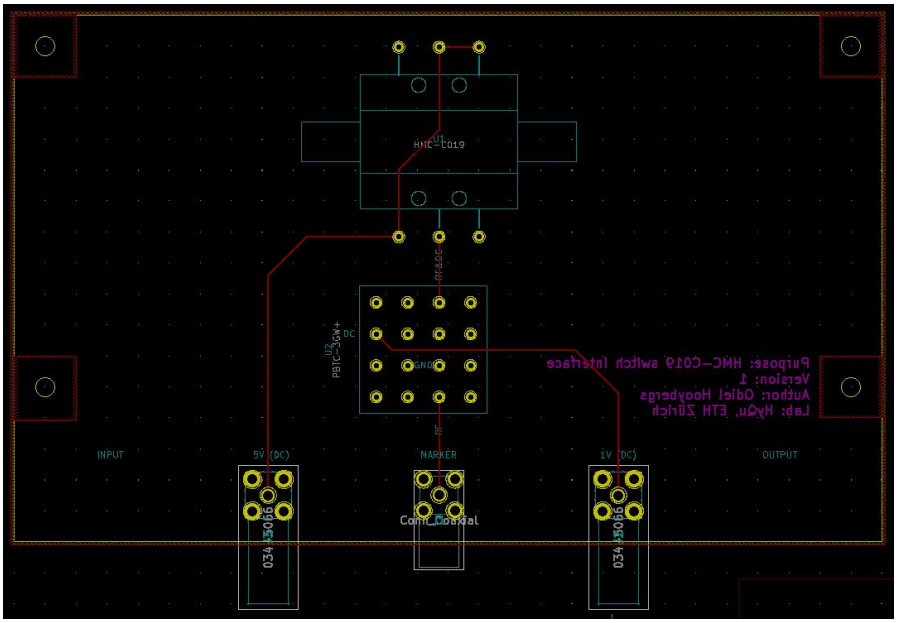

Figure 3.12: PCB of bias tee based voltage offset circuit

Chapter 4

Experimental results

4.1 Opamp circuit PCB

After the PCBs have been delivered, all electrical components have to be soldered on to them. First the surface mounted devices (SMD's) are soldered on the board. To do so, the stencil is perfectly alligned on top of the board and some solder paste is scraped over the stencil, such that all pads are covered with solder paste. Next the stencil is removed and the SMD's are placed on the pads, either by hand directly or with the use of tweezers. After all SMD's are placed on the board perform a quick check whether no paste of different pads is touching and whether all pins are touching the desired pads. Next the device is put in the surface mount soldering oven, where the solder paste is molten in a bath of hot vapor. Once this is finished, the test point clamps can be inserted and all through hole components can be soldered as well. Some of the components have polarity (in particular in the opamp circuit: diodes, LED, electrolytical capacitor C_3 of 1 μF), which means they have to be oriented in the right way when soldering them.

The surface mount soldering works very nice and especially if you need a lot of the same boards, it can be quite time saving to have as many SMT components as possible. Figure 4.1 shows one of the PCBs with all components soldered on to it.

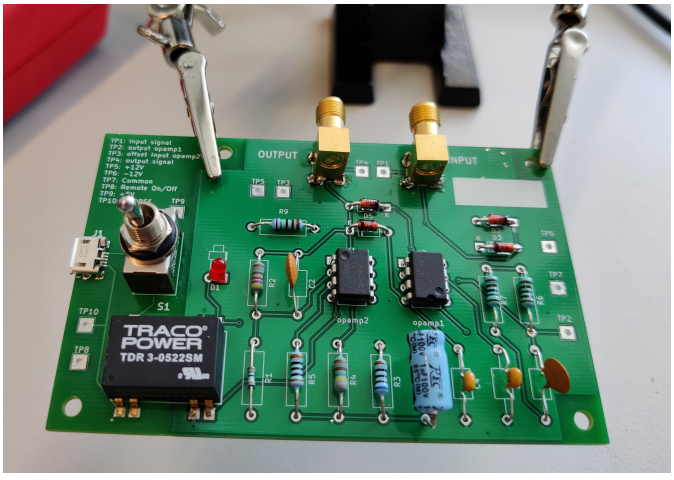

Figure 4.1: Opamp circuit PCB with all components soldered.

At this point the boards are ready for characterization. As a first test a sinusoidally signal with peak-to-peak amplitude 2V and no offset, oscillating at 2 kHz is connected to the input SMA connector. The resulting output (for the [0V,+8V] board) is shown in figure 4.2. This output signal is still oscillating at 2 kHz, but now between the values 0V and +8V, which is the desired result.

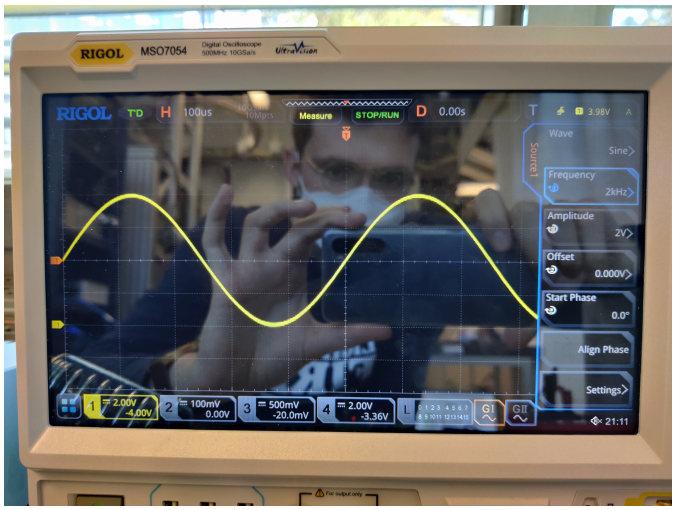

Figure 4.2: Output signal of the [0V,+8V] opamp circuit pcb for a sinusoidally input signal with peak-to-peak amplitude 2V and no offset, oscillating at 2 kHz.

Analogous results are achieved with the [0V,+6V] opamp circuit pcb.

To make a full characterization of the board (i.e. the response for input signals at different frequencies) a bode plot could be made.

4.2 PDH locking

The ultimate purpose of the project was to use this PCB to lock a laser with the PDH locking technique to a cavity. This cavity has similar parameters as the one used for optomechanical coupling experiments (R=99.9% mirrors, FSR 13 GHz). With the help of Tom the whole setup of figure 1.12 was build. First the resonance of the cavity needs to be found. Figure 4.3 shows this. The green line is the laser's input for fast feedback. Here the Red Pitaya was just chosen to output a triangle wave between -1V and +1V, which was then nicely converted by the PCB to the full input range the laser can take between 0V and +6V (as can be seen on the green line). The red line is the voltage signal corresponding to the power of the beam reflected out of the cavity. A drop to 0V in this signal means that there is almost no reflected light and thus the laser is emitting light at resonance. It can be seen that these drops occur around +3V of the fast feedback input voltage. This is desirable because +3V is located at the center of the interval and thus similar corrections could be made to both sides of resonance. Also note how sharp the drops in the reflected power are, causing the need for high precision corrections. The yellow line is the input voltage for the slow feedback and is currently unused.

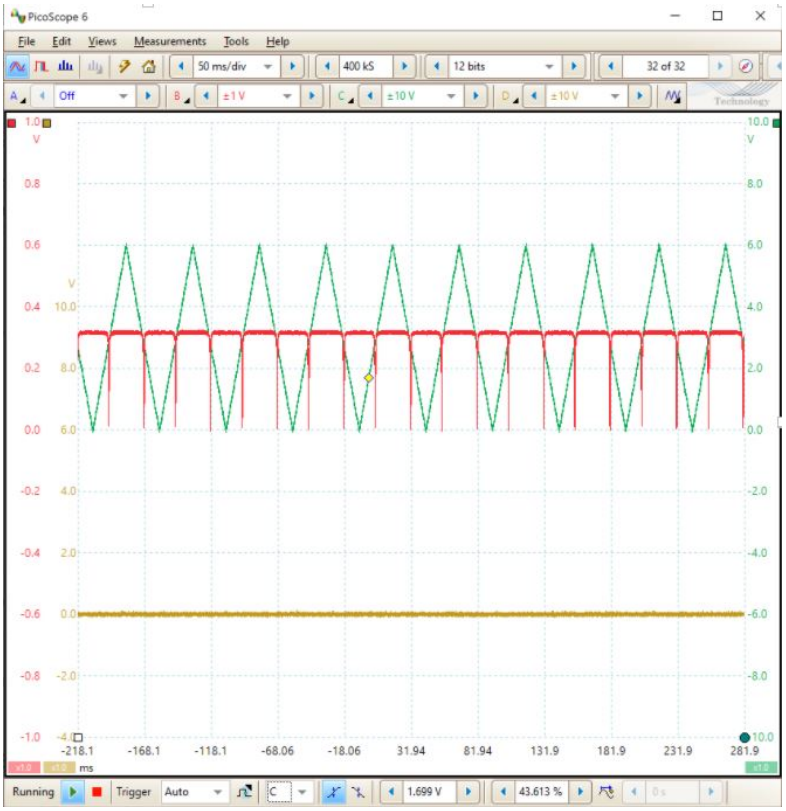

Figure 4.3: Resonance of the cavity found with laser emitting light at 193.5015 THz - 250 MHz.

Once the resonance is found, it is possible to look at the PDH error signal ϵ. This is shown by the yellow line in figure 4.4. The shape of figure 1.10 can easily be recognized (either flipped or not, depending on whether the triangle wave the Red Pitaya is outputing (red line) is rising or falling). Not that the misalignment between these two signals is probably not a physical misalignment but rather an offset in the plot.

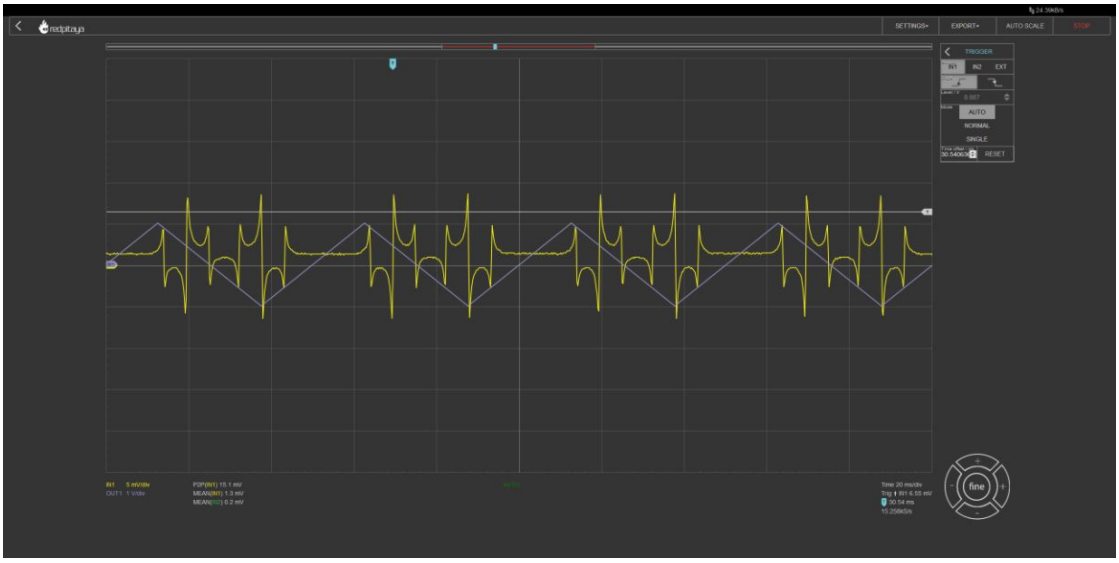

Figure 4.4: Experimental PDH error signal ϵ.

As a final step the laser is effectively locked to the cavity. The Red Pitaya (an FPGA based PID controller) now processes the PDH error signal ϵ. For completion, the used gain parameters K_P, K_I, K_D are given in figure 4.5. Note that hese settings were just to set up the lock initially and get it to a stable working state. To reduce the noise one can then start to optimize the parameters (e.g. so far we haven't used Kd).

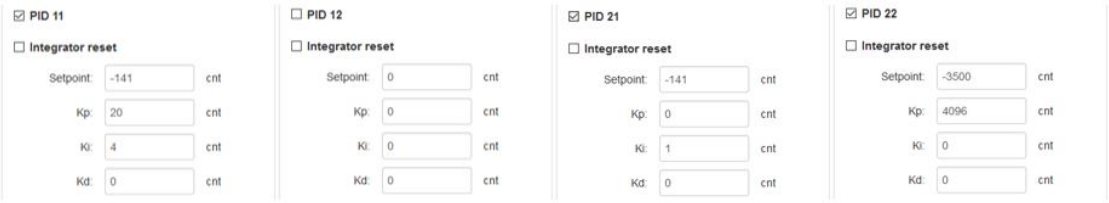

Figure 4.5: Gain parameters for the different PID controllers in the Red Pitaya used for the PDH lock. PID ij (i,j $\in \{1, 2\}$) is the PID controller going from input j to output i. The error signal was fed into input 1. Output 1 was the fast feedback signal sent directly to a piezoelectric element inside the laser and output 2 was the slow feedback signal which is digitally processed by the laser.

The final results are shown in figure 4.6. Both the fast (green) and slow (yellow) feedback input voltages are being used. The reflected power (red) is jittering at 0, meaning that the laser is continuously emitting light on resonance of the cavity. The laser frequency was put to 193.5011 THz with a correcting range for the slow feedback of 500 MHz.

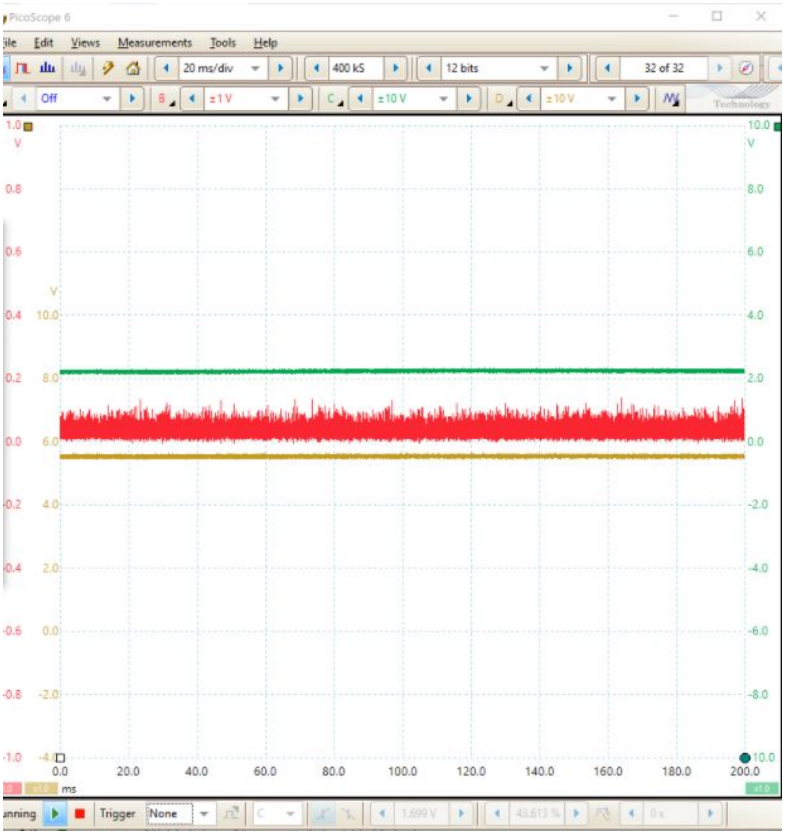

Figure 4.6: Laser locked to cavity.

Now it is also clear what the advantage is of converting the voltage range. Previously both the fast and slow feedback could only take voltages from 0V to 1V because of the voltage range overlap of the Red Pitaya and the laser input. Now they can make use of their full input range from 0V to 6V or 8V. Which is a factor of 6 or 8 higher. The emitted laser light can thus jitter 6 times or drift 8 times more and still be corrected for. The reason for this is that the resonances as shown in figure 4.3 can stay on the slope of the input feedback signal for a longer time (without jumping out of the lock). Note that the feedback inputs in figure 4.6 are just above 2V (green) and 5V (yellow), meaning that without the PCBs converting the range, the system would not be able to lock the laser with these settings, since these voltages are more than 0.5V away from 3V and 4V respectively.

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