Surface Chemical Tuning of Phonon and Electron Transport in Free-Standing Silicon Nanowire Arrays

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Ⓢ Supporting Information

ABSTRACT: We report electronic and phononic transport measurements of monocrystalline batch-fabricated silicon nanowire (SiNW) arrays functionalized with different surface chemistries. We find that hydrogen-terminated SiNWs prepared by vapor HF etching of native-oxide-covered devices show increased electrical conductivity but decreased thermal conductivity. We used the kinetic Monte Carlo method to solve the Boltzmann transport equation and also numerically examine the effect of phonon boundary scattering. Surface transfer doping of the SiNWs by cobaltocene or decamethylcobaltocene drastically improves the electrical conductivity by 2 to 4 orders of magnitude without affecting the thermal conductivity. The results showcase surface chemical control of nanomaterials as a potent pathway that can complement device miniaturization efforts in the quest for more efficient thermoelectric materials and devices.

KEYWORDS: Silicon nanowires, surface transfer doping, electron and phonon transport
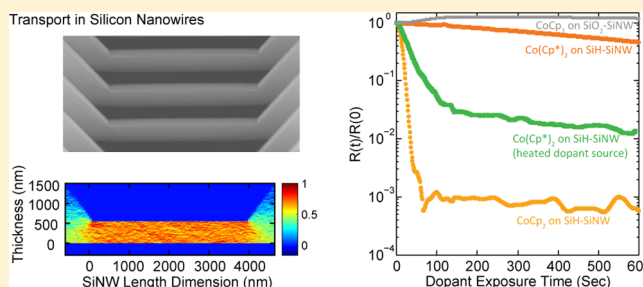
Thermoelectric energy conversion is an important energy technology that can directly utilize available thermal energy sources, such as solar,[1,2] and can complement existing traditional energy conversion systems to improve the overall efficiency. An even more readily available source of thermal energy is fossil fuel-based heat engines, which operate usually below and often far below 50% efficiency.[3] The remaining energy is lost to the environment as low-grade heat that is difficult to harvest by conventional means. One promising route for harnessing such low-temperature (a few 100 °C above the ambient) thermal resources is through thermoelectric devices[4] that directly convert thermal energy into electricity, a most desirable form of energy for its easy transportation, distribution, and usage.

The application of thermoelectric devices is currently limited by their efficiency, which is described by the dimensionless material figure of merit ZT,[5]

$$ZT = \frac{S^2 \sigma T}{\kappa_L + \kappa_e} \tag{1}$$

where S is the Seebeck coefficient, σ is the electrical conductivity, T is the temperature, and κ_L and κ_e are, respectively, the lattice and electron thermal conductivity. An ideal thermoelectric material with a high thermoelectric figure of merit, ZT, should be simultaneously an electrical conductor and a thermal insulator.[6] This conflicting requirement poses a material challenge in the quest to increase ZT; optimization of one conductivity can adversely affect the other, due to their strong interdependencies.[7,8]

Over the past decade, the most successful approach to enhancing ZT has been through device component miniaturization into the deep nanometer range (10^1–10^2 nm).[9–13] This approach reduces lattice conductivity without significantly altering electronic conductivity.[12,13] Semiconducting nanowires in this size range (such as those made of silicon) display a thermal conductivity that is 2 orders of magnitude lower than
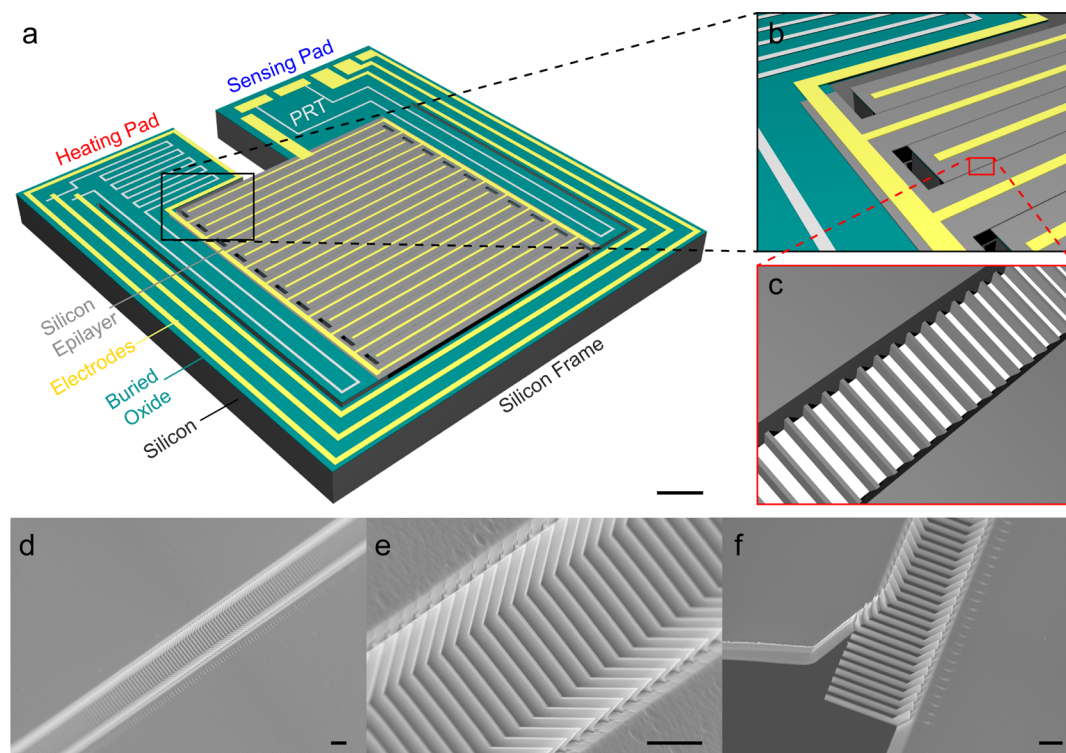
Figure 1. Suspended SiNWs integrated on device. (a) Schematic overview of the measurement device with integrated SiNWs used in thermoelectric measurements. The device consists of heating and sensing pads supported by a U-shaped silicon outer frame. The right insets show interdigitated heating and sensing pads (b) bridged by suspended SiNWs (c). Pt coils (PRT) were deposited as heater on the heating pad to create a temperature gradient along the SiNWs. They are also used as resistance thermometers for both pads. A gold layer was patterned as electrodes for electrical conductivity measurements. The color code is as follows: silicon (gray), silicon dioxide (green), electrodes (gold), PRT (white). (d−f) Representative scanning electron micrographs of free-standing SiNWs. The SiNWs are typically 200 ± 5 nm in width, 600 ± 10 nm in height, and 4 ± 0.1 μm in length. The scale bars are 1 mm (a) and 2 μm (d−f).

the bulk value.[12−15] While promising, further decrease in the diameter runs into technical barriers in fabrication and scalability, as well as fundamental limitations in material stability, quality, and the discreteness of matter.[16] Parallel approaches complementary to miniaturization are clearly needed for further improvements.

A distinguishing characteristic common to all nanoscale devices is their increased surface-to-volume ratio. It is reasonable to postulate that with interface atoms now constituting a substantial fraction of the total volume, their chemical state can become a principal determinant of device properties. In fields as diverse as photovoltaics,[17,18] field-effect sensors,[19−22] and nanomechanics,[23−27] atomic-precision surface chemical control provides up to orders of magnitude improvements in the respective figures of merit. The simple removal of a 1 nm surface native SiO_2, for instance, improves electron transport in silicon nanomembranes.[28−32] Kilohertz- and megahertz-frequency phonon lifetimes in diamond and silicon nanomechanical resonators similarly show up to an order of magnitude improvement when surface chemistry is changed at the monolayer level.[23−27] The effect of surface chemical treatments on phonon transport, however, remains an open question. In light of the extreme sensitivity of electron transport in nanomaterials to the surface condition, a parallel, simultaneous investigation of phonon transport is clearly needed.

Here, we explore this inadequately exploited handle for thermoelectrics. We perform temperature-dependent measurements of the electrical and thermal conductivities of silicon

nanowire (SiNW) arrays after successive surface chemical functionalization treatments. This study was enabled by the batch fabrication of devices with monolithically integrated free-standing SiNWs and by the cleanliness and gentleness of gas-phase processing techniques.[27,33,34]

We choose two prototypical modifications of the silicon surface as model procedures: hydrogen-termination following the removal of surface native oxide and n-type surface charge transfer doping. We measure an immediate increase in electrical conductivity by 1 order of magnitude with a concurrent decrease in thermal conductivity following vapor HF removal of surface native oxide from as-fabricated samples. Furthermore, the electrical conductivity increases by a further 2−4 orders of magnitude when surface charge transfer dopants are applied, in situ, via gas-phase sources to the oxide-free SiNWs. This improvement in electrical transport takes place in the absence of marked changes in thermal conductivity. These results demonstrate that surface chemical tuning is a viable pathway and also a complementary approach to size-miniaturization in the push for high-performance thermoelectric nanostructured materials.

Schematics and scanning electron microscopy (SEM) images of the silicon nanowire (SiNW) samples used for our experiments are shown in Figure 1. The devices were fabricated from SOI wafers and consist of a free-floating heating pad connected to a supported sensing pad by a U-shaped outer frame (Figure 1a). Platinum resistance coils serving as heater and resistance thermometers, gold conducting lines, gold contacts to the silicon nanowires, and bonding pads were

deposited via shadow evaporation. Details of the fabrication procedure are provided in the Supporting Information (SI).

Up to ∼10^5 single crystalline silicon nanowires (SiNWs) with identical dimensions are patterned by e-beam lithography and inductively coupled plasma etching into the top silicon epilayer, while maintaining monolithic contact with the two pads (Figure 1b,c). The term monolithic contacts means that the SiNWs constitute bridges between two micrometer-sized pads with the SiNWs and pads all being part of the same single crystal silicon structure. This method circumvents both thermal and electrical contact resistances and their effects in measurement accuracy.[13,35] Figure 1d−f shows SEM images of SiNWs with identical dimensions. Figure 1e shows that the SiNWs are inside a tapered groove formed during a thinning step of the top silicon layer. The particular geometry (54.7°) is caused by the anisotropy of the alkaline etchant on masked device Si(100). Figure 1f is a view of the end of an array digit (nanowire row), where anisotropic wet etching of a corner in a previous fabrication step caused negligibly few SiNWs to be unintentionally singly clamped. This is shown for completeness. But clearly, such small defects have no influence on the accuracy of the results (note that only 16 ± 2 nanowires are single supported while the same row contains 5000).

The sensing pad was mechanically and thermally anchored to the sample holder (SB2438001, Global Chip Materials, Inc.) with conductive silver paste and a 3 mm × 2 mm piece of a diced silicon chip serving as a raised platform. After wire bonding, the sample was loaded onto the coldfinger of a flow cryostat (Janis Research ST-100) for the measurements. Details of the measurement procedure are described in the SI.

N-type surface charge transfer doping of a bulk silicon crystal has only recently been demonstrated in an X-ray photoelectron spectroscopy-based study.[33] The transfer doping process whereby electrons are transferred from the electron-rich dopant, decamethylcobaltocene $(Co(Cp*)_2)$ to the silicon surface can be understood with the aid of the energy level band diagrams of silicon and of $Co(Cp*)_2$ (Figure 2a). Two sketches, both referenced to the vacuum level E_{VAC}, are shown. The one on the left depicts the energy levels of pure silicon and $Co(Cp*)_2$ before any interaction has taken place. The one on the right shows changes in the energy levels when the two systems in contact are allowed to come into equilibrium. Silicon has an electron affinity of about 4.0 eV.[33] That is, the conduction band minimum (CBM) lies 4.0 eV below E_F. The ionization energy $E_{VAC} - E_{HOMO}$ of $Co(Cp*)_2$ is measured to be about 3.3 eV for the $Co(Cp*)_2$ molecule.[36] Hence, electrons flow from the highest occupied molecular orbital (HOMO) of $Co(Cp*)_2$ into the silicon conduction band upon contact.

The electrons added to silicon and the positive ions in the form of $[Co^+](Cp*)_2$ set up a space charge region that results in an downward band bending, as shown schematically in Figure 2b. The Fermi level E_F of silicon moves toward CBM and the charge transfer saturates when the two Fermi levels converge, such that an equal number of electrons and holes (ions) populate the silicon and $Co(Cp*)_2/[Co^+](Cp*)_2$ sides of the interface.

We have investigated the interaction of SiNWs with gas-phase decamethylcobaltocene $Co(Cp*)_2$ or with the lighter analogue, cobaltocene $Co(Cp)_2$. Figure 2b shows four different experiments involving dopant identity, dopant source temperature, and SiNW surface chemistry as variables. The SiNW samples were held at 203.15 K under high vacuum (1×10^{-6}
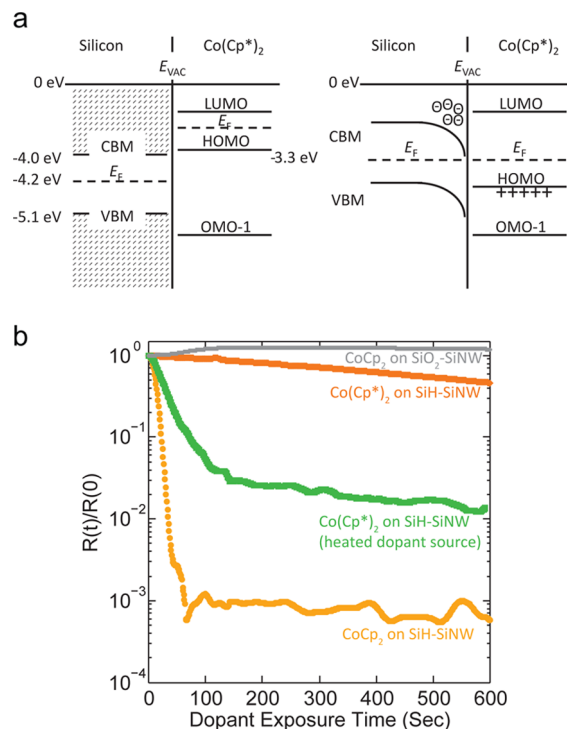
Figure 2. Surface transfer doping of silicon by n-type dopants. (a) Band diagram representation of surface transfer doping of silicon by decamethylcobaltocene $Co(Cp*)_2$. The left-hand side depicts the isolated systems before interaction and charge transfer. Valence and conduction band edges (VBM and CBM) of silicon, the Fermi levels E_F, as well as a few key occupied and unoccupied molecular orbitals (HOMO and the lowest unoccupied molecular orbital (LUMO)) of $Co(Cp*)_2$ are illustrated. The right-hand side depicts the equilibrium situation when sufficient charge transfer has occurred to lineup the Fermi levels. (b) Changes in the electrical resistance of different SiNW samples as a function of exposure time to the vapors of $Co(Cp*)_2$ or of $Co(Cp)_2$. SiNWs with either a native oxide-covered surface or an oxide-free, Si−H terminated surface were studied.

mbar). The valve separating the dopant source from the sample chamber was opened and the electrical resistance of the SiNWs was measured as a function of dopant exposure time.

The electrical resistance decreases sharply, by 3 orders of magnitude, when hydrogen-terminated SiNWs (light orange curve) are exposed to $Co(Cp)_2$ (2.3×10^{-4} mbar). The curve displays exponential behavior with a time constant of 4.8 s (SI). Noise at low resistance values are due to instrumental digital noise because the lock-in amplifier's time constant was not changed during the acquisition. With $Co(Cp*)_2$ as the dopant, one observes much slower kinetics (dark orange curve) when the source is kept at room temperature (dopant vapor pressure below background). Heating the source to yield a chamber pressure of 1×10^{-5} mbar accelerates the process (green curve). Finally, exposure to $Co(Cp)_2$ produces a negligible effect on the resistance of a native oxide-covered SiNWs sample (gray curve).

The data in Figure 2b are consistent with surface charge transfer doping of silicon by $Co(Cp*)_2$[33] and $Co(Cp)_2$. With increasing vapor pressure, more molecules per unit time can physisorb onto the surface due to an increase in collision frequency. Thus, the observed variation in doping kinetics as a function of vapor pressure reflects the prerequisite for physical adhesion of the dopant molecule in the doping process. We have performed additional control experiments to show that the
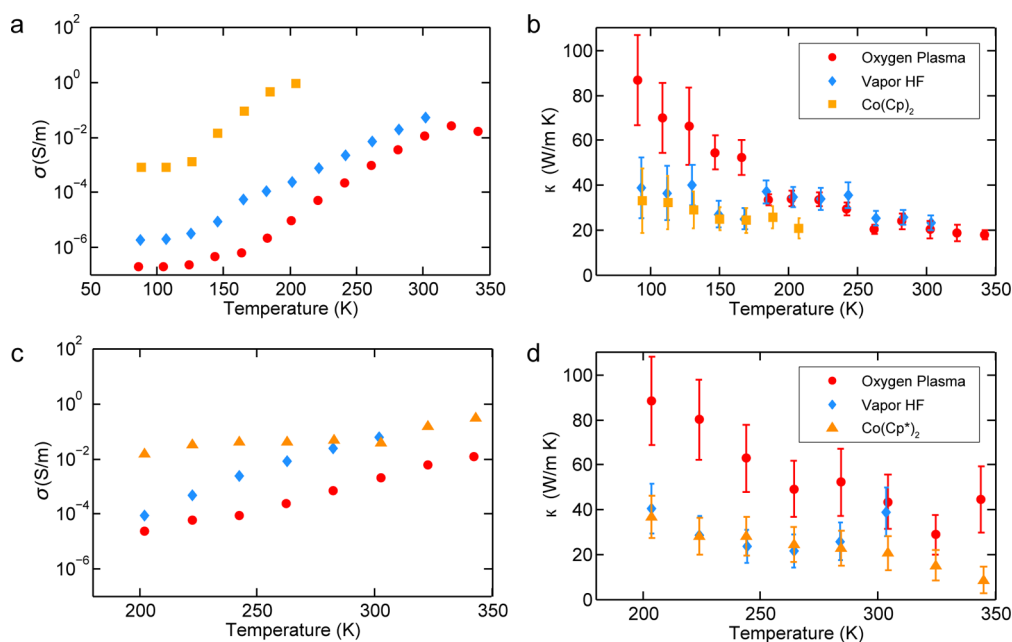
Figure 3. Temperature dependence of electrical and thermal conductivities for various Si nanowires. The temperature dependence of (a) the electrical conductivity σ and (b) the thermal conductivity κ for oxygen plasma, vapor HF-treated, and $Co(Cp)_2$-doped Si nanowires. (c,d) Analogous data for SiNWs when doped with $Co(Cp^*)_2$ at higher temperature range.

electrical resistance can be reversibly modulated by cycles of heated dopant desorption and redeposition (SI). The lack of effect on native-oxide-covered SiNWs (SiO_2–SiNWs) shows that an increase in conductance is not due to a conformal coating of a conductive layer and that intimate, barrierless contact between dopant molecules and the silicon core is necessary. The dramatic drops in electrical resistance of the absorption/reaction curves are thus the experimental signature of n-type transfer doping of SiNWs by $Co(Cp^*)_2$ and $Co(Cp)_2$.

We proceeded to measure the electrical and thermal conductivities of SiNWs as a function of temperature and of different surface chemistries (Figure 3). Measurements were conducted in high vacuum and in the dark to suppress gas-phase thermal conductance and photoconductivity effects.[37,38] Data for two typical samples are shown, one involving $Co(Cp)_2$ doping (Figure 3a,b) and the other involving $Co(Cp^*)_2$ (Figure 3c,d).

Each sample was measured in three surface chemical states. A first round of measurements took place on as-fabricated SiNWs cleaned by 5 min of 600 W oxygen plasma ashing. The samples were then stripped of their surface native oxide in vapor HF and pumped down to high vacuum with about 5 min of transport through ambient atmosphere. After this second measurement, the sample was subjected, without breaking vacuum, to in situ charge transfer doping and measured again. After the three sets of measurements, the entire SiNW arrays were removed by fracturing with mechanical agitation. The background thermal conductance of the U-shaped frame (Figure 1) was then measured to enable isolating the conductance due to the SiNWs.

Electrical transport data show that oxygen plasma-treated SiNWs resulted in electrical conductivities that are consistent with the specified device layer resistivity of the SOI wafer (>1000 Ohm·cm). Subsequent vapor HF exposure increased electrical conductivity by roughly 1 order of magnitude. This behavior is in line with reported literature results[28−32] and is attributed to decreased charge trapping following removal of a defect-rich Si–SiO$_2$ interface. HF-etched samples are also known to become n-doped by the Si–H surface termination. Although the exact mechanism is not fully understood, atmospheric moisture has been suggested to play a role,[28] perhaps due to charge transfer doping by adsorbed water molecules.[39]

Strikingly, exposure of the oxide-free SiNWs to $Co(Cp)_2$ or $Co(Cp^*)_2$ leads to further enhancement of σ by up to 4 orders of magnitude in selected temperature ranges. We attribute this behavior to the injection of electrons into the silicon crystal by charge transfer doping.[33] Together, the data confirm that surface chemistry can be used as a powerful tool to enhance electron transport.

Thermal conductivity data collected in parallel with the above electrical measurements show that the room-temperature values are consistent with previously reported values for nanomembranes.[40,41] Our values are slightly lower because of the change from two-dimensional (2D) planar to 1D nanowire geometry. Furthermore, we find that thermal conductivity is sensitive to surface conditions. Vapor HF treatment of native-oxide-covered SiNWs can reduce their thermal conductivity by up to 50%. Deposition of the charge transfer dopants on the surface only minimally affects the κ values. Any slight drop of κ following surface transfer doping could be due to slight increases in surface roughness following the physisorption of a foreign species.

We have explored several potential explanations for the observations in thermal conductivity. One possible cause is the roughening of SiNW surface during vapor HF etching in the presence of air. Surface roughness has been shown to decrease thermal conductivity by increasing phonon boundary scattering rates.[42,43] AFM analysis of silicon wafer surfaces etched under the same conditions as those used on the SiNW samples shows an increase in rms surface roughness from 0.3 to 0.6 nm (SI). Other causes may include the creation of phonon scattering centers at the surface following HF treatment. We currently have limited understanding of the exact structure of HF-treated
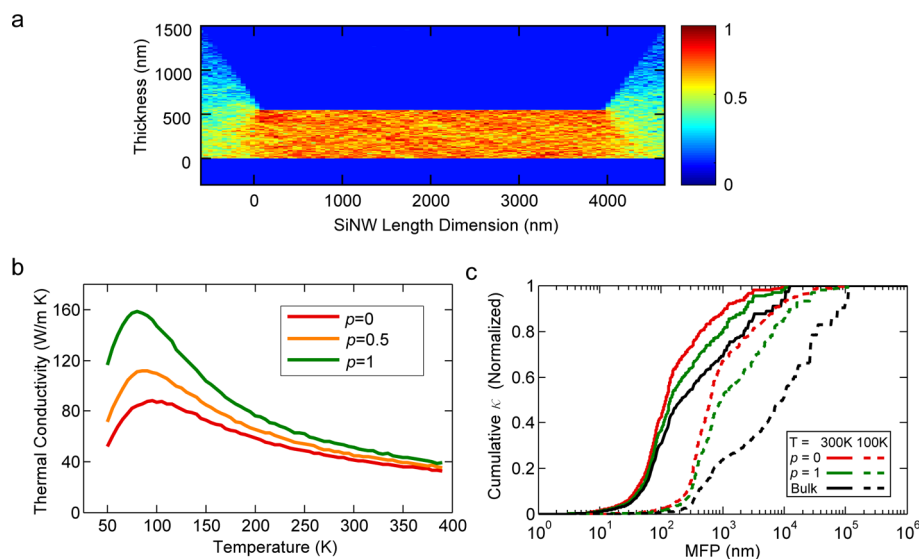
Figure 4. KMC simulations of phonon transport in Si nanowires. The simulated dimensions of nanowire are 200 nm in width, 600 nm in height, and 4 μm in length. (a) Side view of local heat flux density inside the nanowire at 100 K with a fully diffusive surface. Blue regions represent empty space with no heat flux. (b) The temperature-dependent thermal conductivity with different surface states: fully diffusive ($p = 0$), intermediate reflectivity ($p = 0.5$), and perfectly specular ($p = 1$). (c) The normalized cumulative thermal conductivity with respect to the mean free path (MFP) for the cases of different surface states and different temperatures. The results of bulk silicon are also plotted for comparison.

surfaces[34,44,45] and a scattering center may consist of low-density, surface atomic and molecular clusters with vibrational frequencies matching those of heat conducting phonons. Regardless of the exact nature of these scattering centers, increase in their concentration following chemical modification would increase diffusive phonon scattering.

To better understand the thermal conductivity measured in experiments and the effect of diffusive scattering on the thermal conductivity of SiNW, we performed fully 3D simulations of phonon transport in SiNW. The simulations involve solving the Boltzmann transport equation (BTE) using frequency-dependent variance-reduced kinetic Monte Carlo (KMC) method[46,47] coupled with first-principles calculations. The KMC method is a Monte Carlo computer simulation intended for investigating the time evolution of processes occurring in nature. Typically these are processes that occur with known transition rates among states.[48−51] Typical applications of KMC include surface diffusion, dislocation mobility, surface growth, vacancy diffusion in alloys, and so forth. In the current work, we apply the KMC method to solve the BTE to capture the phonon transport behavior. Here, the so-called known transition rates are the scattering rates of phonons. The applications of KMC methods in solving BTE for phonon transport have been developed for several years and much of the information is available in past works.[46−51]

The KMC/BTE procedure stochastically simulates the emission, advection, and scattering of phonon bundles that represent fixed deviational energy from the equilibrium Bose−Einstein distribution. The simulations are based on the phonon distribution, group velocity, and lifetime of bulk silicon, and the results are statistically gathered based on the kinetic processes of phonon bundles. The thermal conductivity is calculated by adding up the contribution of the trajectory of all the phonon bundles to the overall heat flux. The phonon dispersions and phonon lifetimes of bulk silicon are calculated with the Vienna ab initio simulation package (VASP), phonopy, and ShengBTE.[52−54]

The geometry of the simulated SiNW is constructed exactly as presented in the experiments (Figure 1). Phonon bundles are emitted from the left hot wall and annihilated at the right cold wall. During the transit, they can be intrinsically scattered due to a finite lifetime and scattered by the surface boundaries. The heat flux density reconstructed from the advection of phonon bundles is shown in Figure 4a.

We model the surface boundaries with three surface scattering states, that is, fully diffusive ($p = 0$), perfectly smooth ($p = 1$), and with intermediate reflectivity ($p = 0.5$), where p is the probability for specular reflection (specularity parameter). Note that previous work has shown that it takes more than the specularity parameter alone to obtain better agreement between modeling and experiments; the rms roughness, correlation length, and power spectral density will also play a role.[42] The exact dependence of the specularity parameter p on the detailed surface roughness is currently an unresolved issue.[55,56] Nevertheless, the specularity parameter method is believed to provide useful trends for comparison with experiments. The temperature-dependent thermal conductivity of SiNW obtained from KMC simulations is plotted in Figure 4b. We find that increase in diffusive scattering decreases the thermal conductivity.

We further plot the normalized cumulative thermal conductivity with respect to the mean free path (MFP) in the nanostructured SiNW at different temperatures (Figure 4c). Compared with bulk silicon, we find that the effective MFP in nanostructured SiNW is decreased due to the more diffusive phonon transport caused by additional surface boundary scattering.

Comparing experimental and computational results, the measured thermal conductivities of silicon nanowires are smaller than the computational result. The reason is attributed to two aspects: (1) the phonon information (both phonon dispersion and lifetime) in nanostructured SiNWs is fundamentally different from that in the bulk. Although the phonon dispersion will not change markedly when the size of SiNWs goes up to 200 nm, the effect of the finite size is still

possibly responsible for the difference, especially for the phonon lifetime. Recent studies from both ab initio and classical potential approaches show that the largest MFP of phonons in bulk Si could reach a couple of microns and such long MFP phonons contribute significantly to the total thermal conductivity as we recently reported,[57] which clearly suggests that the SiNWs with thickness of the order of a few hundred nanometers could still be affected. Using the phonon information of bulk silicon for simulations in nanostructures might cause some systematic inaccuracy, leading to the discrepancies. This possibility cannot be checked easily because the size of the experimental samples is far larger than what can be currently handled with first-principles calculations.[58,59] (2) The measured thermal conductivity could be possibly affected by additional defects unavoidable in experiments, such as grain boundaries and impurity atoms, whereas the KMC/BTE simulation assumes pristine monocrystalline SiNWs. Even though the substrate SOI device layer is nominally single-crystalline, the fabrication process of SOI wafers involve mechanical thinning and polishing of the top device silicon layer that is known to induce damage and defects that can be nucleation sites for dislocations.[60] It has also been shown experimentally that measured thermal conductivity of SOI silicon films below 1.6 μm are below theoretically predicted values.[61] Such observations were attributed to a higher concentration of defects in the device layer. It should thus be accepted that this type of effect always exists in real experiments and it is difficult to precisely quantify. To a certain extent, it is therefore plausible to also expect such phenomena in SiNWs fabricated from SOI wafers. Despite such discrepancies, the general trends of the thermal conductivity as a function of temperature are consistent for measured (Figure 3b,d) and computed (Figure 4b) results. In particular, both experiment and simulation shows that the effect of increasing diffusive scattering is more pronounced at low temperatures compared to higher temperatures.

In summary, we have experimentally and computationally investigated the effect of surface chemical modification on the transport of electrons and phonons in silicon nanowire arrays with cross-sectional dimensions in the hundreds of nanometers. We found that removing the native oxide layer by vapor-phase-hydrofluoric-acid etching improves electrical conductivity and suppresses thermal conductivity. Subsequent surface transfer doping by the electron-rich dopants cobaltocene and decamethylcobaltcocene drastically amplifies this effect. An up to 4 orders of magnitude increase in electrical conductivity was achieved with a slight drop of thermal conductivity compared to vapor HF-treated SiNWs. By the combined effects of vapor HF etching and charge transfer doping, we were able to independently tune the thermal and electrical conductivities of SiNW arrays toward improved thermoelectric performance. A further investigation of the scope of such tunabilitiy will require separating the contributions of carrier mobility and carrier concentration to the measured electrical conductivity and elucidating the relationship between carrier mobility and lattice thermal conductivity. We project even more dramatic effects with increased surface-to-volume ratio in thinner SiNWs shown to exhibit optimal ZT.[9−13,35,42,62] Our study establishes that carefully optimizing the surface chemistry of nanoscale materials is an important step and a powerful approach toward more efficient thermoelectric materials and devices.

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Notes

The authors declare no competing financial interest.

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