Supplemental Information for: Nanoscale magnets embedded in a microstrip

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Appendix A: Appendix A: Fabrication of Embedded Nanomagnets

1. Wafer Preparation

The fabrication process begins at the wafer scale in order to streamline the initial processes. The wafers used were 10 cm (4-inch) silicon wafers made by MicroChemicals GmbH (article number WTD40525250B1314S102, boron-doped, 1 Ω cm-10 Ω cm, 100 nm oxide layer). In order to ensure consistent alignment between multiple fabrication steps, markers are etched into the wafer itself to provide physical landmarks. While these markers can be seen optically, their main purpose is to enable visibility under SEM.

- Using Laser Writing (DWL 66+, Heidelberg Instruments) and the optical resist AZ 1518 (MicroChemicals GmbH), a periodic grid of alignment markers and chip borders is exposed into the resist layer on top of the wafer and developed using AZ 400K 1:4 MIC developer (MicroChemicals GmbH). Standard hardbake and cleaning measures are performed.

- Using a two-stage RIE etch process (PlasmaPro 80 RIE, Oxford Systems), the silicon oxide layer is breached and subsequently the underlying silicon is etched to a depth of roughly 2 µm. The process step for the oxide breach uses CF_4 at 150 W, 65 mtorr, 20 sccm for 2.5 min. The process step for the silicon etch uses SF_6 & O_2 at 100 W, 100 mtorr, 50 sccm/10 sccm for 2 min. Etch depth into the silicon is not relevant as long as it is within micron range and does not deform the markers in the process. After the RIE etch, the resist is lifted and the wafer is cleaned in solvent baths of acetone and isopropyl alcohol as well as in a mild oxygen plasma.

- Using a BAK 501 LL electron beam evaporator (Evatec AG), 10 nm of titanium and 260 nm of FeCo alloy (65%/35% at.wt.) are evaporated onto the wafer surface without any masking to achieve a uniform film. The titanium serves as adhesion layer, while the FeCo will form the nanomagnets. Once the evaporation is complete, the wafer is subjected to glancing angle IBE in order to further planarize the surface and remove surface impurities, removing ca. 10 nm of material in the process. Once complete, 3 nm of platinum are evaporated onto the FeCo layer as a protection against oxidation, followed by 130 nm of Cr, which serves as a spacer layer for the following process.

2. Hardmask Fabrication

To shape the nanomagnets from the bulk FeCo film, Argon Ion Beam Etching is used, with Cr acting as a spacer layer and a hardmask made from silicon nitride (SiN) acting as physical shield from the argon ion impacts. Before the hardmask is grown, the wafer is diced into smaller chips (10×9 mm) for ease of handling and prototyping.

- Using PECVD, a SiN layer with a thickness of 550 nm is grown on top of the Cr layer. The step is performed at a process temperateure of 300 °C.
- In order to pattern the SiN layer, a negative resist (ma-n 2410, micro resist technology GmbH) is applied and exposed via electron beam lithography (EBL). Prior to resist application, the chips need to be washed thoroughly in acetone and isopropyl alcohol to improve resist adhesion to the SiN film.
- Using the engraved alignment markers, the core positions on the chip are located and exposed with simple circular patterns to form resist pillars. Three different magnets are implemented on each microstrip with a spacing of 5 µm between the centers. The radii written in the exposure pattern are 250 nm, 250 nm, and 325 nm, with corresponding exposure doses of 350 $\mu C/cm^2$, 787.5 $\mu C/cm^2$, and 350 $\mu C/cm^2$. The doses and radii control the width of the resulting resist pillars, and therefore the sizes of the nanomagnets. Development of the resist is achieved with MF 319, a TMAH-based developer.
- Using a two-step RIE process, the resist pattern is then transferred to the SiN film, resulting in the desired SiN hardmask shape. The RIE steps consist of a 180 s etch with 30 sccm of SF_6 at 150 W and 30 mtorr, followed by a 225 s etch with 50 sccm/5 sccm of CHF_3/O_2 at 100 W and 55 mtorr (the second step employs a mixed process gas). The first etch step produces sloped sidewalls while the second produces nearly vertical sidewalls. A combination of the two different etch steps assures an optimized etch profile for IBE. No detritus was observed for sufficiently long etch times.
- Once the RIE process is complete, the negative resist is lifted in a solvent bath of NMP or DMSO at 80 °C. NMP is more effective at lifting quickly and cleanly, however DMSO, which is nontoxic, and has also yielded satifactory results.

3. IBE-assisted Creation of Nanomagnets

Now that the hardmask is in place, Ion Milling of the metallic substrate can begin.

- Using an Ionfab 300 Plus (Oxford Instruments), the entire metallic film surrounding the SiN hardmask is eroded with argon ion bombardment at a beam current of 500 mA while the sample holder is rotated around its central axis. The critical issue in this process is to achieve both an optimal pattern transfer of the hardmask while simultaneously mitigating redeposition. To that end, the incidence angle of the ion beam is varied during the milling step, and the material ejection is monitored using secondary ion mass spectroscopy (SIMS). The process begins with an incidence angle of 20° (from the surface normal, 0° being perpendicular to the surface) for 21 min, eroding 130 nm of Cr, 3 nm of Pt and most of the 250 nm, approximately 235 nm.

- In order to remove redeposited material from the newly created metal pillars' sidewalls, the incidence angle is changed to 80° for 10 min at constant rotation. SIMS readout at such glancing angles is impaired and milling rates for such angles are best calibrated using test- and sacrificial samples.

- The steep 20° angle is resumed for the final step until the elemental signal of the Ti adhesion layer diminishes in the SIMS readout, which typically occurs after around 100 s. This decrease marks the breach of the final metal layer and the completion of the nanomagnet stacks.

- The shape of the nanomagnets is examined using AFM and SEM; to that end, a sacrificial sample is immersed in Cr etch (Cerium Nitrate solution) in order to selectively dissolve the Cr spacer separating the hardmask and the newly created nanomagnet. The existence of the spacer allows the selective separation of the nanomagnet from its hardmask, however the mask needs to remain at this stage for regular samples. Using SEM, the milling outcome and general shape of the nanomagnet is examined, while AFM yields the precise height of the nanomagnet with respect to the silicon surface. In the specific example of the sample measured in this publication, the height of the nanomagnets was determined to be 260 nm.

4. Au Layer Evaporation

Using the determined height of the nanomagnet, a variable-angle evaporation of Ti and Au is conducted to evaporate the Au film onto the silicon surface, thereby covering the free-standing nanomagnet arrays with a Ti/Au metal film. In order to monitor the process, 4 sacrificial chips are created before the evaporation and covered with chromium as a stopping layer. These chips are then coated along with the regular samples.

The coating process needs to leave the chromium spacer exposed for a future liftoff. The sides of the nanomagnets need to be coated homogeneously, ideally in a relatively passive material, and the final Au film needs to match the height of the nanomagnet as closely as possible to minimize topographic features.

- Starting the evaporation at an angle of 60° to the surface normal with a rotating sample holder, 20 nm of Ti is evaporated onto the surface of the chip as well as onto the sidewalls of the nanomagnet arrays. The effective layer thickness on the chip surface due to tilt is 10 nm. The Ti film serves as a crucial adhesion film for the sidewalls of the nanomagnets as well, ensuring no gaps will form between the FeCo and Au films. This is vital to avoid galvanic corrosion effects which are facilitated by trapped moisture in potential gaps, an effect which has been observed on previous device iterations.

- Using the same incidence angle, 100 nm of Au is evaporated, homogeneously coating the surface and sidewalls in a (in case of the sidewalls relatively thin) layer of Au. The effective Au layer thickness on the chip surface due to tilt is 50 nm at this point.

- With an incidence angle of 0°, 100 nm Au are evaporated onto the chip, translating directly to effective layer thickness and mostly leaving the sidewalls unaffected.

- In a third evaporation step, with an incidence angle of 30°, 173 nm of Au is evaporated. This angle is chosen to minimize shadowing effects from the rotating evaporation while still maintaining coverage of the sidewalls.The effective layer thickness on the chip surface due to tilt is 150 nm.

- Using a sacrificial chip introduced previously, the Au layer is masked with AZ 1518 analogously to the marker fabrication, and is etched down with RIE using CHF_3/O_2

with a flow of 45 sccm/2 sccm for 13.5 min at 300 W and 25 mtorr. Conclusion of the etch is verified in SEM and the layer thickness is confirmed to be 300 nm via AFM, yielding a total thickness of 310 nm when including the Ti adhesion layer.

5. Hardmask Liftoff and Polishing

Once the height of the Au film has been determined, the distance between the Au layer surface and the nanomagnet surface can be calculated to be 50 nm in total. It is generally easier to overshoot the Au layer thickness and then erode the excess than the reverse case, as the following steps show:

- Using the same CHF_3/O_2 RIE recipe with a shorter runtime of 107 s, 40 nm of Au are removed in an anisotropic vertical etch, leaving 10 nm of Au layer above the nanomagnet level. Note that vertical IBE has proven to be unreliable to remove material in a strictly vertical etch without shadowing, which in this case must be avoided. Furthermore, care must be taken not to overetch the layer, as a breach of the nanomagnet sidewalls would be catastrophic, corroding the material in the process.
- In order to remove the SiN hardmasks and expose the nanomagnets, the sidewalls of the Cr spacer on top need to be exposed. To do so without eroding the surrounding Au film, 10 nm Cr and 20 nm Ti are evaporated vertically as a protection layer and the whole chip is ion milled at 80° incidence angle for 18 min, which roughly is the time the protection layer can withstand the ion milling at this angle.
- After the glancing angle ion milling step, the protection layer and the SiN hardmasks are removed via Cr etch and the topography is examined in SEM and AFM.
- In case of overshooting the desired milling depth, a generous layer of Au/Ti can be applied and polished down iteratively to avoid another overshoot.
- In case of insufficient milling depth, an application of another Cr/Ti protection layer and a further milling step can reduce the layer thickness further without compromising topography or the nanomagnet itself. Protection layers are especially desirable if the topography is indufficiently flat, otherwise a simple glancing angle milling step can be sufficient.

- Once the nanomagnets are visible below the Au layer in SEM, gentle polishing steps can be made to remove any remaining Au islands on top of the nanomagnet. This is made easier by the comparably high milling rate of Au compared to FeCo at all angles.
- For the embedded nanomagnets measured in this paper, 5 iterative polishing steps have produced a suitable result.

6. Microstrip Creation from Au film

The current state of the sample chip is a planar Au film with FeCo nanomagnets embedded in its surface. In order to pattern a microstrip from the bulk film, the following steps are taken:

- Using e-beam evaporation and PECVD, a 130 nm thick Cr film and a 250 nm thick SiN film are applied to the sample chip.
- Using EBL, a resist bilayer of 50K/950K PMMA (Allresist GmbH) is exposed with a dose of 200 $\mu C/cm^2$. Alignment is again achieved using the etched alignment markers in the bulk substrate.
- The resist is developed using MIBK developer and 40 nm of Cr are evaporated onto the now exposed SiN layer, forming a Cr film in the shape of the desired microstrip, positioned above the nanomagnet array buried below. The resist is then lifted using a solvent bath.
- The Cr layer acts as etch ask for a RIE etch step to etch the SiN film using the CHF_3/O_2 recipe mentioned before, forming the hardmask for the next milling step. A hybrid etch recipe is not critical in this case.
- The chip is ion milled at 20° for a relatively short 10 min until Ti is visible in the SIMS, signalling the removal of the Au layer, then polished at 80° for 5 min to remove redeposited material from the microstrip sidewalls and the Cr spacer sidewalls. A final 2 min are spent milling at 20° to breach the Ti layer and expose the surrounding silicon oxide substrate. This concludes the patterning of the microstrip and allows the SiN hardmask to be lifted using a Cr etch.

- A final layer of Ti/Au with thickness of 3 nm and 12 nm, respectively, is applied identically to the 40 nm thick Cr layer using EBL and PMMA resist.

The final step adding the Ti/Au layer was only performed in response to high noise levels during measurements and poor SNR, significantly improving device performance. This leaves the finished embedded nanomagnet microstrip to be wirebonded to a suitable PCB to be incorporated into the MRFM system. In case of multiple microstrips on a chip unit (which is preferable to increase yield), dicing of the chip is required beforehand. The final microstrip chip has a dimension of 5 mm x 1.5 mm. Fixation to the supporting PCB is achieved by using dried PMMA 950K as glue.

Appendix B: Adiabaticity Plots

The performance characteristics of the two microstrip generations is compared in Fig. S1. Spin signal is measured in dependence of RF pulse strength (shown here as AWG Amplitude) and frequency deviation. A considerable increase in spin signal is observed for the planar microstrip design in comparison to the stacked microstrip design.

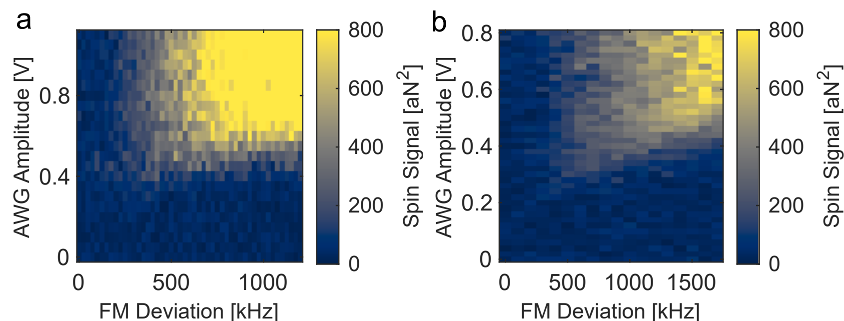

FIG. S1: Comparison of spin inversion pulse characteristics between microstrip device generations for 60 s integration time. Color scale bars are limited to 800 aN^2 for better low-signal contrast. (a) Spin signal recorded with the magnet-in-microstrip device from Fig. 2(b) at a distance of 90 nm above the microstrip surface (sample-magnet separation of 110 nm). High signal is obtained roughly above 400 kHz FM deviation and 0.5 V AWG amplitude, with a measured maximum of 2000 aN^2. (b) Spin signal recorded with a conventional magnet-on-microstrip design from Fig. 2(c) at a sample-magnet separation of 30 nm. The maximum measured spin signal is 900 aN^2.

Appendix C: SNR Measurements for Resolution Determination Measurement

As a supplement for Fig. 3(c), the increase in SNR is shown for the corresponding measurement.

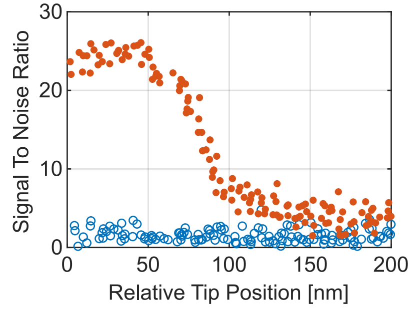

FIG. S2: SNR data corresponding to Fig. 3(c) showing maximum values of 25 at 60 s integration time, demonstrating excellent noise characteristics for the embedded nanomagnet design.